Application Note

PV88080-Dynamic Voltage Control (DVC)

AN-PV-006

Abstract

Dynamic Voltage Control (DVC) facilitates the increase or decrease of power rail voltages dynamically as the load increases on a processor. This functionality saves system power when the loading is low while allowing increased processor clocking when the system needs it. This application note illustrates the use of DVC using the PV88080 PMIC.

Contents

Figures

Tables

1 Terms and Definitions

GUI	Graphical User Interface
HVBuck	High Voltage Buck Converter
LVBuck	Low Voltage Buck Converter

2 References

[1] S. Mittal, "A survey of techniques for improving energy efficiency in embedded computing systems", IJCAET, 6(4), 440–459, 2014.

3 Introduction

The power consumed by processor cores is proportional to the operating frequency and to supply voltage. DVC is used to optimize performance, power consumption, and thermal performance of processor devices. DVC increases voltage to increase processor performance, and decreases voltage to save power. This technique, initially used in laptops and mobile devices [1], is now becoming prevalent in tethered systems.

4 DVC

Traditionally, a mount of resistor divider and MOSFET, as shown in Figure 1, is used to change the divide ratio for adjusting the output voltage of the converter. It needs many components and control signals, and therefore, also a large layout area. The PV88080 provides DVC, which supports adaptive adjustment of the supply voltage dependent on the processor load, via direct register write in the I²C interface. This simplifies the schematic, as shown in Figure 2.The DVC slew rate is also adjustable in the I²C to minimize the overshoot when the output voltage overshoot level is not acceptable. For examples of how the PV88080 DVC minimizes overshoot and undershoot, see Figure 3 and Figure 4.

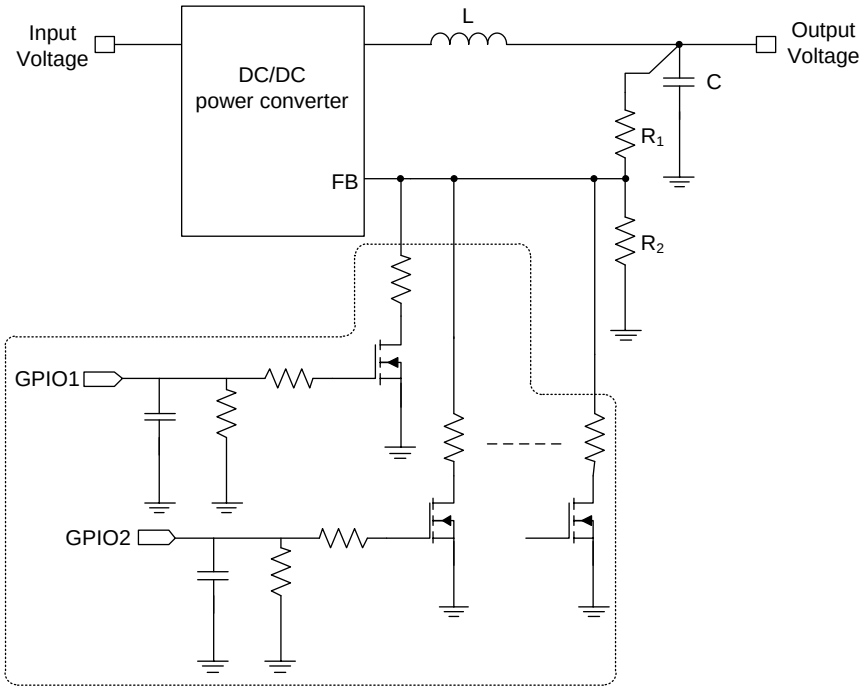

Figure 1: Traditional DVC Solution

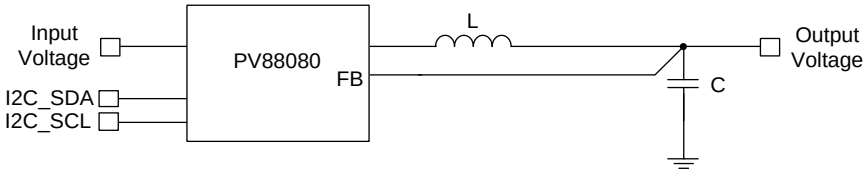

Figure 2: PV88080 Simplified Block Diagram for One Buck Stage

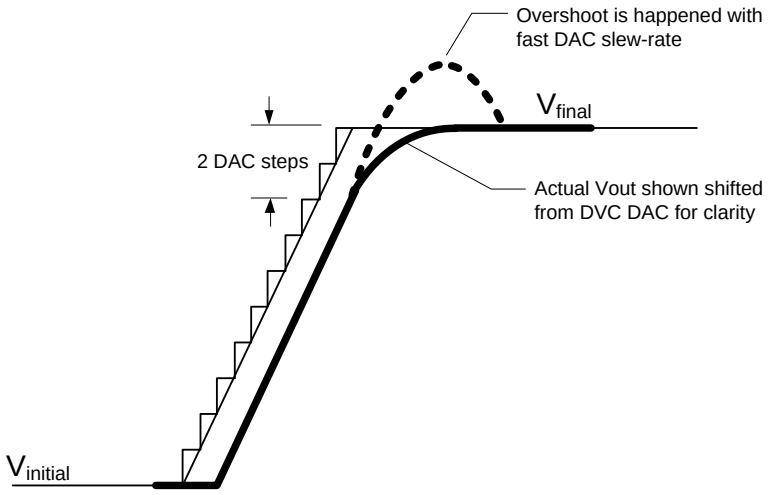

Figure 3: PV88080 DVC Up Transition Measurement Example

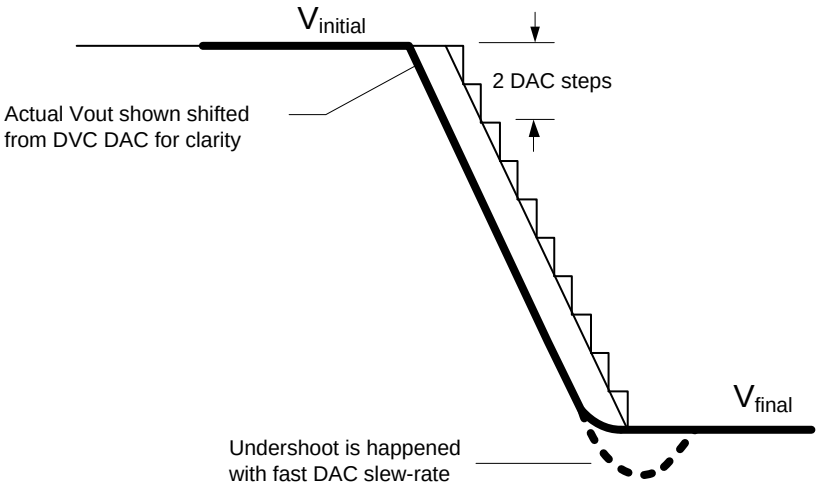

Figure 4: PV88080 DVC Down Transition Measurement Example

4.1 DVC Setting - LVBuck Converter

The LVBuck converters support DVC. The output voltage range of LVBUCK1 is 0.75 V to 3.3 V, and 0.9 V to 3.6 V for LVBucks 2 and 3, see Table 1 and Table 2. The typical core processor voltage is in region 1.

The target voltage is programmable to suit specific processor requirements and can be set in register BUCKx_CONF0[6:0] using **Dialog Semiconductor**'s graphical user interface (GUI), see Figure 5.

Table 1: LVBuck1 Output Voltage Region

Region	Min (V)	Max (V)	Step (mV)
1	0.75	1.39375	6.25
2	1.4	2.19375	6.25
3	1.2	2.7875	12.5
4	2.8	3.3	12.5

Table 2: LVBuck2/3 Output Voltage Region

Region	Min (V)	Max (V)	Step (mV)
1	0.9	1.39375	6.25
2	1.4	2.19375	6.25
3	1.2	2.7875	12.5
4	2.8	3.6	12.5

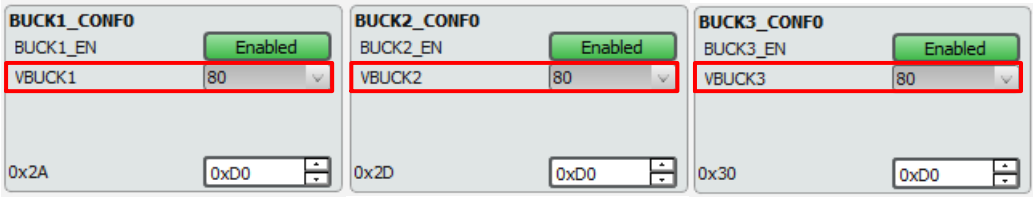

Figure 5: Dialog GUI - BUCKx_CONF0[6:0]

The DVC slew rate is adjustable to prevent overshoot or undershoot on the output voltage by setting register Buckx_CONF3[7:6] in the GUI, see Figure 6. Generally, higher slew rates are more likely to cause overshoot or undershoot. Figure 7 to Figure 10 show the DVC waveform with different slew rates. The overshoot and undershoot caused by faster slew rates are shown in Figure 9 and Figure 10.

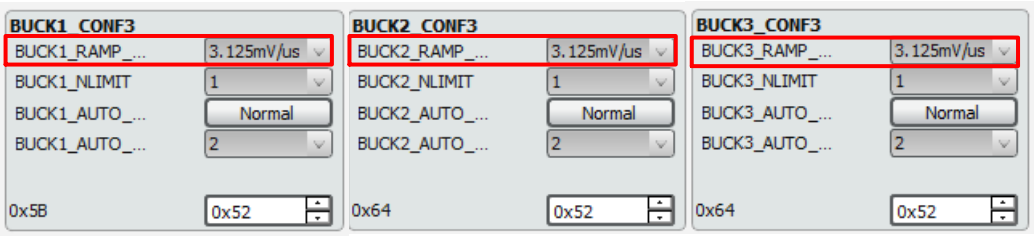

Figure 6: Dialog GUI - BUCKx_CONF3[7:6]

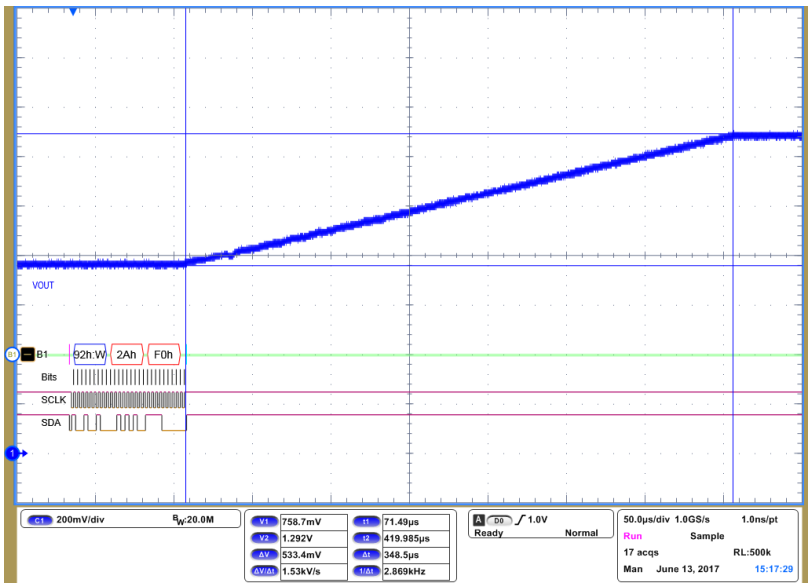

Figure 7: DVC Step-Up with 1.5625 mV/µs Slew Rate

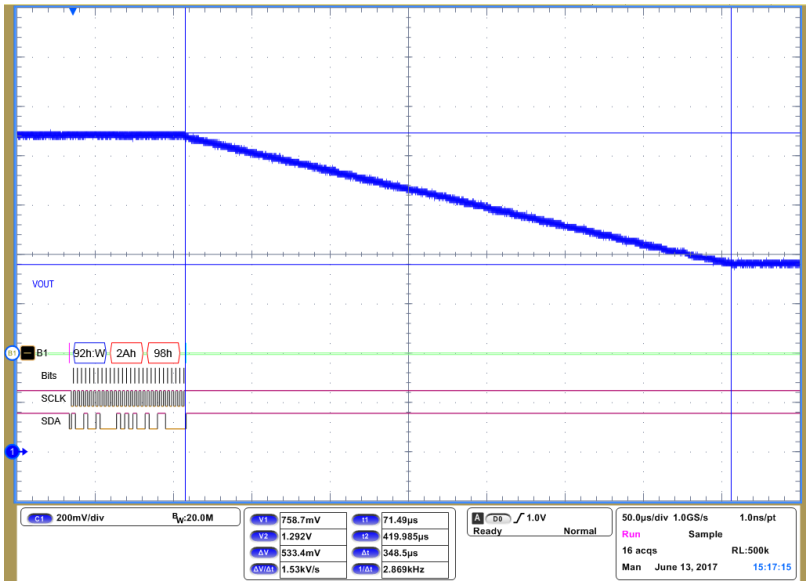

Figure 8: DVC Step-Down with 1.5625 mV/µs Slew Rate

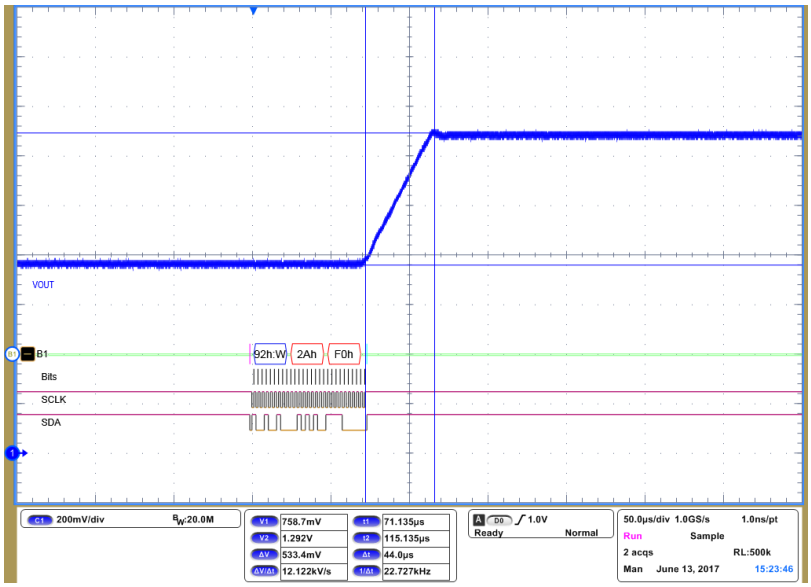

Figure 9: DVC Step-Up with 12.5 mV/µs Slew Rate

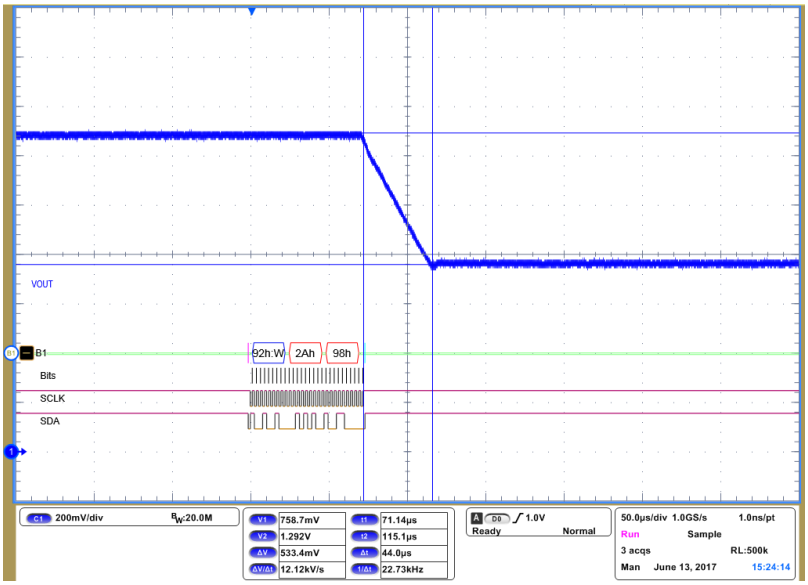

Figure 10: DVC Step-Down with 12.5 mV/µs Slew Rate

For example, a processor is supplied by the LVBuck1 for the typical 1.2 V core voltage. The LVBuck1 output voltage is in region 1, see Table 3. In idle mode, the core voltage of the process is 1.15 V to save power. The slew rate is set to 3.125mV/µs to prevent overshoot. Sending the command 0xD8 to BUCK1_CONF0(0x2A) in the I²C interface, as shown in Figure 11, results in the desired DVC step-down, see Figure 12. The output voltage is set back to 1.2 V by sending the 0xE0 command to BUCK1_CONF0(0x2A), see Figure 13 and Figure 14.

Table 3: LVBuck1 Output Voltage - Region 1

Address	**Name**
0x002A	BUCK1_CONF0

Field name	**Bits**	**Description**
BUCK1_EN	[7]	BUCK1 Enable **Value** / **Description** 0x0 / 0:Disabled 0x1 / 1:Enabled
VBUCK1	[6:0]	Buck1 Target Voltage. V_{OUT} = 0.6 + 0.00625 * VBuck1[6:0] **Value** / **Description** 0x18 / V_{OUT} = 0.6 + 0.00625 * 24 = 0.75 V … / …… 0x7F / V_{OUT} = 0.6 + 0.00625 * 127 = 1.39375 V

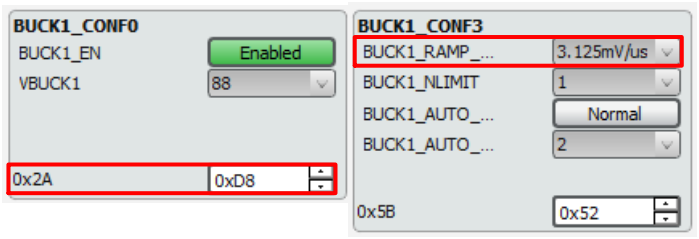

Figure 11: Sending 0xD8 to BUCK1_CONF0in Dialog GUI

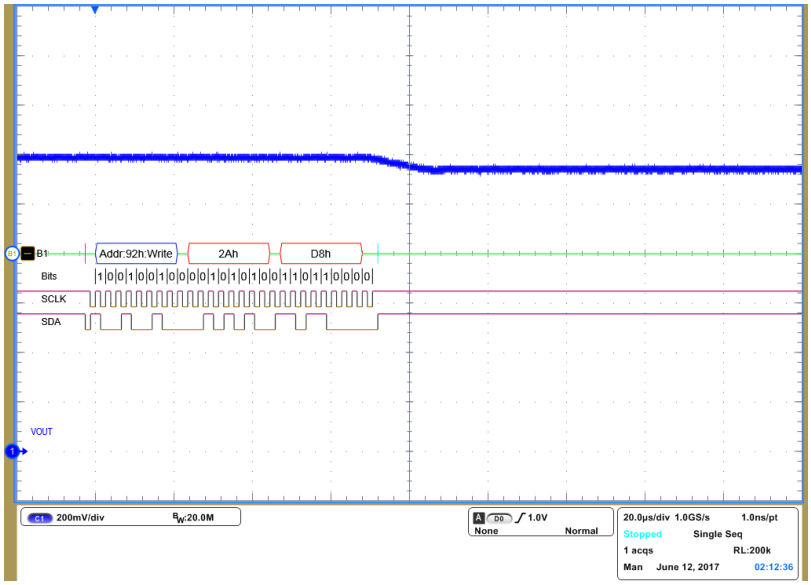

Figure 12: DVC Step-Down from 1.2 V to 1.15 V

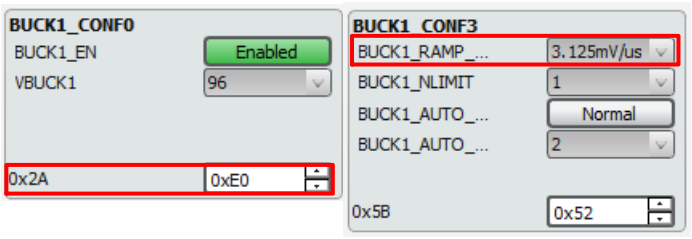

Figure 13: Sending 0xE0 to BUCK1_CONF0 in Dialog GUI

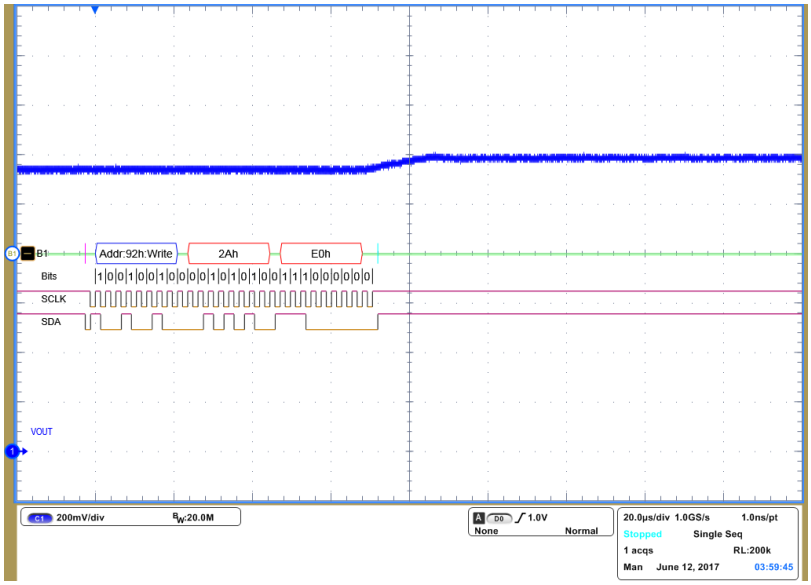

Figure 14: DVC Step-Up from 1.15 V to 1.2 V

4.2 DVC Setting - HVBuck Controller

The HVBUCK controller supports DVC in the 0.8 V to 1.275 V output voltage range with 5 mV, see Table 4. Set register HVBUCK_CONF1[7:0] to the target voltage according to the processor requirement. The HVBUCK DVC slew rate is also adjustable to prevent overshoot or undershoot on the output voltage by setting register HVBuck_CONF2[3:1].

For example, a processor is supplied by the HVBUCK for the typical 1.05 V core voltage. In idle mode, the core voltage of the process is 1.0 V to save power. The slew rate is set to 3.125 mV/µs to prevent overshoot. Sending the commend 0xC8 to HVBUCK_CONF1(0x33) in the I²C interface, as shown in Figure 15, results in the desired DVC step-down, see Figure 16. The output voltage is set back to 1.05 V by sending the commend 0xD2 to HVBUCK_CONF1(0x33), see Figure 17 and Figure 18.

Table 4: HVBuck Output Voltage

Address	**Name**
0x0033	HVBUCK_CONF1

Field name	**Bits**	**Description**	
VHVBUCK	[7:0]	HVBuck Target Voltage. V_{OUT} = 0.005 * VBuck1[6:0]	
		Value	**Description**
		0xA0	V_{OUT} = 0.005 * 160 = 0.8V
		…	……
		0xFF	V_{OUT} = 0.005 * 255 = 1.275 V

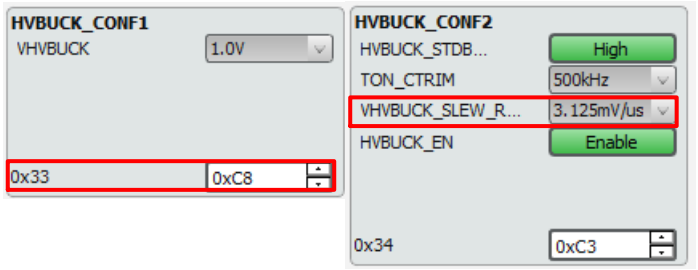

Figure 15: Sending 0xC8 to HVBUCK in Dialog GUI

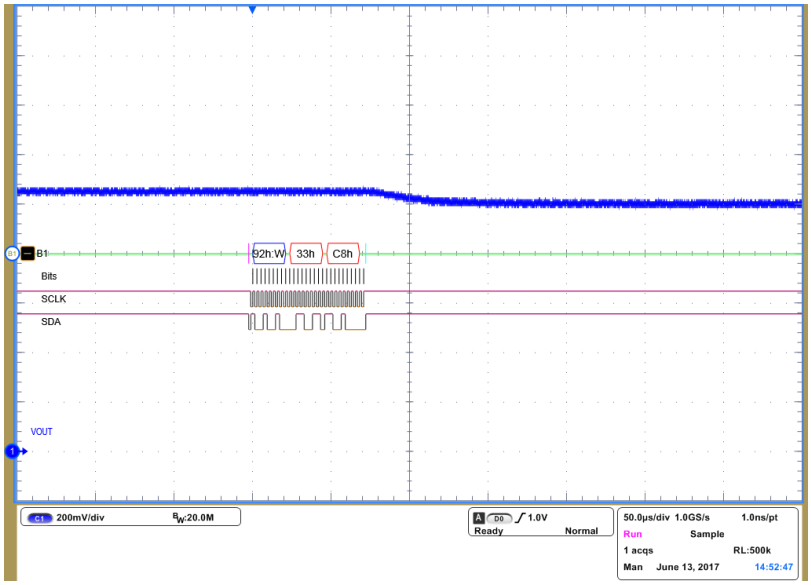

Figure 16: DVC Step-Down from 1.05 V to 1.0 V

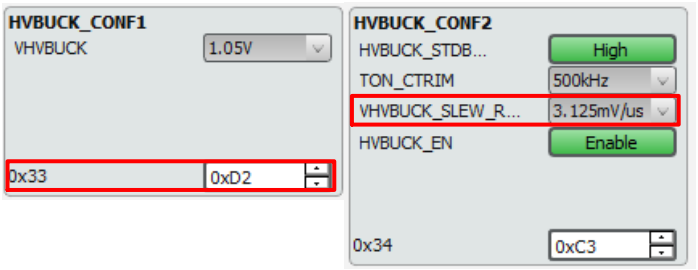

Figure 17: Sending 0xD2 to HVBUCK in Dialog GUI

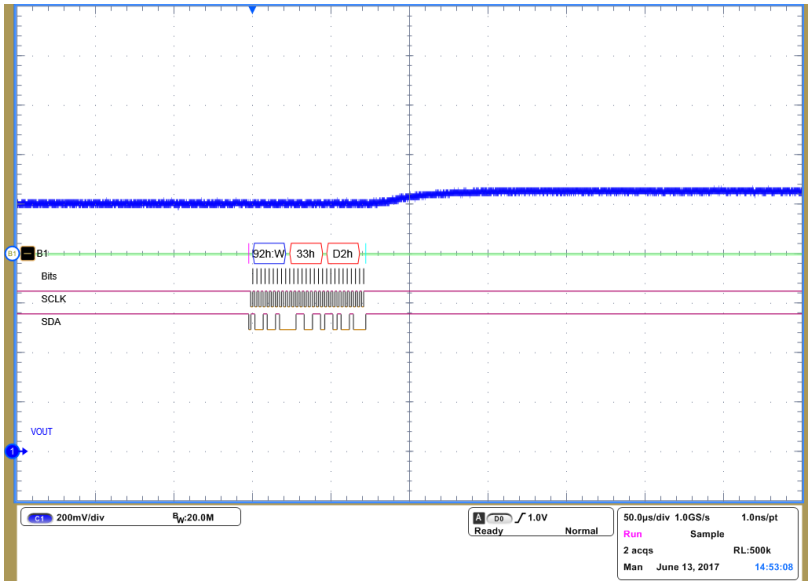

Figure 18: DVC Step-Up from 1.0 V to 1.05 V

5 Conclusions

Both the LVBUCK and HVBUCK in PV88080 support DVC function. The flexible DVC slew rate prevents overshoot and undershoot in different applications. The I^2C interface provides a standard and flexible way to control this feature.

Revision History

Revision	Date	Description
1.0	17-Aug-2017	Initial version.

Disclaimer

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Singapore
Dialog Semiconductor Singapore
Phone: +65 64 8499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 3769 5200

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.