Application Note

Implementing Power Fail Detection or Audio Mute Using The PV88080

AN-PV-002

Abstract

The application note describes how to use the Power Fail Detection and Audio Mute functions of the PV88080.

Contents

Figures

Tables

1 Terms and Definitions

OTP: One Time Programmable memory used in the PV88080 to store operational settings.

2 References

[1] PV88080 Datasheet, Dialog Semiconductor.

3 Introduction

This application note describes how to utilize the power fail/audio mute function on the PV88080. These two functions share a common implementation in that both functions monitor the input rail voltage on the PV88080 and detect a pre-programmed condition (threshold) that when established will cause a interrupt signal to be sent to the host application processor. For the Mute function, there are 4 selectable voltages to choose from configured via OTP. For the Power Fail Detect function, an external resistive divider is used to set the trip point of the on-chip comparator. Once the OTP configured output is asserted the host processor will either begin an orderly shut-down of the system or will signal an on board audio power amp to mute the audio out line. OTP configuration is pre-programmed by Dialog to support the specific customer application.

4 Mute function

This section describes the operation of the Mute function. Figure 1 shows the high level implementation of the function.

VIN_Supply is monitored via the internal resistive divider. When the voltage on the positive side of the comparator falls below VREF, the mute function is activated and a signal is produced on one of three pins depending on OTP programming. This signal can be used to control the audio mute pin of the power amplifier.

The trigger level of audio mute should be higher than POR voltage (Vporhi). When voltage on the internal resistive divider drops to the programmed trigger level of audio mute, the device will send mute signal from one of the three pins via the nIRQ pin as shown in Figure 2. The selected pin can then be connected to the mute pin of Audio Amp on PCB (See Figure 1).

Notice that there is 200us one way de-glitch after voltage rise through MUTE trigger level. The voltage must stay higher than the trigger level for 200us during recovery.

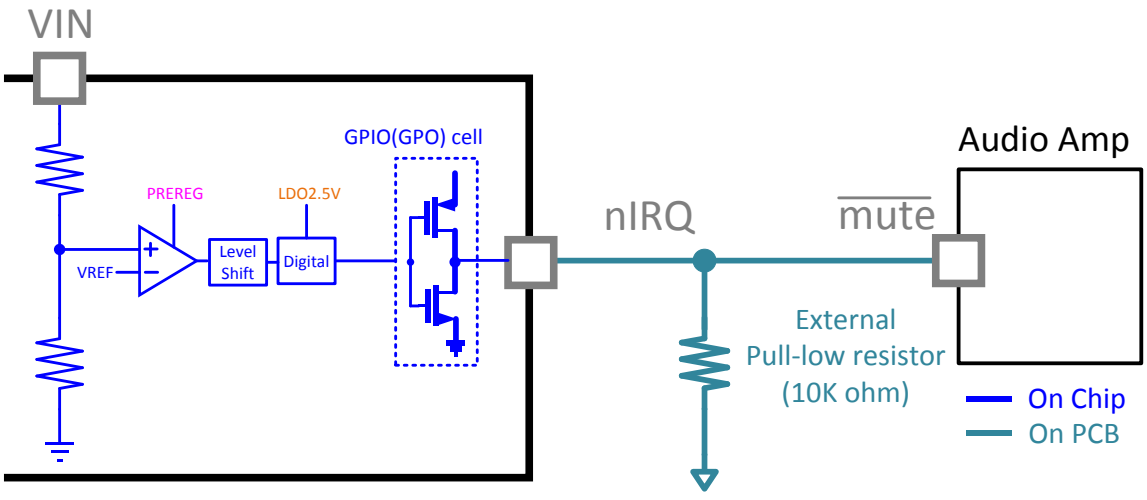

Figure 1: Mute block diagram

Table 1: POR (Power on Reset)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Upper POR threshold	Vporhi		6.5			V
POR Hysteresis Voltage	Vporhys				500	mV

Note 1 PV88080 POR is generated when the Vin_Supply pin voltage rises to 6.5V, A POR event will return the chip to the No POWER condition. All registers will be cleared and the OTP will be reloaded on the next start.

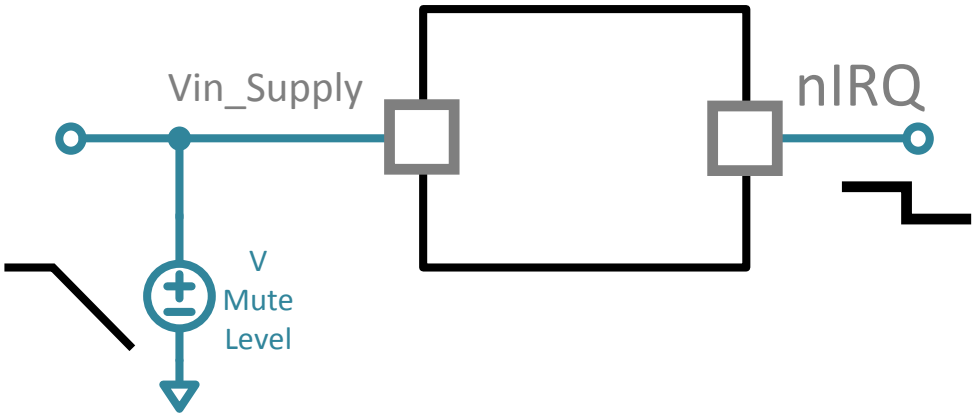

Figure 2: High level operation of the mute function

Table 2: GUI_Mute Level Setting

Based on customer input, the mute level is set by Dialog during the development of the OTP file.

GUI - Control C (0x0E)	V Mute Level Selection
0x32 (00)	8.535/8.53 (V)
0x36 (01)	8.135/8.13 (V)
0x3A (10)	7.43/7.425 (V)
0x3E (11)	6.835/6.83 (V)

Note : The below information is for informational purposes only. These are not user programmable.
Address 0x0E to enable MUTE Function for Green.

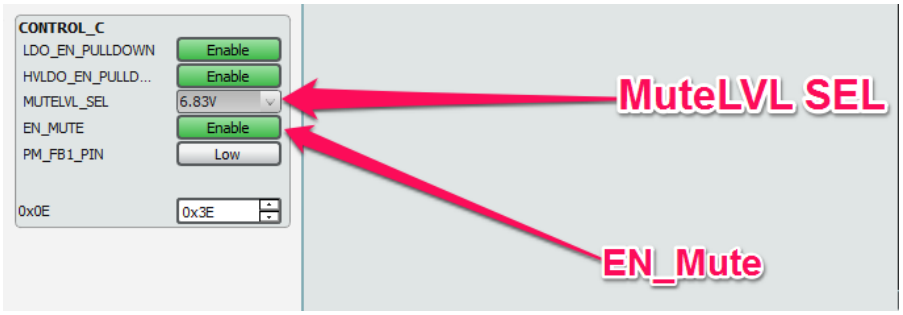

Figure 3: GUI setting 1

Address 0x1B to Setting GPIO_NIRQ_CONF

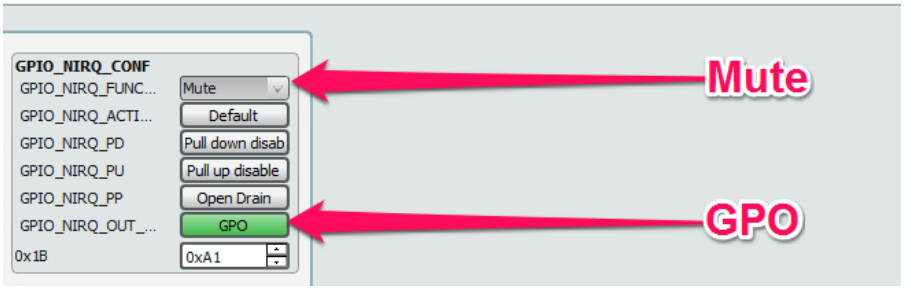

Figure 4: GUI Setting 2

Register Setting - Select a GPIO1 / GPIO2 / nIRQ for Mute

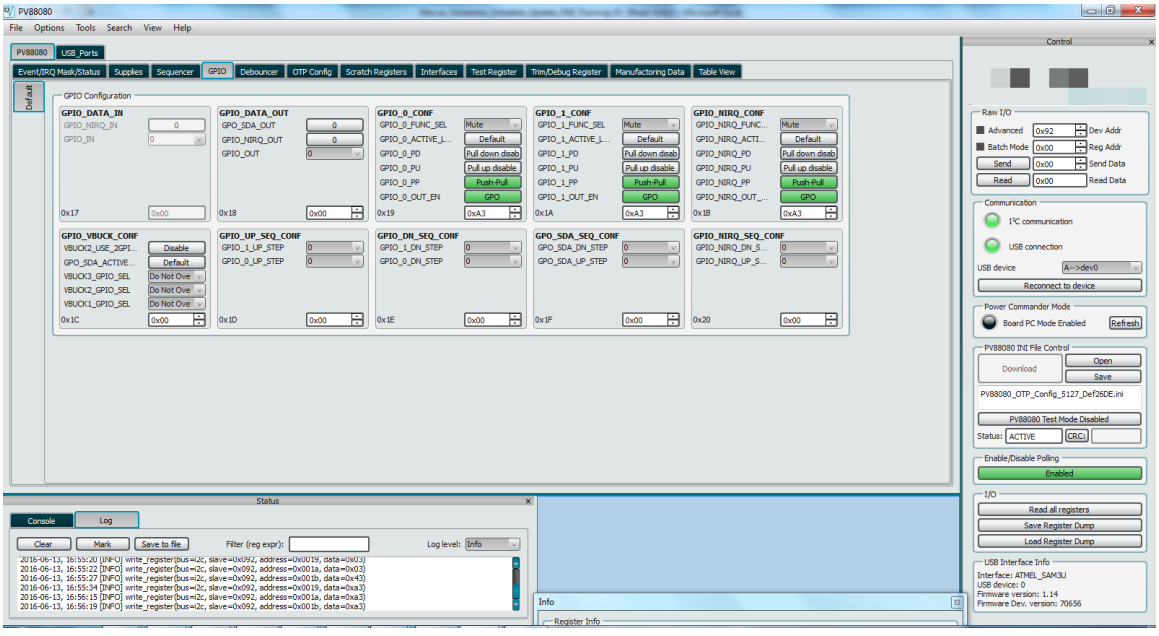

Figure 5: GUI Setting 3

4.1 Summary of the steps need to configure the PV88080 Mute function

- Set VIN=12V
- The PV88080 will enter active mode (we don't need to enable all the bucks)
- Set Register CONTROL_C 0x000E[3:2]=00,01,10,11 (MUTELVL_SEL) respectively
- Set Register CONTROL_C 0x000E[1]=1 (EN_MUTE=1)
- Set Register GPIO_NIRQ_CONF 0x001B[7:0]=1
- Sweep VIN from 12V to 6.5V and monitor nIRQ
- Record the VIN once the nIRQ transitions to the low state.

Typical mute level :

0x000E[3:2]=00 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =8.53V
0x000E[3:2]=01 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =8.13V
0x000E[3:2]=10 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =7.43V
0x000E[3:2]=11 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =6.83V

Figure 6 is the bench measured version of Figure 2.

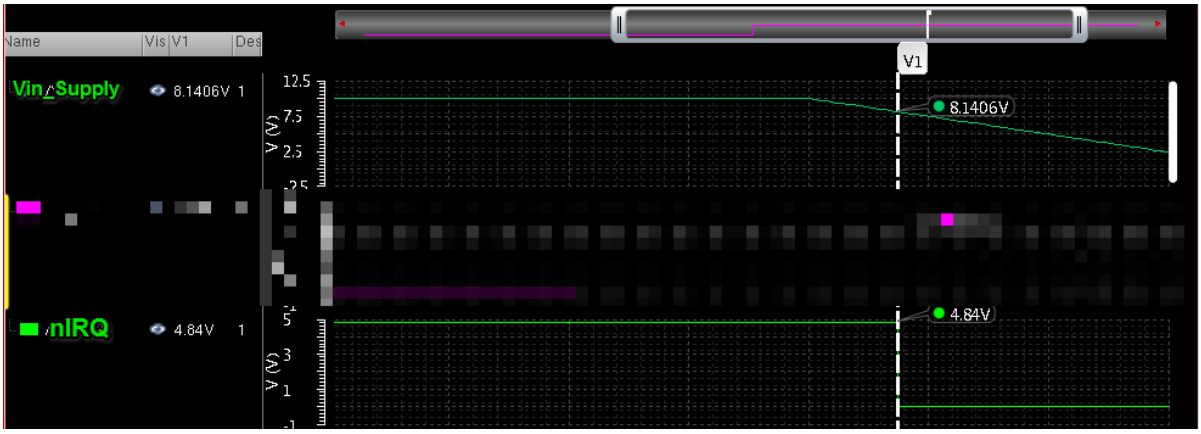

Figure 6: Mute function test

5 Power Fail Detection function

The Power Fail Detection function uses GPIO_2 to monitor the supply voltage as show in Figure 7 For systems not using the GPIO_2 input for power fail detection and power fail detection is enabled in the OTP, GPIO_2 should be pulled up to LDO2P5V (Pin 14) with a 10K ohm resistor.

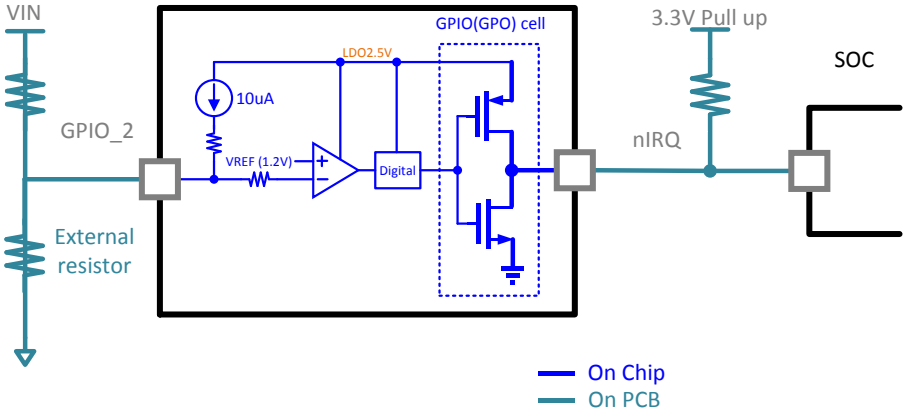

Figure 7: Power Fail function test

Address 0x09 to enable Power Fail Detection

Figure 8: GUI Setting 1

Address 0x1B to Setting GPIO_NIRQ_CONF 0X01

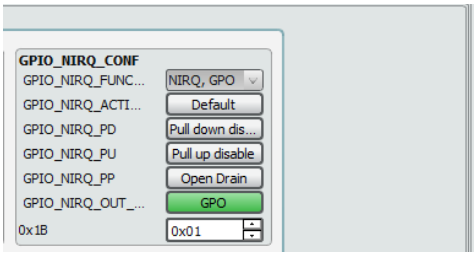

Figure 9: GUI Setting 2

6 Conclusions

The power fail/mute function of the PV88080 can be used to easily control the mute function of an audio amplifier or monitor the supply voltage for low voltage conditions. These functions being fully integrated can result in a reduction in PCB components with corresponding reduction in cost.

Revision History

Revision	Date	Description
1.0	<09-June-2017>	Initial version.
1.1	<07-July-2017>	Syntax and general description/conclusion update
1.4	<06-Oct-2017>	Revised Mute and Power Fail circuit diagram and clarified pin usage. Corrected figure 7 title
1.5	<11-Nov-2017>	Corrected figure 7 title and nIRQ pin location
Change details:		

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

Disclaimer

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Singapore
Dialog Semiconductor Singapore
Phone: +65 64 8499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 3769 5200

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.