

Application Note

Implementing Power Fail Detection or Audio Mute Using The PV88080

AN-PV-002

Abstract

The application note describes how to use the Power Fail Detection and Audio Mute functions of the PV88080.

Implementing Power Fail Detection or Audio Mute Using The PV88080

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Contents

Abstract	1
Contents	2
Figures.....	2
Tables	2
1 Terms and Definitions.....	3
2 References	3
3 Introduction.....	4
4 Mute function	4
4.1 Summary of the steps need to configure the PV88080 Mute function	7
5 Power Fail Detection function.....	7
6 Conclusions	8
Revision History	9

Figures

Figure 1: Mute Block diagram.....	4
Figure 2: High level operation of the mute function.....	5
Figure 3: GUI setting 1	6
Figure 4: GUI Setting 2.....	6
Figure 5: GUI Setting 3.....	6
Figure 6: Mute function test	7
Figure 7: Mute function test	7
Figure 8: GUI Setting 1.....	8
Figure 9: GUI Setting 2.....	8

Tables

Table 1: POR (Power on Reset)	5
Table 2: GUI_Mute Level Setting	5

1 Terms and Definitions

OTP: One Time Programmable memory used in the PV88080 to store operational settings.

2 References

[1] PV88080 Datasheet, Dialog Semiconductor.

3 Introduction

This application note describes how to utilize the power fail/audio mute function on the PV88080. These two functions share a common implementation in that both functions monitor the input rail voltage on the PV88080 and detect a pre-programmed condition (threshold) that when established will cause a interrupt signal to be sent to the host application processor. For the Mute function, there are 4 selectable voltages to choose from configured via OTP. For the Power Fail Detect function, an external resistive divider is used to set the trip point of the on-chip comparator. Once the OTP configured output is asserted the host processor will either begin an orderly shut-down of the system or will signal an on board audio power amp to mute the audio out line. OTP configuration is pre-programmed by Dialog to support the specific customer application.

4 Mute function

This section describes the operation of the Mute function. Figure 1 shows the high level implementation of the function.

VIN_Supply is monitored via the internal resistive divider. When the voltage on the positive side of the comparator falls below VREF, the mute function is activated and a signal is produced on one of three pins depending on OTP programming. This signal can be used to control the audio mute pin of the power amplifier.

The trigger level of audio mute should be higher than POR voltage (Vporhi). When voltage on the internal resistive divider drops to the programmed trigger level of audio mute, the device will send mute signal from one of the three pins via the nIRQ pin as shown in Figure 2. The selected pin can then be connected to the mute pin of Audio Amp on PCB (See Figure 1).

Notice that there is 200us one way de-glitch after voltage rise through MUTE trigger level. The voltage must stay higher than the trigger level for 200us during recovery.

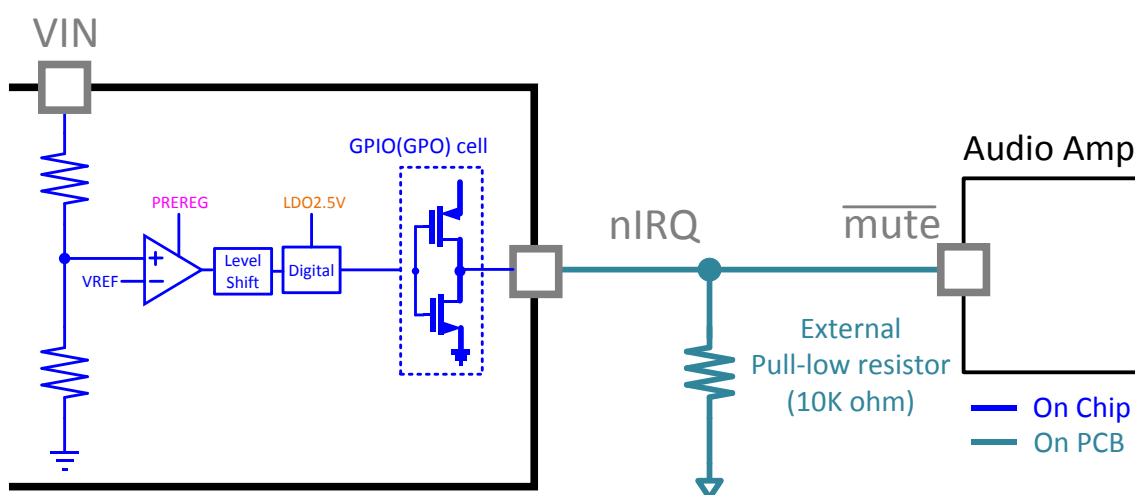


Figure 1: Mute block diagram

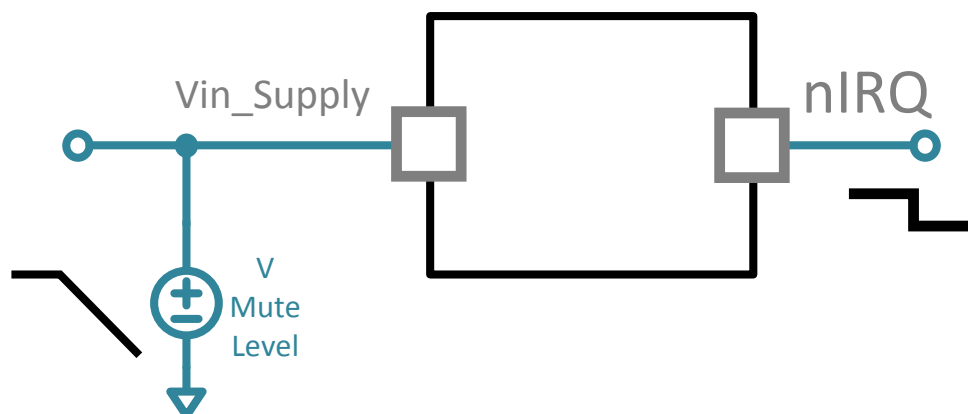
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Table 1: POR (Power on Reset)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Upper POR threshold	Vporhi		6.5			V
POR Hysteresis Voltage	Vporhys				500	mV

Note 1 PV88080 POR is generated when the Vin_Supply pin voltage rises to 6.5V. A POR event will return the chip to the No POWER condition. All registers will be cleared and the OTP will be reloaded on the next start.

**Figure 2: High level operation of the mute function****Table 2: GUI_Mute Level Setting**

Based on customer input, the mute level is set by Dialog during the development of the OTP file.

GUI - Control C (0x0E)	V Mute Level Selection
0x32 (00)	8.535/8.53 (V)
0x36 (01)	8.135/8.13 (V)
0x3A (10)	7.43/7.425 (V)
0x3E (11)	6.835/6.83 (V)

Note : The below information is for informational purposes only. These are not user programmable.
Address 0x0E to enable MUTE Function for Green.

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GPIO_NIRQ_CONF

GPIO_NIRQ_FUNC... Mute

GPIO_NIRQ_ACTI... Default

GPIO_NIRQ_PD Pull down disab

GPIO_NIRQ_PU Pull up disable

GPIO_NIRQ_PP Open Drain

GPIO_NIRQ_OUT... GPO

0x1B 0xA1

Figure 4: GUI Setting 2

The screenshot displays the P8880 USB Parts configuration interface. The main window is titled 'P8880 USB Parts' and contains a 'GPIO Configuration' section. This section is organized into a grid of configuration blocks for various pins (0 to 19). Each block includes a pin number, a 'GPIO_FUNC_SEL' dropdown, and a 'GPIO_FUNC_SEL' button. The pins are configured as follows:

- Pins 0-19: All are set to 'GPIO'.
- GPIO_0_CONF: GPIO_0_FUNC_SEL is set to 'GPIO'.
- GPIO_1_CONF: GPIO_1_FUNC_SEL is set to 'GPIO'.
- GPIO_NIRQ_CONF: GPIO_NIRQ_FUNC_SEL is set to 'GPIO'.
- GPIO_VBRUCK_CONF: VBRUCK_USE_ZGP1 is set to 'Disable'.
- GPIO_DM_SEQ_CONF: GPIO_DM_SEQ_FUNC_SEL is set to 'GPIO'.
- GPIO_SDA_SEQ_CONF: GPIO_SDA_SEQ_FUNC_SEL is set to 'GPIO'.
- GPIO_NIRQ_SEQ_CONF: GPIO_NIRQ_SEQ_FUNC_SEL is set to 'GPIO'.

The 'Status' window at the bottom shows the device is in 'ACTIVE' mode. The 'Console' window at the bottom left displays a log of I2C transactions, including the following commands and responses:

```

2016-06-12, 16:55:20 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:22 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:27 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:28 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:29 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:34 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:35 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:36 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:37 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:38 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:39 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:40 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:41 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:42 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:43 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:44 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:45 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:46 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:47 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:48 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:49 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:50 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:51 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:52 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:53 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:54 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:55 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:56 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:57 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:58 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:55:59 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:00 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:01 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:02 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:03 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:04 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:05 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:06 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:07 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:08 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:09 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:10 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:11 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:12 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:13 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:14 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:15 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:16 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:17 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:18 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:19 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:20 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:21 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:22 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:23 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:24 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:25 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:26 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:27 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:28 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:29 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:30 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:31 [INFO] write_register(bus=2, slave=0x0052, address=0x0019, data=0x03)
2016-06-12, 16:56:32 [INFO] write_register(bus=2, slave=0x0052
```

Figure 5: GUI Setting 3

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4.1 Summary of the steps need to configure the PV88080 Mute function

- Set VIN=12V
- The PV88080 will enter active mode (we don't need to enable all the bucks)
- Set Register CONTROL_C 0x000E[3:2]=00,01,10,11 (MUTELVL_SEL) respectively
- Set Register CONTROL_C 0x000E[1]=1 (EN_MUTE=1)
- Set Register GPIO_NIRQ_CONF 0x001B[7:0]=1
- Sweep VIN from 12V to 6.5V and monitor nIRQ
- Record the VIN once the nIRQ transitions to the low state.

Typical mute level :

0x000E[3:2]=00 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =8.53V
 0x000E[3:2]=01 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =8.13V
 0x000E[3:2]=10 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =7.43V
 0x000E[3:2]=11 (MUTELVL_SEL), nIRQ toggle @ VIN_Supply =6.83V

Figure 6 is the bench measured version of Figure 2.

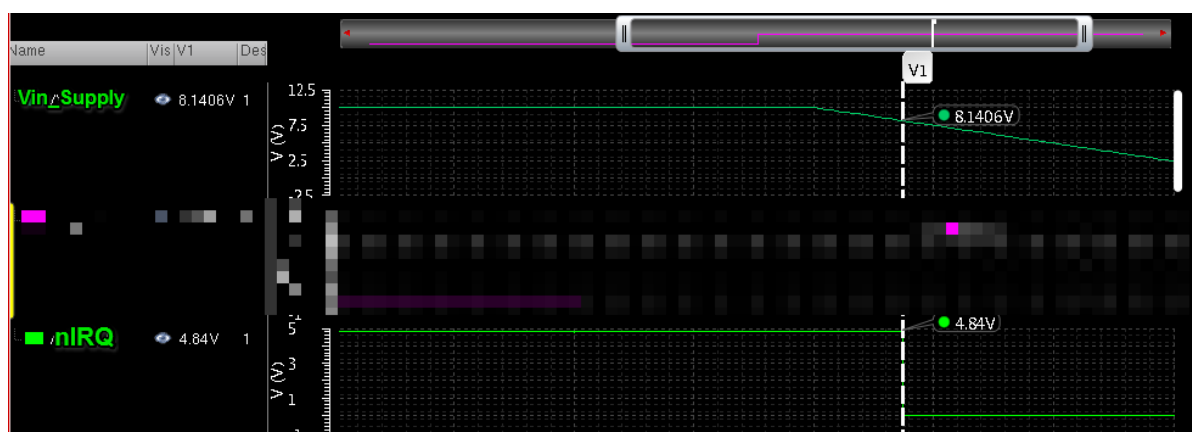


Figure 6: Mute function test

5 Power Fail Detection function

The Power Fail Detection function uses GPIO_2 to monitor the supply voltage as show in Figure 7. For systems not using the GPIO_2 input for power fail detection and power fail detection is enabled in the OTP, GPIO_2 should be pulled up to LDO2P5V (Pin 14) with a 10K ohm resistor.

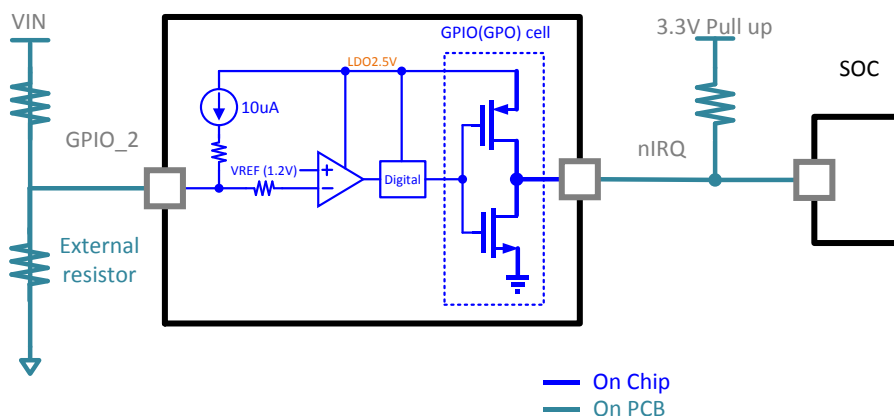


Figure 7: Power Fail function test

Address 0x09 to enable Power Fail Detection



Figure 8: GUI Setting 1

Address 0x1B to Setting GPIO_NIRQ_CONF 0x01

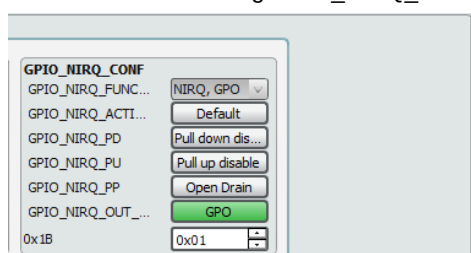


Figure 9: GUI Setting 2

6 Conclusions

The power fail/mute function of the PV88080 can be used to easily control the mute function of an audio amplifier or monitor the supply voltage for low voltage conditions. These functions being fully integrated can result in a reduction in PCB components with corresponding reduction in cost.

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Revision History

Revision	Date	Description
1.0	<09-June-2017>	Initial version.
1.1	<07-July-2017>	Syntax and general description/conclusion update
1.4	<06-Oct-2017>	Revised Mute and Power Fail circuit diagram and clarified pin usage. Corrected figure 7 title
1.5	<11-Nov-2017>	Corrected figure 7 title and nIRQ pin location
Change details:		

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Status	Definition
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