# RL78/F14 Application Note

## Porting guide from 78K0R/Fx3 to RL78/F14

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## Abstract

This application note explains the differences between the functions of the RL78/F14 and the 78K0R/Fx3 (x = B, C, E, F, G) and provides examples when porting.

Under certain use conditions, the operations of the microcontroller might be different from the examples shown in this document. So please evaluate sufficiently the products or systems manufactured by you after porting and check the details of each function in the user's manuals.

## Target Device

| | | | | |
|---|---|---|---|---|
| RL78/F14 (30 pins) : | R5F10PAD, | R5F10PAE | | |
| RL78/F14 (32 pins) : | R5F10PBD, | R5F10PBE | | |
| RL78/F14 (48 pins) : | R5F10PGD, | R5F10PGE, | R5F10PGF, | R5F10PGG, |
| | R5F10PGH, | R5F10PGJ | | |
| RL78/F14 (64 pins) : | R5F10PLE, | R5F10PLF, | R5F10PLG, | R5F10PLH, |
| | R5F10PLJ | | | |
| RL78/F14 (80 pins) : | R5F10PME, | R5F10PMF, | R5F10PMG, | R5F10PMH, |
| | R5F10PMJ | | | |
| RL78/F14 (100 pins) : | R5F10PPE, | R5F10PPF, | R5F10PPG, | R5F10PPH, |
| | R5F10PPJ | | | |
| 78K0R/FB3 (30 pins, 32 pins) : | μPD78F1804, | μPD78F1805, | μPD78F1806, | μPD78F1807 |
| 78K0R/FC3 (40 pins) : | μPD78F1808, | μPD78F1809, | μPD78F1810, | μPD78F1811 |
| 78K0R/FC3 (48 pins) : | μPD78F1812, | μPD78F1813, | μPD78F1814, | μPD78F1815, |
| | μPD78F1816, | μPD78F1817, | μPD78F1826, | μPD78F1827, |
| | μPD78F1828, | μPD78F1829, | μPD78F1830 | |
| 78K0R/FE3 (64 pins) : | μPD78F1818, | μPD78F1819, | μPD78F1820, | μPD78F1821, |
| | μPD78F1822, | μPD78F1831, | μPD78F1832, | μPD78F1833, |
| | μPD78F1834, | μPD78F1835 | | |
| 78K0R/FF3 (80 pins) : | μPD78F1823, | μPD78F1824, | μPD78F1825, | μPD78F1836, |
| | μPD78F1837, | μPD78F1838, | μPD78F1839, | μPD78F1840 |
| 78K0R/FG3 (100 pins) : | μPD78F1841, | μPD78F1842, | μPD78F1843, | μPD78F1844, |
| | μPD78F1845 | | | |

## Contents

# 1. Comparison of functions (General)

This application note explains the differences between the functions of the RL78/F14 and the 78K0R/Fx3 (x = B, C, E, F, G) and provides examples when porting.

Under certain use conditions, the operations of the microcontroller might be different from the examples shown in this document. So please evaluate sufficiently the products or systems manufactured by you after porting and check the details of each function in the user's manuals.

The overview of the comparison of functions between the RL78/F14 and the 78K0R/Fx3 is shown in Table 1-1, and the overview is broken down into Table 1-2 to Table 1-8 by the number of pins for each product.

**Table 1-1 Major functions of RL78/F14 which are portable from 78K0R/Fx3 (1/2)**

| Functions (Note 1) | | RL78/F14 | 78K0R/Fx3 | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 48, 64, 96, 128, 192, 256 Kbytes | 24, 32, 48, 64, 96, 128, 192, 256 Kbytes | 39 |
| | Data flash memory | 4, 8 Kbytes | 16 Kbytes | |
| | RAM | 4, 6, 8, 10, 16, 20 Kbytes | 1.5, 2, 3, 4, 6, 8, 12, 16 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | 32.768 kHz<br>(Provided for products with 48, 64, 80, and 100 pins) | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 23, 25, 38, 52, 68, 86<br>(CMOS/N-ch I/O: 9, 13, 16 (Note 3))<br>Input-only: 3, 5 (Shared with oscillator pins: 2, 4)<br>Output-only: 0, 1 | I/O: 19, 21, 27, 32, 46, 62, 80<br>(CMOS/N-ch I/O: 0, 1, 5 (Note 4))<br>Input-only: 2, 4<br>Output-only: 0, 1<br>N-ch open-drain I/O (6 V tolerance): 0, 4 | 57 |
| Interrupts | External | 9, 13, 14, 15, 16 sources | 8, 9, 10, 11, 12 sources | 63 |
| | Internal | 40, 41, 48 sources | 30, 31, 34, 36, 40, 41, 43, 47, 49 sources | |
| | Key input | 6, 8 channels | 0, 4, 8 channels | |
| | Number of interrupt sources | 49, 50, 54, 55, 62, 63, 64 sources | 38, 39, 43, 46, 50, 51, 54, 55, 58, 59, 61 sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing "1" to the target bit of the port output mode register (POM1, POM6, POM7, POM12). For details, see **CHAPTER 3 PIN assignment** and the user's manual.
4. N-ch open-drain output can be selected by writing "1" to the target bit of the port output mode register (POM4, POM7). For details, see **CHAPTER 3 PIN assignment** and the user's manual.

**Table 1-1 Major functions of RL78/F14 which are portable from 78K0R/Fx3 (2/2)**

| Function (Note 1) | | RL78/F14 | | 78K0R/Fx3 | | Page (Note 2) |
|---|---|---|---|---|---|---|
| DMA | | DTC: 1 circuit (37, 38, 44 sources) | | DMA: 2, 4 channels | | 67 |
| Timer | | TAU0: 8 channels, TAU1: 4, 8 channels | | TAU0：8 channels, TAU1：5, 8 channels,<br>TAU2：0, 4, 8 channels | | 73 |
| | | Timer RD: | 2 channels | - | | |
| | | Timer RJ: | 1 channel | - | | |
| | | - | | 16-bit wakeup timer: | 1 channel | |
| | | Real-time clock: | Provided | - | | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 3, 4 channels<br>·Simplified $I^2C$ (Note 3): 3, 4 channels<br>·UART: 2 channels | | SAU0/SAU1/SAU2<br>·CSI: 2, 3, 4 channels<br>·Simplified $I^2C$ (Note 3): 0, 1, 2 channels<br>·UART: 0, 1 channel | | 105 |
| | $I^2C$ | IICA: | 0, 1 channel | - | | |
| | LIN-UART | RLIN3: | 1, 2 channels | UARTF: | 2 channels (Note 4) | |
| | CAN | RS-CAN lite: | 1 channel | 0, 1 channel | | |
| A/D converter | | 10-bit resolution:<br>10, 12, 15, 18, 19, 20, 25, 31 channels | | 10-bit resolution:<br>6, 8, 11, 15, 16, 24 channels | | 112 |
| D/A converter | | 8-bit resolution: | 1 channel | - | | - |
| Flash memory | | Library is necessary for rewriting flash memory | | Library is necessary for rewriting flash memory | | - |
| Operation frequency | | Grade L: | 32 MHz (MAX.) | (A) grade products: | 24 MHz (MAX.) | - |
| | | Grade K: | 24 MHz (MAX.) | (A2) grade products: | 24 MHz (MAX.) | |
| | | Grade Y: | 24 MHz (MAX.) | | | |
| Operating ambient temperature | | Grade L: | -40 to +105°C | (A) grade products: | -40 to +85°C | - |
| | | Grade K: | -40 to +125°C | (A2) grade products: | -40 to +125°C | |
| | | Grade Y: | -40 to +150°C | | | |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
4. LIN reception can be performed by using TAU in combination.

## 1.1 100-pin Products

**Table 1-2 Major functions of RL78/F14 (100 pins) which are portable from 78K0R/FG3 (1/2)**

| Functions (Note 1) | | RL78/F14 (100 pins) | 78K0R/FG3 (100 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 64, 96, 128, 192, 256 Kbytes | 64, 96, 128, 192, 256 Kbytes | 39 |
| | Data flash memory | 4, 8 Kbytes | 16 Kbytes | |
| | RAM | 6, 8, 10, 16, 20 Kbytes | 4, 6, 8, 12, 16 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | 32.768 kHz | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 86<br>(CMOS/N-ch I/O: 16 (Note 3))<br>Input-only: 5 (Shared with oscillator pins: 4)<br>Output-only: 1 | I/O: 80<br>(CMOS/N-ch I/O: 5 (Note 4))<br>Input-only: 4<br>Output-only: 1<br>N-ch open-drain I/O (6 V tolerance): 4 | 57 |
| Interrupts | External | 16 sources | 12 sources | 63 |
| | Internal | 48 sources | 49 sources | |
| | Key input | 8 channels | 8 channels | |
| | Number of interrupt sources | 64 sources | 61 sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM6, POM7, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
4. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM4, POM7). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.

**Table 1-2 Major functions of RL78/F14 (100 pins) which are portable from 78K0R/FG3 (2/2)**

| Function (Note 1) | | RL78/F14 (100 pins) | | 78K0R/FG3 (100 pins) | | Page (Note 2) |
|---|---|---|---|---|---|---|
| DMA | | DTC: 1 circuit (44 sources) | | DMA: 4 channels | | 67 |
| Timer | | TAU0: 8 channels, TAU1: 8 channels | | TAU0: 8 channels, TAU1: 8 channels, TAU2: 8 channels | | 73 |
| | | Timer RD: | 2 channels | - | | |
| | | Timer RJ: | 1 channel | - | | |
| | | - | | 16-bit wakeup timer: | 1 channel | |
| | | Real-time clock: | Provided | - | | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 4 channels<br>·Simplified $I^2C$ (Note 3): 4 channels<br>·UART: 2 channels | | SAU0/SAU1/SAU2<br>·CSI: 4 channels<br>·Simplified $I^2C$ (Note 3): 2 channels<br>·UART: 1 channels | | 105 |
| | $I^2C$ | IICA: | 1 channel | - | | |
| | LIN-UART | RLIN3: | 2 channels | UARTF: | 2 channels (Note 4) | |
| | CAN | RS-CAN lite: | 1 channel | 1 channel | | |
| A/D converter | | 10-bit resolution: | 31 channels | 10-bit resolution: | 24 channels | 112 |
| D/A converter | | 8-bit resolution: | 1 channel | - | | - |
| Flash memory | | Library is necessary for rewriting flash memory | | Library is necessary for rewriting flash memory | | - |
| Operation frequency | | Grade L:<br>Grade K:<br>Grade Y: | 32 MHz (MAX.)<br>24 MHz (MAX.)<br>24 MHz (MAX.) | (A) grade products:<br>(A2) grade products: | 24 MHz (MAX.)<br>24 MHz (MAX.) | - |
| Operating ambient temperature | | Grade L:<br>Grade K:<br>Grade Y: | -40 to +105°C<br>-40 to +125°C<br>-40 to +150°C | (A) grade products:<br>(A2) grade products: | -40 to +85°C<br>-40 to +125°C | - |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
4. LIN reception can be performed by using TAU in combination.

## 1.2 80-pin Products

**Table 1-3 Major functions of RL78/F14 (80 pins) which are portable from 78K0R/FF3 (1/2)**

| Functions (Note 1) | | RL78/F14 (80 pins) | 78K0R/FF3 (80 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 64, 96, 128, 192, 256 Kbytes | 64, 96, 128, 192, 256 Kbytes | 39 |
| | Data flash memory | 4, 8 Kbytes | 16 Kbytes | |
| | RAM | 6, 8, 10, 16, 20 Kbytes | 4, 6, 8, 12, 16 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | 32.768 kHz | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 68<br>(CMOS/N-ch I/O: 16 (Note 3))<br>Input-only: 5 (Shared with oscillator pins: 4)<br>Output-only: 1 | I/O: 62<br>(CMOS/N-ch I/O: 5 (Note 4))<br>Input-only: 4<br>Output-only: 1<br>N-ch open-drain I/O (6 V tolerance): 4 | 57 |
| Interrupts | External | 14 (Note 6), 16 (Note 5) sources | 12 sources | 63 |
| | Internal | 41 (Note 6), 48 (Note 5) sources | 43 (Note 8), 47 (Note 7) sources | |
| | Key input | 8 channels | 8 channels | |
| | Number of interrupt sources | 55 (Note 6), 64 (Note 5) sources | 55 (Note 8), 59 (Note 7) sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM6, POM7, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
4. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM4, POM7). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
5. R5F10PMx (x = G, H, J) products
6. R5F10PMx (x = E, F) products
7. µPD78F18yy (yy = 36, 37, 38, 39, 40) products
8. µPD78F18yy (yy = 23, 24, 25) products

**Table 1-3 Major functions of RL78/F14 (80 pins) which are portable from 78K0R/FF3 (2/2)**

| Function (Note 1) | | RL78/F14 (80 pins) | 78K0R/FF3 (80 pins) | Page (Note 2) |
|---|---|---|---|---|
| DMA | | DTC: 1 circuit (38 (Note 4), 44 (Note 3) sources) | DMA: 4 channels | 67 |
| Timer | | TAU0: 8 channels, TAU1: 4 (Note 4), 8(Note 3), channels | TAU0: 8 channels, TAU1: 8 channels, TAU2: 4 channels | 73 |
| | | Timer RD: 2 channels | - | |
| | | Timer RJ: 1 channel | - | |
| | | - | 16-bit wakeup timer: 1 channel | |
| | | Real-time clock: Provided | - | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 4 channels<br>·Simplified $I^2C$ (Note 5): 4 channels<br>·UART: 2 channels | SAU0/SAU1/SAU2<br>·CSI: 3 channels<br>·Simplified $I^2C$ (Note 5): 2 channels<br>·UART: 1 channels | 105 |
| | $I^2C$ | IICA: 1 channels | - | |
| | LIN-UART | RLIN3:1 (Note 4), 2 (Note 3) channels | UARTF: 2 channels (Note 6) | |
| | CAN | RS-CAN lite: 1 channel | 0 (Note 8), 1 (Note 7) channel | |
| A/D converter | | 10-bit resolution: 20 (Note 4), 25 (Note 3) channels | 10-bit resolution: 16 channels | 112 |
| D/A converter | | 8-bit resolution: 1 channel | - | - |
| Flash memory | | Library is necessary for rewriting flash memory | Library is necessary for rewriting flash memory | - |
| Operation frequency | | Grade L: 32 MHz (MAX.)<br>Grade K: 24 MHz (MAX.)<br>Grade Y: 24 MHz (MAX.) | (A) grade products: 24 MHz (MAX.)<br>(A2) grade products: 24 MHz (MAX.) | - |
| Operating ambient temperature | | Grade L: -40 to +105°C<br>Grade K: -40 to +125°C<br>Grade Y: -40 to +150°C | (A) grade products: -40 to +85°C<br>(A2) grade products: -40 to +125°C | - |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. R5F10PMx (x = G, H, J) products
4. R5F10PMx (x = E, F) products
5. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
6. LIN reception can be performed by using TAU in combination.
7. µPD78F18yy (yy = 36, 37, 38, 39, 40) products
8. µPD78F18yy (yy = 23, 24, 25) products

## 1.3 64-pin Products

**Table 1-4 Major functions of RL78/F14 (64 pins) which are portable from 78K0R/FE3 (1/2)**

| Functions (Note 1) | | RL78/F14 (64 pins) | 78K0R/FE3 (64 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 64, 96, 128, 192, 256 Kbytes | 32, 48, 64, 96, 128, 192, 256 Kbytes | 39 |
| | Data flash memory | 4, 8 Kbytes | 16 Kbytes | |
| | RAM | 6, 8, 10, 16, 20 Kbytes | 2, 3, 4, 6, 8, 12, 16 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | 32.768 kHz | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 52<br>(CMOS/N-ch I/O: 16 (Note 3))<br>Input-only: 5 (Shared with oscillator pins: 4)<br>Output-only: 1 | I/O: 46<br>(CMOS/N-ch I/O: 5 (Note 4))<br>Input-only: 4<br>Output-only: 1<br>N-ch open-drain I/O (6 V tolerance): 4 | 57 |
| Interrupts | External | 14 (Note 6), 15 (Note 5) sources | 10 (Note 8), 11 (Note 7) sources | 63 |
| | Internal | 41 (Note 6), 48 (Note 5) sources | 41 (Note 8), 43 (Note 10), 47 (Note 9) sources | |
| | Key input | 8 channels | 8 channels | |
| | Number of interrupt sources | 55 (Note 6), 63 (Note 5) sources | 51 (Note 8), 54 (Note 10), 58 (Note 9) sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes
1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM6, POM7, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
4. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM4, POM7). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
5. R5F10PLx (x = G, H, J) products
6. R5F10PLx (x = E, F) products
7. µPD78F18yy (yy = 21, 22, 31, 32, 33, 34, 35) products
8. µPD78F18yy (yy = 18, 19, 20) products
9. µPD78F18yy (yy = 31, 32, 33, 34, 35) products
10. µPD78F18yy (yy = 21, 22) products

**Table 1-4 Major functions of RL78/F14 (64 pins) which are portable from 78K0R/FE3 (2/2)**

| Function (Note 1) | | RL78/F14 (64 pins) | 78K0R/FE3 (64 pins) | Page (Note 2) |
|---|---|---|---|---|
| DMA | | DTC: 1 circuit (38 (Note 4), 44 (Note 3) sources) | DMA: 4 channels | 67 |
| Timer | | TAU0: 8 channels, TAU1: 4 (Note 4), 8 (Note 3) channels | TAU0: 8 channels, TAU1: 8 channels, TAU2: 4 channels | 73 |
| | | Timer RD: 2 channels | - | |
| | | Timer RJ: 1 channel | - | |
| | | - | 16-bit wakeup timer: 1 channel | |
| | | Real-time clock: Provided | - | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 4 channels<br>·Simplified $I^2C$ (Note 5): 4 channels<br>·UART: 2 channels | SAU0/SAU1/SAU2<br>·CSI: 3 channels<br>·Simplified $I^2C$ (Note 5): 1 (Note 8), 2 (Note 7) channels<br>·UART: 0 (Note 8) , 1 (Note 7) channels | 105 |
| | $I^2C$ | IICA: 1 channel | - | |
| | LIN-UART | RLIN3: 1 (Note 4), 2 (Note 3) channels | UARTF: 2 channels (Note 6) | |
| | CAN | RS-CAN lite: 1 channel | 0 (Note 10), 1 (Note 9) channel | |
| A/D converter | | 10-bit resolution: 19 (Note 4) , 20 (Note 3) channels | 10-bit resolution: 15 channels | 112 |
| D/A converter | | 8-bit resolution: 1 channel | - | - |
| Flash memory | | Library is necessary for rewriting flash memory | Library is necessary for rewriting flash memory | - |
| Operation frequency | | Grade L: 32 MHz (MAX.)<br>Grade K: 24 MHz (MAX.)<br>Grade Y: 24 MHz (MAX.) | (A) grade products: 24 MHz (MAX.)<br>(A2) grade products: 24 MHz (MAX.) | - |
| Operating ambient temperature | | Grade L: -40 to +105°C<br>Grade K: -40 to +125°C<br>Grade Y: -40 to +150°C | (A) grade products: -40 to +85°C<br>(A2) grade products: -40 to +125°C | - |

Notes
1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. R5F10PLx (x = G, H, J) products
4. R5F10PLx (x = E, F) products
5. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
6. LIN reception can be performed by using TAU in combination.
7. μPD78F18yy (yy = 21, 22, 31, 32, 33, 34, 35) products
8. μPD78F18yy (yy = 18, 19, 20) products
9. μPD78F18yy (yy = 31, 32, 33, 34, 35) products
10. μPD78F18yy (yy = 18, 19, 20, 21, 22) products

## 1.4 48-pin Products

**Table 1-5 Major functions of RL78/F14 (48 pins) which are portable from 78K0R/FC3 (48 pins) (1/2)**

| Functions (Note 1) | | RL78/F14 (48 pins) | 78K0R/FC3 (48 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 48, 64, 96, 128, 192, 256 Kbytes | 24, 32, 48, 64, 96, 128, 192, 256 Kbytes | 39 |
| | Data flash memory | 4, 8 Kbytes | 16 Kbytes | |
| | RAM | 4, 6, 8, 10, 16, 20 Kbytes | 1.5, 2, 3, 4, 6, 8, 12, 16 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | 32.768 kHz | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 38<br>(CMOS/N-ch I/O: 16 (Note 3))<br>Input-only: 5 (Shared with oscillator pins: 4)<br>Output-only: 1 | I/O: 32<br>(CMOS/N-ch I/O: 1 (Note 4))<br>Input-only: 4<br>Output-only: 1<br>N-ch open-drain I/O (6 V tolerance): 4 | 57 |
| Interrupts | External | 13 (Note 6), 14 (Note 5) sources | 10 sources | 63 |
| | Internal | 41 (Note 6), 48 (Note 5) sources | 36 (Note 8), 40 (Note 7) sources | |
| | Key input | 8 channels | 4 channels | |
| | Number of interrupt sources | 54 (Note 6), 62 (Note 5) sources | 46 (Note 8), 50 (Note 7) sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM6, POM7, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
4. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM7). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
5. R5F10PGx (x = G, H, J) products
6. R5F10PGx (x = D, E, F) products
7. µPD78F18yy (yy = 26, 27, 28, 29, 30) products
8. µPD78F18yy (yy = 12, 13, 14, 15, 16, 17) products

**Table 1-5 Major functions of RL78/F14 (48 pins) which are portable from 78K0R/FC3 (48 pins) (2/2)**

| Function (Note 1) | | RL78/F14 (48 pins) | 78K0R/FC3 (48 pins) | Page (Note 2) |
|---|---|---|---|---|
| DMA | | DTC: 1 circuit: (38 (Note 4), 44 (Note 3) sources) | DMA: 4 channels | 67 |
| Timer | | TAU0: 8 channels, TAU1: 4 (Note 4), 8 (Note 3) channels | TAU0: 8 channels, TAU1: 8 channels | 73 |
| | | Timer RD: 2 channels | - | |
| | | Timer RJ: 1 channel | - | |
| | | - | 16-bit wakeup timer: 1 channel | |
| | | Real-time clock: Provided | - | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 4 channels<br>·Simplified $I^2C$ (Note 5): 4 channels<br>·UART: 2 channels | SAU0/SAU1<br>·CSI: 2 channels<br>·Simplified $I^2C$ (Note 5): 1 channel | 105 |
| | $I^2C$ | IICA 1 channel | - | |
| | LIN-UART | RLIN3:1 (Note 4), 2 (Note 3) channels | UARTF: 2 channels (Note 6) | |
| | CAN | RS-CAN lite: 1 channel | 0 (Note 8), 1 (Note 7) channel | |
| A/D converter | | 10-bit resolution: 15 (Note 4), 18 (Note 3) channels | 10-bit resolution: 11 channels | 112 |
| D/A converter | | 8-bit resolution: 1 channel | - | - |
| Flash memory | | Library is necessary for rewriting flash memory | Library is necessary for rewriting flash memory | - |
| Operation frequency | | Grade L: 32 MHz (MAX.)<br>Grade K: 24 MHz (MAX.)<br>Grade Y: 24 MHz (MAX.) | (A) grade products: 24 MHz (MAX.)<br>(A2) grade products: 24 MHz (MAX.) | - |
| Operating ambient temperature | | Grade L: -40 to +105°C<br>Grade K: -40 to +125°C<br>Grade Y: -40 to +150°C | (A) grade products: -40 to +85°C<br>(A2) grade products: -40 to +125°C | - |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. R5F10PGx (x = G, H, J) products
4. R5F10PGx (x = D, E, F) products
5. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
6. LIN reception can be performed by using TAU in combination.
7. µPD78F18yy (yy = 26, 27, 28, 29, 30) products
8. µPD78F18yy (yy = 12, 13, 14, 15, 16, 17) products

## 1.5 40-pin Products

Since the RL78/F14 does not support 40-pin products, Table 1-6 shows the comparison of major functions between the 48-pin products of the RL78/F14 and the 40-pin products of the 78K0R/FC3.

**Table 1-6 Major functions of RL78/F14 (48 pins) which are portable from 78K0R/FC3 (40 pins) (1/2)**

| Functions (Note 1) | | RL78/F14 (48 pins) | 78K0R/FC3 (40 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 48, 64, 96, 128, 192, 256 Kbytes | 24, 32, 48, 64 Kbytes | 39 |
| | Data flash memory | 4, 8 Kbytes | 16 Kbytes | |
| | RAM | 4, 6, 8, 10, 16, 20 Kbytes | 1.5, 2 ,3 ,4 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | 32.768 kHz | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 38<br>(CMOS/N-ch I/O: 16 (Note 3))<br>Input-only: 5 (Shared with oscillator pins: 4)<br>Output-only: 1 | I/O: 27<br>(CMOS/N-ch I/O: 1 (Note 4))<br>Input-only: 2<br>N-ch open-drain I/O (6 V tolerance): 4 | 57 |
| Interrupts | External | 13 (Note 6), 14 (Note 5) sources | 9 sources | 63 |
| | Internal | 41 (Note 6), 48 (Note 5) sources | 34 sources | |
| | Key input | 8 channels | 4 channels | |
| | Number of interrupt sources | 54 (Note 6), 62 (Note 5) sources | 43 sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM6, POM7, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
4. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM7). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.
5. R5F10PGx (x = G, H, J) products
6. R5F10PGx (x = D, E, F) products

**Table 1-6 Major functions of RL78/F14 (48 pins) which are portable from 78K0R/FC3 (40 pins) (2/2)**

| Function (Note 1) | | RL78/F14 (48 pins) | 78K0R/FC3 (40 pins) | Page (Note 2) |
|---|---|---|---|---|
| DMA | | DTC: 1 circuit (38 (Note 4), 44 (Note 3) sources) | DMA: 2 channels | 67 |
| Timer | | TAU0: 8 channels,<br>TAU1: 4 (Note 4), 8 (Note 3) channels | TAU0: 8 channels,<br>TAU1: 8 channels | 73 |
| | | Timer RD: 2 channels | - | |
| | | Timer RJ: 1 channel | - | |
| | | - | 16-bit wakeup timer: 1 channel | |
| | | Real-time clock: Provided | - | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 4 channels<br>·Simplified $I^2C$ (Note 5): 4 channels<br>·UART: 2 channels | SAU0/SAU1<br>·CSI: 2 channels<br>·Simplified $I^2C$ (Note 5): 1 channel | 105 |
| | $I^2C$ | IICA: 1 channel | - | |
| | LIN-UART | RLIN3:1 (Note 4), 2 (Note 3) channels | UARTF: 2 channels (Note 6) | |
| | CAN | RS-CAN lite: 1 channel | - | |
| A/D converter | | 10-bit resolution: 15 (Note 4), 18 (Note 3) channels | 10-bit resolution: 8 channels | 112 |
| D/A converter | | 8-bit resolution: 1 channel | - | - |
| Flash memory | | Library is necessary for rewriting flash memory | Library is necessary for rewriting flash memory | - |
| Operation frequency | | Grade L: 32 MHz (MAX.)<br>Grade K: 24 MHz (MAX.)<br>Grade Y: 24 MHz (MAX.) | (A) grade products: 24 MHz (MAX.)<br>(A2) grade products: 24 MHz (MAX.) | - |
| Operating ambient temperature | | Grade L: -40 to +105°C<br>Grade K: -40 to +125°C<br>Grade Y: -40 to +150°C | (A) grade products: -40 to +85°C<br>(A2) grade products: -40 to +125°C | - |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. R5F10PGx (x = G, H, J) products
4. R5F10PGx (x = D, E, F) products
5. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
6. LIN reception can be performed by using TAU in combination.

## 1.6 32-pin Products

**Table 1-7 Major functions of RL78/F14 (32 pins) which are portable from 78K0R/FB3 (32 pins) (1/2)**

| Functions (Note 1) | | RL78/F14 (32 pins) | 78K0R/FB3 (32 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 48, 64 Kbytes | 24, 32, 48, 64 Kbytes | 39 |
| | Data flash memory | 4 Kbytes | 16 Kbytes | |
| | RAM | 4, 6 Kbytes | 1.5, 2, 3, 4 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | - | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | On-chip oscillator | low-speed ($f_{IL}$): 15 kHz (TYP.)<br>high-speed ($f_{IH}$): 64 MHz (TYP.)<br>48 MHz (TYP.)<br>32 MHz (TYP.)<br>24 MHz (TYP.)<br>16 MHz (TYP.)<br>12 MHz (TYP.)<br>8 MHz (TYP.)<br>4 MHz (TYP.)<br>1 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 8 MHz (TYP.)<br>4 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 25<br>(CMOS/N-ch I/O: 13 (Note 3))<br>Input-only: 3 (Shared with oscillator pins: 2) | I/O: 19<br>(CMOS/N-ch I/O: -)<br>Input-only: 2<br>N-ch open-drain I/O (6 V tolerance): 4 | 57 |
| Interrupts | External | 9 sources | 8 sources | 63 |
| | Internal | 41 sources | 31 sources | |
| | Key input | 6 channels | - | |
| | Number of interrupt sources | 50 sources | 39 sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM6, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.

**Table 1-7 Major functions of RL78/F14 (32 pins) which are portable from 78K0R/FB3 (32 pins) (2/2)**

| Function (Note 1) | | RL78/F14 (32 pins) | | 78K0R/FB3 (32 pins) | | Page (Note 2) |
|---|---|---|---|---|---|---|
| DMA | | DTC: 1 circuit (37 sources) | | DMA: 2 channels | | 67 |
| Timer | | TAU0: 8 channels, TAU1: 4 channels | | TAU0: 8 channels, TAU1: 5 channels | | 73 |
| | | Timer RD: | 2 channels | - | | |
| | | Timer RJ: | 1 channel | - | | |
| | | - | | 16-bit wakeup timer: | 1 channel | |
| | | Real-time clock: | Provided | - | | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 3 channels<br>·Simplified $I^2C$ (Note 3): 3 channels<br>·UART: 2 channels | | SAU0/SAU1<br>·CSI: 2 channels<br>·Simplified $I^2C$ (Note 3): 1 channel | | 105 |
| | $I^2C$ | IICA: | 1 channel | - | | |
| | LIN-UART | RLIN3: | 1 channel | UARTF: | 2 channels (Note 4) | |
| | CAN | RS-CAN lite: | 1 channel | - | | |
| A/D converter | | 10-bit resolution: | 10 channels | 10-bit resolution: | 6 channels | 112 |
| D/A converter | | 8-bit resolution: | 1 channel | - | | - |
| Flash memory | | Library is necessary for rewriting flash memory | | Library is necessary for rewriting flash memory | | - |
| Operation frequency | | Grade L:<br>Grade K:<br>Grade Y: | 32 MHz (MAX.)<br>24 MHz (MAX.)<br>24 MHz (MAX.) | (A) grade products:<br>(A2) grade products: | 24 MHz (MAX.)<br>24 MHz (MAX.) | - |
| Operating ambient temperature | | Grade L:<br>Grade K:<br>Grade Y: | -40 to +105°C<br>-40 to +125°C<br>-40 to +150°C | (A) grade products:<br>(A2) grade products: | -40 to +85°C<br>-40 to +125°C | - |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
4. LIN reception can be performed by using TAU in combination.

## 1.7 30-pin Products

**Table 1-8 Major functions of RL78/F14 (30 pins) which are portable from 78K0R/FB3 (30 pins) (1/2)**

| Functions (Note 1) | | RL78/F14 (30 pins) | 78K0R/FB3 (30 pins) | Page (Note 2) |
|---|---|---|---|---|
| CPU | | RL78 CPU core | 78K0R CPU core | 20 |
| Memory | Code flash memory | 48, 64 Kbytes | 24, 32, 48, 64 Kbytes | 39 |
| | Data flash memory | 4 Kbytes | 16 Kbytes | |
| | RAM | 4, 6 Kbytes | 1.5, 2, 3, 4 Kbytes | |
| Reset | Number of reset sources | 7 | 7 | 42 |
| | Power-on-clear | When power supply is rising: 1.56 V (TYP.)<br>When power supply is falling: 1.55 V (TYP.) | When power supply is rising: 1.61 V (TYP.)<br>When power supply is falling: 1.59 V (TYP.) | |
| Voltage detection function | | Voltage is detected: 1 point<br>·Interrupt & reset mode: 4 levels<br>·Reset mode: 6 levels<br>·Interrupt mode: 6 levels | Voltage is detected: 1 point<br>·Reset mode 10 levels<br>·Interrupt mode 10 levels | 48 |
| Clock | Main system clock | 1 MHz to 20 MHz | 2 MHz to 20 MHz | 49 |
| | Subsystem clock | - | - | |
| | On-chip oscillator | Low-speed ($f_{IL}$): 15 kHz (TYP.)<br>High-speed ($f_{IH}$): 1, 4, 8, 12, 16, 24, 32, 48, 64 MHz (TYP.) | Low-speed ($f_{IL}$): 30 kHz (TYP.)<br>High-speed ($f_{IH}$): 4, 8 MHz (TYP.) | |
| | PLL | PLL multiplication factor: ×3, ×4, ×6, ×8 | PLL multiplication factor: ×1, ×6, ×8 | |
| | WDT-dedicated low-speed on-chip oscillator | 15 kHz (TYP.) | - | |
| | Clock monitor function | Provided | Provided | |
| I/O port | | I/O: 23<br>(CMOS/N-ch I/O: 9 (Note 3))<br>Input-only: 3 (Shared with oscillator pins: 2) | I/O: 21<br>(CMOS/N-ch I/O: -)<br>Input-only: 2 | 57 |
| Interrupts | External | 9 sources | 8 sources | 63 |
| | Internal | 40 sources | 30 sources | |
| | Key input | 8 channels | - | |
| | Number of interrupt sources | 49 sources | 38 sources | |
| Watchdog timer | | Provided | Provided | 65 |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. N-ch open-drain output can be selected by writing “1” to the target bit of the port output mode register (POM1, POM12). For details, see **CHAPTER 3 PIN assignment** and the user’s manual.

**Table 1-8 Major functions of RL78/F14 (30 pins) which are portable from 78K0R/FB3 (30 pins) (2/2)**

| Function (Note 1) | | RL78/F14 (30 pins) | | 78K0R/FB3 (30 pins) | | Page (Note 2) |
|---|---|---|---|---|---|---|
| DMA | | DTC: 1 circuit (37 sources) | | DMA: 2 channels | | 67 |
| Timer | | TAU0: 8 channels, TAU1: 4 channels | | TAU0: 8 channels, TAU1: 5 channels | | 73 |
| | | Timer RD: | 2 channels | - | | |
| | | Timer RJ: | 1 channel | - | | |
| | | - | | 16-bit wakeup timer: | 1 channel | |
| | | Real-time clock: | Provided | - | | |
| Serial interface | SAU | SAU0/SAU1<br>·CSI: 3 channels<br>·Simplified $I^2C$ (Note 3): 3 channels<br>·UART: 2 channels | | SAU0/SAU1<br>·CSI: 2 channels | | 105 |
| | $I^2C$ | - | | - | | |
| | LIN-UART | RLIN3: | 1 channel | UARTF: | 2 channels (Note 4) | |
| | CAN | RS-CAN lite: | 1 channel | CAN: | Not provided | |
| A/D converter | | 10-bit resolution: | 12 channels | 10-bit resolution: | 8 channels | 112 |
| D/A converter | | 8-bit resolution: | 1 channel | - | | - |
| Flash memory | | Library is necessary for rewriting flash memory | | Library is necessary for rewriting flash memory | | - |
| Operation frequency | | Grade L: | 32 MHz (MAX.) | (A) grade products: | 24 MHz (MAX.) | - |
| | | Grade K: | 24 MHz (MAX.) | (A2) grade products: | 24 MHz (MAX.) | |
| | | Grade Y: | 24 MHz (MAX.) | | | |
| Operating ambient temperature | | Grade L: | -40 to +105°C | (A) grade products: | -40 to +85°C | - |
| | | Grade K: | -40 to +125°C | (A2) grade products: | -40 to +125°C | |
| | | Grade Y: | -40 to +150°C | | | |

Notes 1. This table does not show all the functions provided for the RL78/F14.
2. The details about porting each function are described on the pages shown.
3. The simplified $I^2C$ (SAU) can perform only master transmission and master reception.
4. LIN reception can be performed by using TAU in combination.

## 2. CPU

Table 2-1 shows the comparison of CPU functions between the RL78/F14 and the 78K0R/Fx3.

**Table 2-1 Comparison of CPU functions between RL78/F14 and 78K0R/Fx3**

| Functions | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Central processing unit | RL78 CPU core | 78K0R CPU core |
| Number of primitive instructions | 81 instructions (Note 1) | 75 instructions |
| Minimum instruction execution time | 31.25 ns ($f_{CLK}$ = 32 MHz) | 41.67 ns ($f_{CLK}$ = 24 MHz) |
| Multiplier /divider (Note 2) | Multiply: 16 bits × 16 bits (signed)<br>16 bits × 16 bits (unsigned) | Multiply: 16 bits ×16 bits = 32 bits |
| | Divide: 32 bits ÷ 32 bits (unsigned) | Divide: 32 bits ÷ 32 bits<br>= 32 bits, 32-bit remainder (division) |
| | Multiply-accumulate: 16 bits × 16 bits + 32 bits (signed)<br>16 bits × 16 bits + 32 bits (unsigned) | - |
| | Arithmetic instructions (extended instruction set): supported | |
| Flag registers | PSW register: 8-bit register<br>·CY flag: Carry flag<br>·ISP0/1 flag: In-service priority flag<br>·AC flag: Auxiliary carry flag<br>·RBS0/1 flag: Register bank select flag<br>·Z flag: Zero flag<br>·IE flag: Interrupt request enable flag | PSW register: 8-bit register<br>·CY flag: Carry flag<br>·ISP0/1 flag: In-service priority flag<br>·AC flag: Auxiliary carry flag<br>·RBS0/1 flag: Register bank select flag<br>·Z flag: Zero flag<br>·IE flag: Interrupt request enable flag |
| General-purpose registers | (8-bit general-purpose register)<br>X register A register<br>C register B register<br>E register D register<br>L register H register<br>(16-bit general-purpose register)<br>→ AX register<br>→ BC register<br>→ DE register<br>→ HL register<br>Two of 8-bit registers above can be used in a pair as a 16-bit register. | (8-bit general-purpose register)<br>X register A register<br>C register B register<br>E register D register<br>L register H register<br>(16-bit general-purpose register)<br>→ AX register<br>→ BC register<br>→ DE register<br>→ HL register<br>Two of 8-bit registers above can be used in a pair as a 16-bit register. |
| Number of register banks | 4 | 4 |

Notes 1. The difference from 78K0R/Fx3 is 6 instructions; multiply, divide, and multiply & accumulate instructions.

2. The RL78/F14 supports Multiply/divide/multiply & accumulate instructions.

# 3. PIN assignment

The comparison of pin assignments between the RL78/F14 (48 pins) and the 78K0R/FC3 (48 pins) is shown in Table 3-1.

Also, the comparison of the pin functions between the RL78/F14 and the 78K0R/Fx3 is shown in Table 3-2 to Table 3-8, broken down by the number of pins for each product.

## 3.1 Comparison of pin assignments (Example of 48-pin products)

**Table 3-1 Comparison of pin assignments between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (1/5)**

| Pin No. | RL78/F14 | 78K0R/FC3 | Match determination | Differences in functions |
|---|---|---|---|---|
| 1 | P120 | P120 | ● | [RL78] N-ch open-drain output can be selected using the POM12 register |
| | INTP4 | INTP0 | ▲ | |
| | TI07 | TI11 | ▲ | |
| | TO07 | TO11 | ▲ | |
| | - | EXLVI | | [78K0R] Potential input for external low-voltage detection (Note 1) |
| | SO01 | - | | [RL78] Serial data output from CSI01 |
| | ANI25 | - | | [RL78] Analog input pin |
| | TRDIOD0 | - | | [RL78] Timer RD timer input/output |
| 2 | P41 | P41 | ● | |
| | TI10 | TI07 | ▲ | |
| | TO10 | TO07 | ▲ | |
| | - | TOOL1 | | [78K0R] Clock output for debugger (Note 1) |
| | TRJIO0 | - | | [RL78] Timer RJ timer input/output |
| | SNZOUT2 | - | | [RL78] SNOOZE status output |
| | VCOUT | - | | [RL78] Comparator output pin |
| 3 | P40 | P40 | ● | [RL78] After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected). |
| | TOOL0 | TOOL0 | ● | |
| | - | TI05 | | [78K0R] External count clock input to 16-bit timer |
| | - | TO05 | | [78K0R] 16-bit timer output |
| 4 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ | ● | |
| 5 | P124 | P124 | ● | |
| | EXCLKS | EXCLKS | ● | |
| | XT2 | - | | [RL78] Resonator connection pin for the subsystem clock |
| 6 | P123 | P123 | ● | |
| | XT1 | - | | [RL78] Resonator connection pin for the subsystem clock |
| 7 | - | FLMD0 | | [78K0R] Pin for setting flash memory programming mode (Note 1) |
| | P137 | - | | [RL78] Input port |
| | INTP0 | - | | [RL78] External interrupt input |
| 8 | P122 | P122 | ● | |
| | X2 | X2 | ● | |
| | EXCLK | EXCLK | ● | |
| 9 | P121 | P121 | ● | |
| | X1 | X1 | ● | |
| 10 | REGC | REGC | ● | |
| 11 | $V_{SS}$ | $V_{SS}$ | ● | |
| | - | $EV_{SS}$ | | |
| 12 | $V_{DD}$ | $V_{DD}$ | ● | |
| | - | $EV_{DD}$ | | |
| 13 | P60 | P60 | ● | [RL78] N-ch open-drain output can be selected using the POM6 register |
| | $\overline{\text{SCK00}}$ | $\overline{\text{SCK00}}$ | ● | |
| | SCL00 | SCL11 | ▲ | |
| 14 | P61 | P61 | ● | [RL78] N-ch open-drain output can be selected using the POM6 register |
| | SI00 | SI00 | ● | |
| | SDA00 | SDA11 | ▲ | |
| | RXD0 | - | | [RL78] Serial data input to UART0 |

Remark The functions indicated by the outline characters on a black background are selected after a reset.

● = From the functions and names point of view, the pins are the same as the RL78/F14 pins.

▲ = The functions are the same; however the names of the pins are different.

**Table 3-1 Comparison of pin assignments between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (2/5)**

| Pin No. | RL78/F14 | 78K0R/FC3 | Match determination | Differences in functions |
|---|---|---|---|---|
| 15 | P62 | P62 | ● | [RL78] N-ch open-drain output can be selected using the POM6 register |
| | SO00 | SO00 | ● | |
| | TXD0 | - | | [RL78] Serial data output from UART0 |
| | SCLA0 | - | | [RL78] Clock input/output for IICA0 |
| 16 | P63 | P63 | ● | [RL78] N-ch open-drain output can be selected using the POM6 register |
| | $\overline{SSI00}$ | $\overline{SSI00}$ | ● | |
| | SDAA0 | - | | [RL78] Serial data input/output for IICA0 |
| 17 | P00 | P00 | ● | |
| | TI05 | TI05 | ● | |
| | TO05 | TO05 | ● | |
| | INTP9 | INTP7 | ▲ | |
| 18 | P140 | P140 | ● | [78K0R] Output port after a reset |
| | PCLBUZ0 | PCL | ▲ | [78K0R] Clock output<br>[RL78] Clock output/buzzer output |
| 19 | P130 | P130 | ● | [78K0R, RL78] Output port after a reset |
| | RESOUT | RESOUT | ● | |
| 20 | P73 | P73 | ● | [RL78] (Note 2) |
| | KR3 | KR3 | ● | |
| | - | LRxD1 | | [78K0R] Serial data input to LIN-UART1 → [RL78: 33 pin] |
| | - | INTPLR1 | | [78K0R] LIN-UART1 external interrupt input → [RL78: 33 pin] |
| | CRXD0 | CRxD | ● | [78K0R] (Note 3) |
| | $\overline{SSI11}$ | - | | [RL78] Slave select input to CSI11 |
| | SNZOUT7 | - | | [RL78] SNOOZE status output |
| 21 | P72 | P72 | ● | [RL78] N-ch open-drain output can be selected using the POM7 register |
| | KR2 | KR2 | ● | |
| | SO11 | LTxD1 | ▲ | [78K0R] Serial data output from LIN-UART1 → [RL78:34 pin]<br>[RL78] Serial data output from CSI11. |
| | ANI28 | - | | [RL78] A/D converter analog input (Note 4) |
| | CTXD0 | CTxD | ● | [78K0R] (Note 3) |
| | SNZOUT6 | - | | [RL78] SNOOZE status output |
| 22 | P71 | P71 | ● | [RL78] N-ch open-drain output can be selected using the POM7 register |
| | KR1 | KR1 | ● | |
| | INTP6 | INTP6 | ● | |
| | TI17 | TI17 | ● | [RL78] (Note 4) |
| | TO17 | TO17 | ● | [RL78] (Note 4) |
| | ANI27 | - | | [RL78] A/D converter analog input (Note 4) |
| | $\overline{SCK11}$ | - | | [RL78] Clock input/output for CSI11 |
| | SCL11 | - | | [RL78] Clock output from simplified $I^2C$ |
| | SNZOUT5 | - | | [RL78] SNOOZE status output |

Remark The functions indicated by the outline characters on a black background are selected after a reset.

● = From the functions and names point of view, the pins are the same as the RL78/F14 pins.

▲ = The functions are the same; however the names of the pins are different.

**Table 3-1 Comparison of pin assignments between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (3/5)**

| Pin No. | RL78/F14 | 78K0R/FC3 | Match determination | Differences in functions |
|---|---|---|---|---|
| 23 | P70 | P70 | ● | [RL78] N-ch open-drain output can be selected using the POM7 register. |
| | KR0 | KR0 | ● | |
| | INTP8 | INTP5 | ▲ | |
| | TI15 | TI15 | ● | [RL78] (Note 4) |
| | TO15 | TO15 | ● | [RL78] (Note 4) |
| | - | LVIOUT | | [78K0R] Low-voltage detection flag output (Note 1) |
| | ANI26 | - | | [RL78] A/D converter analog input (Note 4) |
| | SI11 | - | | [RL78] Serial data input to CSI11 |
| | SDA11 | - | | [RL78] Serial data input/output for simplified $I^2C$ |
| | SNZOUT4 | - | | [RL78] SNOOZE status output |
| 24 | P32 | P32 | ● | |
| | INTP7 | INTP4 | ▲ | |
| | TI16 | TI13 | ▲ | [RL78] (Note 4) |
| | TO16 | TO13 | ▲ | [RL78] (Note 4) |
| 25 | P30 | P30 | ● | |
| | $\overline{SSI00}$ | $\overline{SSI00}$ | ● | |
| | INTP2 | INTP2 | ● | |
| | TI01 | TI01 | ● | |
| | TO01 | TO01 | ● | |
| | TRDIOD1 | - | | [RL78] Timer RD1 input/output |
| | SNZOUT0 | - | | [RL78] SNOOZE status output |
| 26 | P17 | P17 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | $\overline{SCK00}$ | $\overline{SCK00}$ | ● | |
| | TI00 | TI14 | ▲ | |
| | TO00 | TO14 | ▲ | |
| | TRDIOB1 | - | | [RL78] Timer RD1 input/output |
| | SCL00 | - | | [RL78] Clock output for simplified $I^2C$ |
| | INTP3 | - | | [RL78] External interrupt request input for which the valid edge can be specified |
| 27 | P16 | P16 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | SI00 | SI00 | ● | |
| | TI02 | TI12 | ▲ | |
| | TO02 | TO12 | ▲ | |
| | TRDIOC1 | - | | [RL78] Timer RD1 input/output |
| | SDA00 | - | | [RL78] Serial data input/output for simplified $I^2C$ |
| | RXD0 | - | | [RL78] Serial data input to UART0 |
| | TOOLRXD | - | | [RL78] UART reception pin for the external device connection used during flash memory programming |
| 28 | P15 | P15 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | SO00 | SO00 | ● | |
| | TI05 | TI10 | ▲ | |
| | TO05 | TO10 | ▲ | |
| | TRDIOA1 | - | | [RL78] Timer RD1 input/output |
| | TRDIOA0 | - | | [RL78] Timer RD0 input/output |
| | TRDCLK0 | - | | [RL78] Timer RD external clock input |
| | TXD0 | - | | [RL78] Serial data output from UART0 |
| | TOOLTXD | - | | [RL78] UART transmission pin for the external device connection used during flash memory programming |
| | RTC1HZ | - | | [RL78] Real-time clock correction clock (1 Hz) output |

Remark The functions indicated by the outline characters on a black background are selected after a reset.
● = From the functions and names point of view, the pins are the same as the RL78/F14 pins.
▲ = The functions are the same; however the names of the pins are different.

**Table 3-1 Comparison of pin assignments between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (4/5)**

| Pin No. | RL78/F14 | 78K0R/FC3 | Match determination | Differences in functions |
|---|---|---|---|---|
| 29 | P31 | P31 | ● | |
| | INTP2 | INTP2 | ● | |
| | STOPST | STOPST | ● | |
| | TI14 | TI11 | ▲ | [RL78] (Note 4) |
| | TO14 | TO11 | ▲ | [RL78] (Note 4) |
| 30 | P14 | P14 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | TI06 | TI06 | ● | |
| | TO06 | TO06 | ● | |
| | LRXD0 | LRxD0 | ● | |
| | - | INTPLR0 | | [78K0R] LIN-UART0 external interrupt |
| | TRDIOC0 | - | | [RL78] Timer RD0 input/output |
| | $\overline{SCK01}$ | - | | [RL78] Clock input/output for CSI01 |
| | SCL01 | - | | [RL78] Clock output from simplified $I^2C$ |
| 31 | P13 | P13 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | LTXD0 | LTxD0 | ● | |
| | TI04 | TI04 | ● | |
| | TO04 | TO04 | ● | |
| | TRDIOA0 | - | | [RL78] Timer RD0 input/output |
| | TRDCLK0 | - | | [RL78] Timer RD external clock input |
| | SI01 | - | | [RL78] Slave select input to CSI01 |
| | SDA01 | - | | [RL78] Serial data input/output for simplified $I^2C$ |
| 32 | P12 | P12 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | SO10 | SO10 | ● | |
| | INTP5 | INTP3 | ▲ | |
| | TI11 | TI16 | ▲ | |
| | TO11 | TO16 | ▲ | |
| | TRDIOD0 | - | | [RL78] Timer RD0 input/output |
| | TXD1 | - | | [RL78] Serial data output from UART1 |
| | SNZOUT3 | - | | [RL78] SNOOZE status output |
| 33 | P11 | P11 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | SI10 | SI10 | ● | |
| | LRXD1 | LRxD1 | ● | [RL78] (Note 4) |
| | TI12 | TI02 | ▲ | |
| | TO12 | TO02 | ▲ | |
| | - | INTPLR1 | | [78K0R] LIN-UART1 external interrupt input |
| | TRDIOB0 | - | | [RL78] Timer RD0 input/output |
| | SDA10 | - | | [RL78] Serial data input/output for simplified $I^2C$ |
| | RXD1 | - | | [RL78] Serial data input to UART1 |
| | CRXD0 | CRxD | ● | [78K0R] (Note 3) |
| 34 | P10 | P10 | ● | [RL78] N-ch open-drain output can be selected using the POM1 register. |
| | $\overline{SCK10}$ | $\overline{SCK10}$ | ● | |
| | LTXD1 | LTxD1 | ● | [RL78] (Note 4) |
| | TI13 | TI00 | ▲ | |
| | TO13 | TO00 | ▲ | |
| | TRJO0 | - | | [RL78] Timer RJ output |
| | SCL10 | - | | [RL78] Clock output from simplified $I^2C$ |
| | CTXD0 | CTxD | ● | [78K0R] (Note 3) |
| 35 | $AV_{REFP}$ | $AV_{REF}$ | ● | |
| | P33 | - | | [RL78] Input/output port |
| | ANI0 | - | | [RL78] A/D converter analog input ($V_{DD}$) |
| 36 | $AV_{REFM}$ | $AV_{SS}$ | ● | |
| | P34 | - | | [RL78] Input/output port |
| | ANI1 | - | | [RL78] A/D converter analog input ($V_{DD}$) |

Remark The functions indicated by the outline characters on a black background are selected after a reset.

● = From the functions and names point of view, the pins are the same as the RL78/F14 pins.

▲ = The functions are the same; however the names of the pins are different.

**Table 3-1 Comparison of pin assignments between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (5/5)**

| Pin No. | RL78/F14 | 78K0R/FC3 | Match determination | Differences in functions |
|---|---|---|---|---|
| 37 | P80 | P80 | ● | |
| | ANI2 | ANI00 | ▲ | |
| | ANO0 | - | | [RL78] D/A converter output |
| 38 | P81 | P81 | ● | |
| | ANI3 | ANI01 | ▲ | |
| | IVCMP00 | - | | [RL78] Comparator analog voltage input |
| 39 | P82 | P82 | ● | |
| | ANI4 | ANI02 | ▲ | |
| | IVCMP01 | - | | [RL78] Comparator analog voltage input |
| 40 | P83 | P83 | ● | |
| | ANI5 | ANI03 | ▲ | |
| | KR0 | - | | [RL78] Key interrupt input |
| | IVCMP02 | - | | [RL78] Comparator analog voltage input |
| 41 | P84 | P84 | ● | |
| | ANI6 | ANI04 | ▲ | |
| | KR1 | - | | [RL78] Key interrupt input |
| | IVCMP03 | - | | [RL78] Comparator analog voltage input |
| 42 | P85 | P85 | ● | |
| | ANI7 | ANI05 | ▲ | |
| | KR2 | - | | [RL78] Key interrupt input |
| | IVREF0 | - | | [RL78] Comparator reference voltage input pin |
| 43 | P86 | P86 | ● | |
| | ANI8 | ANI06 | ▲ | |
| | KR3 | - | | [RL78] Key interrupt input |
| 44 | P87 | P87 | ● | |
| | ANI9 | ANI07 | ▲ | |
| | KR4 | - | | [RL78] Key interrupt input |
| 45 | P90 | P90 | ● | |
| | ANI10 | ANI08 | ▲ | |
| | KR5 | - | | [RL78] Key interrupt input |
| 46 | P91 | P91 | ● | |
| | ANI11 | ANI09 | ▲ | |
| | KR6 | - | | [RL78] Key interrupt input |
| 47 | P92 | P92 | ● | |
| | ANI12 | ANI10 | ▲ | |
| | KR7 | - | | [RL78] Key interrupt input |
| 48 | P125 | P125 | ● | |
| | INTP1 | INTP1 | ● | |
| | TI03 | TI03 | ● | |
| | TO03 | TO03 | ● | |
| | - | ADTRG | | [78K0R] A/D converter external trigger input (Note 1) |
| | ANI24 | - | | [RL78] A/D converter analog input ($EV_{DD}$) |
| | TRDIOB0 | - | | [RL78] Timer RD0 input/output |
| | $\overline{SSI01}$ | - | | [RL78] Slave select input to CSI01 (SPI01) |
| | SNZOUT1 | - | | [RL78] SNOOZE status output |

Remark The functions indicated by the outline characters on a black background are selected after a reset.
- ● = From the functions and names point of view, the pins are the same as the RL78/F14 pins.
- ▲ = The functions are the same; however the names of the pins are different.

Notes
1. Pin only available on the 78K0R/FC3.
2. In R5F10PGG, R5F10PGH, and R5F10PGJ, be sure to clear the PMC73 bit to “0”.
3. µPD78F1812-78F1817 products are not equipped with either CRxD pin or CTxD pin.
4. R5F10PGD, R5F10PGE, and R5F10PGF products are not equipped with the pin function.

## 3.2 Comparison of pin functions between each product

### 3.2.1 100-pin products

**Table 3-2 Comparison of pin functions between RL78/F14 (100 pins) and 78K0R/FG3 (1/3)**

| Pin number | RL78/F14 (100 pins) | 78K0R/FG3 (100 pins) | Differences in functions |
|---|---|---|---|
| 1 | P153/SCK11 | P153/SCK11 | |
| 2 | P152/SI11 | P152/SI11 | |
| 3 | P151/SO11 | P151/SO11 | |
| 4 | P150/SSI11 | P150 | [RL78] SSI11 function is added |
| 5 | P47/INTP13 | P47/INTP8 | |
| 6 | P46/TI12/TO12 | P46/TI12/TO12 | |
| 7 | P45/TI10/TO10 | P45/TI10/TO10 | |
| 8 | P44/TI07/TO07 | P44/TI07/TO07 | |
| 9 | P43/LRXD0 | P43/RxD2/INTPR2/SDA20 | [RL78] LRXD0 function added<br>[78K0R] RxD2/INTPR2/SDA20 functions deleted |
| 10 | P42/LTXD0 | P42/TxD2/SCL20 | [RL78] LTXD0 function added<br>[78K0R] TxD2/SCL20 functions deleted |
| 11 | P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 12 | P40 (Note 2)/TOOL0 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 13 | RESET | RESET | |
| 14 | P124/XT2/EXCLKS | P124/EXCLKS | [RL78] XT2 function added |
| 15 | P123/XT1 | P123 | [RL78] XT1 function added |
| 16 | P137/INTP0 | FLMD0 | [RL78] P137/INTP0 functions added<br>[78K0R] FLMD0 function deleted |
| 17 | P122/X2/EXCLK | P122/X2/EXCLK | |
| 18 | P121/X1 | P121/X1 | |
| 19 | REGC | REGC | |
| 20 | $V_{SS}$ | $V_{SS}$ | |
| 21 | $EV_{SS0}$ | $EV_{SS0}$ | |
| 22 | $V_{DD}$ | $V_{DD}$ | |
| 23 | $EV_{DD0}$ | $EV_{DD0}$ | |
| 24 | P60 (Note 1)/SCK00/SCL00 | P60/SCK00/SCL11 | |
| 25 | P61 (Note 1)/SI00/SDA00 (Note 1)/RXD0 | P61/SI00/SDA11 | [RL78] RXD0 function added |
| 26 | P62 (Note 1)/SO00/TXD0/SCLA0 (Note 1) | P62/SO00 | [RL78] TXD0/SCLA0 functions added |
| 27 | P63 (Note 1)/SSI00/SDAA0 (Note 1) | P63/SSI00 | [RL78] SDAA0 function added |
| 28 | P64/TI14/TO14/SNZOUT3 | P64/TI14/TO14 | [RL78] SNZOUT3 function added |
| 29 | P65/TI16/TO16/SNZOUT2 | P65/TI16/TO16 | [RL78] SNZOUT2 function added |
| 30 | P66/TI00/TO00 | P66/TI00/TO00 | |
| 31 | P67/TI02/TO02 | P67/TI02/TO02 | |
| 32 | P154/SNZOUT7 | P154/TI24/TO24 | [RL78] SNZOUT7 function added<br>[78K0R] TI24/TO24 functions deleted |
| 33 | P155/SNZOUT6 | P155/TI25/TO25 | [RL78] SNZOUT6 function added<br>[78K0R] TI25/TO25 functions deleted |
| 34 | P00/TI05/TO05/INTP9 | P00/TI05/TO05/INTP7 | |
| 35 | P156/SNZOUT5 | P156/TI26/TO26 | [RL78] SNZOUT5 function added<br>[78K0R] TI26/TO26 functions deleted |
| 36 | P157/SNZOUT4 | P157/TI27/TO27 | [RL78] SNZOUT4 function added<br>[78K0R] TI27/TO27 functions deleted |
| 37 | P140/PCLBUZ0 | P140/PCL | |
| 38 | P130/RESOUT | P130/RESOUT | |
| 39 | P77/KR7/SSI10/INTP12 | P77/KR7/SSI01 | [RL78] INTP12 function added |
| 40 | P76/KR6/SCK10 | P76/KR6/SCK01 | |
| 41 | P75/KR5/SI10/RXD1 | P75/KR5/SI01 | [RL78] RXD1 function added |
| 42 | P74/ANI30/KR4/SO10/TXD1 | P74/KR4/SO01 | [RL78] ANI30/TXD1 functions added |
| 43 | $EV_{SS1}$ | $EV_{SS1}$ | |

**Table 3-2 Comparison of pin functions between RL78/F14 (100 pins) and 78K0R/FG3 (2/3)**

| Pin number | RL78/F14 (100 pins) | 78K0R/FG3 (100 pins) | Differences in functions |
|---|---|---|---|
| 44 | P73/ANI29/KR3/CRXD0/SSI11/SNZOUT7 | P73/KR3/CRxD/LRxD1/INTPLR1 | [RL78] ANI29/SSI11/SNZOUT7 functions added<br>[78K0R] LRxD1/INTPLR1 functions deleted |
| 45 | P72 (Note 1)/ANI28/KR2/CTXD0/SO11/ SNZOUT6 | P72/KR2/CTxD/LTxD1 | [RL78] ANI28/SO11/SNZOUT6 functions added<br>[78K0R] LTxD1 function deleted |
| 46 | P71 (Note 1)/ANI27/KR1/TI17/TO17/INTP6/ SCK11/SCL11/SNZOUT5 | P71/KR1/INTP6/TI17/TO17 | [RL78] ANI27/SCK11/SCL11/SNZOUT5 functions added |
| 47 | P70 (Note 1)/ANI26/KR0/TI15/TO15/INTP8/ SI11/SDA11 (Note 1)/SNZOUT4 | P70/KR0/INTP5/TI15/TO15/LVIOUT | [RL78] ANI26/SI11/SDA11/SNZOUT4 functions added<br>[78K0R] LVIOUT function deleted |
| 48 | P03/RTC1HZ | P03 | [RL78] RTC1HZ function added |
| 49 | P32/TI16/TO16/INTP7 | P32/INTP4/TI13/TO13 | |
| 50 | P30/TI01/TO01/TRDIOD1/SSI00/INTP2/ SNZOUT0 | P30/SSI00/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT0 functions added |
| 51 | P17 (Note 1)/TI00/TO00/TRDIOB1/SCK00/ SCL00/INTP3 | P17/SCK00/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 52 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA00 (Note 1)/RXD0/TOOLRXD | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |
| 53 | $EV_{DD1}$ | $EV_{DD1}$ | |
| 54 | P15 (Note 1)/TI05/TO05/TRDIOA1/TRDIOA0/ TRDCLK0/SO00/TXD0/TOOLTXD/RTC1HZ | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/TXD0/ TOOLTXD/RTC1HZ functions added |
| 55 | P31/TI14/TO14/STOPST/INTP2 | P31/INTP2/STOPST/TI11/TO11 | |
| 56 | P50/SSI01/INTP3 | P50/TI20/TO20/INTP3 | [78K0R] TI20/TO20 functions deleted |
| 57 | P51/SO01/INTP11 | P51/TI21/TO21 | [RL78] SO01/INTP11 functions added<br>[78K0R] TI21/TO21 functions deleted |
| 58 | P52/SCK01/STOPST | P52/TI22/TO22/STOPST | [RL78] SCK01 function added<br>[78K0R]TI22/TO22 functions deleted |
| 59 | P53/SI01/INTP10 | P53/TI23/TO23 | [RL78] SI01/INTP10 functions added<br>[78K0R] TI23/TO23 functions deleted |
| 60 | P14 (Note 1)/TI06/TO06/TRDIOC0/SCK01/ SCL01/LRXD0 | P14/LRxD0/INTPLR0/TI06/TO06 | [RL78] TRDIOC0/SCK01/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 61 | P13 (Note 1)/TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01 (Note 1)/LTXD0 | P13/LTxD0/TI04/TO04 | [RL78] TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 62 | P12 (Note 1)/TI11/TO11/TRDIOD0/INTP5/ SO10/TXD1/SNZOUT3 | P12/SO10/INTP3/TI16/TO16 | [RL78] TRDIOD0/TXD1/SNZOUT3 functions added |
| 63 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/LRXD1/CRXD0 | P11/SI10/LRxD1/INTPLR1/CRxD/TI02/TO02 | [RL78] TRDIOB0/SDA10/RXD1 functions added |
| 64 | P10 (Note 1)/TI13/TO13/TRJO0/SCK10/ SCL10/LTXD1/CTXD0 | P10/SCK10/LTxD1/CTxD/TI00/TO00 | [RL78] TRJO0/SCL10 functions added |
| 65 | P54/TI11/TO11/SSI10 | P54/TI11/TO11 | [RL78] SSI10 function added |
| 66 | P55/TI13/TO13 | P55/TI13/TO13 | |
| 67 | P56/TI15/TO15/SNZOUT1 | P56/TI15/TO15 | [RL78] SNZOUT1 function added |
| 68 | P57/TI17/TO17/SNZOUT0 | P57/TI17/TO17 | [RL78] SNZOUT0 function added |
| 69 | P107/LRXD1 | P107/ANI23 | [RL78] LRXD1 function added<br>[78K0R] ANI23 function deleted |
| 70 | P106/LTXD1 | P106/ANI22 | [RL78] LTXD1 function added<br>[78K0R] ANI22 function deleted |
| 71 | P105/ANI23 | P105/ANI21 | |
| 72 | P104/ANI22 | P104/ANI20 | |
| 73 | P33/$AV_{REFP}$/ANI0 | $AV_{REF}$ | [RL78] P33/ANI0 functions added |
| 74 | P34/$AV_{REFM}$/ANI1 | $AV_{SS}$ | [RL78] P34/ANI1 functions added |

**Table 3-2 Comparison of pin functions between RL78/F14 (100 pins) and 78K0R/FG3 (3/3)**

| Pin number | RL78/F14 (100 pins) | 78K0R/FG3 (100 pins) | Differences in functions |
|---|---|---|---|
| 75 | P80/ANI2/ANO0 | P80/ANI00 | [RL78] ANO0 function added |
| 76 | P81/ANI3/IVCMP00 | P81/ANI01 | [RL78] IVCMP00 function added |
| 77 | P82/ANI4/IVCMP01 | P82/ANI02 | [RL78] IVCMP01 function added |
| 78 | P83/ANI5/IVCMP02 | P83/ANI03 | [RL78] IVCMP02 function added |
| 79 | P84/ANI6/IVCMP03 | P84/ANI04 | [RL78] IVCMP03 function added |
| 80 | P85/ANI7/IVREF0 | P85/ANI05 | [RL78] IVREF0 function added |
| 81 | P86/ANI8 | P86/ANI06 | |
| 82 | P87/ANI9 | P87/ANI07 | |
| 83 | P90/ANI10 | P90/ANI08 | |
| 84 | P91/ANI11 | P91/ANI09 | |
| 85 | P92/ANI12 | P92/ANI10 | |
| 86 | P93/ANI13 | P93/ANI11 | |
| 87 | P94/ANI14 | P94/ANI12 | |
| 88 | P95/ANI15 | P95/ANI13 | |
| 89 | P96/ANI16 | P96/ANI14 | |
| 90 | P97/ANI17 | P97/ANI15 | |
| 91 | P100/ANI18 | P100/ANI16 | |
| 92 | P101/ANI19 | P101/ANI17 | |
| 93 | P102/ANI20 | P102/ANI18 | |
| 94 | P103/ANI21 | P103/ANI19 | |
| 95 | P02/TI06/TO06 | P02/TI06/TO06 | |
| 96 | P127/TI03/TO03 | P127/TI03/TO03 | |
| 97 | P126/TI01/TO01 | P126/TI01/TO01 | |
| 98 | P01/TI04/TO04 | P01/TI04/TO04 | |
| 99 | P125/ANI24/TI03/TO03/TRDIOB0/$\overline{\text{SSI01}}$/INTP1/SNZOUT1 | P125/INTP1/ADTRG/TI03/TO03 | [RL78] ANI24/TRDIOB0/$\overline{\text{SSI01}}$/SNZOUT1 functions added<br>[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |
| 100 | P120 (Note 1)/ANI25/TI07/TO07/TRDIOD0/SO01/INTP4 | P120/INTP0/EXLVI | [RL78] TI07/TO07/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 6, 7, 12).

2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).

### 3.2.2 80-pin products

**Table 3-3 Comparison of pin functions between RL78/F14 (80 pins) and 78K0R/FF3 (1/2)**

| Pin number | RL78/F14 (80 pins) | 78K0R/FF3 (80 pins) | Differences in functions |
|---|---|---|---|
| 1 | P120 (Note 1)/ANI25/TI07/TO07/TRDIOD0/ SO01/INTP4 | P120/INTP0/EXLVI | [RL78] ANI25/TI07/TO07/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |
| 2 | P47/INTP13 (Note 3) | P47/INTP8 | |
| 3 | P46/TI12/TO12 | P46/TI12/TO12 | |
| 4 | P45/TI10/TO10 | P45/TI10/TO10 | |
| 5 | P44/TI07/TO07 | P44/TI07/TO07 | |
| 6 | P43/LRXD0 | P43/RxD2/INTPR2/SDA20 | [RL78] LRXD0 function added<br>[78K0R] RxD2/INTPR2/SDA20 functions deleted |
| 7 | P42/LTXD0 | P42/TxD2/SCL20 | [RL78] LTXD0 function added<br>[78K0R] TxD2/SCL20 functions deleted |
| 8 | P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 9 | P40 (Note 2)/TOOL0 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 10 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ | |
| 11 | P124/XT2/EXCLKS | P124/EXCLKS | [RL78] XT2 function added |
| 12 | P123/XT1 | P123 | [RL78] XT1 function added |
| 13 | P137/INTP0 | FLMD0 | [RL78] P137/INTP0 functions added<br>[78K0R] FLMD0 function deleted |
| 14 | P122/X2/EXCLK | P122/X2/EXCLK | |
| 15 | P121/X1 | P121/X1 | |
| 16 | REGC | REGC | |
| 17 | $V_{SS}$ | $V_{SS}$ | |
| 18 | $EV_{SS0}$ | $EV_{SS}$ | |
| 19 | $V_{DD}$ | $V_{DD}$ | |
| 20 | $EV_{DD0}$ | $EV_{DD}$ | |
| 21 | P60 (Note 1)/SCK00/SCL00 | P60/SCK00/SCL11 | |
| 22 | P61 (Note 1)/SI00/SDA00 (Note 1)/RXD0 | P61/SI00/SDA11 | [RL78] RXD0 function added |
| 23 | P62 (Note 1)/SO00/TXD0/SCLA0 (Note 1) | P62/SO00 | [RL78] TXD0/SCLA0 functions added |
| 24 | P63 (Note 1)/SSI00/SDAA0 (Note 1) | P63/SSI00 | [RL78] SDAA0 function added |
| 25 | P64/TI14 (Note 3)/TO14 (Note 3)/SNZOUT3 | P64/TI14/TO14 | [RL78] SNZOUT3 function added |
| 26 | P65/TI16 (Note 3)/TO16 (Note 3)/SNZOUT2 | P65/TI16/TO16 | [RL78] SNZOUT2 function added |
| 27 | P66/TI00/TO00 | P66/TI00/TO00 | |
| 28 | P67/TI02/TO02 | P67/TI02/TO02 | |
| 29 | P00/TI05/TO05/INTP9 | P00/TI05/TO05/INTP7 | |
| 30 | P140/PCLBUZ0 | P140/PCL | |
| 31 | P130/RESOUT | P130/RESOUT | |
| 32 | P77/KR7/SSI10/INTP12 (Note 3) | P77/KR7/SSI01 | [RL78] INTP12 function added |
| 33 | P76/KR6/SCK10 | P76/KR6/SCK01 | |
| 34 | P75/KR5/SI10/RXD1 | P75/KR5/SI01 | [RL78] RXD1 function added |
| 35 | P74/ANI30 (Note 3)/KR4/SO10/TXD1 | P74/KR4/SO01 | [RL78] ANI30/TXD1 functions added |
| 36 | P73/ANI29 (Note 3)/KR3/CRXD0/SSI11/ SNZOUT7 | P73/KR3/CRxD (Note 4)/LRxD1/INTPLR1 | [RL78] ANI29/SSI11/SNZOUT7 functions added<br>[78K0R] LRxD1/INTPLR1 functions deleted |
| 37 | P72 (Note 1)/ANI28 (Note 3)/KR2/CTXD0/ SO11/SNZOUT6 | P72/KR2/CTxD (Note 4)/LTxD1 | [RL78] ANI28/SO11/SNZOUT6 functions added<br>[78K0R] LTxD1 function deleted |
| 38 | P71 (Note 1)/ANI27 (Note 3)/KR1/ TI17 (Note 3)/TO17 (Note 3)/INTP6/SCK11/ SCL11/SNZOUT5 | P71/KR1/INTP6/TI17/TO17 | [RL78] ANI27/SCK11/SCL11/SNZOUT5 functions added |
| 39 | P70 (Note 1)/ANI26 (Note 3)/KR0/ TI15 (Note 3)/TO15 (Note 3)/INTP8/SI11/ SDA11 (Note 1)/SNZOUT4 | P70/KR0/INTP5/TI15/TO15/LVIOUT | [RL78] ANI26/SI11/SDA11/SNZOUT4 functions added<br>[78K0R] LVIOUT function deleted |
| 40 | P32/TI16 (Note 3)/TO16 (Note 3)/INTP7 | P32/INTP4/TI13/TO13 | |
| 41 | P30/TI01/TO01/TRDIOD1/SSI00/INTP2/ SNZOUT0 | P30/SSI00/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT0 functions added |
| 42 | P17 (Note 1)/TI00/TO00/TRDIOB1/SCK00/ SCL00/INTP3 | P17/SCK00/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 43 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA00 (Note 1)/RXD0/TOOLRXD | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |

**Table 3-3 Comparison of pin functions between RL78/F14 (80 pins) and 78K0R/FF3 (2/2)**

| Pin number | RL78/F14 (80 pins) | 78K0R/FF3 (80 pins) | Differences in functions |
|---|---|---|---|
| 44 | P15 (Note 1)/TI05/TO05/TRDIOA1/TRDIOA0/ TRDCLK0/SO00/TXD0/TOOLTXD/RTC1HZ | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/TXD0/ TOOLTXD/RTC1HZ functions added |
| 45 | P31/TI14 (Note 3)/TO14 (Note 3)/STOPST/ INTP2 | P31/INTP2/STOPST/TI11/TO11 | |
| 46 | P50/SSI01/INTP3 | P50/TI20/TO20/INTP3 | [RL78] SSI01 function added<br>[78K0R] TI20/TO20 functions deleted |
| 47 | P51/SO01/INTP11 | P51/TI21/TO21 | [RL78] SO01/INTP11 functions added<br>[78K0R] TI21/TO21 functions deleted |
| 48 | P52/SCK01/STOPST | P52/TI22/TO22/STOPST | [RL78]SCK01 function added<br>[78K0R] TI22/TO22 functions deleted |
| 49 | P53/SI01/INTP10 | P53/TI23/TO23 | [RL78]SI01/INTP10 functions added<br>[78K0R] TI23/TO23 functions deleted |
| 50 | P14 (Note 1)/TI06/TO06/TRDIOC0/SCK01/ SCL01/LRXD0 | P14/LRxD0/INTPLR0/TI06/TO06 | [RL78]TRDIOC0/SCK01/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 51 | P13 (Note 1)/TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01 (Note 1)/LTXD0 | P13/LTxD0/TI04/TO04 | [RL78]TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 52 | P12 (Note 1)/TI11/TO11/TRDIOD0/INTP5/ SO10/TXD1/SNZOUT3 | P12/SO10/INTP3/TI16/TO16 | [RL78]TRDIOD0/TXD1/SNZOUT3 functions added |
| 53 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/LRXD1 (Note 3)/CRXD0 | P11/SI10/LRxD1/INTPLR1/CRxD (Note 4)/ TI02/TO02 | [RL78]TRDIOB0/SDA10/RXD1 functions added<br>[78K0R] INTPLR1 function deleted |
| 54 | P10/TI13/TO13/TRJO0/SCK10/SCL10/ LTXD1 (Note 3)/CTXD0 | P10/SCK10/LTxD1/CTxD (Note 4)/TI00/TO00 | [RL78]TRJO0/SCL10 functions added |
| 55 | P54/TI11/TO11/SSI10 | P54/TI11/TO11 | [RL78]SSI10 function added |
| 56 | P55/TI13/TO13 | P55/TI13/TO13 | |
| 57 | P56/TI15 (Note 3)/TO15 (Note 3)/SNZOUT1 | P56/TI15/TO15 | [RL78]SNZOUT1 function added |
| 58 | P57/TI17 (Note 3)/TO17 (Note 3)/SNZOUT0 | P57/TI17/TO17 | [RL78]SNZOUT0 function added |
| 59 | P33/$AV_{REFP}$/ANI0 | $AV_{REF}$ | [RL78]P33/ANI0 functions added |
| 60 | P34/$AV_{REFM}$/ANI1 | $AV_{SS}$ | [RL78]P34/ANI1 functions added |
| 61 | P80/ANI2/ANO0 | P80/ANI00 | [RL78]ANO0 function added |
| 62 | P81/ANI3/IVCMP00 | P81/ANI01 | [RL78]IVCMP00 function added |
| 63 | P82/ANI4/IVCMP01 | P82/ANI02 | [RL78]IVCMP01 function added |
| 64 | P83/ANI5/IVCMP02 | P83/ANI03 | [RL78]IVCMP02 function added |
| 65 | P84/ANI6/IVCMP03 | P84/ANI04 | [RL78]IVCMP03 function added |
| 66 | P85/ANI7/IVREF0 | P85/ANI05 | [RL78]IVREF0 function added |
| 67 | P86/ANI8 | P86/ANI06 | |
| 68 | P87/ANI9 | P87/ANI07 | |
| 69 | P90/ANI10 | P90/ANI08 | |
| 70 | P91/ANI11 | P91/ANI09 | |
| 71 | P92/ANI12 | P92/ANI10 | |
| 72 | P93/ANI13 | P93/ANI11 | |
| 73 | P94/ANI14 | P94/ANI12 | |
| 74 | P95/ANI15 | P95/ANI13 | |
| 75 | P96/ANI16 (Note 5) | P96/ANI14 | |
| 76 | P97/ANI17 (Note 5) | P97/ANI15 | |
| 77 | P02/TI06/TO06 | P02/TI06/TO06 | |
| 78 | P126/TI01/TO01 | P126/TI01/TO01 | |
| 79 | P01/TI04/TO04 | P01/TI04/TO04 | |
| 80 | P125/ANI24/TI03/TO03/TRDIOB0/SSI01/ INTP1/SNZOUT1 | P125/INTP1/ADTRG/TI03/TO03 | [RL78]ANI24/TRDIOB0/SSI01/SNZOUT1<br>[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 6, 7, 12).
2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).
3. R5F10PME and R5F10PMF products are not equipped with the pin function.
4. μPD78F1823-78F1825 products are not equipped with either CRxD pin or CTxD pin.
5. In R5F10PME and R5F10PMF products, ANI26 and ANI27, both of which are ANI pins and use $EV_{DD}$ as power supply, are available instead of ANI16 and ANI17, respectively.

### 3.2.3 64-pin products

**Table 3-4 Comparison of pin functions between RL78/F14 (64 pins) and 78K0R/FE3 (1/2)**

| Pin number | RL78/F14 (64 pins) | 78K0R/FE3 (64 pins) | Differences in functions |
|---|---|---|---|
| 1 | P120 (Note 1)/ANI25/TI07/TO07/TRDIOD0/ SO01/INTP4 | P120/INTP0/EXLVI/TI11/TO11 | [RL78] ANI25/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |
| 2 | P43/LRXD0 | P43/RxD2 (Note 6)/INTPR2 (Note 6)/SDA20 (Note 6) | [RL78] LRXD0 function added<br>[78K0R] RxD2/INTPR2/SDA20 functions deleted |
| 3 | P42/LTXD0 | P42/TxD2 (Note 6)/SCL20 (Note 6) | [RL78] LTXD0 function added<br>[78K0R] TxD2/SCL20 functions deleted |
| 4 | P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 5 | P40 (Note 2)/TOOL0 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 6 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ | |
| 7 | P124/XT2/EXCLKS | P124/EXCLKS | [RL78] XT2 function added |
| 8 | P123/XT1 | P123 | [RL78] XT1 function added |
| 9 | P137/INTP0 | FLMD0 | [RL78] P137/INTP0 functions added<br>[78K0R] FLMD0 function deleted |
| 10 | P122/X2/EXCLK | P122/X2/EXCLK | |
| 11 | P121/X1 | P121/X1 | |
| 12 | REGC | REGC | |
| 13 | $V_{SS}$ | $V_{SS}$ | |
| 14 | $EV_{SS0}$ | $EV_{SS}$ | |
| 15 | $V_{DD}$ | $V_{DD}$ | |
| 16 | $EV_{DD0}$ | $EV_{DD}$ | |
| 17 | P60 (Note 1)/$\overline{\text{SCK00}}$/SCL00 | P60/$\overline{\text{SCK00}}$/SCL11 | |
| 18 | P61 (Note 1)/SI00/SDA00 (Note 1)/RXD0 | P61/SI00/SDA11 | [RL78] RXD0 function added |
| 19 | P62 (Note 1)/SO00/TXD0/SCLA0 (Note 1) | P62/SO00 | [RL78] TXD0/SCLA0 functions added |
| 20 | P63 (Note 1)/$\overline{\text{SSI00}}$/SDAA0 (Note 1) | P63/$\overline{\text{SSI00}}$ | [RL78] SDAA0 function added |
| 21 | P00/TI05/TO05/INTP9 | P00/TI05/TO05/INTP7 | |
| 22 | P140/PCLBUZ0 | P140/PCL | |
| 23 | P130/RESOUT | P130/RESOUT | |
| 24 | P77/KR7/$\overline{\text{SSI10}}$/INTP12 (Note 4) | P77/KR7/$\overline{\text{SSI01}}$ | [RL78] INTP12 function added |
| 25 | P76/KR6/$\overline{\text{SCK10}}$ | P76/KR6/$\overline{\text{SCK01}}$ | |
| 26 | P75/KR5/SI10/RXD1 | P75/KR5/SI01 | [RL78] RXD1 function added |
| 27 | P74 (Note 3)/KR4/SO10/TXD1 | P74/KR4/SO01 | [RL78] TXD1 function added |
| 28 | P73 (Note 3)/KR3/CRXD0/$\overline{\text{SSI11}}$/SNZOUT7 | P73/KR3/CRxD (Note 5)/LRxD1/INTPLR1 | [RL78] $\overline{\text{SSI11}}$/SNZOUT7 functions added<br>[78K0R] LRxD1/INTPLR1 functions deleted |
| 29 | P72 (Note 1, 3）/KR2/CTXD0/SO11/SNZOUT6 | P72/KR2/CTxD (Note 5)/LTxD1 | [RL78] SO11/SNZOUT6 functions added<br>[78K0R] LTxD1 function deleted |
| 30 | P71 (Note 1, 3）/KR1/TI17 (Note 4)/ TO17 (Note 4)/INTP6/$\overline{\text{SCK11}}$/SCL11/ SNZOUT5 | P71/KR1/INTP6/TI17/TO17 | [RL78] $\overline{\text{SCK11}}$/SCL11/SNZOUT5 functions added |
| 31 | P70 (Note 1)/ANI26 (Note 4)/KR0/ TI15 (Note 4)/TO15 (Note 4)/INTP8/SI11/ SDA11 (Note 1)/SNZOUT4 | P70/KR0/INTP5/TI15/TO15/LVIOUT | [RL78] ANI26/SI11/SDA11/SNZOUT4 functions added<br>[78K0R] LVIOUT function deleted |
| 32 | P32/TI16 (Note 4)/TO16 (Note 4)/INTP7 | P32/INTP4/TI13/TO13 | |
| 33 | P30/TI01/TO01/TRDIOD1/$\overline{\text{SSI00}}$/INTP2/ SNZOUT0 | P30/$\overline{\text{SSI00}}$/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT0 functions added |
| 34 | P17 (Note 1)/TI00/TO00/TRDIOB1/$\overline{\text{SCK00}}$/ SCL00/INTP3 | P17/$\overline{\text{SCK00}}$/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 35 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA00 (Note 1)/RXD0/TOOLRXD | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |
| 36 | P15 (Note 1)/TI05/TO05/TRDIOA1/TRDIOA0/ TRDCLK0/SO00/TXD0/TOOLTXD/RTC1HZ | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/TXD0/ TOOLTXD/RTC1HZ functions added |
| 37 | P31/TI14 (Note 4)/TO14 (Note 4)/STOPST/ INTP2 | P31/INTP2/STOPST/TI11/TO11 | |
| 38 | P50/$\overline{\text{SSI01}}$/INTP3 | P50/TI20/TO20/INTP3 | [RL78] $\overline{\text{SSI01}}$ function added<br>[78K0R] TI20/TO20 functions deleted |

**Table 3-4 Comparison of pin functions between RL78/F14 (64 pins) and 78K0R/FE3 (2/2)**

| Pin number | RL78/F14 (64 pins) | 78K0R/FE3 (64 pins) | Differences in functions |
|---|---|---|---|
| 39 | P51/SO01/INTP11 | P51/TI21/TO21 | [RL78] SO01/INTP11 functions added<br>[78K0R] TI21/TO21 functions deleted |
| 40 | P52/SCK01/STOPST | P52/TI22/TO22/STOPST | [RL78] SCK01 function added<br>[78K0R] TI22/TO22 functions deleted |
| 41 | P53/SI01/INTP10 | P53/TI23/TO23 | [RL78] SI01/INTP10 functions added<br>[78K0R] TI23/TO23 functions deleted |
| 42 | P14 (Note 1)/TI06/TO06/TRDIOC0/SCK01/ SCL01/LRXD0 | P14/LRxD0/INTPLR0/TI06/TO06 | [RL78] TRDIOC0/SCK01/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 43 | P13 (Note 1)/TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01 (Note 1)/LTXD0 | P13/LTxD0/TI04/TO04 | [RL78] TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 44 | P12 (Note 1)/TI11/TO11/TRDIOD0/INTP5/ SO10/TXD1/SNZOUT3 | P12/SO10/INTP3/TI16/TO16 | [RL78] TRDIOD0/TXD1/SNZOUT3 functions added |
| 45 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/LRXD1 (Note 4)/CRXD0 | P11/SI10/LRxD1/INTPLR1/CRxD (Note 5)/ TI02/TO02 | [RL78] TRDIOB0/SDA10/RXD1 functions added<br>[78K0R] INTPLR1 function deleted |
| 46 | P10 (Note 1)/TI13/TO13/TRJO0/SCK10/ SCL10/LTXD1 (Note 4)/CTXD0 | P10/SCK10/LTxD1/CTxD (Note 5)/TI00/TO00 | [RL78] TRJO0/SCL10 functions added |
| 47 | P33/$AV_{REFP}$/ANI0 | $AV_{REF}$ | [RL78] P33/ANI0 functions added |
| 48 | P34/$AV_{REFM}$/ANI1 | $AV_{SS}$ | [RL78] P34/ANI1 functions added |
| 49 | P80/ANI2/ANO0 | P80/ANI00 | [RL78] ANO0 function added |
| 50 | P81/ANI3/IVCMP00 | P81/ANI01 | [RL78] IVCMP00 function added |
| 51 | P82/ANI4/IVCMP01 | P82/ANI02 | [RL78] IVCMP01 function added |
| 52 | P83/ANI5/IVCMP02 | P83/ANI03 | [RL78] IVCMP02 function added |
| 53 | P84/ANI6/IVCMP03 | P84/ANI04 | [RL78] IVCMP03 function added |
| 54 | P85/ANI7/IVREF0 | P85/ANI05 | [RL78] IVREF0 function added |
| 55 | P86/ANI8 | P86/ANI06 | |
| 56 | P87/ANI9/KR0 | P87/ANI07 | [RL78] KR0 function added |
| 57 | P90/ANI10/KR1 | P90/ANI08 | [RL78] KR1 function added |
| 58 | P91/ANI11/KR2 | P91/ANI09 | [RL78] KR2 function added |
| 59 | P92/ANI12/KR3 | P92/ANI10 | [RL78] KR3 function added |
| 60 | P93/ANI13/KR4 | P93/ANI11 | [RL78] KR4 function added |
| 61 | P94/ANI14/KR5 | P94/ANI12 | [RL78] KR5 function added |
| 62 | P95/ANI15/KR6 | P95/ANI13 | [RL78] KR6 function added |
| 63 | P96/ANI16 (Note 7)/KR7 | P96/ANI14 | [RL78] KR7 function added |
| 64 | P125/ANI24/TI03/TO03/TRDIOB0/SSI01/ INTP1/SNZOUT1 | P125/INTP1/ADTRG/TI03/TO03 | [RL78] ANI24/TRDIOB0/SSI01/SNZOUT1 functions added<br>[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 6, 7, 12).
2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).
3. In R5F10PLG, R5F10PLH, and R5F10PLJ products, be sure to clear PMC71 to PMC74 bits to "0".
4. R5F10PLE and R5F10PLF products are not equipped with the pin function.
5. μPD78F1818-78F1822 products are not equipped with either CRxD pin or CTxD pin.
6. μPD78F1818-78F1820 products are not equipped with RxD2, INTPR2, SDA20, TxD2, or SCL20 pins.
7. In R5F10PLE and R5F10PLF products, ANI26, which is an ANI pin and uses $EV_{DD}$ as power supply, is available instead of ANI16.

### 3.2.4 48-pin products

**Table 3-5 Comparison of pin functions between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (1/2)**

| Pin number | RL78/F14 (48 pins) | 78K0R/FC3 (48 pins) | Differences in functions |
|---|---|---|---|
| 1 | P120 (Note 1)/ANI25/TI07/TO07/TRDIOD0/ SO01/INTP4 | P120/INTP0/EXLVI/TI11/TO11 | [RL78] ANI25/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |
| 2 | P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 3 | P40 (Note 2)/TOOL0 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 4 | RESET | RESET | |
| 5 | P124/XT2/EXCLKS | P124/EXCLKS | [RL78] XT2 function added |
| 6 | P123/XT1 | P123 | [RL78] XT1 function added |
| 7 | P137/INTP0 | FLMD0 | [RL78] P137/INTP0 functions added<br>[78K0R] FLMD0 function deleted |
| 8 | P122/X2/EXCLK | P122/X2/EXCLK | |
| 9 | P121/X1 | P121/X1 | |
| 10 | REGC | REGC | |
| 11 | $V_{SS}$ | $V_{SS}/EV_{SS}$ | [78K0R] $EV_{SS}$ function deleted |
| 12 | $V_{DD}$ | $V_{DD}/EV_{DD}$ | [78K0R] $EV_{DD}$ function deleted |
| 13 | P60 (Note 1)/SCK00/SCL00 | P60/SCK00/SCL11 | |
| 14 | P61 (Note 1)/SI00/SDA00 (Note 1)/RXD0 | P61/SI00/SDA11 | [RL78] RXD0 function added |
| 15 | P62 (Note 1)/SO00/TXD0/SCLA0 (Note 1) | P62/SO00 | [RL78] TXD0/SCLA0 functions added |
| 16 | P63 (Note 1)/SSI00/SDAA0 (Note 1) | P63/SSI00 | [RL78] SDAA0 function added |
| 17 | P00/TI05/TO05/INTP9 | P00/TI05/TO05/INTP7 | |
| 18 | P140/PCLBUZ0 | P140/PCL | |
| 19 | P130/RESOUT | P130/RESOUT | |
| 20 | P73 (Note 3)/KR3/CRXD0/SSI11/SNZOUT7 | P73/KR3/CRxD (Note 5)/LRxD1/INTPLR1 | [RL78] SSI11/SNZOUT7 functions added<br>[78K0R] LRxD1/INTPLR1 functions deleted |
| 21 | P72 (Note 1)/ANI28 (Note 4)/KR2/CTXD0/ SO11/SNZOUT6 | P72/KR2/CTxD (Note 5)/LTxD1 | [RL78] ANI28/SO11/SNZOUT6 functions added<br>[78K0R] LTxD1 function deleted |
| 22 | P71 (Note 1)/ANI27 (Note 4)/KR1/ TI17 (Note 4)/TO17 (Note 4)/INTP6/SCK11/ SCL11/SNZOUT5 | P71/KR1/INTP6/TI17/TO17 | [RL78] ANI27/SCK11/SCL11/SNZOUT5 functions added |
| 23 | P70 (Note 1)/ANI26 (Note 4)/KR0/ TI15 (Note 4)/TO15 (Note 4)/INTP8/SI11/ SDA11 (Note 1)/SNZOUT4 | P70/KR0/INTP5/TI15/TO15/LVIOUT | [RL78] ANI26/SI11/SDA11/SNZOUT4 functions added<br>[78K0R] LVIOUT function deleted |
| 24 | P32/TI16 (Note 4)/TO16 (Note 4)/INTP7 | P32/INTP4/TI13/TO13 | |
| 25 | P30/TI01/TO01/TRDIOD1/SSI00/INTP2/ SNZOUT0 | P30/SSI00/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT functions added |
| 26 | P17 (Note 1)/TI00/TO00/TRDIOB1/SCK00/ SCL00/INTP3 | P17/SCK00/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 27 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA00 (Note 1)/RXD0/TOOLRXD | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |
| 28 | P15 (Note 1)/TI05/TO05/TRDIOA1/TRDIOA0/ TRDCLK0/SO00/TXD0/TOOLTXD/RTX1HZ | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/TXD0/ TOOLTXD/RTX1HZ functions added |
| 29 | P31/TI14 (Note 4)/TO14 (Note 4)/ STOPST/INTP2 | P31/INTP2/STOPST/TI11/TO11 | |
| 30 | P14 (Note 1)/TI06/TO06/TRDIOC0/SCK01/ SCL01/LRXD0 | P14/LRxD0/INTPLR0/TI06/TO06 | [RL78] TRDIOC0/SCK01/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 31 | P13 (Note 1)/TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01 (Note 1)/LTXD0 | P13/LTxD0/TI04/TO04 | [RL78] TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 32 | P12 (Note 1)/TI11/TO11/TRDIOD0/INTP5/ SO10/TXD1/SNZOUT3 | P12/SO10/INTP3/TI16/TO16 | [RL78] TRDIOD0/TXD1/SNZOUT3 functions added |
| 33 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/LRXD1 (Note 4)/CRXD0 | P11/SI10/LRxD1/INTPLR1/CRxD (Note 5)/ TI02/TO02 | [RL78] TRDIOB0/SDA10/RXD1 functions added<br>[78K0R] INTPLR1 function deleted |
| 34 | P10 (Note 1)/TI13/TO13/TRJO0/SCK10/ SCL10/LTXD1 (Note 4)/CTXD0 | P10/SCK10/LTxD1/CTxD (Note 5)/TI00/TO00 | [RL78] TRJO0/SCL10 functions added |
| 35 | $P33/AV_{REFP}$/ANI0 | $AV_{REF}$ | [RL78] P33/ANI0 functions added |
| 36 | $P34/AV_{REFM}$/ANI1 | $AV_{SS}$ | [RL78] P34/ANI1 functions added |
| 37 | P80/ANI2/ANO0 | P80/ANI00 | [RL78] ANO0 function added |
| 38 | P81/ANI3/IVCMP00 | P81/ANI01 | [RL78] IVCMP00 function added |

**Table 3-5 Comparison of pin functions between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins) (2/2)**

| Pin number | RL78/F14 (48 pins) | 78K0R/FC3 (48 pins) | Differences in functions |
|---|---|---|---|
| 39 | P82/ANI4/IVCMP01 | P82/ANI02 | [RL78] IVCMP01 function added |
| 40 | P83/ANI5/KR0/IVCMP02 | P83/ANI03 | [RL78] KR0/IVCMP02 functions added |
| 41 | P84/ANI6/KR1/IVCMP03 | P84/ANI04 | [RL78] KR1/IVCMP03 functions added |
| 42 | P85/ANI7/KR2/IVREF0 | P85/ANI05 | [RL78] KR2/IVREF0 functions added |
| 43 | P86/ANI8/KR3 | P86/ANI06 | [RL78] KR3 function added |
| 44 | P87/ANI9/KR4 | P87/ANI07 | [RL78] KR4 function added |
| 45 | P90/ANI10/KR5 | P90/ANI08 | [RL78] KR5 function added |
| 46 | P91/ANI11/KR6 | P91/ANI09 | [RL78] KR6 function added |
| 47 | P92/ANI12/KR7 | P92/ANI10 | [RL78] KR7 function added |
| 48 | P125/ANI24/TI03/TO03/TRDIOB0/$\overline{\text{SSI01}}$/INTP1/SNZOUT1 | P125/INTP1/ADTRG/TI03/TO03 | [RL78] ANI24/TRDIOB0/$\overline{\text{SSI01}}$/SNZOUT1 functions added<br>[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 6, 7, 12).
2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).
3. In R5F10PGG, R5F10PGH, and R5F10PGJ products, be sure to clear the PMC73 bit to "0".
4. R5F10PGD, R5F10PGE and R5F10PGF products are not equipped with the pin function.
5. μPD78F1812-78F1817 products are not equipped with either CRxD pin or CTxD pin.

### 3.2.5 40-pin products

The RL78/F14 does not support 40-pin products. Table 3-6 shows the comparison of pin functions between the RL78/F14 (48 pins) and the 78K0R/FC3 (40 pins).

**Table 3-6 Comparison of pin functions between RL78/F14 (40 pins) and 78K0R/FC3 (48 pins) (1/2)**

| RL78/F14 Pin number | RL78/F14 (48 pins) | 78K0R/FC3 Pin number | 78K0R/FC3 (40 pins) | Differences in functions |
|---|---|---|---|---|
| 1 | P120 (Note 1)/ANI25/TI07/TO07/ TRDIOD0/SO01/INTP4 | 1 | P120/INTP0/EXLVI/TI11/TO11 | [RL78] ANI25/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |
| 2 | P41/TI10/TO10/TRJIO0/VCOUT0/ SNZOUT2 | 2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 3 | P40 (Note 2)/TOOL0 | 3 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 4 | RESET | 4 | RESET | |
| 5 | P124/XT2/EXCLKS | 5 | FLMD0 | [RL78] P124/XT2/EXCLKS functions added<br>[78K0R] FLMD0 function deleted |
| 6 | P123/XT1 | - | - | [RL78] P123/XT1 functions added |
| 7 | P137/INTP0 | - | - | [RL78] P137/INTP0 functions added |
| 8 | P122/X2/EXCLK | 6 | P122/X2/EXCLK | |
| 9 | P121/X1 | 7 | P121/X1 | |
| 10 | REGC | 8 | REGC | |
| 11 | $V_{SS}$ | 9 | $V_{SS}$/$EV_{SS}$ | [78K0R] $EV_{SS}$ function deleted |
| 12 | $V_{DD}$ | 10 | $V_{DD}$/$EV_{DD}$ | [78K0R] $EV_{DD}$ function deleted |
| 13 | P60 (Note 1)/SCK00/SCL00 | 11 | P60/SCL11 | [RL78] SCK00 function added |
| 14 | P61 (Note 1)/SI00/SDA00 (Note 1)/RXD0 | 12 | P61/SDA11 | [RL78] SI00/ RXD0 functions added |
| 15 | P62 (Note 1)/SO00/TXD0/ SCLA0 (Note 1) | 13 | P62 | [RL78] SO00/TXD0/SCLA0 functions added |
| 16 | P63 (Note 1)/SSI00/SDAA0 (Note 1) | 14 | P63 | [RL78] SSI00/SDAA0 functions added |
| 17 | P00/TI05/TO05/INTP9 | - | - | [RL78] P00/TI05/TO05/INTP9 functions added |
| 18 | P140/PCLBUZ0 | - | - | [RL78] P140/PCLBUZ0 functions added |
| 19 | P130/RESOUT | - | - | [RL78] P130/RESOUT functions added |
| 20 | P73 (Note 4)/KR3/CRXD0/SSI11/ SNZOUT7 | 15 | P73/KR3/LRXD1/INTPLR1 | [RL78] CRXD0/SSI11/SNZOUT7 functions added<br>[78K0R] LRXD1/INTPLR1 functions deleted |
| 21 | P72 (Note 1)/ANI28 (Note 3)/KR2/CTXD0/ SO11/SNZOUT6 | 16 | P72/KR2/LTxD1 | [RL78] ANI28/CTXD0/SO11/SNZOUT6 functions added<br>[78K0R] LTxD1 function deleted |
| 22 | P71 (Note 1)/ANI27 (Note 3)/KR1/ TI17 (Note 3)/TO17 (Note 3)/INTP6/ SCK11/SCL11/SNZOUT5 | 17 | P71/KR1/INTP6/TI17/TO17 | [RL78] ANI27/SCK11/SCL11/SNZOUT5 functions added |
| 23 | P70 (Note 1)/ANI26 (Note 3)/KR0/ TI15 (Note 3)/TO15 (Note 3)/INTP8/SI11/ SDA11 (Note 1)/SNZOUT4 | 18 | P70/KR0/INTP5/TI15/TO15/LVIOUT | [RL78] ANI26/SI11/SDA11/SNZOUT4 functions added<br>[78K0R] LVIOUT function deleted |
| 24 | P32/TI16 (Note 3)/TO16 (Note 3)/INTP7 | 19 | P32/INTP4/TI13/TO13 | |
| 25 | P30/TI01/TO01/TRDIOD1/SSI00/INTP2/ SNZOUT0 | 20 | P30/SSI00/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT0 functions added |
| 26 | P17 (Note 1)/TI00/TO00/TRDIOB1/ SCK00/SCL00/INTP3 | 21 | P17/SCK00/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 27 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA00 (Note 1)/RXD0/TOOLRXD | 22 | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |
| 28 | P15 (Note 1)/TI05/TO05/TRDIOA1/ TRDIOA0/TRDCLK0/SO00/TXD0/ TOOLTXD/RTX1HZ | 23 | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/ TXD0/TOOLTXD/RTX1HZ functions added |
| 29 | P31/TI14 (Note 3)/TO14 (Note 3)/ STOPST/INTP2 | 24 | P31/INTP2/STOPST/TI11/TO11 | |
| 30 | P14 (Note 1)/TI06/TO06/TRDIOC0/ SCK01/SCL01/LRXD0 | 25 | P14/LRXD0/INTPLR0/TI06/TO06 | [RL78] TRDIOC0/SCK01/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 31 | P13 (Note 1)/TI04/TO04/TRDIOA0/ TRDCLK0/SI01/SDA01 (Note 1)/LTXD0 | 26 | P13/LTXD0/TI04/TO04 | [RL78] TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 32 | P12 (Note 1)/TI11/TO11/TRDIOD0/ INTP5/SO10/TXD1/SNZOUT3 | 27 | P12/SO10/INTP3/TI16/TO16 | [RL78] TRDIOD0/TXD1/SNZOUT3 functions added |
| 33 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/ LRXD1 (Note 3)/CRXD0 | 28 | P11/SI10/LRxD1/INTPLR1/TI02/TO02 | [RL78] TRDIOB0/SDA10/RXD1/CRXD0 functions added |

**Table 3-6 Comparison of pin functions between RL78/F14 (40 pins) and 78K0R/FC3 (48 pins) (2/2)**

| RL78/F14 Pin number | RL78/F14 (48 pins) | 78K0R/FC3 Pin number | 78K0R/FC3 (40 pins) | Differences in functions |
|---|---|---|---|---|
| 34 | P10 (Note 1)/TI13/TO13/TRJO0/SCK10/ SCL10/LTXD1 (Note 3)/CTXD0 | 29 | P10/SCK10/LTXD1/TI00/TO00 | [RL78] TRJO0/SCL10/CTXD0 functions added |
| 35 | P33/$AV_{REFP}$/ANI0 | 30 | $AV_{REF}$ | [RL78] P33/ANI0 functions added |
| 36 | P34/$AV_{REFM}$/ANI1 | 31 | $AV_{SS}$ | [RL78] P34/ANI1 functions added |
| 37 | P80/ANI2/ANO0 | 32 | P80/ANI00 | [RL78] ANO0 function added |
| 38 | P81/ANI3/IVCMP00 | 33 | P81/ANI01 | [RL78] IVCMP00 function added |
| 39 | P82/ANI4/IVCMP01 | 34 | P82/ANI02 | [RL78] IVCMP01 function added |
| 40 | P83/ANI5/KR0/IVCMP02 | 35 | P83/ANI03 | [RL78] KR0/IVCMP02 functions added |
| 41 | P84/ANI6/KR1/IVCMP03 | 36 | P84/ANI04 | [RL78] KR1/IVCMP03 functions added |
| 42 | P85/ANI7/KR2/IVREF0 | 37 | P85/ANI05 | [RL78] KR2/IVREF0 functions added |
| 43 | P86/ANI8/KR3 | 38 | P86/ANI06 | [RL78] KR3 function added |
| 44 | P87/ANI9/KR4 | 39 | P87/ANI07 | [RL78] KR4 function added |
| 45 | P90/ANI10/KR5 | - | - | [RL78] P90/ANI10/KR5 functions added |
| 46 | P91/ANI11/KR6 | - | - | [RL78] P91/ANI11/KR6 functions added |
| 47 | P92/ANI12/KR7 | - | - | [RL78] P92/ANI12/KR7 functions added |
| 48 | P125/ANI24/TI03/TO03/TRDIOB0/SSI01/ INTP1/SNZOUT1 | 40 | P125/INTP1/ADTRG/TI03/TO03 | [RL78] ANI24/TRDIOB0/SSI01/SNZOUT1 functions added<br>[[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 6, 7, 12).
2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).
3. R5F10PGD, R5F10PGE and R5F10PGF products are not equipped with the pin function.
4. In R5F10PGG, R5F10PGH, and R5F10PGJ products, be sure to clear the PMC73 bit to "0".

### 3.2.6 32-pin products

**Table 3-7 Comparison of pin functions between RL78/F14 (32 pins) and 78K0R/FB3 (32 pins)**

| Pin number | RL78/F14 (32 pins) | 78K0R/FB3 (32 pins) | Differences in functions |
|---|---|---|---|
| 1 | P120 (Note 1)/ANI25/TI07/TO07/TRDIOD0/ SO01/INTP4 | P120/INTP0/EXLVI/TI11/TO11 | [RL78] ANI25/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |
| 2 | P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 3 | P40 (Note 2)/TOOL0 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 4 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ | |
| 5 | P137/INTP0 | FLMD0 | [RL78] P137/INTP0 functions added<br>[78K0R] FLMD0 function deleted |
| 6 | P122/X2/EXCLK | P122/X2/EXCLK | |
| 7 | P121/X1 | P121/X1 | |
| 8 | REGC | REGC | |
| 9 | $V_{SS}$ | $V_{SS}/EV_{SS}$ | [78K0R] $EV_{SS}$ function deleted |
| 10 | $V_{DD}$ | $V_{DD}/EV_{DD}$ | [78K0R] $EV_{DD}$ function deleted |
| 11 | P60 (Note 1)/$\overline{\text{SCK00}}$/SCL00 | P60/$\overline{\text{SCK00}}$/SCL11 | |
| 12 | P61 (Note 1)/SI00/SDA00 (Note 1)/RXD0 | P61/SI00/SDA11 | [RL78] RXD0 function added |
| 13 | P62 (Note 1)/SO00/TXD0/SCLA0 (Note 1) | P62/SO00 | [RL78] TXD0/SCLA0 functions added |
| 14 | P63 (Note 1)/$\overline{\text{SSI00}}$/SDAA0 (Note 1) | P63/$\overline{\text{SSI00}}$ | [RL78] SDAA0 function added |
| 15 | P30/TI01/TO01/TRDIOD1/$\overline{\text{SSI00}}$/INTP2/ SNZOUT0 | P30/$\overline{\text{SSI00}}$/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT0 functions added |
| 16 | P17 (Note 1)/TI00/TO00/TRDIOB1/$\overline{\text{SCK00}}$/ SCL00/INTP3 | P17/$\overline{\text{SCK00}}$/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 17 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA00 (Note 1)/RXD0/TOOLRXD | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |
| 18 | P15 (Note 1)/TI05/TO05/TRDIOA1/TRDIOA0/ TRDCLK0/SO00/TXD0/TOOLTXD/RTC1HZ | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/TXD0/ TOOLTXD/RTC1HZ functions added |
| 19 | P14 (Note 1)/TI06/TO06/TRDIOC0/$\overline{\text{SCK01}}$/ SCL01/LRXD0 | P14/LRxD0/INTPLR0/TI06/TO06 | [RL78] TRDIOC0/$\overline{\text{SCK01}}$/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 20 | P13 (Note 1)/TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01 (Note 1)/LTXD0 | P13/LTxD0/TI04/TO04 | [RL78] TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 21 | P12 (Note 1)/TI11/TO11/TRDIOD0/INTP5/ SO10/TXD1/SNZOUT3 | P12/SO10/INTP3/TI16/TO16 | [RL78] TRDIOD0/TXD1/SNZOUT3 functions added |
| 22 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/CRXD0 | P11/SI10/LRxD1/INTPLR1/TI02/TO02/INTP5 | [RL78] TRDIOB0/SDA10/RXD1/CRXD0 functions added<br>[78K0R] LRxD1/INTPLR1/INTP5 functions deleted |
| 23 | P10 (Note 1)/TI13/TO13/TRJO0/$\overline{\text{SCK10}}$/ SCL10/CTXD0 | P10/$\overline{\text{SCK10}}$/LTxD1/TI00/TO00/INTP4 | [RL78] TRJO0/SCL10/CTXD0 functions added<br>[78K0R] LTxD1/INTP4 functions deleted |
| 24 | P33/$AV_{REFP}$/ANI0 | $AV_{REF}$ | [RL78] P33/ANI0 functions added |
| 25 | P34/$AV_{REFM}$/ANI1 | $AV_{SS}$ | [RL78] P34/ANI1 functions added |
| 26 | P80/ANI2/KR0/ANO0 | P80/ANI00 | [RL78] KR0/ANO0 functions added |
| 27 | P81/ANI3/KR1/IVCMP00 | P81/ANI01 | [RL78] KR1/IVCMP00 functions added |
| 28 | P82/ANI4/KR2/IVCMP01 | P82/ANI02 | [RL78] KR2/IVCMP01 functions added |
| 29 | P83/ANI5/KR3/IVCMP02 | P83/ANI03 | [RL78] KR3/IVCMP02 functions added |
| 30 | P84/ANI6/KR4/IVCMP03 | P84/ANI04 | [RL78] KR4/IVCMP03 functions added |
| 31 | P85/ANI7/KR5/IVREF0 | P85/ANI05 | [RL78] KR5/IVREF0 functions added |
| 32 | P125/ANI24/TI03/TO03/TRDIOB0/$\overline{\text{SSI01}}$/ INTP1/SNZOUT1 | P125/INTP1/ADTRG/TI03/TO03 | [RL78] ANI24/TRDIOB0/$\overline{\text{SSI01}}$/SNZOUT1 functions added<br>[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 6, 12).

2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).

### 3.2.7 30-pin products

**Table 3-8 Comparison of pin functions between RL78/F14 (30 pins) and 78K0R/FB3 (30 pins)**

| Pin number | RL78/F14 (30 pins) | 78K0R/FB3 (30 pins) | Differences in functions |
|---|---|---|---|
| 1 | P84/ANI6/KR4/IVCMP03 | P84/ANI04 | [RL78] KR4/IVCMP03 functions added |
| 2 | P85/ANI7/KR5/IVREF0 | P85/ANI05 | [RL78] KR5/IVREF0 functions added |
| 3 | P86/ANI8/KR6 | P86/ANI06 | [RL78] KR6 functions added |
| 4 | P87/ANI9/KR7 | P87/ANI07 | [RL78] KR7 functions added |
| 5 | P125/ANI24/TI03/TO03/TRDIOB0/SSI01/ INTP1/SNZOUT1 | P125/INTP1/ADTRG/TI03/TO03 | [RL78] ANI24/TRDIOB0/SSI01/SNZOUT1 functions added<br>[78K0R] ADTRG function deleted → A/D conversion is available by ELC (Event: INTP1) |
| 6 | P120 (Note 1)/ANI25/TI07/TO07/TRDIOD0/ SO01/INTP4 | P120/INTP0/EXLVI/TI11/TO11 | [RL78] ANI25/TRDIOD0/SO01 functions added<br>[78K0R] EXLVI function deleted |
| 7 | P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2 | P41/TOOL1/TI07/TO07 | [RL78] TRJIO0/VCOUT0/SNZOUT2 functions added<br>[78K0R] TOOL1 function deleted |
| 8 | P40 (Note 2)/TOOL0 | P40/TOOL0/TI05/TO05 | [78K0R] TI05/TO05 functions deleted |
| 9 | RESET | RESET | |
| 10 | P137/INTP0 | FLMD0 | [RL78] P137/INTP0 functions added<br>[78K0R] FLMD0 function deleted |
| 11 | P122/X2/EXCLK | P122/X2/EXCLK | |
| 12 | P121/X1 | P121/X1 | |
| 13 | REGC | REGC | |
| 14 | $V_{SS}$ | $V_{SS}/EV_{SS}$ | [78K0R] $EV_{SS}$ function deleted |
| 15 | $V_{DD}$ | $V_{DD}/EV_{DD}$ | [78K0R] $EV_{DD}$ function deleted |
| 16 | P30/TI01/TO01/TRDIOD1/SSI00/INTP2/ SNZOUT0 | P30/SSI00/INTP2/TI01/TO01 | [RL78] TRDIOD1/SNZOUT0 functions added |
| 17 | P17 (Note 1)/TI00/TO00/TRDIOB1/SCK00/ SCL00/INTP3 | P17/SCK00/TI14/TO14 | [RL78] TRDIOB1/SCL00/INTP3 functions added |
| 18 | P16 (Note 1)/TI02/TO02/TRDIOC1/SI00/ SDA0 (Note 1)/RXD0/TOOLRXD | P16/SI00/TI12/TO12 | [RL78] TRDIOC1/SDA00/RXD0/TOOLRXD functions added |
| 19 | P15 (Note 1)/TI05/TO05/TRDIOA1/TRDIOA0/ TRDCLK0/SO00/TXD0/TOOLTXD/RTC1HZ | P15/SO00/TI10/TO10 | [RL78] TRDIOA1/TRDIOA0/TRDCLK0/TXD0/ TOOLTXD/RTC1HZ functions added |
| 20 | P14 (Note 1)/TI06/TO06/TRDIOC0/SCK01/ SCL01/LRXD0 | P14/LRxD0/INTPLR0/TI06/TO06 | [RL78] TRDIOC0/SCK01/SCL01 functions added<br>[78K0R] INTPLR0 function deleted |
| 21 | P13 (Note 1)/TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01 (Note 1)/LTXD0 | P13/LTxD0/TI04/TO04 | [RL78] TRDIOA0/TRDCLK0/SI01/SDA01 functions added |
| 22 | P12 (Note 1)/TI11/TO11/TRDIOD0/INTP5/ SO10/TXD1/SNZOUT3 | P12/SO10/INTP3/TI16/TO16 | [RL78] TRDIOD0/TXD1/SNZOUT3 functions added |
| 23 | P11 (Note 1)/TI12/TO12/TRDIOB0/SI10/ SDA10 (Note 1)/RXD1/CRXD0 | P11/SI10/LRxD1/INTPLR1/TI02/TO02/INTP5 | [RL78] TRDIOB0/SDA10/RXD1/CRXD0 functions added<br>[78K0R] LRxD1/INTPLR1/INTP5 functions deleted |
| 24 | P10 (Note 1)/TI13/TO13/TRJO0/SCK10/ SCL10/CTXD0 | P10/SCK10/LTxD1/TI00/TO00/INTP4 | [RL78] TRJO0/SCL10/CTXD0 functions added<br>[78K0R] LTxD1/ INTP4 functions deleted |
| 25 | P33/$AV_{REFP}$/ANI0 | $AV_{REF}$ | [RL78] P33/ANI0 functions added |
| 26 | P34/$AV_{REFM}$/ANI1 | $AV_{SS}$ | [RL78] P34/ANI1 functions added |
| 27 | P80/ANI2/KR0/ANO0 | P80/ANI00 | [RL78] KR0/ANO0 functions added |
| 28 | P81/ANI3/KR1/IVCMP00 | P81/ANI01 | [RL78] KR1/IVCMP00 functions added |
| 29 | P82/ANI4/KR2/IVCMP01 | P82/ANI02 | [RL78] KR2/IVCMP01 functions added |
| 30 | P83/ANI5/KR3/IVCMP02 | P83/ANI03 | [RL78] KR3/IVCMP02 functions added |

Remark The underlined pin functions are active after a reset.

Notes 1. N-ch open-drain output can be selected by setting the POMx registers (x = 1, 12).

2. After a reset release, the PU40 bit is set to "1" (On-chip pull-up resistor connected).

# 4. Memory

Table 4-1 shows the comparison of the memory size between each product of the RL78/F14; whereas Table 4-2 shows that of the 78K0R/Fx3.

**Table 4-1 Comparison of memory size between each product of RL78/F14**

| Code flash memory | Data flash memory | RAM | 30 pins | 32 pins | 48 pins | 64 pins | 80 pins | 100 pins |
|---|---|---|---|---|---|---|---|---|
| 48 Kbytes | 4 Kbytes | 4 Kbytes | ○ | ○ | ○ | - | - | - |
| 64 Kbytes | | 6 Kbytes | ○ | ○ | ○ | ○ | ○ | ○ |
| 96 Kbytes | | 8 Kbytes | - | - | ○ | ○ | ○ | ○ |
| 128 Kbytes | 8 Kbytes | 10 Kbytes | - | - | ○ | ○ | ○ | ○ |
| 192 Kbytes | | 16 Kbytes | - | - | ○ | ○ | ○ | ○ |
| 256 Kbytes | | 20 Kbytes | - | - | ○ | ○ | ○ | ○ |

○ : Provided
- : Not provided

**Table 4-2 Comparison of memory size between each product of 78K0R/Fx3**

| Code flash memory | Data flash memory | High-speed RAM | 78K0R/FB3 | | 78K0R/FC3 | | 78K0R/FE3 | 78K0R/FF3 | 78K0R/FG3 |
|---|---|---|---|---|---|---|---|---|---|
| | | | 30 pins | 32 pins | 40 pins | 48 pins | 64 pins | 80 pins | 100 pins |
| 24 Kbytes | 16 Kbytes | 1.5 Kbytes | ○ | ○ | ○ | ○ | - | - | - |
| 32 Kbytes | | 2 Kbytes | ○ | ○ | ○ | ○ | ○ | - | - |
| 48 Kbytes | | 3 Kbytes | ○ | ○ | ○ | ○ | ○ | - | - |
| 64 Kbytes | | 4 Kbytes | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| 96 Kbytes | | 6 Kbytes | - | - | - | ○ | ○ | ○ | ○ |
| 128 Kbytes | | 8 Kbytes | - | - | - | ○ | ○ | ○ | ○ |
| 192 Kbytes | | 12 Kbytes | - | - | - | ○ | ○ | ○ | ○ |
| 256 Kbytes | | 16 Kbytes | - | - | - | ○ | ○ | ○ | ○ |

○ : Provided
- : Not provided

**<Key Points on Porting>**

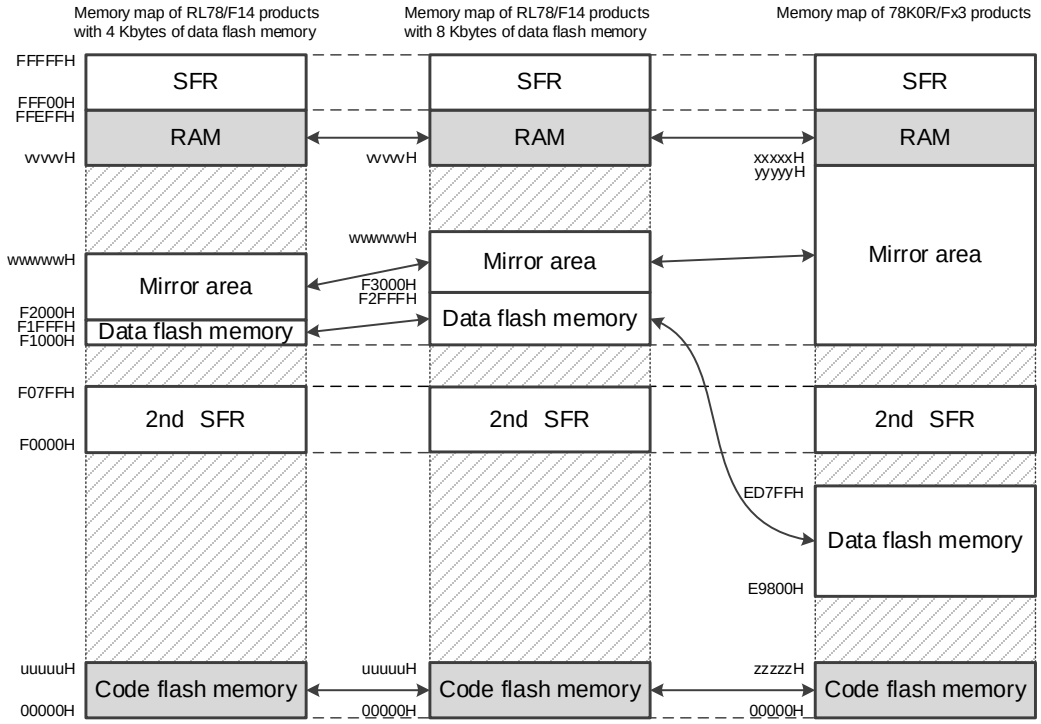
**·Data flash memory**

The size of the data flash memory of the 78K0R/Fx3 is 16 Kbytes; whereas that of the RL78/F14 is either 4 Kbytes or 8 Kbytes, i.e. smaller than that of the 78K0R/Fx3. Confirm that this difference would not lead to problems.

## 4.1 Memory

Figure 4-1shows the memory maps of the RL78/F14 and the 78K0R/Fx3.

In terms of RAM and ROM, the allocated addresses of each memory are the same between the RL78/F14 and the 78K0R/Fx3. However, the allocated addresses of each mirror area and data flash memory area differ between the RL78/F14 and the 78K0R/Fx3. In the RL78/F14, the data flash memory size depends on the product and each mirror area is allocated from F2000H to FDEFFH (47.75 Kbytes), from F3000H to FAEFFH (31.75 Kbytes), or F2000H to FBFFFH (40 Kbytes), depending on the product. For your information, the RAM area and the mirror area of the 78K0R/Fx3 are allocated consecutively.




Allocated addresses of memory of RL78/F14 and 78K0R/Fx3

| Memory size | | | Applied family | Allocated address | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code flash memory | Data flash memory | High-speed RAM (RAM in RL78/F14) | | Code flash memory | | Data flash memory | | High-speed RAM (RAM in RL78/F14) | | Mirror area | | | SFR | | 2nd SFR | |
| | | | | Start address | End address | Start address | End address | Start address | End address | Start address | End address | Size (supplementation) | Start address | End address | Start address | End address |
| 256 Kbytes | 8 Kbytes | 20 Kbytes | RL78/F14 | 00000H | 3FFFFH | F1000H | F2FFFH | FAF00H | FFEFFH | F3000H | FAEFFH | 31.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| | 16 Kbytes | 16 Kbytes | 78K0R/Fx3 | 00000H | 3FFFFH | E9800H | ED7FFH | FBF00H | FFEFFH | F1000H | FBEFFH | 43.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 192 Kbytes | 8 Kbytes | 16 Kbytes | RL78/F14 | 00000H | 2FFFFH | F1000H | F2FFFH | FBF00H | FFEFFH | F3000H | FAEFFH | 31.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| | 16 Kbytes | 12 Kbytes | 78K0R/Fx3 | 00000H | 2FFFFH | E9800H | ED7FFH | FCF00H | FFEFFH | F1000H | FCEFFH | 47.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 128 Kbytes | 8 Kbytes | 10 Kbytes | RL78/F14 | 00000H | 1FFFFH | F1000H | F2FFFH | FD700H | FFEFFH | F3000H | FAEFFH | 31.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| | 16 Kbytes | 8 Kbytes | 78K0R/Fx3 | 00000H | 1FFFFH | E9800H | ED7FFH | FDF00H | FFEFFH | F1000H | FDEFFH | 51.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 96 Kbytes | 4Kbytes | 8 Kbytes | RL78/F14 | 00000H | 17FFFH | F1000H | F1FFFH | FDF00H | FFEFFH | [Except 100 pins] F2000H [100-pins] F3000H | [Except 100 pins] FDEFFH [100 pins] FAEFFH | [Except 100 pins] 47.75 Kbytes [100 pins] 31.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| | 16 Kbytes | 6 Kbytes | 78K0R/Fx3 | 00000H | 17FFFH | E9800H | ED7FFH | FE700H | FFEFFH | F1000H | FE6FFH | 53.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 64 Kbytes | 4Kbytes | 6 Kbytes | RL78/F14 | 00000H | 0FFFFH | F1000H | F1FFFH | FE700H | FFEFFH | [Except 100 pins] F2000H [100 pins] F3000H | [Except 100 pins] FDEFFH [100 pins] FAEFFH | [Except 100 pins] 47.75 Kbytes [100 pins] 31.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| | 16 Kbytes | 4 Kbytes | 78K0R/Fx3 | 00000H | 0FFFFH | E9800H | ED7FFH | FEF00H | FFEFFH | F1000H | FEEFFH | 55.75Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 48 Kbytes | 4Kbytes | 4 Kbytes | RL78/F14 | 00000H | 0BFFFH | F1000H | F1FFFH | FEF00H | FFEFFH | F2000H | FBFFFH | 40 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| | 16 Kbytes | 3 Kbytes | 78K0R/Fx3 | 00000H | 0BFFFH | E9800H | ED7FFH | FF300H | FFEFFH | F1000H | FF2FFH | 56.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 32 Kbytes | 16 Kbytes | 2 Kbytes | 78K0R/Fx3 | 00000H | 07FFFH | E9800H | ED7FFH | FF700H | FFEFFH | F1000H | FF6FFH | 57.75 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |
| 24 Kbytes | 16 Kbytes | 1.5 Kbytes | 78K0R/Fx3 | 00000H | 05FFFH | E9800H | ED7FFH | FF900H | FFEFFH | F1000H | FF8FFH | 58.25 Kbytes | FFF00H | FFFFFH | F0000H | F07FFH |

**Figure 4-1 Memory maps of RL78/F14 and 78K0R/Fx3**

## 4.2 Illegal-memory access detection

This function triggers a reset if a memory space specified as access-prohibited is accessed.

Both of the RL78/F14 and the 78K0R/Fx3 are provided with this function; however, there are several differences in the illegal-memory access detection functions of the RL78/F14 and the 78K0R/Fx3, as shown in Table 4-3.

Confirm that these differences would not lead to problems.

**Table 4-3 Comparison of illegal-memory access detection functions between RL78/F14 and 78K0R/Fx3**

| | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Manipulation instruction for IAWCTL register | 8-bit memory manipulation instruction | 1-bit memory manipulation instruction or 8-bit memory manipulation instruction |
| Controlling Invalid memory access detection | ·Setting the WDTON bit of the option byte to "1" always enables the invalid memory access detection function regardless of the setting of the IAWEN bit.<br>·Clearing the WDTON bit of the option byte to "0" and setting the IAWEN bit to “1” enable the invalid memory access detection function. | ·Setting IAWEN bit to “1” enables the invalid memory access detection function. |
| Safety support function | - | Setting the GDIAW bit of the GUARD register to “1” enables the write access to the IAWCTL register |
| Restriction in write access to IAWEN bit | Only writing “1” to the IAWEN bit is valid. | - |

**<Key Points on Porting>**

·**Memory space specified as access-prohibited**

The size of the code flash memory and the RAM that are subject to illegal-memory access detection is set, using the invalid memory access detection function in the 78K0R/Fx3; however, in the RL78/F14, the size depends on the memory size of the product.

·**SFR Guard Function**

Safety Support Function of the 78K0R/Fx3 corresponds to SFR Guard Function of the RL78/F14; however, the registers protected by these functions differ, so make sure to take this into consideration when porting.

·**IAWCTL register manipulation instruction**

In the 78K0R/Fx3, the IAWCTL register can be accessed using an 8-bit memory manipulation instruction or a 1-bit memory manipulation instruction. On the other hand, in the RL78/F14, the register can be accessed using only an 8-bit memory manipulation, so make sure to take this into consideration when porting.

## 5. Reset

Reset sources are the same between the RL78/F14 and the 78K0R/Fx3. However, in the RL78/F14 and the 78K0R/Fx3, the configuration of the POC circuit and the voltage detector circuit differs. Also, they have different register information related to reset. Table 5-1 shows the comparison of each register status between the RL78/F14 and the 78K0R/Fx3 when a reset request is generated.

- Target registers: RESF, POCRES, LVIM, LVIS

**Table 5-1 Comparison of register status between RL78/F14 and 78K0R/Fx3 when reset request is generated**

| Reset sources | RL78/F14 | | | | | | | | | | 78K0R/Fx3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RESF (Note 1) | | | | POCRES | | LVIM | | | LVIS (Note 2) | RESF (Note 1) | | | | | POCRES | LVIM (Note 3) | LVIS (Note 4) |
| | TRAP | WDCLRF | IAWRF | LVIRF | POCRES0 | CLKRF | LVISEN | LVIOMSK | LVIF | | TRAP | WDRF | CLKRF | IAWRF | LVIRF | POCRES_0 | | |
| RESET input | ● | | | | - | ● | ● | - | | ● | ● | | | | | - | ● | ● |
| Reset by POC/POR | ● | | | | ● | | ● | - | | ● | ● | | | | | ● | ● | ● |
| Reset by execution of illegal instruction | ▲ | - | | | - | | ● | - | | ● | ▲ | - | | | | - | ● | ● |
| Reset by WDT | - | ▲ | - | | - | | ● | - | | ● | - | ▲ | - | | | - | ● | ● |
| Reset by clock monitor | - | ▲ | - | | - | ▲ | ● | - | | ● | - | | ▲ | - | | - | ● | ● |
| Reset by Illegal-memory access | - | | ▲ | - | - | | ● | - | | ● | - | | | ▲ | - | - | ● | ● |
| Reset by LVI/LVD | - | | | ▲ | - | | - | | | - | - | | | | ▲ | - | - | - |

●: Cleared (Initialized), ▲: Set, -: Held

Notes 1. Reading RESF register sets each bit to "0".

2. This register is initialized in the event of a reset except when the reset is triggered by an LVD event. The default value differs depending on LVIMDS[1:0] bits of the user option byte (000C1H/020C1H).
   When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
   When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
   When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H
3. This register is initialized in the event of a reset except when the reset is triggered by an LVI event. The default value differs depending on LVIOFF bit of the user option byte (000C1H/020C1H).
   When option byte LVIOFF = 0: 82H
   When option byte LVIOFF = 1: 00H
4. The generation of reset signal other than LVI initializes this register to 09H.

## 5.1 Reset function

The Power-on-reset function in the RL78/F14 corresponds to the Power-on-clear function in the 78K0R/Fx3.

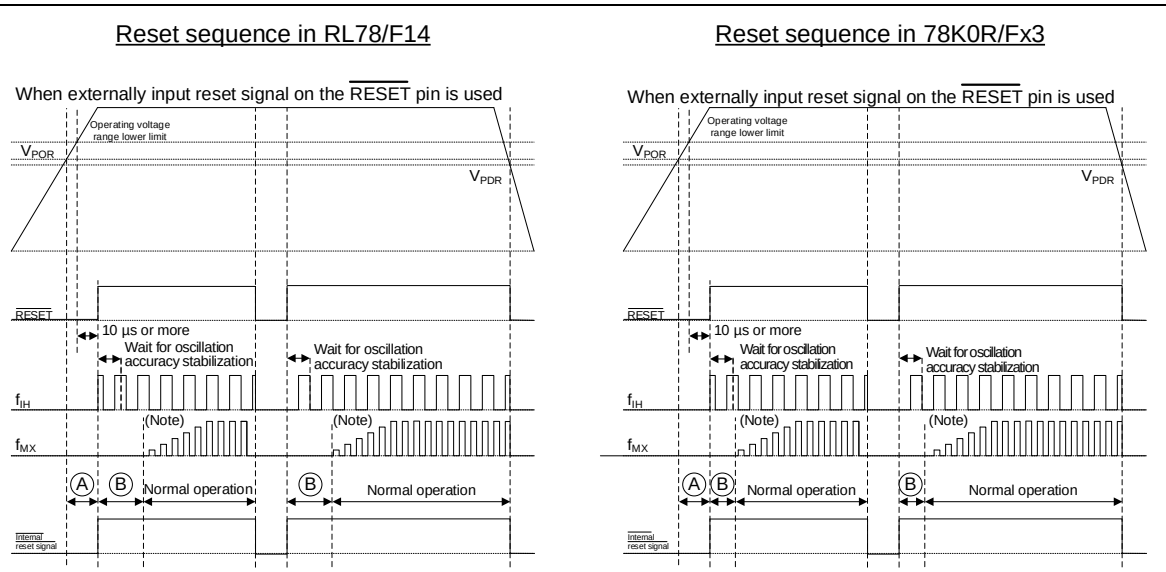
Table 5-2 shows the comparison of reset functions between the RL78/F14 and the 78K0R/Fx3.

**Table 5-2 Comparison of reset functions between RL78/F14 and 78K0R/Fx3**

| | | RL78/F14 | | 78K0R/Fx3 | |
|---|---|---|---|---|---|
| | | After first release of POR | After second release of POR | After first release of POC | After second release of POC |
| A: Voltage stabilization waiting time (Note) | | 0.99 ms (TYP.)<br>2.30 ms (MAX.) | - | 1.905 ms to 5.518 ms | - |
| B: Reset processing time (Note) | When LVD is in use | 0.672 ms (TYP.)<br>0.832 ms (MAX.) | 0.531 ms (TYP.)<br>0.675 ms (MAX.) | 0.195 ms to 0.322 ms | |
| | When LVD is off | 0.399 ms (TYP.)<br>0.519 ms (MAX.) | 0.259 ms (TYP.)<br>0.362 ms (MAX.) | | |
| Power supply rise detection voltage ($V_{POR}$) | | 1.56 V (TYP.) | | 1.61 V (TYP.) | |
| POR power supply fall detection voltage ($V_{PDR}$) | | 1.55 V (TYP.) | | 1.59 V (TYP.) | |

Note See **Figure 5-1** and **Figure 5-2**

Figure 5-1 shows the comparison of the reset sequences by the $\overline{\text{RESET}}$ pin between the RL78/F14 and the 78K0R/Fx3.

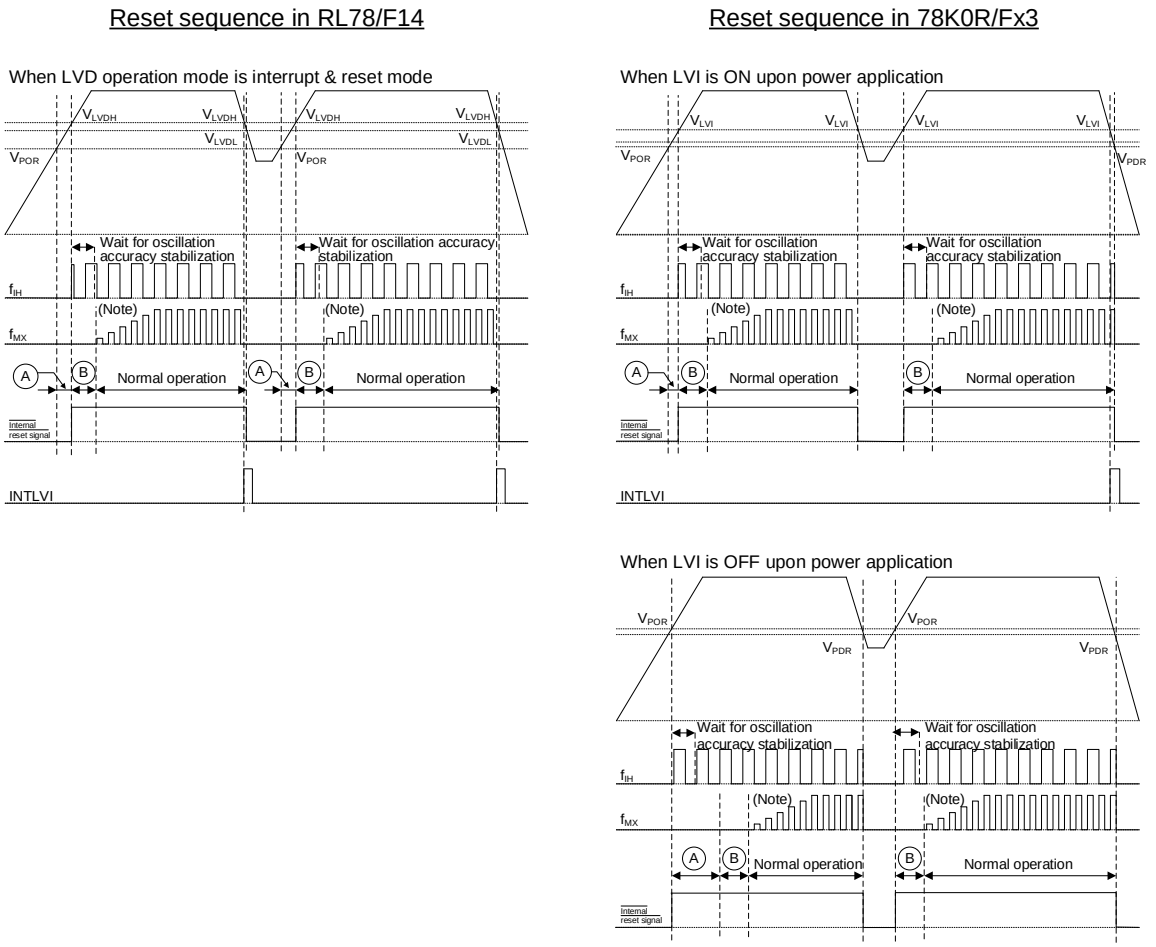



Note Set the start of oscillation via software.

Remark A: Voltage stabilization waiting time, B: Reset processing time
(A and B in the figure correspond to A and B in Table 5-2, respectively.)

**Figure 5-1 Comparison of reset sequences by $\overline{\text{RESET}}$ pins between RL78/F14 and 78K0R/Fx3**

Figure 5-2 shows the comparison of the reset sequences between the RL78/F14 and the 78K0R/Fx3.




Note Set the start of oscillation via software.

Remark A: Voltage stabilization waiting time, B: Reset processing time
(A and B in the figure correspond to A and B in Table 5-2, respectively.)

**Figure 5-2 Comparison of reset sequences between RL78/F14 and 78K0R/Fx3**

**<Key Points on Porting>**

·**Power supply voltage rising time**

The maximum power supply voltage rising slope between the RL78/F14 and the 78K0R/Fx3 differs significantly as shown in Figure 5-3 below.
Confirm that this difference would not lead to problems when you examine the specifications of your products or systems.

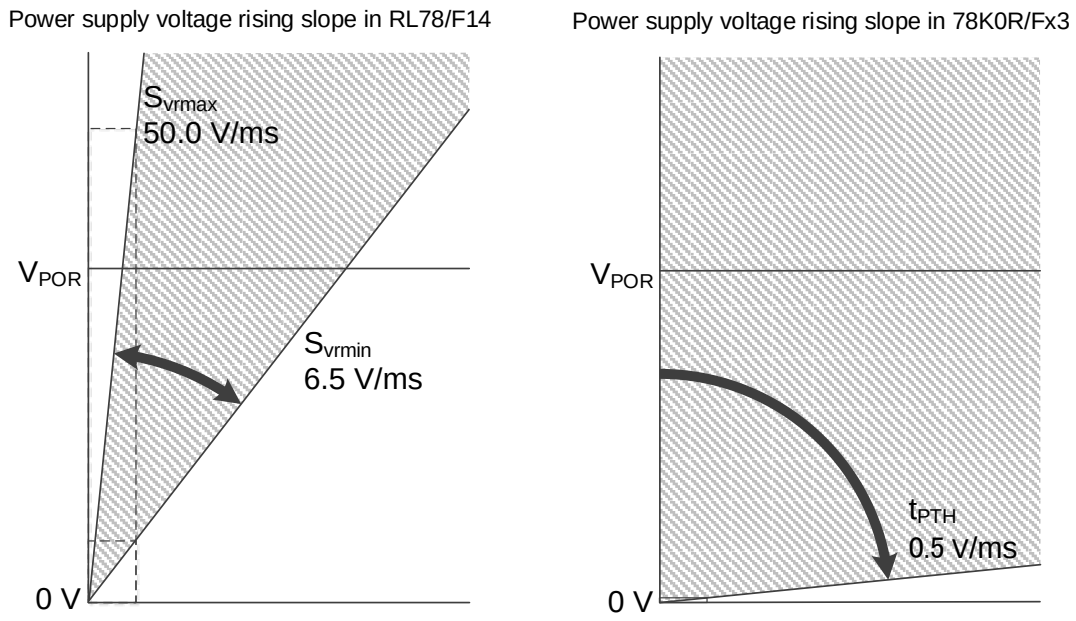



**Figure 5-3 Comparison of power supply voltage rising slope between RL78/F14 and 78K0R/Fx3**

# 6. Power supply

Table 6-1 shows the comparison of the power supply pins between the RL78/F14 and the 78K0R/Fx3.

**Table 6-1 Comparison of power supply pins between RL78/F14 and 78K0R/Fx3**

| Pins | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Power supply pins | $V_{DD}$<br>$EV_{DD0}$, $EV_{SS0}$<br>(Provided for products with 64, 80, or 100 pins) (Note 2)<br>$EV_{DD1}$, $EV_{SS1}$<br>(Provided for products with 100 pins) (Note 2)<br>$V_{SS}$ | $V_{DD}$<br>$EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, $EV_{SS1}$<br>(Provided for products with 100 pins) (Note 3)<br>$EV_{DD}$, $EV_{SS}$<br>(Provided for products with 30, 32, 40, 48, 64, or 80 pins) (Note 3)<br>$V_{SS}$ |
| Analog power supply pins | - | $AV_{SS}$ |
| | $AV_{REFP}$, $AV_{REFM}$ | $AV_{REF}$ |
| Regulator output pin for internal operation | REGC (Note 1) | REGC (Note 1) |

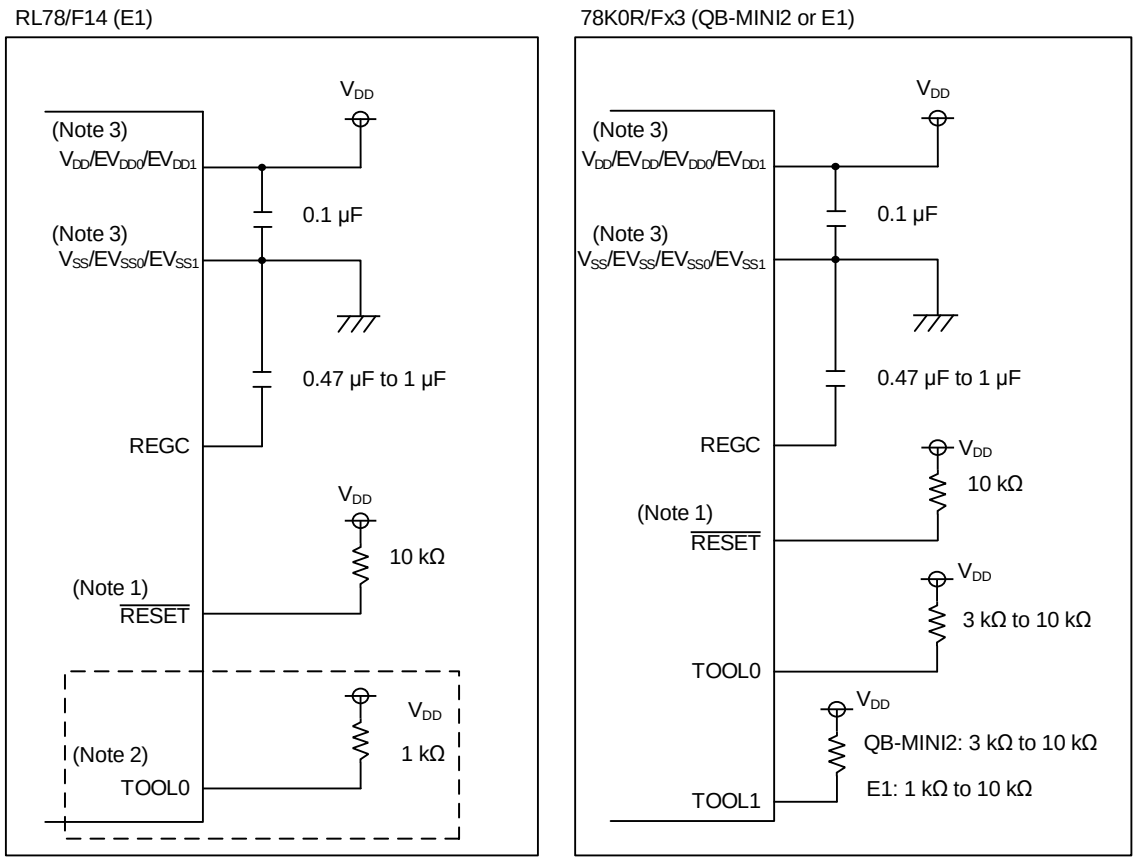
Notes 1. The REGC pin is used for stabilizing the internal voltage by being connected to a capacitor (bypass capacitor) (0.47 to 1 µF). For this reason, connect the REGC pin to GND via a bypass capacitor.

2. In the products for which none of $EV_{DD0}$ pin, $EV_{DD1}$ pin, $EV_{SS0}$ pin, nor $EV_{SS1}$ pin are provided (i.e. the products with 48 or fewer pins), it can be expressed as "$EV_{DD1} = EV_{DD0} = V_{DD}$" and "$EV_{SS1} = EV_{SS0} = V_{SS}$". In the products for which neither $EV_{DD1}$ pin nor $EV_{SS1}$ pin is provided (i.e. the products with 64 or 80 pins), it can be expressed as " $EV_{DD1}$=$EV_{DD0}$" and " $EV_{SS1}$=$EV_{SS0}$".

3. In the products for which none of $EV_{DD0}$ pin, $EV_{DD1}$ pin, $EV_{SS0}$ pin, nor $EV_{SS1}$ pin are provided (i.e. the products with 80 or fewer pins), it can be expressed as "$EV_{DD1} = EV_{DD0} = EV_{DD}$" and "$EV_{SS1} = EV_{SS0} = EV_{SS}$".

## 6.1 Basic circuit architecture

Figure 6-1 shows the necessary connections of the pins in order to operate the RL78/F14 and the 78K0R/Fx3.




Notes 1. Connect the $\overline{\text{RESET}}$ pin via resistor to $V_{DD}$.

2. When E1 is not connected to RL78/F14, the pin connection indicated by the dotted line in the figure is not necessary. This document shows the pin connection when serial communication via a single-line UART (E1) is performed using the TOOL0 pin. Perform the necessary pin connection as needed since the commnunication mode might differ depending on the flash memory programmer you use.

3. The power supply pins differ depending on the products, as shown below.

RL78/F14 Power supply pins

| RL78/F14 | 30 pins | 32 pins | 48 pins | 64 pins | 80 pins | 100 pins |
|---|---|---|---|---|---|---|
| $V_{DD}$ | ○ | ○ | ○ | ○ | ○ | ○ |
| $EV_{DD0}$ | - | - | - | ○ | ○ | ○ |
| $EV_{DD1}$ | - | - | - | - | - | ○ |
| $V_{SS}$ | ○ | ○ | ○ | ○ | ○ | ○ |
| $EV_{SS0}$ | - | - | - | ○ | ○ | ○ |
| $EV_{SS1}$ | - | - | - | - | - | ○ |

○: Provided -: Not provided

78K0R/Fx3 power supply pins

| 78K0R/Fx3 | 30 pins | 32 pins | 40 pins | 48 pins | 64 pins | 80 pins | 100 pins |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| $EV_{DD0}$ | - | - | - | - | - | - | ○ |
| $EV_{DD1}$ | - | - | - | - | - | - | ○ |
| $EV_{DD}$ | ○ | ○ | ○ | ○ | ○ | ○ | - |
| $V_{SS}$ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| $EV_{SS0}$ | - | - | - | - | - | - | ○ |
| $EV_{SS1}$ | - | - | - | - | - | - | ○ |
| $EV_{SS}$ | ○ | ○ | ○ | ○ | ○ | ○ | - |

○: Provided -: Not provided

**Figure 6-1 Comparison of connections of pins between RL78/F14 and 78K0R/Fx3**

**<Key Points on Porting>**

·**Resistance for TOOL0**

As shown in Figure 6-1, the pull-up resistance for TOOL0 differs between the 78K0R/Fx3 and the RL78/F14.
3 kΩ to 10 kΩ is set in the 78K0R/Fx3. On the other hand, 1 kΩ is set in the RL78/F14. Attention must be paid when you design boards.

## 6.2 Voltage detection function

Table 6-2 shows the comparison of voltage detection functions between the RL78/F14 and the 78K0R/Fx3.

The RL78/F14 is not equipped with either a detection function of input voltage from external input pin or a low-voltage detection flag output (LVIOUT), with which the 78K0R/Fx3 is equipped.

The low-voltage detection level can be selected as one of 10 levels in the 78K0R/Fx3. On the other hand, it can be selected as one of 6 levels (4 levels in interrupt & reset mode) in the RL78/F14 as shown in Table 6-3. Confirm that this difference would not lead to problems when you examine the specifications of your products or systems.

**Table 6-2 Comparison of voltage detection functions between RL78/F14 and 78K0R/Fx3**

| | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Interrupt & reset | $V_{DD} < V_{LVDH}$ → Generates an internal interrupt<br>$V_{DD} < V_{LVDL}$ → Generates an internal reset signal<br>$V_{DD} \geq V_{LVDH}$ → Releases the reset signal | - |
| Reset | $V_{DD} < V_{LVD}$ → Generates an internal reset signal<br>$V_{DD} \geq V_{LVD}$ → Releases the reset signal | $V_{DD} < V_{LVI}$ → Generates an internal reset signal<br>$V_{DD} \geq V_{LVI}$ → Releases the reset signal |
| Interrupt | When the supply voltage drops and becomes lower than $V_{LVD}$ ($V_{DD} < V_{LVD}$) → Generates an internal interrupt<br>When the supply voltage rises and becomes $V_{LVD}$ or higher ($V_{DD} \geq V_{LVD}$) → Generates an internal interrupt<br>When the supply voltage rises and becomes $V_{LVD}$ or higher ($V_{DD} \geq V_{LVD}$) at power on →Releases the reset signal | When the supply voltage drops and becomes lower than $V_{LVI}$ ($V_{DD} < V_{LVI}$) → Generates an internal interrupt<br>When the supply voltage rises and becomes $V_{LVI}$ or higher ($V_{DD} \geq V_{LVI}$) → Generates an internal interrupt |
| External input internal reset | - | EXLVI < $V_{EXLVI}$<br>→ Generates an internal reset signal<br>EXLVI ≥ $V_{EXLVI}$<br>→ Releases the reset signal |
| External input interrupt | - | When the input voltage drops lower than $V_{EXLVI}$ (EXLVI < $V_{EXLVI}$) → Generates an internal interrupt<br>When the input voltage becomes $V_{EXLVI}$ or higher (EXLVI ≥ $V_{EXLVI}$) → Generates an internal interrupt |

Remark $V_{LVD}$ indicates the low-voltage detection level of the RL78/F14 and $V_{LVI}$ indicates that of the 78K0R/Fx3. EXLVI indicates the input voltage. $V_{EXLVI}$ indicates the detection voltage.

**Table 6-3 Comparison of low-voltage detection levels between RL78/F14 and 78K0R/Fx3**

| | RL78/F14 | | 78K0R/Fx3 |
|---|---|---|---|
| Interrupt & reset<br>$V_{LVDH}$, $V_{LVDL}$ | $V_{LVDH}$ | $V_{LVDL}$ | - |
| | 4.42 V (TYP.) (When power supply is rising) and 4.32 V (TYP.) (When power supply is falling)<br>4.62 V (TYP.) (When power supply is rising) and 4.52 V (TYP.) (When power supply is falling)<br>3.32 V (TYP.) (When power supply is rising) and 3.15 V (TYP.) (When power supply is falling)<br>4.74 V (TYP.) (When power supply is rising) and 4.64 V (TYP.) (When power supply is falling) | 2.75 V (TYP.) (When power supply is falling) | |
| Reset/Interrupt<br>$V_{LVD}$ $V_{LVI}$ (Note 1) | 2.81 V (TYP.) (When power supply is rising) and 2.75 V (TYP.) (When power supply is falling)<br>3.02 V (TYP.) (When power supply is rising) and 2.96 V (TYP.) (When power supply is falling)<br>3.22 V (TYP.) (When power supply is rising) and 3.15 V (TYP.) (When power supply is falling)<br>4.42 V (TYP.) (When power supply is rising) and 4.32 V (TYP.) (When power supply is falling)<br>4.62 V (TYP.) (When power supply is rising) and 4.52 V (TYP.) (When power supply is falling)<br>4.74 V (TYP.) (When power supply is rising) and 4.64 V (TYP.) (When power supply is falling) | | 2.84 V (TYP.)<br>2.99 V (TYP.)<br>3.15 V (TYP.)<br>3.30 V (TYP.)<br>3.45 V (TYP.)<br>3.61 V (TYP.)<br>3.76 V (TYP.)<br>3.92 V (TYP.)<br>4.07 V (TYP.)<br>4.22 V (TYP.) |
| External input $V_{EXLVI}$ (Note 2) | - | | 1.21 V (TYP.) |

Notes 1. $V_{LVD}$ indicates the low-voltage detection level of the RL78/F14 and $V_{LVI}$ indicates that of the 78K0R/Fx3.

2. RL78/F14 products are not equipped with $V_{EXLVI}$.

# 7. Clock generator

Table 7-1 shows the comparison of functions of the clock generator between the RL78/F14 and the 78K0R/Fx3.

**Table 7-1 Comparison of functions of clock generator between RL78/F14 and 78K0R/Fx3**

| Functions | RL78/F14 | | 78K0R/Fx3 | |
|---|---|---|---|---|
| Main system clock | $f_X$ : | 1 MHz to 20 MHz | $f_X$ : | 2 MHz to 20 MHz |
| Subsystem clock | $f_{SUB}$ : | 32.768 kHz (Products with 48, 64, 80, or 100pins) | - | |
| On-chip oscillator | Low-speed ($f_{IL}$): | 15 kHz (TYP.) | Low-speed ($f_{IL}$): | 30 kHz (TYP.) |
| | High-speed ($f_{IH}$): | 64 MHz (TYP.) (Note) | High-speed ($f_{IH}$): | 8 MHz (TYP.) |
| | | 48 MHz (TYP.) (Note) | | 4 MHz (TYP.) |
| | | 32 MHz (TYP.) | | |
| | | 24 MHz (TYP.) | | |
| | | 16 MHz (TYP.) | | |
| | | 12 MHz (TYP.) | | |
| | | 8 MHz (TYP.) | | |
| | | 4 MHz (TYP.) | | |
| | | 1 MHz (TYP.) | | |
| PLL | $f_{PLL}$ : | 64 MHz | $f_{PLL}$ : | 24 MHz |
| | | 48 MHz | | 16 MHz |
| | | 32 MHz | | |
| | | 24 MHz | | |
| WDT-dedicated low-speed on-chip oscillator clock | $f_{WDT}$ : | 15 kHz (TYP.) | - | |

Note When 64 MHz or 48 MHz is selected as $f_{IH}$, the initial setting of the $f_{MP}$ clock division register (MDIV) is "division by 2" after a reset release.

**<Key Points on Porting>**

·**Temperature Restriction in operation frequency**

The maximum operation frequencies of Grade K (-40 to +125°C) and Grade Y (-40 to +150°C) in the RL78/F14 are 24 MHz. Therefore do not select 32 MHz or 64 MHz as the frequency of the high-speed on-chip oscillator.

## 7.1 Procedure for setting X1 clock (main system clock) after reset release

In the same way that the CPU in the 78K0R/Fx3 starts operating with the internal high-speed oscillation clock ($f_{IH}$) after a reset release, the CPU in the RL78/F14 starts operating with the high-speed on-chip oscillator ($f_{IH}$) after a reset release.

The frequency of the high-speed on-chip oscillator ($f_{IH}$) in the RL78/F14 can be selected from among 64, 48, 32, 24, 16, 12, 8, 4, or 1 MHz by using the user option byte (000C2H/020C2H). Selecting 64 MHz or 48 MHz as $f_{IH}$ provides the MDIV register with its default value, i.e. 01H ($f_{MP}$/2 is selected) so that the CPU/peripheral clock is set to 32 MHz or 24 MHz after a reset release, respectively. As for the option bytes, see the user's manual.

The oscillaiton of each X1 clock ($f_x$) of the RL78/F14 and the 78K0R/Fx3 has stopped.

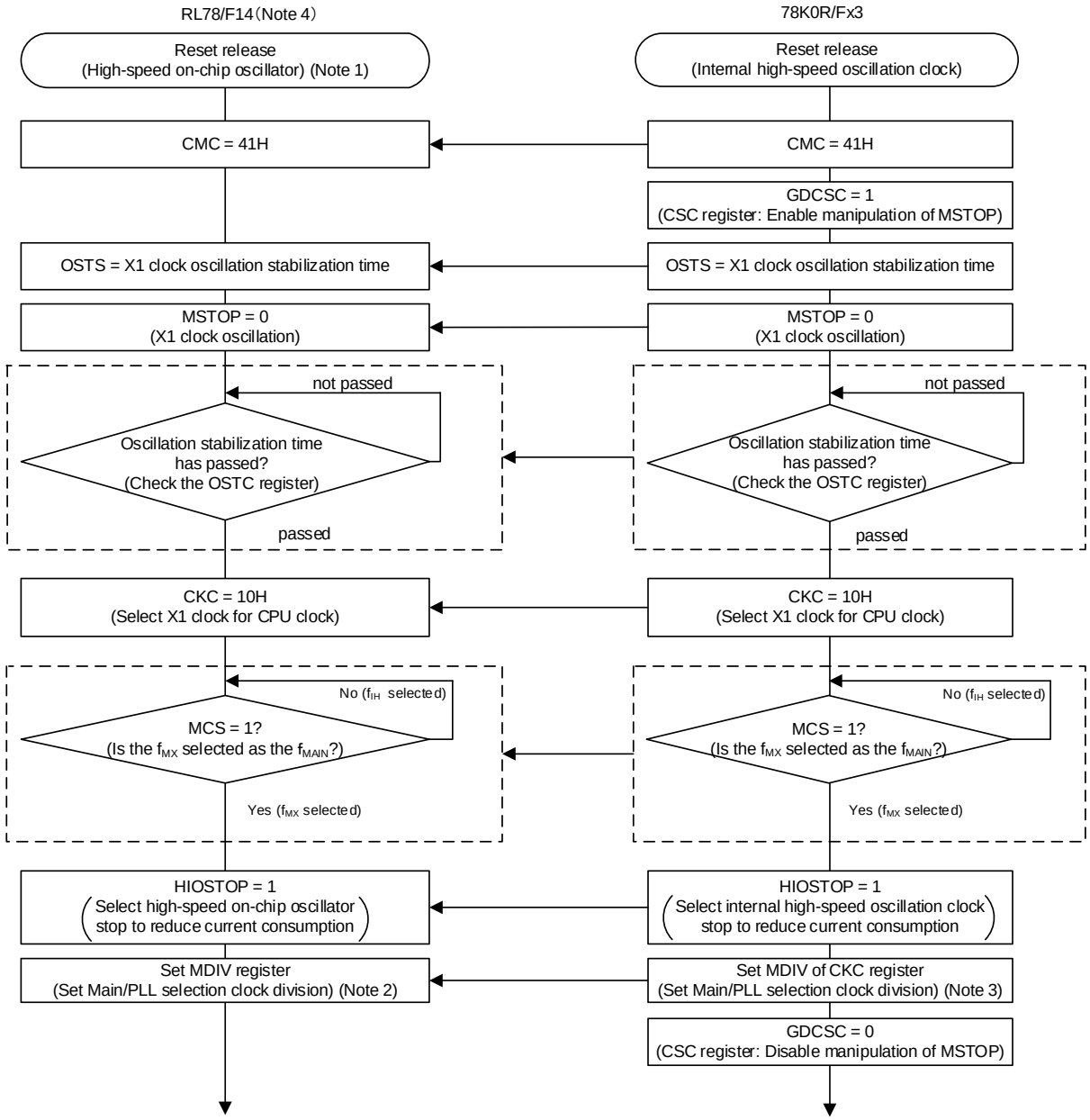
**<Key Points on Porting>**

**·Specific-register manipulation protection register**

The protection against manipulation of the clock operation status control register is enabled or disabled by the GDCSC bit in the procedure for setting the X1 clock executed after a reset in 78K0R/Fx3 (See **Figure 7-1**).

The GDCSC bit in the 78K0R/Fx3 is disabled during reset. The GCSC bit in the RL78/F14 is equivalent to the GDCSC bit; however, the GCSC bit is set to "0" (The clock control function and the register guard function of the voltage detector are disabled) after a reset. See the user's manual for details.

Figure 7-1 shows the procedure for setting the X1 clock after reset in the RL78/F14 and the 78K0R/Fx3.




Notes 1. In the RL78/F14, the CPU clock setting after a reset release is selected using the user option byte. Since the frequency of the CPU clock differs from that in the 78K0R/Fx3, the timing when the WDT counter is cleared and starts counting again differs. Be sure to evaluate after porting.

2. Set the frequency after division of the clock to be no higher than 32 MHz for the Grade L products, and no higher than 24 MHz for the Grade K and Grade Y products.
3. Set the frequency after the division of the clock to be no higher than 24 MHz.
4. The RL78/F14 is provided with the SFR guard function, but the setting for the function is ommitted, because the function is disabled after reset.

**Figure 7-1 Procedure for setting X1 Clock after reset in RL78/F14 and 78K0R/Fx3**

## 7.2 PLL Clock

Table 7-2 shows some examples of porting the code for PLL clock from the 78K0R/Fx3 to the RL78/F14.

**Table 7-2 Example of porting code for PLL clock from 78K0R/Fx3 to RL78/F14**

| $f_{PLL}$ | RL78/F14 | | | 78K0R/Fx3 | | | |
|---|---|---|---|---|---|---|---|
| | PLL input clock ($f_{MAIN}$) | PLL division (PLLDIV0) | PLL multiplication (PLLMUL) | PLL input clock ($f_{MAIN}$) | PLL division (PLLDIV0) | PLL multiplication (OPTPLL) | Division (PLLDIV1) |
| 64 MHz | 8 MHz | Division by 2 | Multiplying by 16 | Setting prohibited | | | |
| 48 MHz | 8 MHz | Division by 2 | Multiplying by 12 | Setting prohibited | | | |
| 32 MHz | 8 MHz | Division by 4 | Multiplying by 16 | Setting prohibited | | | |
| | 4 MHz | Division by 2 | Multiplying by 16 | | | | |
| 24 MHz | 8 MHz | Division by 4 | Multiplying by 12 | 8 MHz | Division by 2 | Multiplying by 6 | Division by 1 |
| | 4 MHz | Division by 2 | Multiplying by 12 | 4 MHz | Division by 1 | Multiplying by 6 | Division by 1 |
| 16 MHz | Setting prohibited | | | 8 MHz | Division by 2 | Multiplying by 8 | Division by 2 |
| | | | | 4 MHz | Division by 1 | Multiplying by 8 | Division by 2 |

## 7.3 Clock monitor function

Whether the clock oscillation has stopped or not can be detected by using the clock monitor function. The clock monitor function samples the main system clock and the PLL clock using the low-speed on-chip oscillator ($f_{SL}$). An internal reset signal or an internal interrupt signal is generated when each clock stops as follows:

- When oscillation of the main system clock stops: An internal reset signal is generated.
- When the PLL clock stops: The clock through mode is forcibly selected (the SELPLLS bit is cleared) and an internal interrupt signal is generated.

**<Key Points on Porting>**

**·Restrictions when using low-speed on-chip oscillator**

One of the ways to disable the oscillation stop detection function in the RL78/F14 is to stop the oscillation of the low-speed on-chip oscillator.

If peripheral functions which use the low-speed on-chip oscillator as shown below are used for your product, confirm that stopping oscillation of low-speed on-chip oscillator would not lead to problems.

- Low-speed on-chip oscillator clock frequency ($f_{IL}$).

  TAU0 Channel 1, Clock monitor, Timer RJ (WUTMMCK0 bit = 1)

- Subsystem/low-speed on-chip oscillator select clock frequency ($f_{IL}$).

  Clock output/buzzer output, Timer RJ, Timer RD

# 8. Current

Table 8-1 shows the comparison of the current of each operating mode between the RL78/F14 and the 78K0R/Fx3.

**Table 8-1 Comparison of current of each operating mode between RL78/F14 and 78K0R/Fx3**

| | Total current (Conditions: $f_{MX}$ = 20 MHx, $f_{CLK}$ = $f_{MX}$) | | | | | |
|---|---|---|---|---|---|---|
| | RL78/F14 | | | | 78K0R/Fx3 | |
| Operation mode | Grade L | 9.0 mA (MAX.) | | | (A) grade products | 15.0 mA (MAX.) |
| | Grade K | | | | (A2) grade products | 15.5 mA (MAX.) |
| | Grade Y | 9.5 mA (MAX.) | | | - | |
| HALT mode | Grade L | 6.0 mA (MAX.) | | | (A) grade products | 8.0 mA (MAX.) |
| | Grade K | | | | (A2) grade products | |
| | Grade Y | 6.5 mA (MAX.) | | | - | |
| STOP mode | Grade L | 30 pins | | 0.03 mA (MAX.) $T_A$ = +105°C | (A) grade products | 0.025 mA (MAX.) $T_A$ = +85°C |
| | | 32 pins | | 0.03 mA (MAX.) $T_A$ = +105°C | | |
| | | 48 pins, 64 pins, 80 pins | Products with up to 96 Kbytes of code flash memory | 0.03 mA (MAX.) $T_A$ = +105°C | | |
| | | | Products with at least 128 Kbytes of code flash memory | 0.05 mA (MAX.) $T_A$ = +105°C | | |
| | | 100 pins | | 0.05 mA (MAX.) $T_A$ = +105°C | | |
| | Grade K | 30 pins | | 0.06 mA (MAX.) $T_A$ = +125°C | (A2) grade products | 0.120 mA (MAX.) $T_A$ = +125°C |
| | | 32 pins | | 0.06 mA (MAX.) $T_A$ = +125°C | | |
| | | 48 pins, 64 pins, 80 pins | Products with up to 96 Kbytes of code flash memory | 0.06 mA (MAX.) $T_A$ = +125°C | | |
| | | | Products with at least 128 Kbytes of code flash memory | 0.10 mA (MAX.) $T_A$ = +125°C | | |
| | | 100 pins | | 0.10 mA (MAX.) $T_A$ = +125°C | | |
| | Grade Y | 30 pins | | 0.15 mA (MAX.) $T_A$ = +150°C | - | |
| | | 32 pins | | 0.15 mA (MAX.) $T_A$ = +150°C | | |
| | | 48 pins, 64 pins, 80 pins | Products with up to 96 Kbytes of code flash memory | 0.15 mA (MAX.) $T_A$ = +150°C | | |
| | | | Products with at least 128 Kbytes of code flash memory | 0.25 mA (MAX.) $T_A$ = +150°C | | |
| | | 100 pins | | 0.25 mA (MAX.) $T_A$ = +150°C | | |

Table 8-2 shows the comparison of the current of each function between the RL78/F14 and the 78K0R/Fx3.

**Table 8-2 Comparison of current of each function between RK78/F14 and 78K0R/Fx3**

| Items | RL78/F14 | | 78K0R/Fx3 | |
|---|---|---|---|---|
| Watchdog timer operating current | Grade L | 0.22 mA (TYP.) $f_{IL}$ = 15 kHz | (A) grade products | 0.52 mA (TYP.) $f_{IL}$ = 30 kHz |
| | Grade K | | (A2) grade products | |
| | Grade Y | | - | |
| A/D converter operating current | Grade L | 1.7 mA (MAX.) When conversion at maximum speed | (A) grade products | 3.2 mA (MAX.) When conversion at maximum speed |
| | Grade K | | (A2) grade products | |
| | Grade Y | | - | |
| LVI (LVD) operating current | Grade L | 0.08 µA (TYP.) | (A) grade products | 9.0 µA (TYP.) |
| | Grade K | | (A2) grade products | |
| | Grade Y | | - | |

**<Key Points on Porting>**

·**STOP Mode current (1)**

The current in the 78K0R/Fx3 (A) grade is 0.025 mA; whereas that in the RL78/F14 Grade L is either 0.03 mA or 0.05 mA, i.e. higher than that in the 78K0R/Fx3 (A) grade products.

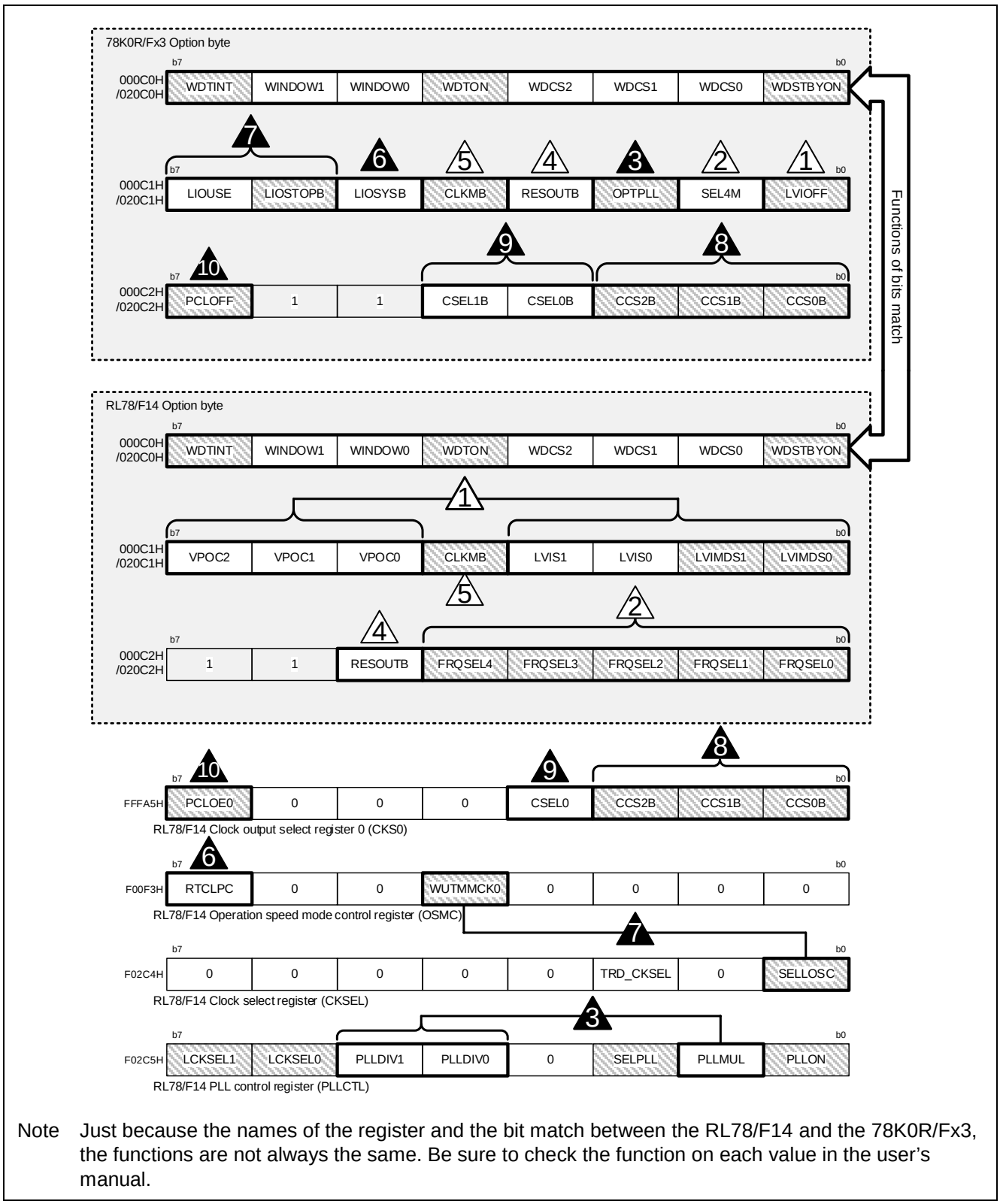
So confirm that it would not lead to problems when porting from the 78K0R/Fx3 (A) grade products to the RL78/F14 Grade L products.

·**STOP Mode current (2)**

When porting from the 78K0R/Fx3 (A2) grade products to the RL78/F14 Grade K products, take into consideration that the current in the RL78/F14 Grade K is either 0.06 mA or 0.10 mA, whereas that in the 78K0R/Fx3 (A2) grade is 0.120 mA.

## 9. Option byte

Some parts of the option bytes in the 78K0R/Fx3 are relocated to other registers in the RL78/F14. Figure 9-1 shows the comparison of the register configuration of the option bytes between the RL78/F14 and the 78K0R/Fx3.




Note Just because the names of the register and the bit match between the RL78/F14 and the 78K0R/Fx3, the functions are not always the same. Be sure to check the function on each value in the user's manual.

**Figure 9-1 Comparison of register configuration of option byte between RL78/F14 and 78K0R/Fx3**

**Table 9-1 Supplementary information for comparison of register configuration of option byte between RL78/F14 and 78K0R/Fx3**

| Number | Functions | |
|---|---|---|
| △1 | Setting for the low-voltage detector | Option bytes of 78K0R/Fx3 → Option bytes of RL78/F14 |
| △2 | Internal high-speed oscillation clock (On-chip oscillator) frequency selection | |
| △4 | P130 function selection (Normal output port/RESOUT pin) | |
| △5 | Clock monitor operation control | |
| ▲3 | PLL multiplication selection | Option bytes of 78K0R/Fx3 → Other control registers of RL78/F14 |
| ▲6 | Internal low-speed oscillation ($f_{IL}$)→ Setting for the peripheral hardware clock ($f_{CLK}$) | |
| ▲7 | Setting for the internal low-speed oscillation operation | |
| ▲8 | Clock output selection ($f_{MAIN}$/$f_{PLL}$/$f_{IL}$/$f_{SUB}$) | |
| ▲9 | Clock output division value selection | |
| ▲10 | Clock output enable/disable | |

**<Key Points on Porting>**

·**Power-on-reset**

In order to operate the RL78/F14 equivalent functionality to that of the Power-on-clear circuit in the 78K0R/Fx3, set the following values to the option bytes:

Option byte 000C1/020C1H: LVIMDS1, LVIMDS0 = 1, 1 (Reset mode)

·**Voltage detection level**

The voltage detection levels of the power-on-reset circuit in the RL78/F14 are different from those in the 78K0R/Fx3. The voltage drop detection threshold in the RL78/F14 cannot be set to the same value as the 78K0R/Fx3; however, the closest value can be set by using the option byte. Confirm that the difference would not lead to problems.

## 10. Protect function

The RL78/F14 is provided with the SFR guard function, which is equivalent to the safety support function (the GUARD register) in the 78K0R/Fx3.

The SFR guard function can be controlled by the invalid memory access detection control register (IAWCTL).

If the SFR guard function is specified, writing to SFRs which are subject to the guard is disabled, but reading from these SFRs can be carried out.

The functions and bits protected by SFR guard function are shown below.

·**Port function**

Control bit: GPORT bit (bit 2 of the IAWCTL register)

Guarded SFR: PMxx, PUxx, PIMxx, POMxx, PMCxx, PITHLxx, ADPC, PIORx

·**Interrupt function**

Control bit: GINT bit (bit 1 of the IAWCTL register)

Guarded SFR: IFxx, MKxx, PRxx, EGPx, EGNx

·**Clock control function and voltage detector**

Control bit: GCSC bit (bit 0 of the IAWCTL register)

Guarded SFR: CMC, CSC, OSTS, CKC, PER0, PER1, PER2, OSMC, LVIM, LVIS,
CANCKSEL, LINCKSEL, CKSEL, PLLCTL, MDIV, RTCCL, POCRES, STPSTC

**<Key Points on Porting>**

·**Protected condition after reset release**

In the 78K0R/Fx3, writing to the special registers such as the registers for the low-voltage detector (LVI) and clock control is prohibited by the GUARD register after a reset release.

In the RL78/F14, writing to the special registers which control the port function, the interrupt function, the clock control function, and the low-voltage detector function is valid. If you need to operate the RL78/F14 in the same way as the 78K0R/Fx3, disable writing to the corresponding SFRs by setting the corresponding control bit of the IAWCTL register.

# 11. I/O Port

## 11.1 Port configuration

The comparison of the I/O ports between the RL78/F14 and the 78K0R/Fx3 is shown in Table 11-1 to Table 11-7, broken down by the number of pins for each product.

### 11.1.1 100-pin products

**Table 11-1 Comparison of I/O ports between RL78/F14 (100 pins) and 78K0R/FG3**

| | RL78/F14 (100 pins) | 78K0R/FG3 (100 pins) |
|---|---|---|
| I/O ports | P00 to P03<br>P10 to P17 (Note 1)<br>P30 to P34<br>P40 to P47<br>P50 to P57<br>P60 to P63 (Note 1), P64 to P67<br>P70 to P72 (Note 1), P73 to P77<br>P80 to P87<br>P90 to P97<br>P100 to P107<br>P120 (Note 1), P121 to P124 (Note 3), P125 to P127<br>P130 (Note 4), P137 (Note 3)<br>P140<br>P150 to P157 | P00 to P03<br>P10 to P17<br>P30 to P32<br>P40 to P41, P42 to P43 (Note 2), P44 to P47<br>P50 to P57<br>P60 to P67<br>P70 to P71, P72 (Note 2), P73, P74 (Note 2), P75, P76 (Note 2), P77<br>P80 to P87<br>P90 to P97<br>P100 to P107<br>P120, P121 to P124 (Note 3), P125 to P127<br>P130 (Note 4)<br>P140<br>P150 to P157 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM6, POM7, POM12) to “1”.
2. N-ch open-drain output ($V_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM4, POM7) to “1”.
3. The ports are input-only.
4. The ports are output-only.

### 11.1.2 80-pin products

**Table 11-2 Comparison of I/O ports between RL78/F14 (80 pins) and 78K0R/FF3**

| | RL78/F14 (80 pins) | 78K0R/FF3 (80 pins) |
|---|---|---|
| I/O ports | P00 to P02<br>P10 to P17 (Note 1)<br>P30 to P34<br>P40 to P47<br>P50 to P57<br>P60 to P63 (Note 1), P64 to P67<br>P70 to P72 (Note 1), P73 to P77<br>P80 to P87<br>P90 to P97<br>P120 (Note 1), P121 to P124 (Note 3), P125 to P126<br>P130 (Note 4), P137 (Note 3)<br>P140 | P00 to P02<br>P10 to P17<br>P30 to P32<br>P40 to P41, P42 to P43 (Note 2),P44 to P47<br>P50 to P57<br>P60 to P67<br>P70 to P71, P72 (Note 2), P73, P74 (Note 2), P75, P76 (Note 2), P77<br>P80 to P87<br>P90 to P97<br>P120, P121 to P124 (Note 3), P125 to P126<br>P130 (Note 4)<br>P140 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM6, POM7, POM12) to “1”.
2. N-ch open-drain output ($V_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM4, POM7) to “1”.
3. The ports are input-only.
4. The ports are output-only.

### 11.1.3 64-pin products

**Table 11-3 Comparison of I/O ports between RL78/F14 (64 pins) and 78K0R/FE3**

| | RL78/F14 (64 pins) | 78K0R/FE3 (64 pins) |
|---|---|---|
| I/O ports | P00<br>P10 to P17 (Note 1)<br>P30 to P34<br>P40 to P43<br>P50 to P53<br>P60 to P63 (Note 1)<br>P70 to P72 (Note 1), P73 to P77<br>P80 to P87<br>P90 to P96<br>P120 (Note 1), P121 to P124 (Note 3), P125<br>P130 (Note 4), P137 (Note 3)<br>P140 | P00<br>P10 to P17<br>P30 to P32<br>P40 to P41, P42 to P43 (Note 2)<br>P50 to P53<br>P60 to P63<br>P70 to P71, P72 (Note 2),P73, P74 (Note 2), P75, P76 (Note 2), P77<br>P80 to P87<br>P90 to P96<br>P120, P121 to P124 (Note 3), P125<br>P130 (Note 4)<br>P140 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM6, POM7, POM12) to “1”.
2. N-ch open-drain output ($V_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM4, POM7) to “1”.
3. The ports are input-only.
4. The ports are output-only.

### 11.1.4 48-pin products

**Table 11-4 Comparison of I/O ports between RL78/F14 (48 pins) and 78K0R/FC3 (48 pins)**

| | RL78/F14 (48 pins) | 78K0R/FC3 (48 pins) |
|---|---|---|
| I/O ports | P00<br>P10 to P17 (Note 1)<br>P30 to P34<br>P40, P41<br>P60 to P63 (Note 1)<br>P70 to P72 (Note 1), P73<br>P80 to P87<br>P90 to P92<br>P120 (Note 1), P121 to P124 (Note 3), P125<br>P130 (Note 4), P137 (Note 3)<br>P140 | P00<br>P10 to P17<br>P30 to P32<br>P40, P41<br>P60 to P63<br>P70 to P71, P72 (Note 2), P73<br>P80 to P87<br>P90 to P92<br>P120, P121 to P124 (Note 3), P125<br>P130 (Note 4)<br>P140 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM6, POM7, POM12) to “1”.
2. N-ch open-drain output ($V_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM7) to “1”.
3. The ports are input-only.
4. The ports are output-only.

### 11.1.5 40-pin products

**Table 11-5 Comparison of I/O ports between RL78/F14 (48 pins) and 78K0R/FC3 (40 pins)**

| | RL78/F14 (48 pins) | 78K0R/FC3 (40 pins) |
|---|---|---|
| I/O ports | P00<br>P10 to P17 (Note 1)<br>P30 to P34<br>P40 to P41<br>P60 to P63 (Note 1)<br>P70 to P72 (Note 1), P73<br>P80 to P87<br>P90 to P92<br>P120 (Note 1), P121 to P124 (Note 3), P125<br>P130 (Note 4), P137 (Note 3)<br>P140 | <br>P10 to P17<br>P30 to P32<br>P40 to P41<br>P60 to P63<br>P70 to P71, P72 (Note 2), P73<br>P80 to P87<br><br>P120, P121 to P122 (Note 3), P125 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM6, POM7, POM12) to “1”.
2. N-ch open-drain output ($V_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM7) to “1”.
3. The ports are input-only.
4. The port is output-only.

### 11.1.6 32-pin products

**Table 11-6 Comparison of I/O ports between RL78/F14 (32 pins) and 78K0R/FB3 (32 pins)**

| | RL78/F14 (32 pins) | 78K0R/FB3 (32 pins) |
|---|---|---|
| I/O ports | P10 to P17 (Note 1)<br>P30, P33 to P34<br>P40 to P41<br>P60 to P63 (Note 1)<br>P80 to P85<br>P120 (Note 1), P121 to P122 (Note 2), P125<br>P137 (Note 2) | P10 to P17<br>P30<br>P40 to P41<br>P60 to P63<br>P80 to P85<br>P120, P121 to P122 (Note 2), P125 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM6, POM12) to “1”.
2. The ports are input-only.

### 11.1.7 30-pin products

**Table 11-7 Comparison of I/O ports between RL78/F14 (30 pins) and 78K0R/FB3 (30 pins)**

| | RL78/F14 (30 pins) | 78K0R/FB3 (30 pins) |
|---|---|---|
| I/O ports | P10 to P17 (Note 1)<br>P30, P33 to P34<br>P40 to P41<br>P80 to P87<br>P120 (Note 1), P121 to P122 (Note 2), P125<br>P137 (Note 2) | P10 to P17<br>P30<br>P40 to P41<br>P80 to P87<br>P120, P121 to P122 (Note 2), P125 |

Notes 1. N-ch open-drain output ($EV_{DD}$ tolerance) can be selected by setting the corresponding bit of the port output mode registers (POM1, POM12) to “1”.
2. The ports are input-only.

## 11.2 Comparison of Port functions between RL78/F14 and 78K0R/Fx3

Table 11-8 shows the comparison of the port functions between the RL78/F14 and the 78K0R/Fx3.

**Table 11-8 Comparison of Port functions between RL78/F14 and 78K0R/Fx3**

| | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Port I/O setting | Port mode registers: PMxx (Note 1)<br>0: Output mode<br>1: Input mode | |
| Port output latch | Port registers: Pxx<br>0: Output “L”<br>1: Output “H” | |
| Pull-up control | Pull-up resistor option registers: PUxx (Note 1)<br>The function can be selected individually for each pin.<br>The setting is valid only when the input port mode is selected. | |
| Specifying threshold level for input ports | Port input mode registers: PIMxx (Note 1)<br>Port input threshold control register: PITHLxx (Note 1)<br>Selectable for each pin<br>·PIMxx = 0, PITHLxx = 0<br>→ Schmitt1 input buffer $V_{IL}$ = 0.35$EV_{DD}$<br>·PIMxx = 0, PITHLxx = 1<br>→ Schmitt3 input buffer $V_{IL}$ = 0.5$EV_{DD}$<br>·PIMxx = 1, PITHLxx = 0<br>→ TTL input buffer $V_{IL}$ = 0.8V | Port input mode registers: PIMxx<br>The function can be selected individually for each pin.<br>·PIMxx = 0<br>→ Normal input buffer $V_{IL}$ = 0.35$EV_{DD}$<br>·PIMxx = 1<br>→ TTL input buffer $V_{IL}$ = 0.8V |
| Port read selection | Port mode select register: PMS (Note 2)<br>0: The value of Pmn is read when the port is set to output mode.<br>1: The pin output level is read when the port is set to output mode. | - |
| Port assignment | Peripheral I/O redirection registers: PIOR0 to PIOR8 (Note 1) | - |

Notes 1. In the RL78/F14, it is possible to enable/disable the register write protection with the SFR guard function.
2. The setting applies to all the ports.

**<Key Points on Porting>**

**·Setting for Port functions**

The following registers are used to switch the pins to a port function pin or an analog input pin in the RL78/F14. To use a pin as a port function pin, set the corresponding register to the port function pin (digital input/output).

- Port mode control registers: PMC7, PMC9, PMC12
- A/D port configuration register: ADPC

## 11.3 Connection of unused pins

Table 11-9 shows the comparison of the connections of unused pins between the RL78/F14 and the 78K0R/Fx3, providing an example of each product with 100 pins, i.e. the RL78/F14 (100 pins) and the 78K0R/FG3.

**Table 11-9 Comparison of connections of unused pins between RL78/F14 (100 pins) and 78K0R/FG3**

| Port type | RL78/F14 (100 pins) | | | 78K0R/FG3 (100 pins) | | |
|---|---|---|---|---|---|---|
| | Corresponding pins | Connection of unused pins | | Corresponding pins | Connection of unused pins | |
| I/O ports | P33, P34<br>P80 to P87<br>P90 to P97<br>P100 to P105<br>P121 to P124 | input | Connect to $V_{DD}$ or $V_{SS}$ via resistor, independently. | P00 to P03<br>P10 to P17<br>P30 to P32<br>P40 to P47<br>P50 to P57<br>P60 to P67<br>P70 to P77<br>P80 to P87<br>P90 to P97<br>P100 to P107<br>P120 to P127<br>P130<br>P140<br>P150 to P157 | input | Connect to $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ via resistor, independently (Note 2). |
| | | output | Leave open | | | |
| | P00 to P03<br>P10 to P17<br>P30 to P32<br>P40 to P47<br>P50 to P57<br>P60 to P67<br>P70 to P77<br>P106 to P107<br>P120, P125 to P127<br>P140<br>P150 to P157 | input | Connect to $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ via resistor, independently (Note 2). | | output | Leave open |
| | | output | Leave open | | | |
| Input-only ports | P121 to P124<br>P137 | Connect to $V_{DD}$ or $V_{SS}$ via resistor, Independently. | | P121 to P124 | Connect to $V_{DD}$ or $V_{SS}$ via resistor, Independently. | |
| Output-only ports | P130 (Note 1) | Leave open | | P130 (Note 1) | Leave open | |

Notes 1. Do not apply reversal supply voltage to the pin because the pin cannot be set to the input mode by a program.

2. Power supply pins differ, depending on the products. See **Table 11-10** and **Table 11-11** for the power supplies and the corresponding pins for each product.

**Table 11-10 RL78/F14 Pin I/O buffer power supplies**

| Product | Power supply | Corresponding pins |
|---|---|---|
| R5F10PPx (x = E, F, G, H, J) | $EV_{DD0}$, $EV_{DD1}$ | P00-P03, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P106, P107, P120, P125-P127, P130, P140, P150-P157 |
| | $V_{DD}$ | P33, P34, P80-P87, P90-P97, P100-P105, P121-P124, P137 |
| R5F10PMx (x = E, F) | $EV_{DD0}$ | P00-P02, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P96, P97, P120, P125, P126, P130, P140 |
| | $V_{DD}$ | P33, P34, P80-P87, P90-P95, P121-P124, P137 |
| R5F10PMx (x = G, H, J) | $EV_{DD0}$ | P00-P02, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P120, P125, P126, P130, P140 |
| | $V_{DD}$ | P33, P34, P80-P87, P90-P97, P121-P124, P137 |
| R5F10PLx (x = E, F) | $EV_{DD0}$ | P00, P10-P17, P30-P32, P40-P43, P50-P53, P60-P63, P70-P77, P96, P120, P125, P130, P140 |
| | $V_{DD}$ | P33, P34, P80-P87, P90-P95, P121-P124, P137 |
| R5F10PLx (x = G, H, J) | $EV_{DD0}$ | P00, P10-P17, P30-P32, P40-P43, P50-P53, P60-P63, P70-P77, P120, P125, P130, P140 |
| | $V_{DD}$ | P33, P34, P80-P87, P90-P96, P121-P124, P137 |
| R5F10PGx (x = D, E, F, G, H, J) | $V_{DD}$ | P00, P10-P17, P30-P34, P40, P41, P60-P63, P70-P73, P80-P87, P90-P92, P120-P125, P130, P137, P140 |
| R5F10PBx (x = D, E) | $V_{DD}$ | P10-P17, P30, P33, P34, P40, P41, P60-P63, P80-P85, P120-P122, P125, P137 |
| R5F10PAx (x = D, E) | $V_{DD}$ | P10-P17, P30, P33, P34, P40, P41, P80-P87, P120-P122, P125, P137 |

**Table 11-11 78K0R/Fx3 Pin I/O buffer power supplies**

| Product | Power supply | Corresponding pins |
|---|---|---|
| 78K0R/FG3 | $AV_{REF}$ | P80-P87, P90-P97, P100-P107 |
| | $EV_{DD0}$, $EV_{DD1}$ | P00-P03, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P120, P125-P127, P130, P140, P150-P157 |
| | $V_{DD}$ | P121-P124 |
| 78K0R/FF3 | $AV_{REF}$ | P80-P87, P90-P97 |
| | $EV_{DD}$ | P00-P02, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P120, P125, P126, P130, P140 |
| | $V_{DD}$ | P121-P124 |
| 78K0R/FE3 | $AV_{REF}$ | P80-P87, P90-P96 |
| | $EV_{DD}$ | P00, P10-P17, P30-P32, P40-P43, P50-P53, P60-P63, P70-P77, P120, P125, P130, P140 |
| | $V_{DD}$ | P121-P124 |
| 78K0R/FC3 (48 pins) | $AV_{REF}$ | P80-P87, P90-P92 |
| | $EV_{DD}$ | P00, P10-P17, P30-P32, P40, P41, P60-P63, P70-P73, P120, P125, P130, P140 |
| | $V_{DD}$ | P121-P124 |
| 78K0R/FC3 (40 pins) | $AV_{REF}$ | P80-P87 |
| | $EV_{DD}$ | P10-P17, P30-P32, P40, P41, P60-P63, P70-P73, P120, P125 |
| | $V_{DD}$ | P121, P122 |
| 78K0R/FB3 (32 pins) | $AV_{REF}$ | P80-P85 |
| | $EV_{DD}$ | P10-P17, P30, P40, P41, P60-P63, P120, P125 |
| | $V_{DD}$ | P121, P122 |
| 78K0R/FB3 (30 pins) | $AV_{REF}$ | P80-P87 |
| | $EV_{DD}$ | P10-P17, P30, P40, P41, P120, P125 |
| | $V_{DD}$ | P121, P122 |

# 12. Interrupts

Table 12-1 shows the comparison of the interrupt sources between the RL78/F14 and the 78K0R/Fx3.

**Table 12-1 Comparison of interrupt sources between RL78/F14 and 78K0R/Fx3 (1/2)**

| Vector table address | RL78/F14 | | | | | | | 78K0R/Fx3 | | | | | | | Key points on porting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | FB3 | | FC3 | | FE3 | FF3 | FG3 | |
| | Interrpt source | 30 pins | 32 pins | 48 pins | 64 pins | 80 pins | 100 pins | Interrpt source | 30 pins | 32 pins | 40 pins | 48 pins | 64 pins | 80 pins | 100 pins | |
| 00000H | RESET | ○ | ○ | ○ | ○ | ○ | ○ | RESET | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | POR | ○ | ○ | ○ | ○ | ○ | ○ | POC | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | LVD | ○ | ○ | ○ | ○ | ○ | ○ | LVI | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | WDT | ○ | ○ | ○ | ○ | ○ | ○ | WDT | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | TRAP | ○ | ○ | ○ | ○ | ○ | ○ | TRAP | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | IAW | ○ | ○ | ○ | ○ | ○ | ○ | IAW | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | CLM | ○ | ○ | ○ | ○ | ○ | ○ | CLKM | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00002H | reserved | | | | | | | reserved | | | | | | | | |
| 00004H | INTWDTI | ○ | ○ | ○ | ○ | ○ | ○ | INTWDTI | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00006H | INTLVI | ○ | ○ | ○ | ○ | ○ | ○ | INTLVI | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00008H | INTP0 | ○ | ○ | ○ | ○ | ○ | ○ | INTP0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 0000AH | INTP1 | ○ | ○ | ○ | ○ | ○ | ○ | INTP1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 0000CH | INTP2 | ○ | ○ | ○ | ○ | ○ | ○ | INTP2 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 0000EH | INTP3 | ○ | ○ | ○ | ○ | ○ | ○ | INTP3 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00010H | INTP4 | ○ | ○ | ○ | ○ | ○ | ○ | INTP4 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | INTSPM | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 00012H | INTP5 | ○ | ○ | ○ | ○ | ○ | ○ | INTP5 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | INTCMP0 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 00014H | INTP13 | - | - | - | - | ○Note 3 | ○ | | | | | | | | | |
| | INTCLM | ○ | ○ | ○ | ○ | ○ | ○ | INTCLM | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00016H | INTST0 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| | INTCSI00 | ○ | ○ | ○ | ○ | ○ | ○ | INTCSI00 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | INTIIC00 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 00018H | INTSR0 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| | INTCSI01 | ○ | ○ | ○ | ○ | ○ | ○ | INTCSI01 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | INTIIC01 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 0001AH | INTTRD0 | ○ | ○ | ○ | ○ | ○ | ○ | INTDMA0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use the corresponding interrupt of DTC |
| 0001CH | INTTRD1 | ○ | ○ | ○ | ○ | ○ | ○ | INTDMA1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use the corresponding interrupt of DTC |
| 0001EH | INTTRJ0 | ○ | ○ | ○ | ○ | ○ | ○ | INTWUTM | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use Timer RJ, TAU or Timer RD |
| 00020H | INTRAM | ○ | ○ | ○ | ○ | ○ | ○ | INTFL | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Allocated to 00062H |
| 00022H | INTLIN0TRM | ○ | ○ | ○ | ○ | ○ | ○ | INTLT0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00024H | INTLIN0RVC | ○ | ○ | ○ | ○ | ○ | ○ | INTLR0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00026H | INTLIN0STA | ○ | ○ | ○ | ○ | ○ | ○ | INTLS0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | INTLIN0 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 00028H | INTIICA0 | - | ○ | ○ | ○ | ○ | ○ | INTPLR0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use 0004AH (INTLIN0WUP) |
| 0002AH | INTP8 | - | - | ○ | ○ | ○ | ○ | INTP8 | - | - | - | - | - | ○ | ○ | |
| | INTRTC | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 0002CH | INTTM00 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM00 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 0002EH | INTTM01 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM01 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00030H | INTTM02 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM02 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00032H | INTTM03 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM03 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00034H | INTAD | ○ | ○ | ○ | ○ | ○ | ○ | INTAD | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00036H | INTP6 | - | - | ○ | ○ | ○ | ○ | INTLT1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use 00066H (INTLIN1TRM) |
| | INTTM11H | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 00038H | INTP7 | - | - | ○ | ○ | ○ | ○ | INTLR1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use 00068H (INTLIN1RVC) |
| | INTTM13H | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 0003AH | INTP9 | - | - | ○ | ○ | ○ | ○ | INTLS1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use 0006AH (INTLIN1STA) |
| | INTTM01H | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 0003CH | INTP10 | - | - | - | ○ | ○ | ○ | INTPLR1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Use 00064H (INTLIN1WUP) |
| | INTTM03H | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| 0003EH | INTST1 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| | INTCSI10 | - | - | ○ | ○ | ○ | ○ | INTCSI10 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| | INTIIC10 | - | - | ○ | ○ | ○ | ○ | | | | | | | | | |
| 00040H | INTSR1 | ○ | ○ | ○ | ○ | ○ | ○ | | | | | | | | | |
| | INTCSI11 | - | - | ○ | ○ | ○ | ○ | INTCSI11 | - | - | - | - | - | - | ○ | |
| | INTIIC11 | - | - | ○ | ○ | ○ | ○ | INTIIC11 | - | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00042H | INTTM04 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM04 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00044H | INTTM05 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM05 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00046H | INTTM06 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM06 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 00048H | INTTM07 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM07 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |
| 0004AH | INTP11 | - | - | - | ○ | ○ | ○ | INTP6 | - | - | ○ | ○ | ○ | ○ | ○ | Allocated to 00036H |
| | INTLIN0WUP | ○ | ○ | ○ | ○ | ○ | ○ | INTKR | - | - | ○ | ○ | ○ | ○ | ○ | Allocated to 0004CH |
| 0004CH | INTKR | ○ | ○ | ○ | ○ | ○ | ○ | INTP7 | - | - | - | ○ | ○ | ○ | ○ | Allocated to 00038H |
| 0004EH | INTCAN0ERR | ○ | ○ | ○ | ○ | ○ | ○ | INTC0ERR | - | - | ○Note 1 | ○Note 1 | ○Note 1 | ○Note 1 | ○ | |
| 00050H | INTCAN0WUP | ○ | ○ | ○ | ○ | ○ | ○ | INTC0WUP | - | - | ○Note 1 | ○Note 1 | ○Note 1 | ○Note 1 | ○ | |
| 00052H | INTCAN0CFR | ○ | ○ | ○ | ○ | ○ | ○ | INTC0REC | - | - | ○Note 1 | ○Note 1 | ○Note 1 | ○Note 1 | ○ | |
| 00054H | INTCAN0TRM | ○ | ○ | ○ | ○ | ○ | ○ | INTC0TRX | - | - | ○Note 1 | ○Note 1 | ○Note 1 | ○Note 1 | ○ | |
| 00056H | INTCANGRFR | ○ | ○ | ○ | ○ | ○ | ○ | INTTM10 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Allocated to 0005AH |
| 00058H | INTCANGERR | ○ | ○ | ○ | ○ | ○ | ○ | INTTM11 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Allocated to 0005CH |
| 0005AH | INTTM10 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM12 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Allocated to 0005EH |
| 0005CH | INTTM11 | ○ | ○ | ○ | ○ | ○ | ○ | INTTM13 | - | - | ○ | ○ | ○ | ○ | ○ | Allocated to 00060H |
| 0005EH | INTTM12 | ○ | ○ | ○ | ○ | ○ | ○ | INTMD | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Corresponding interrupt does not exist (division instruction) |

**Table 12-1 Comparison of interrupt sources between RL78/F14 and 78K0R/Fx3 (2/2)**

| Vector table address | RL78/F14 Interrpt source | 30 pins | 32 pins | 48 pins | 64 pins | 80 pins | 100 pins | 78K0R/Fx3 Interrpt source | FB3 30 pins | FB3 32 pins | FC3 40 pins | FC3 48 pins | FE3 64 pins | FF3 80 pins | FG3 100 pins | Key points on porting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00060H | INTTM13 | ○ | ○ | ○ | ○ | ○ | ○ | INTST2 | - | - | - | - | ○Note 2 | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another UART) |
| | | | | | | | | INTIIC20 | - | - | - | - | ○Note 2 | ○ | ○ | Corresponding interrupt does not exist(Use the corresponding function of another I2C) |
| 00062H | INTFLNote 6 | ○ | ○ | ○ | ○ | ○ | ○ | INTSR2 | - | - | - | - | ○Note 2 | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another UART) |
| 00064H | INTP12 | - | - | - | ○Note 4 | ○Note 3 | ○ | INTPR2 | - | - | - | - | ○Note 2 | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another INTP) |
| | INTLIN1WUP | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | | | | | | | | | |
| 00066H | INTLIN1TRM | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM14 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Allocated to 0006CH |
| 00068H | INTLIN1RVC | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM15 | - | - | ○ | ○ | ○ | ○ | ○ | Allocated to 0006EH |
| 0006AH | INTLIN1STA | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM16 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | Allocated to 00070H |
| | INTLIN1 | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | | | | | | | | | |
| 0006CH | INTTM14 | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM17 | - | - | ○ | ○ | ○ | ○ | ○ | Allocated to 00072H |
| 0006EH | INTTM15 | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM20 | - | - | - | - | ○ | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another timer) |
| 00070H | INTTM16 | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM21 | - | - | - | - | ○ | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another timer) |
| 00072H | INTTM17 | - | - | ○Note 5 | ○Note 4 | ○Note 3 | ○ | INTTM22 | - | - | - | - | ○ | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another timer) |
| 00074H | reserved | | | | | | | INTTM23 | - | - | - | - | ○ | ○ | ○ | Corresponding interrupt does not exist (Use the corresponding function of another timer) |
| 00076H | reserved | | | | | | | INTTM25 | - | - | - | - | - | - | ○ | Corresponding interrupt does not exist (Use the corresponding function of another timer) |
| 00078H | reserved | | | | | | | INTTM27 | - | - | - | - | - | - | ○ | Corresponding interrupt does not exist (Use the corresponding function of another timer) |
| 0007AH | reserved | | | | | | | INTDMA2 | - | - | - | ○ | ○ | ○ | ○ | Use the corresponding DTC interrupt |
| 0007CH | reserved | | | | | | | INTDMA3 | - | - | - | ○ | ○ | ○ | ○ | Use the corresponding DTC interrupt |
| 0007EH | BRK | ○ | ○ | ○ | ○ | ○ | ○ | BRK | ○ | ○ | ○ | ○ | ○ | ○ | ○ | |

Notes 1. Only provided for the CAN incorporated products (FF3: µPD78F1836 to 78F1840, FE3: µPD78F1831 to 78F1835, FC3: µPD78F1826 to 78F1830).
2. Only provided for the µPD78F1821, µPD78F1822, µPD78F1831 to 78F1835 of the 78K0R/FE3 (64 pins).
3. Only provided for the products with 128 Kbytes to 256 Kbytes of code flash memory (R5F10PMG, R5F10PMH, R5F10PMJ).
4. Only provided for the products with 128 Kbytes to 256 Kbytes of code flash memory (R5F10PLG, R5F10PLH, R5F10PLJ).
5. Only provided for the products with 128 Kbytes to 256 Kbytes of code flash memory (R5F10PGG, R5F10PGH, R5F10PGJ).
6. Do not use this interrupt because it is a reserved function.

**<Key Points on Porting>**

**·Vector table (1)**

Whether in the RL78/F14 or the 78K0R/Fx3, some of the interrupt sources are allocated to the same vector table address. When the interrupt sources shown below occur at the same time, determine which of the interrupt sources causes the interrupt by using such as the INTFLG0 register.

[Target interrupt sources for RL78/F14]

INTP4/INTSPM (0010H), INTP5/INTCMP0 (0012H), INTP13/INTCLM (0014H), INTP8/INTRTC (002AH), INTP11/INTLIN0WUP (004AH), INTP12/INTLIN1WUP(0064H)

**·Vector table (2)**

Whether in the RL78/F14 or the 78K0R/Fx3, some of the interrupt sources are allocated to the same vector table address. When the interrupt sources shown below occur at the same time, it is not possible to determine which of interrupt sources causes the interrupt. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

[Target interrupt sources for RL78/F14]

INTP6/INTTM11H (0036H), INTP7/INTTM13H (0038H), INTP9/INTTM01H (003AH),

INTP10/INTTM03H (003CH)

# 13. Watchdog timer

Table 13-1 shows the comparison of the functions of the watchdog timer (WDT) between the RL78/F14 and the 78K0R/Fx3.

**Table 13-1 Comparison of functions of WDT between RL78/F14 and 78K0R/Fx3**

| Comparison targets | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Operation clock | WDT-dedicated low-speed on-chip oscillator clock ($f_{WDT}$) | Internal low-speed oscillation clock. |
| Start timing of counter | After a reset release (When WDTON bit of the option byte is set to “1”) | |
| Count operations | Increment | |
| How to refresh WDT | Writing “ACH” to the WDTE register | |
| Count period | Setting value of the bits WDCS2 to WDCS0 of the option byte determines<br>[When $f_{WDT}$ = 17.25 kHz (MAX.)]<br>3.71 ms<br>7.42 ms<br>14.84 ms<br>29.68 ms<br>118.72 ms<br>474.89 ms<br>949.79 ms<br>3799.18 ms | Setting value of the bits WDCS2 to WDCS0 of the option byte determines<br>[When $f_{IL}$ = 33 kHz (MAX.)]<br>3.88 ms<br>7.76 ms<br>15.52 ms<br>31.03 ms<br>124.12 ms<br>496.48 ms<br>992.97 ms<br>3971.88 ms |
| Operation when condition, under which reset occurs due to WDT, is met | An internal reset signal is generated | |
| Conditions under which reset occurs due to WDT | ·If the watchdog timer counter overflows.<br>·If data is written to the WDTE register during a window close period.<br>·If a 1-bit manipulation instruction is executed on the WDTE register<br>·If data other than “ACH” is written to the WDTE register | |
| How to determine whether reset occurs due to WDT or not | Determined by checking the WDCLRF bit of the RESF register; this bit is set to “1” when an internal reset request occurs due to WDT. | Determined by checking the WDRF bit of the RESF register; this bit is set to “1” when an internal reset request occurs due to WDT. |
| Window open period | The value of the WINDOW1 and WINDOW0 bits determines the window open period<br>50%<br>75%<br>100% | The value of the WINDOW1 and WINDOW0 bits determines the window open period<br>25%<br>50%<br>75%<br>100% |
| Operation in HALT mode | Whether the WDT operation stops or continues in the HALT/STOP mode can be determined by setting the WDSTBYON bit of the option byte after setting the WDTON bit of the option byte to “1”. | The value of the LIOUSE bit of the option byte determines whether the internal low-speed oscillation operation is enabled or stopped in HALT mode.<br>Whether the WDT operation stops or continues when HALT mode is set while the internal low-speed oscillation is operating can be determined by setting the WDSTBYON bit of the option byte after setting the WDTON bit of the option byte to “1”. |
| Operation in STOP mode | | The value of the LIOSTOPB bit of the option byte determines whether the internal low-speed oscillation operation is enabled or stopped in STOP mode.<br>Whether the WDT operation stops or continues when STOP mode is set while the internal low-speed oscillation is operating can be determined by setting the WDSTBYON bit of the option byte after setting the WDTON bit of the option byte to “1”. |

**<Key Points on Porting>**

**·WDT operations in HALT/STOP mode**

In the 78K0R/Fx3, the LIOUSE bit and the LIOSTOPB bit are used to enable or stop the internal low-speed oscillator in HALT mode and STOP mode, respectively. On the other hand, in the RL78/F14, the WDTON bit is used to enable or stop the WDT-dedicated low-speed on-chip oscillator clock in HALT/STOP mode. For this reason, in the RL78/F14, once the WDT counter operation is enabled by the WDTON bit of the option byte, the WDT operation is stopped or started by using the WDSTBYON bit of the option byte.

**·WDT interval interrupt operation**

The timing of the WDT interval interrupt differs between the RL78/F14 and the 78K0R/Fx3 as shown below. Confirm that the difference would not lead to problems.

- RL78/F14: When 75% of overflow time + 1/2 $f_{WDT}$ is reached.
- 78K0R/Fx3: When 75% of overflow time is reached.

**·Window open period**

The setting of 25% can be selected as the window open period in the 78K0R/Fx3. On the other hand, the setting of 25% does not exist in the RL78/F14. When the window open period is 25% in the 78K0R/Fx3 and it is other than 100% in the RL78/F14, confirm that the difference would not lead to problems.

# 14. DTC

Table 14-1 shows the comparison between the DTC functions in the RL78/F14 and the DMA functions in the 78K0R/Fx3. Figure 14-1 shows the comparison between the DTC data transfer sequence and the DMA data transfer sequence. Figure 14-2 shows the comparison of the functions between the DTC activation sources and the DMA start sources.

**Table 14-1 Comparison between DTC functions in RL78/F14 and DMA functions in 78K0R/Fx3**

<table>
<tr><th>Comparison targets</th><th colspan="4">RL78/F14 DTC</th><th colspan="3">78K0R/Fx3 DMA</th></tr>
<tr><td>Transfer direction</td><td colspan="4">·SFR → SFR<br>·SFR → RAM<br>·RAM → SFR<br>·RAM → RAM<br>·Mirror area → SFR<br>·Mirror area → RAM<br>·Data flash memory → SFR<br>·Data flash memory → RAM</td><td colspan="3">·SFR → RAM<br>·RAM → SFR</td></tr>
<tr><td>Unit of transfers</td><td colspan="4">·8 bits<br>·16 bits</td><td colspan="3">·8 bits<br>·16 bits</td></tr>
<tr><td>Transfer mode</td><td colspan="4">·Normal mode<br>·Repeat mode<br>·High-speed transfer</td><td colspan="3">·Single-transfer mode</td></tr>
<tr><td rowspan="3">Maximum size of block to be transferred</td><td colspan="2">Normal mode (8-bit transfer)</td><td colspan="2">256 bytes/1 byte (high-speed transfer)</td><td colspan="3" rowspan="3">·Single-transfer mode: 2048 bytes</td></tr>
<tr><td colspan="2">Normal mode (16-bit transfer)</td><td colspan="2">512 bytes/2 bytes (high-speed transfer)</td></tr>
<tr><td colspan="2">Repeat mode</td><td colspan="2">255 bytes/<br>1 byte at 8-bit transfer (high-speed transfer)/<br>2 bytes at 16-bit transfer (high-speed transfer)</td></tr>
<tr><td rowspan="4">Activation sources</td><td colspan="2">30 pins<br>32 pins</td><td colspan="2">37 sources (Note 1)</td><td>30 pins<br>32 pins<br>40 pins</td><td>15 sources (Note 6)</td></tr>
<tr><td rowspan="3">48 pins<br>64 pins<br>80 pins</td><td>Products with up to 96 Kbytes of code flash memory</td><td>38 sources (Note 1)</td><td rowspan="3">48 pins<br>64 pins<br>80 pins</td><td rowspan="3">32 sources (Note 2)</td></tr>
<tr><td>Products with at least 128 Kbytes of code flash memory</td><td>44 sources (Note 1)</td></tr>
<tr><td colspan="2">100 pins</td><td>44 sources (Note 1)</td><td>100 pins</td></tr>
<tr><td>Number of clocks for each transfer operation</td><td colspan="4">For each DTC transfer operation: 14 clocks (MAX.)<br>Number of clocks (Details) (Note 3)<br>·Vector read =1 clock<br>·Control data read = 4 clocks<br>·Control data write-back = 3 clocks<br>·Data read = 4 clocks<br>·Data write = 2 clocks<br><br>For each high-speed DTC transfer operation: 5 clocks (MAX.)<br>Number of clocks (Details)<br>·Vector read and control data read = 1 clock<br>·Control data write-back = 1 clock<br>·Data read = 1 clock<br>·Data write = 2 clocks</td><td colspan="3">For each transfer: 2 clocks (MAX.)</td></tr>
<tr><td>Control data DTC vector address area</td><td colspan="4">The 256-bytes area is allocated in the order of the DTC vector table area (46 bytes), the reserved area (18 bytes), and the DTC control data area (192 bytes). The start address of this area is specified by the DTCBAR register (Fxx00H: xx is specified by the DTCBAR register).</td><td colspan="3">Via DMA, data can be transferred from/to the internal RAM area (excluding the general-purpose registers); the lower limit and the upper limit of the area are shown below.<br><table><tr><th colspan="2">Size</th><th rowspan="2">yy (Note 4)</th><th colspan="2">RAM address</th></tr><tr><th>Code Flash Memory</th><th>RAM</th><th>Lower limit</th><th>Upper limit</th></tr><tr><td>24 Kbytes</td><td>1.5 Kbytes</td><td>04, 08, 12</td><td>FF900H</td><td>FFEFFH</td></tr><tr><td>32 Kbytes</td><td>2 Kbytes</td><td>05, 09, 13, 18</td><td>FF700H</td><td>FFEFFH</td></tr><tr><td>48 Kbytes</td><td>3 Kbytes</td><td>06, 10, 14, 19</td><td>FF300H</td><td>FFEFFH</td></tr><tr><td>64 Kbytes</td><td>4 Kbytes</td><td>07, 11, 15, 20, 23, 26, 31, 36, 41</td><td>FEF00H</td><td>FFEFFH</td></tr><tr><td>96 Kbytes</td><td>6 Kbytes</td><td>16, 21, 24, 27, 32, 37, 42</td><td>FE700H</td><td>FFEFFH</td></tr><tr><td>128 Kbytes</td><td>8 Kbytes</td><td>17, 22, 25, 28, 33, 38, 43</td><td>FDF00H</td><td>FFEFFH</td></tr><tr><td>192 Kbytes</td><td>12 Kbytes</td><td>29, 34, 39, 44</td><td>FCF00H</td><td>FFEFFH</td></tr><tr><td>256 Kbytes</td><td>16 Kbytes</td><td>30, 35, 40, 45</td><td>FBF00H</td><td>FFEFFH</td></tr></table></td></tr>
<tr><td>Transfer pending</td><td colspan="4">Supported</td><td colspan="3">Supported</td></tr>
<tr><td>High-speed transfer</td><td colspan="4">Supported (2 types)</td><td colspan="3">-</td></tr>
<tr><td>Operation in HALT mode</td><td colspan="4">Operable</td><td colspan="3">Operable</td></tr>
<tr><td>Operation in STOP mode</td><td colspan="4">DTC activation sources can be accepted<br>(Transition to SNOOZE mode enables DTC transfer)</td><td colspan="3">Operation is stopped (Note 5)</td></tr>
</table>

Notes 1. For each activation source, one set of control data is selectable from among 24 sets of the control data.

2. For two channels of DMA0 and DMA1, 15 sources are selectable. On the other hand, for two channels of DMA2 and DMA3, 17 sources are selectable (Among the trigger numbers to which the start sources are assigned, there are two trigger numbers, each of which is shared by two start sources). For details, see the user's manual.

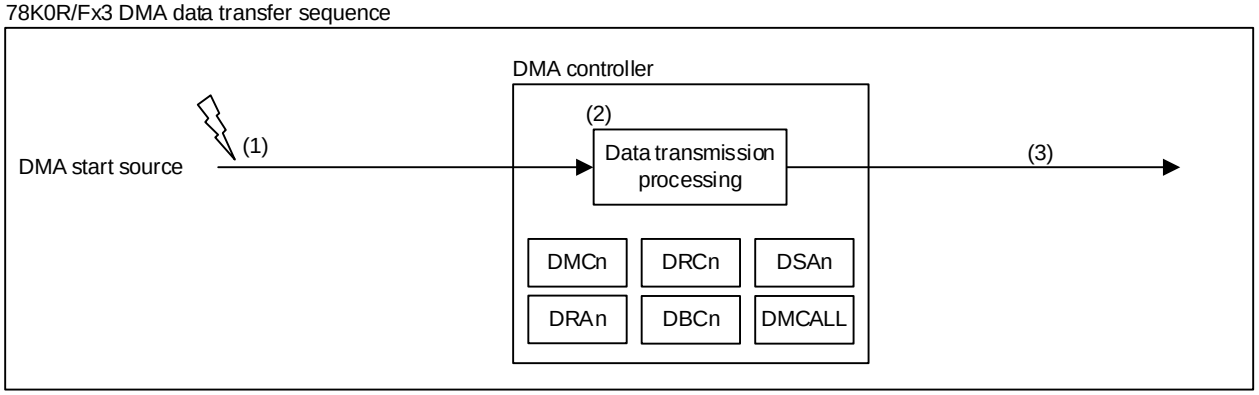
3. When all the following conditions are met, the number of the clocks for the transfer operation reaches the maximum.
   - The data is transferred from the data flash memory to the SFR, or from the data flash memory to the RAM.
   - The DTCCTj registers, the DTRLDj registers, the DTSARj registers, and the DTDARj registers are written back.
   - The setting of the DTCCR register is any of the following (1) to (3).
     (1) Normal mode (MODE = 0), the destination address is incremented (DAMOD = 1), and the source address is incremented (SAMOD = 1).
     (2) Repeat mode (MODE = 1), the transfer source is specified as the repeat area (RPTSEL = 1), and the destination address is incremented (DAMOD = 1).
     (3) Repeat mode (MODE = 1), the transfer destination is specified as the repeat area (RPTSEL=0), and the source address is incremented (SAMOD=1).

4. "yy" indicates the lower 2 bits of a part number of the product of "µPD78F18yy".

5. If a DMA transfer and a STOP instruction execution contend, the DMA transfer might be corrupted. Therefore stop the DMA before executing the stop instruction.

6. For two channels of DMA0 and DMA1, 15 sources are selectable.

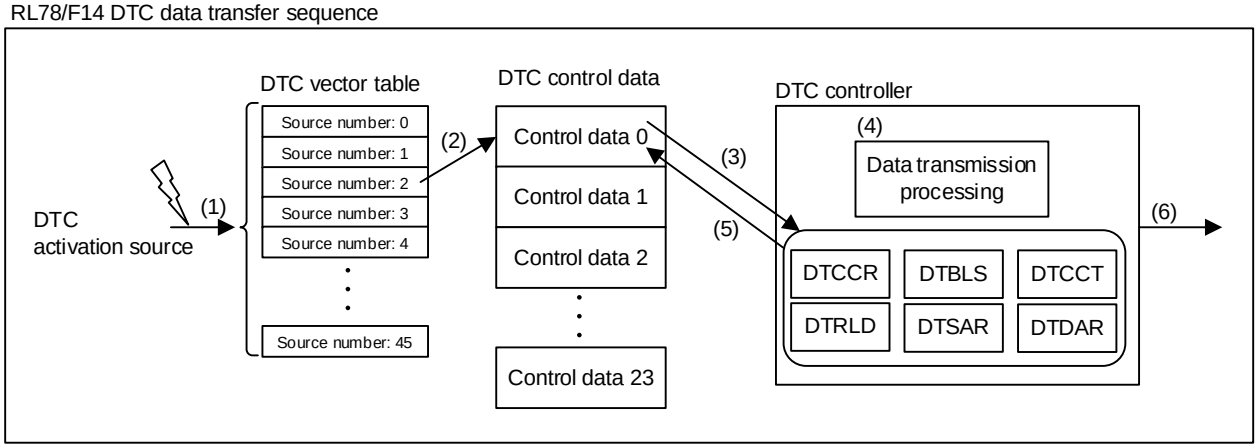
78K0R/Fx3 DMA data transfer sequence




<DMA operation>

(1) An interrupt request which is a DMA start source is generated.
(2) Data transfer is started based on the setting of the DMA-related registers.
(3) Data transfer has been completed.

RL78/F14 DTC data transfer sequence




<DTC operation>

(1) Generation of an interrupt request which is a DTC activation source triggers reading the DTC vector corresponding to the source number and obtaining the control data number.
(2) The control data, corresponding to the control data number and obtained during the procedure of (1) , is read. And then the values to be written to the DTC-related registers are read.
(3) The values read during the procedure of (2) are written to the DTC-related registers.
(4) Data transfer is started based on the setting values written to the DTC-related registers.
(5) After data transfer, the values of the DTC-related registers are written back to the control data area.
(6) Data transfer has been completed.

**Figure 14-1 Comparison between DTC data transfer sequence in RL78/F14 and DMA data transfer sequence in 78K0R/Fx3**

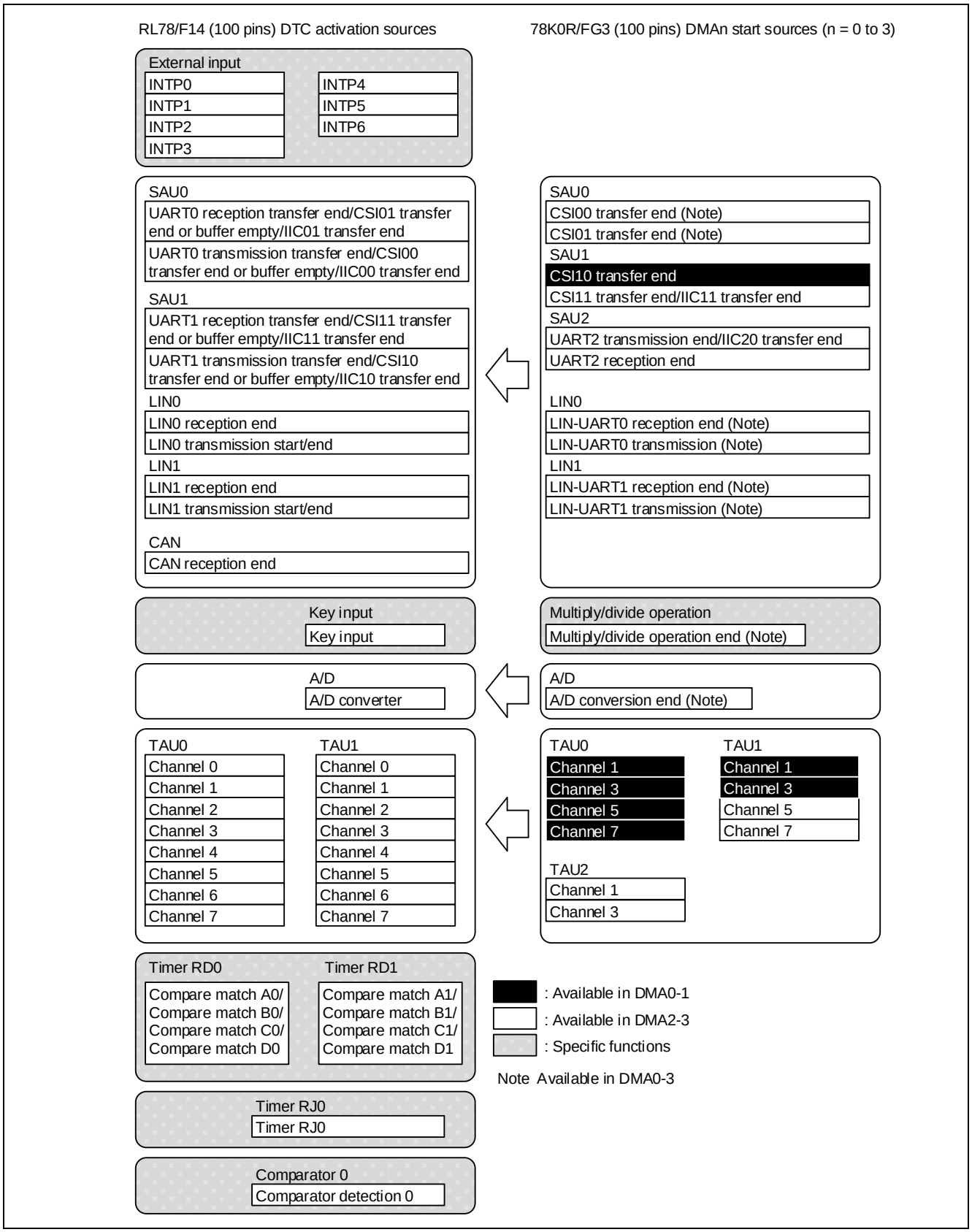



**Figure 14-2 Comparison of functions between DTC activation sources in RL78/F14 (100 pins) and DMA start sources in 78K0R/FG3**

**<Key Points on Porting>**

·**Setting to disable/enable operation**

The RL78/F14 can activate/deactivate the DTC by controlling the clock supply to the DTC, in the same way as done with the DENn flags of the DRCn registers in the 78K0R/Fx3. The DTCEN bit of the peripheral enable register 1 (PER1) is used for the setting. When using the DTC, be sure to set the DTCEN bit to "1" (the input clock supply is enabled) before accessing the DTC-related registers.

·**High-speed transfer**

In the RL78/F14, the normal DTC transfer requires up to 14 clocks at a maximum. For this reason, consider the use of high-speed DTC transfer in the RL78/F14, if the number of clocks for the transfer operation needs to be close to that of the 78K0R/Fx3. However, the source address for high-speed DTC transfer is limited to the SFR area (including the 2nd SFR area). Also, the required number of clocks for high-speed DTC transfer is up to 5 clocks at a maximum. Confirm these differences from the DMA in the 78K0R/Fx3 would not lead to problems. For details on how to use these features, refer to the user's manuals.

·**Setting for DTC source address register and DTC destination address register**

In the same way as done with the DRA3-0 registers in the 78K0R/Fx3, the lower 16 bits of the transfer source address and the transfer destination address are set to the DTC source address register (DTSARi) and the DTC destination address register (DTDARj), respectively. The sum of the value set to the DTSARi/DTDARj registers and F0000H is used as the transfer source/destination address.

## 15. Timer

The possible examples of porting from the timers in the 78K0R/Fx3 to those in the RL78/F14 are shown below:

·From the timer array unit (referred as TAU from here) in the 78K0R/Fx3 to that in the RL78/F14

·From the 16-bit wakeup timer (referred as WUTM from here) in the 78K0R/Fx3 to the Timer RJ in the RL78/F14

·From the TAU in the 78K0R/Fx3 to the Timer RD in the RL78/F14

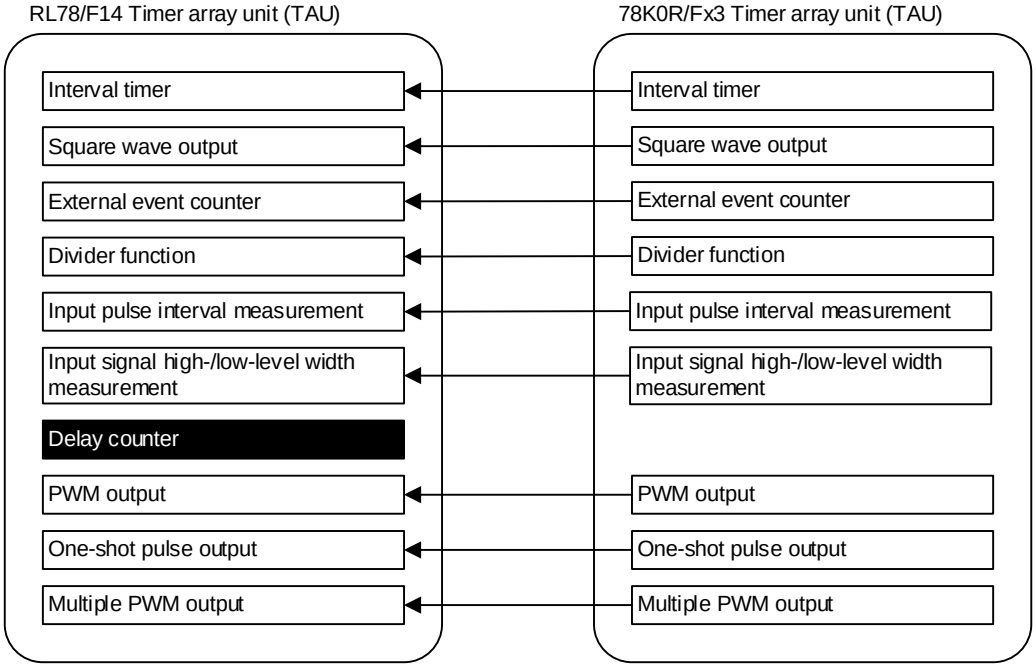
**<Key Points on Porting>**

·**Number of channels of TAU**

In the 78K0R/Fx3, TAU consists of any of "8 channels + 5 channels", "8 channels × 2 units", "8 channels × 2 units + 4 channels", or "8 channels × 3 units". On the other hand, in the RL78/F14 with up to 80 pins and up to 96 Kbytes of the code flash memory, the TAU consists of "8 channels + 4 channels". Due to this fact, depending on the choice of the RL78/F14 product, there may be a shortage of the number of the necessary channels when TAU is used. For the details of number of channels of the TAU, see the following pages.

## 15.1 Porting code for TAU in 78K0R/Fx3 over to that in RL78/F14

Figure 15-1 shows the relationship between each mode of the TAU in the RL78/F14 and that in the 78K0R/Fx3.




RL78/F14 TAU: 16-bit timers, 2 units
Unit 0: 8 channels
Unit 1: 4 channels or 8 channels
Two channels are necessary for the PWM output, the one-shot pulse output, and the multiple PWM output.

78K0R/Fx3 TAU: 16-bit timers, 2 units or 3 units
Unit 0: 8 channels
Unit 1: 5 channels or 8 channels
Unit 2: 4 channels or 8 channels
Two channels are necessary for the PWM output, the one-shot pulse output, and the multiple PWM output.

Note The outline characters on a black background indicate inapplicable functions for porting.

**Figure 15-1 Relationship between each mode of TAU in RL78/F14 and that in 78K0R/Fx3**

Table 15-1 and Table 15-2 show the number of channels of the TAU in each product of the RL78/F14 and the 78K0R/Fx3, respectively. Also, Table 15-3 and Table 15-4 show the available channels of the TAU in each product of the RL78/F14 and the 78K0R/Fx3, respectively. For the assignment of TAU I/O pins (TImn, TOmn), see **CHAPTER 3 PIN assignment**.

**Table 15-1 Number of channels of TAU in each product in RL78/F14**

| Unit | 30 pins | 32 pins | 48 pins | | 64 pins | | 80 pins | | 100 pins |
|---|---|---|---|---|---|---|---|---|---|
| | | | Code flash memory | | Code flash memory | | Code flash memory | | |
| | | | 48 Kbytes to 96 Kbytes | 128 Kbytes to 256 Kbytes | 64 Kbytes to 96 Kbytes | 128 Kbytes to 256 Kbytes | 64 Kbytes to 96 Kbytes | 128 Kbytes to 256 Kbytes | |
| TAU0 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| TAU1 | 4 | 4 | 4 | 8 | 4 | 8 | 4 | 8 | 8 |
| Total | 12 | 12 | 12 | 16 | 12 | 16 | 12 | 16 | 16 |

**Table 15-2 Number of channels of TAU in each product in 78K0R/Fx3**

| Unit | 78K0R/FB3 | | 78K0R/FC3 | | 78K0R/FE3 | 78K0R/FF3 | 78K0R/FG3 |
|---|---|---|---|---|---|---|---|
| | 30 pins | 32 pins | 40 pins | 48 pins | 64 pins | 80 pins | 100 pins |
| TAU0 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| TAU1 | 5 | 5 | 8 | 8 | 8 | 8 | 8 |
| TAU2 | - | - | - | - | 4 | 4 | 8 |
| Total | 13 | 13 | 16 | 16 | 20 | 20 | 24 |

- : Not provided

**Table 15-3 Available channels of TAU in each product of RL78/F14**

| Unit | Channel | 30 pins | 32 pins | 48 pins | | 64 pins | | 80 pins | | 100 pins |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Code flash memory | | Code flash memory | | Code flash memory | | |
| | | | | 48 Kbytes to 96 Kbytes | 128 Kbytes to 256 Kbytes | 64 Kbytes to 96 Kbytes | 128 Kbytes to 256 Kbytes | 64 Kbytes to 96 Kbytes | 128 Kbytes to 256 Kbytes | |
| TAU0 | 0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 2 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 3 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 4 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 5 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 6 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 7 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| TAU1 | 0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 2 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 3 | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 4 | - | - | - | ○ | - | ○ | - | ○ | ○ |
| | 5 | - | - | - | ○ | - | ○ | - | ○ | ○ |
| | 6 | - | - | - | ○ | - | ○ | - | ○ | ○ |
| | 7 | - | - | - | ○ | - | ○ | - | ○ | ○ |

○ : Available
- : Not available

**Table 15-4 Available channels of TAU in each product of 78K0R/Fx3**

| Unit | Channel | 78K0R/FB3 | | 78K0R/FC3 | | 78K0R/FF3 | 78K0R/FE3 | 78K0R/FG3 |
|---|---|---|---|---|---|---|---|---|
| | | 30 pins | 32 pins | 40 pins | 48 pins | 64 pins | 80 pins | 100 pins |
| TAU0 | 0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 2 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 3 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 4 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 5 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 6 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 7 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| TAU1 | 0 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 1 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 2 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 3 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 4 | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | 5 | - | - | ○ | ○ | ○ | ○ | ○ |
| | 6 | - | - | ○ | ○ | ○ | ○ | ○ |
| | 7 | - | - | ○ | ○ | ○ | ○ | ○ |
| TAU2 | 0 | - | - | - | - | ○ | ○ | ○ |
| | 1 | - | - | - | - | ○ | ○ | ○ |
| | 2 | - | - | - | - | ○ | ○ | ○ |
| | 3 | - | - | - | - | ○ | ○ | ○ |
| | 4 | - | - | - | - | - | - | ○ |
| | 5 | - | - | - | - | - | - | ○ |
| | 6 | - | - | - | - | - | - | ○ |
| | 7 | - | - | - | - | - | - | ○ |

○ : Available
- : Not available

The one-shot pulse output, the PWM output, and the multiple PWM output of the TAU in the RL78/F14 and the 78K0R/Fx3 are realized by using the combination of a master channel and a slave channel.

The possible combinations of a master channel and a slave channel are common between the RL78/F14 and the 78K0R/Fx3, depending on the number of the channels per unit of the TAU.

The number of the channels per unit of the TAU is any of 8 channels, 5 channels, or 4 channels. Each unit of TAU in the RL78/F14 and the 78K0R/Fx3 is categorized into one of the three as shown in Table 15-5.

The possible combinations of a master channel and a slave channel of the TAU are shown in Table 15-6, Table 15-7, and Table 15-8, broken down by the number of the channels per unit of the TAU; 8 channels, 5 channels, and 4 channels, respectively.

**Table 15-5 Categorization of TAU by number of channels per unit of TAU in RL78/F14 and 78K0R/Fx3**

| Number of channels per unit | Applicable units | |
|---|---|---|
| | RL78/F14 | 78K0R/Fx3 |
| 8 channels | TAU0<br>TAU1 of 48-pin products with at least 128 Kbytes of code flash memory<br>TAU1 of 64-pin products with at least 128 Kbytes of code flash memory<br>TAU1 of 80-pin products with at least 128 Kbytes of code flash memory<br>TAU 1 of 100-pin products | TAU0<br>TAU1 of 40-pin products (78K0R/FC3)<br>TAU1 of 48-pin products (78K0R/FC3)<br>TAU1 of 64-pin products (78K0R/FE3 )<br>TAU1 of 80-pin products (78K0R/FF3)<br>TAU1 and TAU2 of 100-pin products (78K0R/FG3) |
| 5 channels | - | TAU1 of 30-pin products (78K0R/FB3)<br>TAU1 of 32-pin products (78K0R/FB3) |
| 4 channels | TAU1 of 30-pin products<br>TAU1 of 32-pin products<br>TAU1 of 48-pin products with up to 96 Kbytes of code flash memory<br>TAU1 of 64-pin products with up to 96 Kbytes of code flash memory<br>TAU1 of 80-pin products with up to 96 Kbytes of code flash memory | TAU2 of 64-pin products (78K0R/FE3)<br>TAU2 of 80-pin products (78K0R/FF3) |

**Table 15-6 Possible combinations of master channel and slave channel of TAU, common between RL78/F14 and 78K0R/Fx3 (8 channels per unit)**

| Channels set as master channels,<br>Master channels are set by "TMRmn.MASTERmn = 1".<br>(m: Unit number, n: Channel number) | Channels which can be set as slave channels |
|---|---|
| Channel 0 | Channel 1 to 7 |
| Channel 2 | Channel 3 to 7 |
| Channel 4 | Channel 5 to 7 |
| Channel 6 | Channel 7 |
| Channel 0 and 2 | Operable in combination with Channel 0 → Channel 1<br>Operable in combination with Channel 2 → Channel 3 to 7 |
| Channel 0 and 4 | Operable in combination with Channel 0 → Channel 1 to 3<br>Operable in combination with Channel 4 → Channel 5 to 7 |
| Channel 0 and 6 | Operable in combination with Channel 0 → Channel 1 to 5<br>Operable in combination with Channel 6 → Channel 7 |
| Channel 2 and 4 | Operable in combination with Channel 2 → Channel 3<br>Operable in combination with Channel 4 → Channel 5 to 7 |
| Channel 2 and 6 | Operable in combination with Channel 2 → Channel 3 to 5<br>Operable in combination with Channel 6 → Channel 7 |
| Channel 4 and 6 | Operable in combination with Channel 4 → Channel 5<br>Operable in combination with Channel 6 → Channel 7 |
| Channel 0, 2, and 4 | Operable in combination with Channel 0 → Channel 1<br>Operable in combination with Channel 2 → Channel 3<br>Operable in combination with Channel 4 → Channel 5 to 7 |
| Channel 0, 2, and 6 | Operable in combination with Channel 0 → Channel 1<br>Operable in combination with Channel 2 → Channel 3 to 5<br>Operable in combination with Channel 6 → Channel 7 |
| Channel 0, 4, and 6 | Operable in combination with Channel 0 → Channel 1 to 3<br>Operable in combination with Channel 4 → Channel 5<br>Operable in combination with Channel 6 → Channel 7 |
| Channel 2, 4, and 6 | Operable in combination with Channel 2 → Channel 3<br>Operable in combination with Channel 4 → Channel 5<br>Operable in combination with Channel 6 → Channel 7 |
| Channel 0, 2, 4, and 6 | Operable in combination with Channel 0 →1<br>Operable in combination with Channel 2 →3<br>Operable in combination with Channel 4 →5<br>Operable in combination with Channel 6 →7 |

**Table 15-7 Possible combinations of master channel and slave channel of TAU in 78K0R/Fx3 (5 channels per unit)**

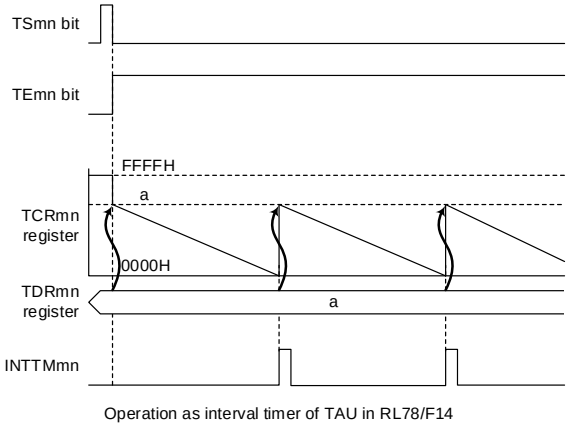
| Channels set as master channels,<br>Master channels are set by "TMRmn.MASTERmn = 1".<br>(m: Unit number, n: Channel number) | Channels which can be set as slave channels |
|---|---|
| Channel 0 | Channel 1 to 4 |
| Channel 2 | Channel 3 to 4 |
| Channel 0 and 2 | Operable in combination with Channel 0 → Channel 1<br>Operable in combination with Channel 2 → Channel 3 to 4 |

**Table 15-8 Possible combinations of master channel and slave channel of TAU, common between RL78/F14 and 78K0R/Fx3 (4 channels per unit)**

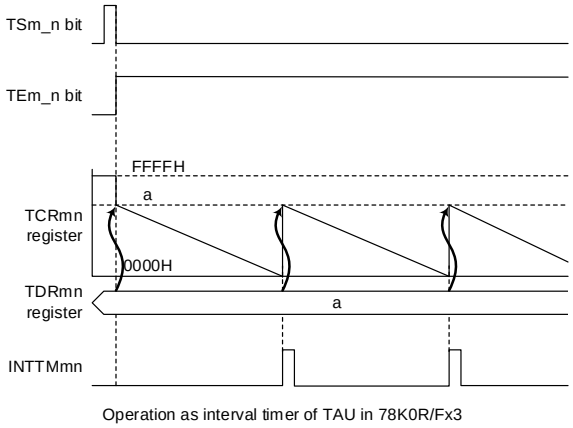
| Channels set as master channels<br>Master channels are set by "TMRmn.MASTERmn = 1".<br>(m: Unit number, n: Channel number) | Channels which can be set as slave channels |
|---|---|
| Channel 0 | Channel 1 to 3 |
| Channel 2 | Channel 3 |
| Channel 0 and 2 | Operable in combination with Channel 0 → Channel 1<br>Operable in combination with Channel 2 → Channel 3 |

### 15.1.1 Porting code for interval timer of TAU

Figure 15-2 shows the comparison of the operation as the interval timer of the TAU between the RL78/F14 and the 78K0R/Fx3.




Operation as interval timer of TAU in RL78/F14




Operation as interval timer of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TDRmn register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSmn bit | TSm_n bit |
| Status of timer operation | TEmn bit | TEm_n bit |
| Interrupt request | INTTMmn | INTTMmn |

m: TAU Unit number (m = 0, 1, 2)

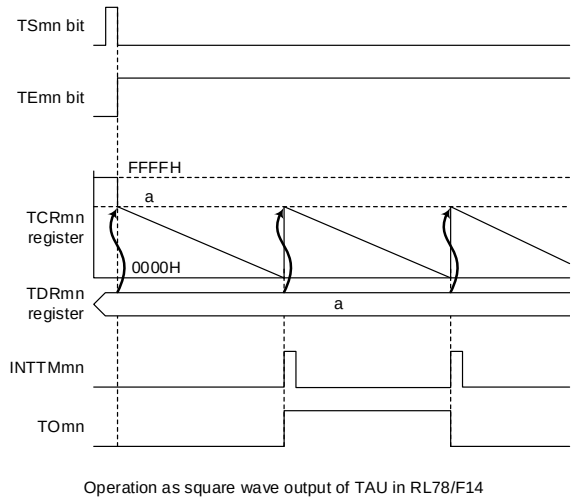
n: TAU Channel number (n = 0 to 7)

Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

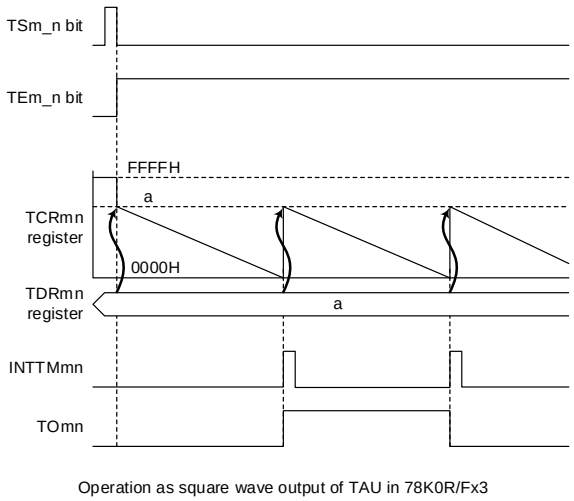
**Figure 15-2 Comparison of operation as interval timer of TAU between RL78/F14 and 78K0R/Fx3**

### 15.1.2 Porting code for square wave output function of TAU

Figure 15-3 shows the comparison of the operation as the square wave output of the TAU between the RL78/F14 and the 78K0R/Fx3.




Operation as square wave output of TAU in RL78/F14




Operation as square wave output of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TDRmn register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSmn bit | TSm_n bit |
| Status of timer operation | TEmn bit | TEm_n bit |
| Interrupt request | INTTMmn | INTTMmn |
| Output pin | TOmn pin | TOmn pin |

m: TAU Unit number (m = 0, 1, 2)

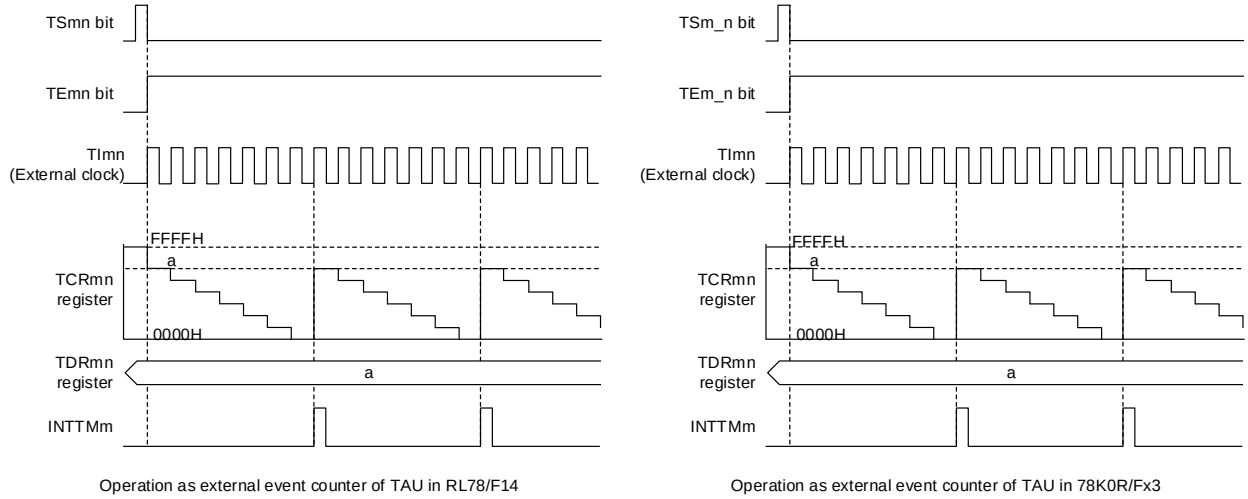
n: TAU Channel number (n = 0 to 7)

Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

**Figure 15-3 Comparison of operation as square wave output of TAU between RL78/F14 and 78K0R/Fx3**

### 15.1.3 Porting code for external event counter of TAU

Figure 15-4 shows the comparison of the operation as the external event counter of the TAU between the RL78/F14 and the 78K0R/Fx3.




Operation as external event counter of TAU in RL78/F14

Operation as external event counter of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TDRmn register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSmn bit | TSm_n bit |
| Status of timer operation | TEmn bit | TEm_n bit |
| Interrupt request | INTTMmn | INTTMmn |
| External clock input pin | TImn pin | TImn pin |

m: TAU Unit number (m = 0, 1, 2)

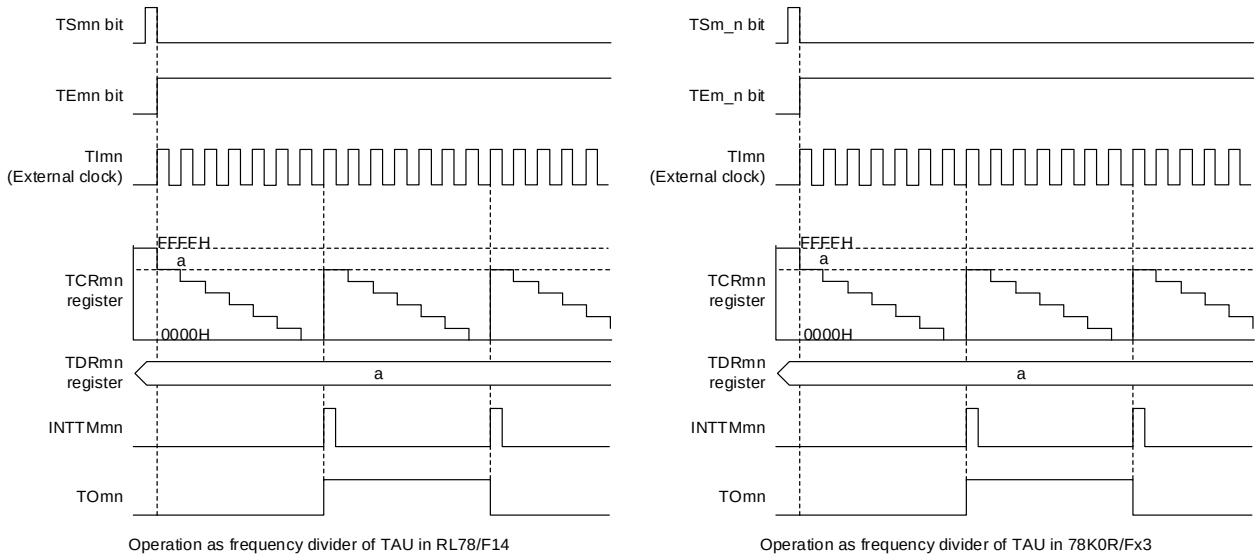
n: TAU Channel number (n = 0 to 7)

Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

**Figure 15-4 Comparison of operation as external event counter of TAU between RL78/F14 and 78K0R/Fx3**

### 15.1.4 Porting code for divider function of TAU

Figure 15-5 shows the comparison of the operation as a frequency divider of the TAU between the RL78/F14 and the 78K0R/Fx3.




| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TDRmn register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSmn bit | TSm_n bit |
| Status of timer operation | TEmn bit | TEm_n bit |
| Interrupt request | INTTMmn | INTTMmn |
| External clock input pin | TImn pin | TImn pin |
| Output pin | TOmn pin | TOmn pin |

m: TAU Unit number (m = 0, 1, 2)

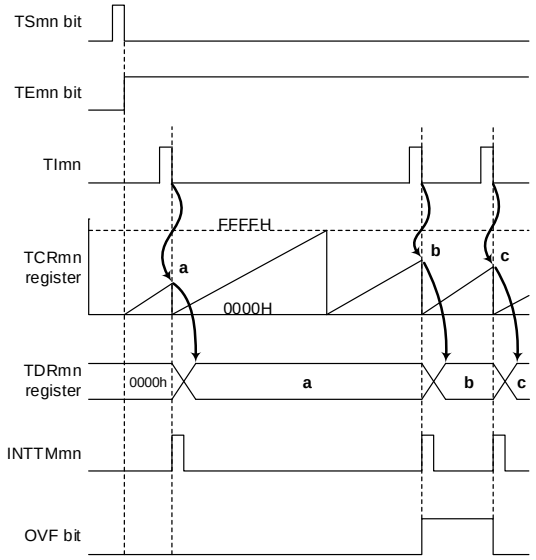
n: TAU Channel number (n = 0 to 7)

Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

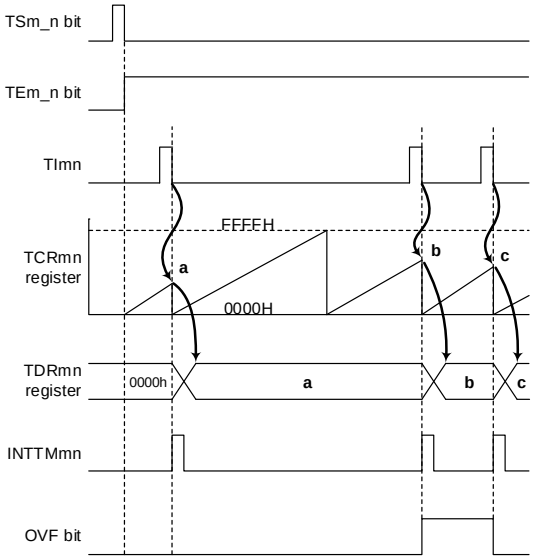
**Figure 15-5 Comparison of operation as frequency divider of TAU between RL78/F14 and 78K0R/Fx3**

### 15.1.5 Porting code for input pulse interval measurement function of TAU

Figure 15-6 shows the comparison of the operation as the input pulse interval measurement of the TAU between the RL78/F14 and the 78K0R/Fx3.




Example of operation as input pulse interval measurement of TAU in RL78/F14




Example of operation as input pulse interval measurement of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSmn bit | TSm_n bit |
| Status of timer operation | TEmn bit | TEm_n bit |
| Measurement pulse input pin | TImn pin | TImn pin |
| Storing measured value | TDRmn register (16 bits) | TDRmn register (16 bits) |
| Interrupt request | INTTMmn | INTTMmn |
| Overflow flag | OVF bit | OVF bit |

m: TAU Unit number (m = 0, 1, 2)

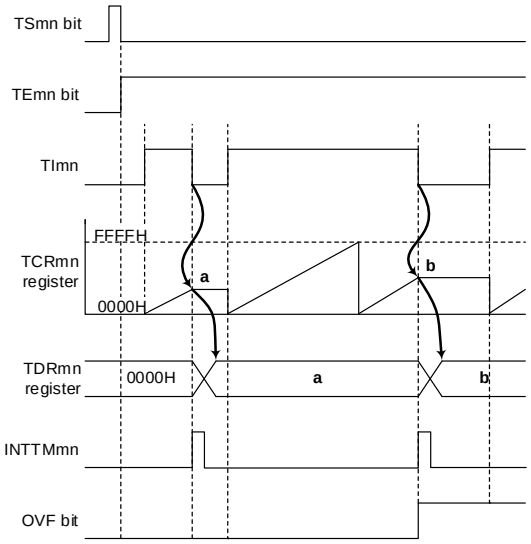
n: TAU Channel number (n = 0 to 7)

Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

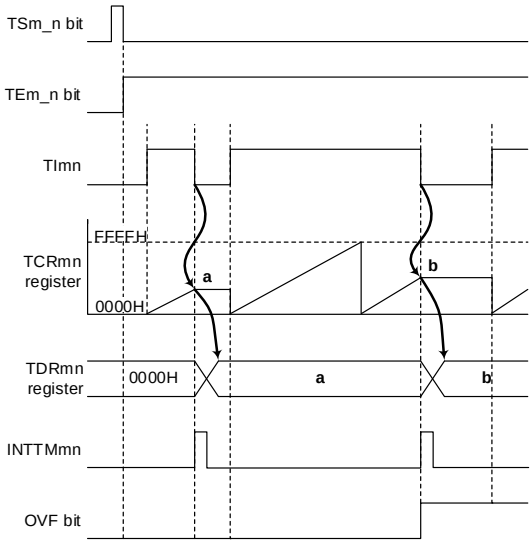
**Figure 15-6 Comparison of operation as input pulse interval measurement of TAU between RL78/F14 and 78K0R/Fx3**

### 15.1.6 Porting code for input signal high-/low-level width measurement function

Figure 15-7 shows the comparison of the operation as the input signal high-/low-level width measurement of the TAU between the RL78/F14 and the 78K0R/Fx3.




Example of operation as input signal high-/low-level width measurement of TAU in RL78/F14




Example of operation as input signal high-/low-level width measurement of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSmn bit | TSm_n bit |
| Status of timer operation | TEmn bit | TEm_n bit |
| Measurement pulse input pin | TImn pin | TImn pin |
| Storing measured value | TDRmn register (16 bits) | TDRmn register (16 bits) |
| Interrupt request | INTTMmn | INTTMmn |
| Overflow flag | OVF bit | OVF bit |

m: TAU Unit number (m = 0, 1, 2)

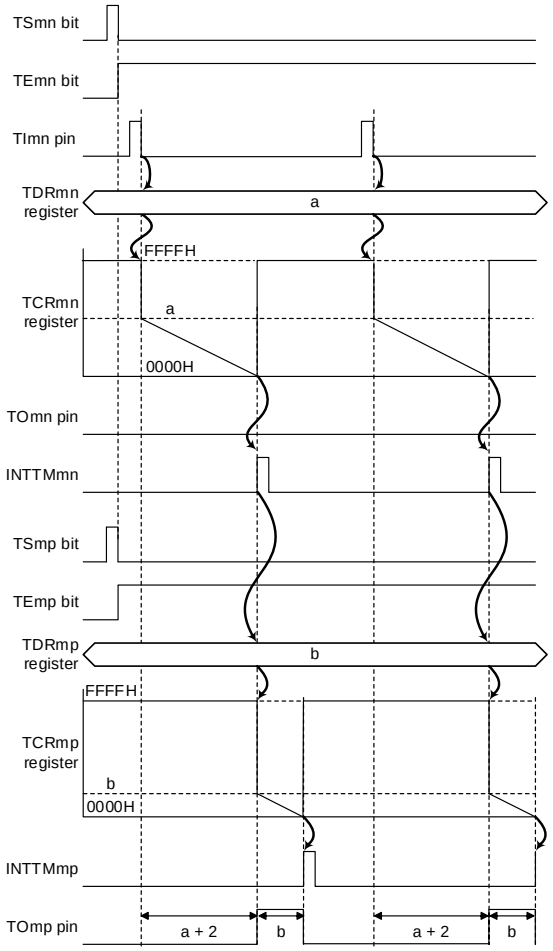
n: TAU Channel number (n = 0 to 7)

Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

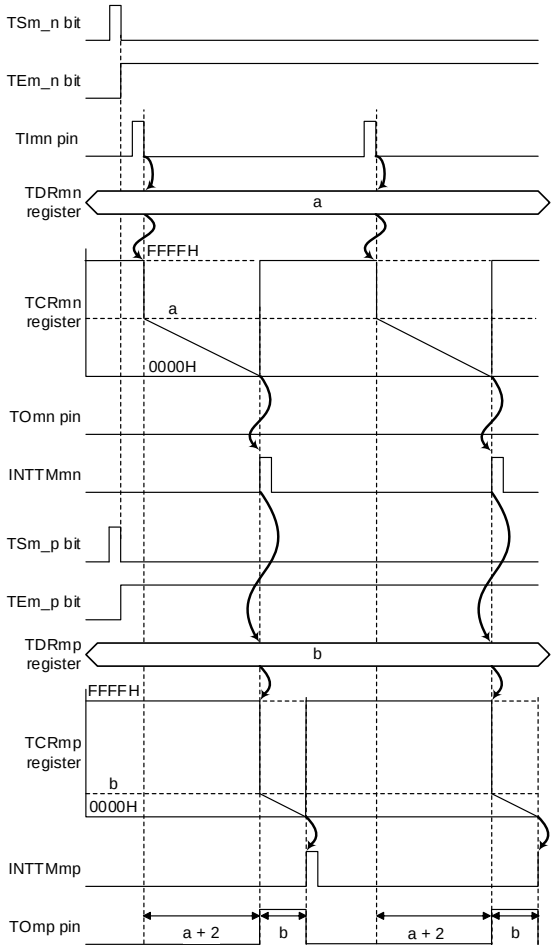
**Figure 15-7 Comparison of operation as input signal high-/low-level width measurement of TAU between RL78/F14 and 78K0R/Fx3**

### 15.1.7 Porting code for one-shot pulse output function of TAU

The one-shot pulse output of the TAU in the RL78/F14 and the 78K0R/Fx3 is realized by using the combination of a master channel and a slave channel. For the possible combinations of a master channel and a slave channel, see **Table 15-6** to **Table 15-8**. Figure 15-8 shows the comparison of the operation as the one-shot pulse output function between the RL78/F14 and the 78K0R/Fx3.




Operation as one-shot pulse output function of TAU in RL78/F14




Operation as one-shot pulse output function of TAU in 78K0R/Fx3

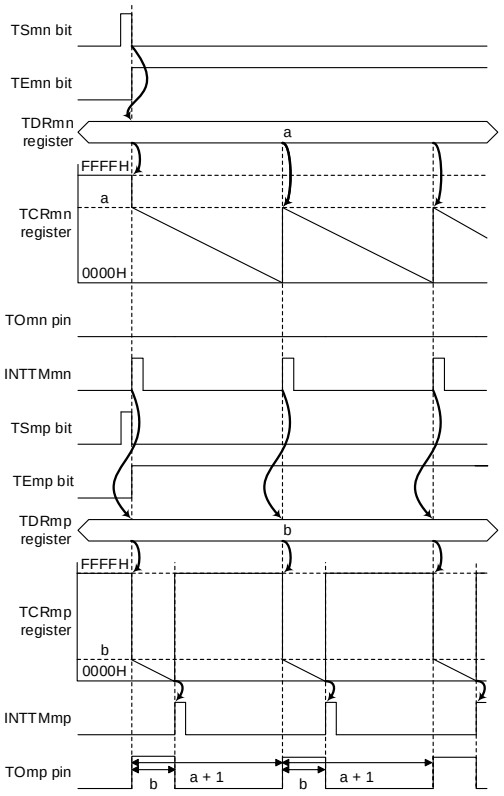
| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TDRmn register (16 bits)<br>TDRmp register (16 bits) | TDRmn register (16 bits)<br>TDRmp register (16 bits) |
| Counter start | TSmn bit<br>TSmp bit | TSm_n bit<br>TSm_p bit |
| Status of timer operation | TEmn bit<br>TEmp bit | TEm_n bit<br>TEm_p bit |
| Count start trigger input | TImn pin | TImn pin |
| Interrupt request | INTTMmn<br>INTTMmp | INTTMmn<br>INTTMmp |
| Output pin | TOmp pin | TOmp pin |

m: TAU Unit number (m = 0, 1, 2)
n: Master channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)
Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

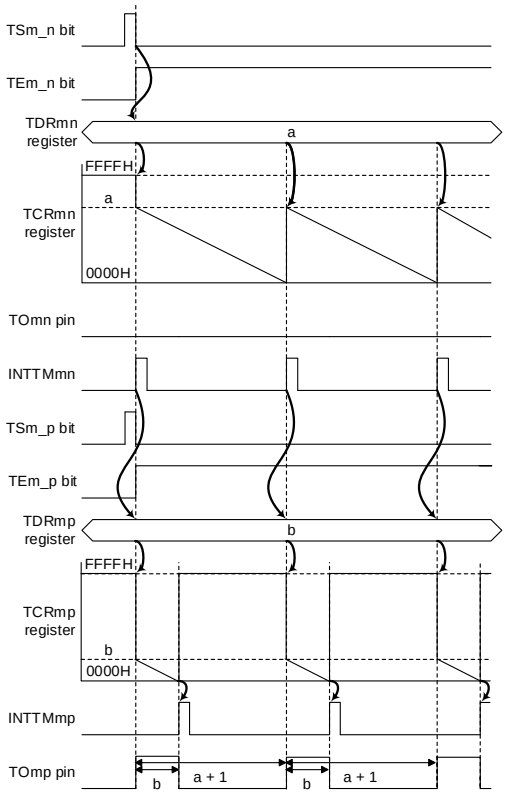
**Figure 15-8 Comparison of operation as one-shot pulse output function between RL78/F14 and 78K0R/Fx3**

### 15.1.8 Porting code for PWM function of TAU

The PWM output of the TAU in the RL78/F14 and the 78K0R/Fx3 is realized by using the combination of a master channel and a slave channel. For the possible combinations of a master channel and a slave channel, see **Table 15-6** to **Table 15-8**. Figure 15-9 shows the comparison of the operation as the PWM output between the RL78/F14 and the 78K0R/Fx3.




Example of operation as PWM output of TAU in RL78/F14




Example of operation as PWM output of TAU in 78K0R/Fx3

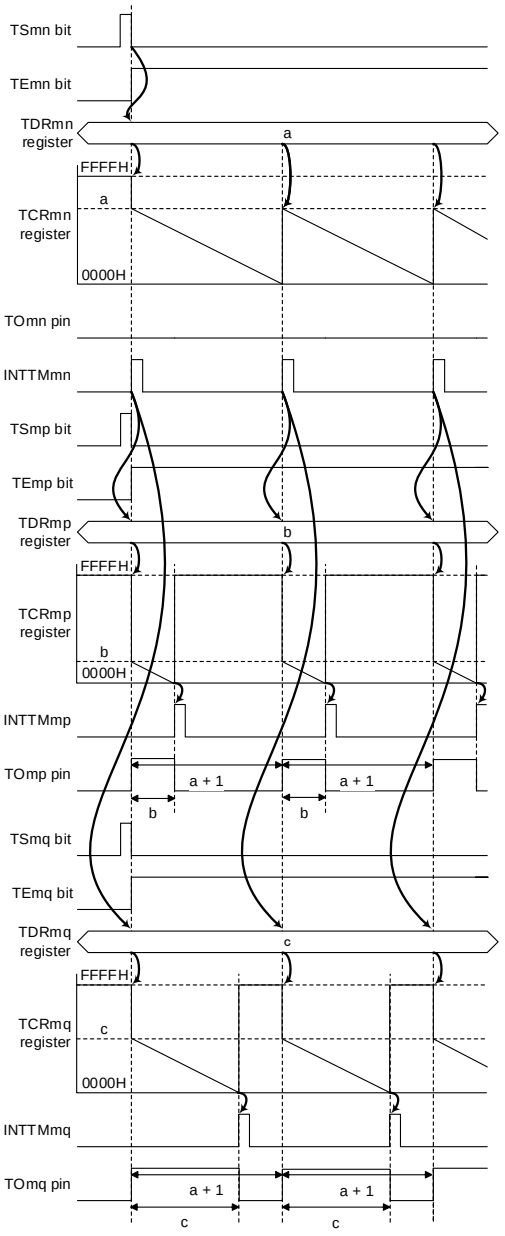
| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSmn bit<br>TSmp bit | TSm_n bit<br>TSm_p bit |
| Status of timer operation | TEmn bit<br>TEmp bit | TEm_n bit<br>TEm_p bit |
| PWM period setting | TDRmn register (16 bits) | TDRmn register (16 bits) |
| PWM duty setting | TDRmp register (16 bits) | TDRmp register (16 bits) |
| Interrupt request | INTTMmn<br>INTTMmp | INTTMmn<br>INTTMmp |
| PWM output pin | TOmp pin | TOmp pin |

m: TAU Unit number (m = 0, 1, 2)
n: Master channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)
Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

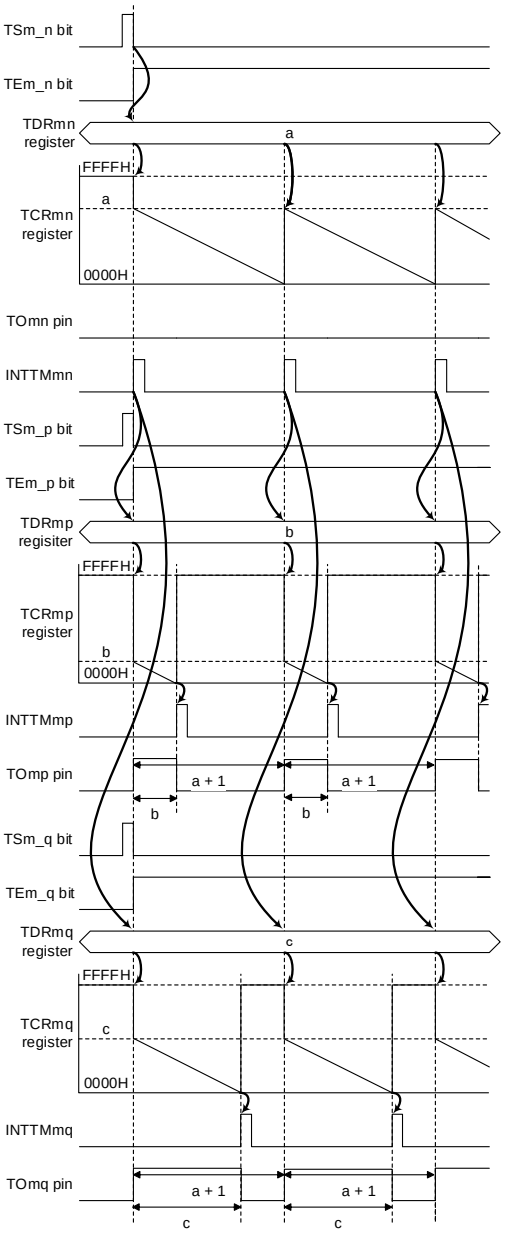
**Figure 15-9 Comparison of operation as PWM output between RL78/F14 and 78K0R/Fx3**

### 15.1.9 Porting code for multiple PWM output function

The multiple PWM output of the TAU in the RL78/F14 and the 78K0R/Fx3 is realized by using the combination of a master channel and a slave channel. For the possible combinations of a master channel and a slave channel, see **Table 15-6** to **Table 15-8**. Figure 15-10 shows the comparison of the operation as the multiple PWM output between the RL78/F14 and the 78K0R/Fx3.




Example of operation as multiple PWM output of TAU in RL78/F14




Example of operation as multiple PWM output of TAU in 78K0R/Fx3

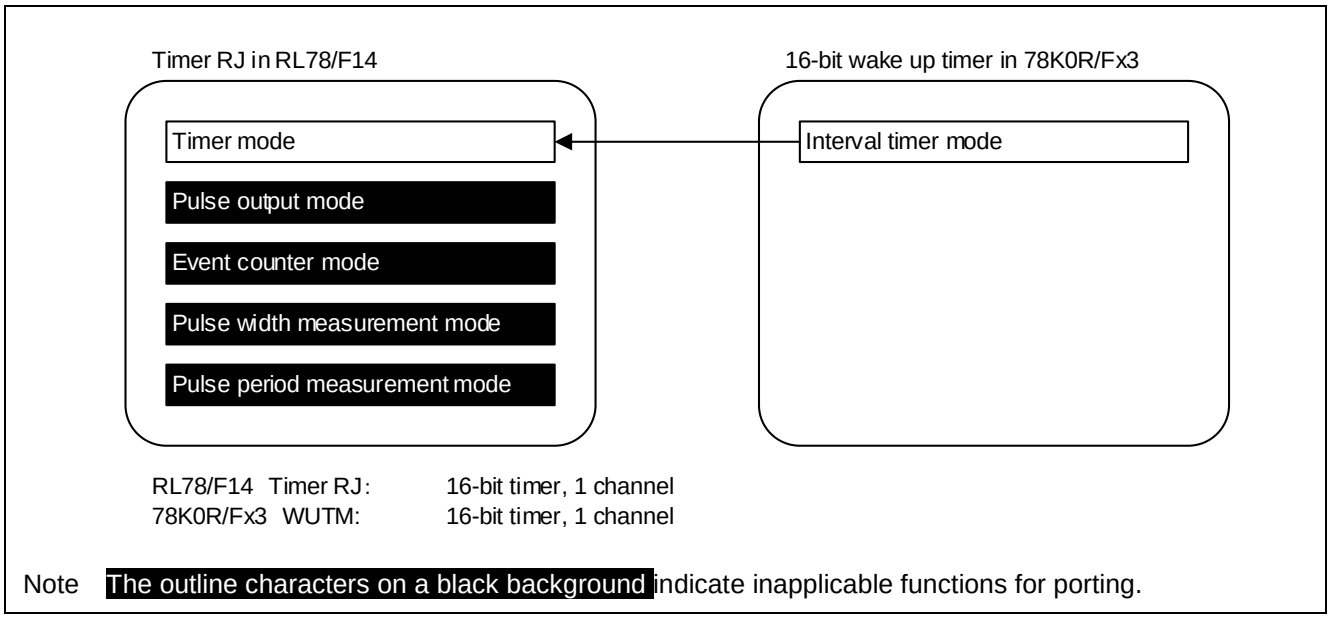
| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSmn bit<br>TSmp bit<br>TSmq bit | TSm_n bit<br>TSm_p bit<br>TSm_q bit |
| Status of timer operation | TEmn bit<br>TEmp bit<br>TEmq bit | TEm_n bit<br>TEm_p bit<br>TEm_q bit |
| PWM period setting | TDRmn register (16 bits) | TDRmn register (16 bits) |
| PWM duty setting | TDRmp register (16 bits)<br>TDRmq register (16 bits) | TDRmp register (16 bits)<br>TDRmq register (16 bits) |
| Interrupt request | INTTMmn<br>INTTMmp<br>INTTMmq | INTTMmn<br>INTTMmp<br>INTTMmq |
| PWM output pin | TOmp pin<br>TOmq pin | TOmp pin<br>TOmq pin |

m: TAU Unit number (m = 0, 1, 2)
n: Master channel number (n = 0, 2, 4, 6)
p, q: Slave channel number (n < p, q ≤ 7)
Caution The number of units and channels of TAU differs depending on the product. See **Table 15-3** for the RL78/F14 and **Table 15-4** for the 78K0R/Fx3.

**Figure 15-10 Comparison of operation as multiple PWM output between RL78/F14 and 78K0R/Fx3**

## 15.2 Porting code for functions of 16-bit wakeup timer over to that for Timer RJ

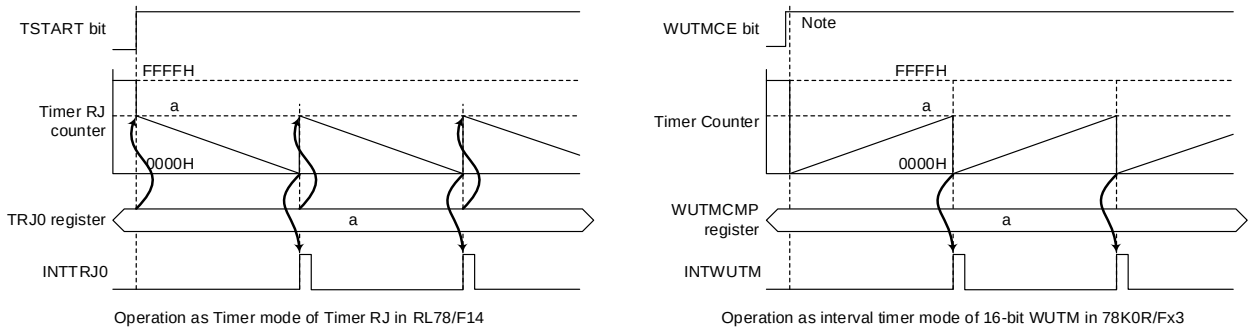
Figure 15-11 shows the relationship between each mode of the Timer RJ in the RL78/F14 and that of the 16-bit WUTM in the 78K0R/Fx3.




Note The outline characters on a black background indicate inapplicable functions for porting.

**Figure 15-11 Relationship between each mode of Timer RJ in RL78/F14 and that of 16-bit WUTM in 78K0R/Fx3**

Figure 15-12 shows the comparison of the operation as the timer mode of Timer RJ in the RL78/F14 and that as the interval timer mode of the 16-bit WUTM in the 78K0R/Fx3.




| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TRJ0 register (16 bits) | WUTMCMP register (16 bits) |
| Counter start | TSTART bit | WUTMCE bit |
| Interrupt request | INTTRJ0 | INTWUTM |

Note Within two input clocks counted from the time when the WUDMCE bit is set to "1", the internal operation clock becomes enabled and then WUTM starts counting up.

Remark In the RL78/F14, the count source for Timer RJ is selected from among $f_{CLK}$, $f_{CLK}/2$, $f_{CLK}/8$, $f_{IL}$, $f_{SL}$, or event input from the event link controller (ELC). See the user's manual for details.

**Figure 15-12 Comparison of 16-bit WUTM operation and Timer RJ operation**

**<Key Points on Porting>**

·**Count mode**

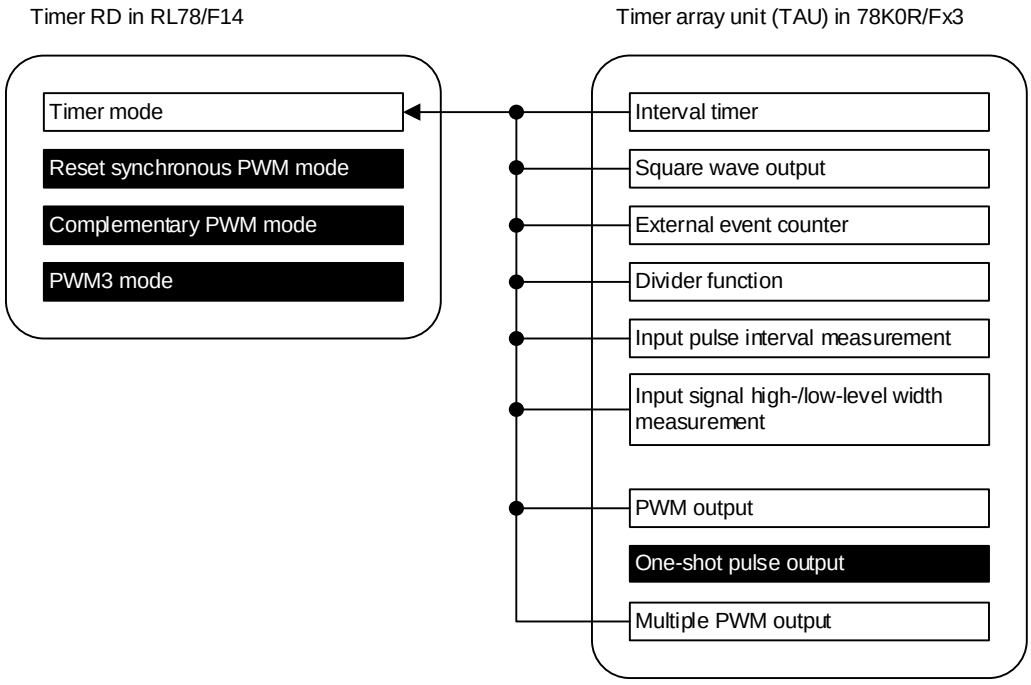
Unlike the timer counter of the 16-bit WUTM in the 78K0R/Fx3, the Timer RJ in the RL78/F14 operates as a down counter. Confirm that this difference would not lead to problems.

## 15.3 Porting code for TAU functions over to that for Timer RD functions

Figure 15-13 shows the relationship between each mode of the Timer RD in the RL78/F14 and that of the TAU in the 78K0R/Fx3.

Depending on the choice of the RL78/F14 product, porting code for the TAU in the 78K0R/Fx3 over to that in the RL78/F14 might cause a shortage of TAU channels.

For example, the total number of TAU channels in the 78K0R/FG3 (100 pins) is 24 channels (8 channels × 3); whereas that in the RL78/F14 (100 pins) is 16 channels (8 channels × 2), i.e. smaller than that in the 78K0R/FG3 (100 pins) by 8 channels. In order to compensate for possible channel shortages, several examples using the Timer RD instead of the TAU are shown below. For the number of the channels of the TAU in each product of the RL78/F14 and the 78K0R/Fx3, see **Table 15-1** and **Table 15-2**.




Timer RD in RL78/F14: 16-bit timer, 2 units

TAU in 78K0R/Fx3: 16-bit timer, 2 units or 3 units
TAU0: 8 channels
TAU1: 5 channels or 8 channels
TAU2: 4 channels or 8 channels
Two channels are necessary for the PWM output, the one-shot pulse output, and the Multiple PWM output

Note The outline characters on a black background indicate inapplicable functions for porting.

**Figure 15-13 Relationship between each mode of Timer RD in RL78/F14 and that of TAU in 78K0R/Fx3**

**·Count sources for TAU and Timer RD**

The count source for the TAU in the 78K0R/Fx3 is the clock obtained by the frequency-division of $f_{CLK}$ by 1 to $2^{15}$. On the other hand, the count source for the Timer RD in the RL78/F14 is the clock determined by the following setting values.

- Clock source selected as CPU/peripheral hardware clock frequency ($f_{CLK}$)
- Value of FRQSEL4 bit (frequency of high-speed on-chip oscillator (high-speed OCO))
- Value of TRD_CKSEL bit in CKSEL register (Timer RD clock selection)
- Value of the bits TCK2 to TCK0 in TRDCRi (Timer RD count source select)

Table 15-9 shows the available count sources for the Timer RD in the RL78/F14.

**Table 15-9 Available count sources for Timer RD in RL78/F14 (1/3)**

| CPU operation clock source ($f_{CLK}$) | Value of FRQSEL4 bit (Frequency of high-speed OCO) | Value of TRD_CKSEL | Value of bits TCK2 to TCK0 (Available count sources for Timer RD) (Note 1) |
|---|---|---|---|
| High-speed OCO<br>$f_{MP} = f_{IH}$<br>(CSS = 0) | 1: Either 64 MHz or 48 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{IH}$ |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: Setting prohibited |
| | 0: Any of 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, or 1 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{CLK}$ |
| | | | ○ 001B: $f_{CLK}/2$ |
| | | | ○ 010B: $f_{CLK}/4$ |
| | | | ○ 011B: $f_{CLK}/8$ |
| | | | ○ 100B: $f_{CLK}/32$ |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: Setting prohibited |

○: When this value is selected, the clock source of the Timer RD and that of the TAU ($f_{CLK}$) become the same.

Notes 1. Start the clock source used as the timer RD count source, before setting the TRD_CKSEL bit and the bits TCK2 to TCK0.

2. In the PWM3 mode, setting this value (the external signal input to the TRDCLK0 pin) is prohibited.

**Table 15-9 Available count sources for Timer RD in RL78/F14 (2/3)**

| CPU operation clock source ($f_{CLK}$) | Value of FRQSEL4 bit (Frequency of high-speed OCO) | Value of TRD_CKSEL | Value of bits TCK2 to TCK0 (Available count sources for Timer RD) (Note 1) |
|---|---|---|---|
| Low-speed OCO<br>$f_{SL} = f_{IL}$<br>(CSS = 1) | 1: Either 64 MHz or 48 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | ○ 000B: $f_{IH}$ |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | 0: Any of 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, or 1 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{CLK}$ |
| | | | ○ 001B: $f_{CLK}/2$ |
| | | | ○ 010B: $f_{CLK}/4$ |
| | | | ○ 011B: $f_{CLK}/8$ |
| | | | ○ 100B: $f_{CLK}/32$ |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | ○ 000B: $f_{IL}$ |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| X1 clock<br>$f_{MP} = f_{MX}$<br>(CSS = 0) | 1: Either 64 MHz or 48 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: Setting prohibited |
| | 0: Any of 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, or 1 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{CLK}$ |
| | | | ○ 001B: $f_{CLK}/2$ |
| | | | ○ 010B: $f_{CLK}/4$ |
| | | | ○ 011B: $f_{CLK}/8$ |
| | | | ○ 100B: $f_{CLK}/32$ |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: Setting prohibited |

○: When this value is selected, the clock source of the Timer RD and that of the TAU ($f_{CLK}$) become the same.

Notes 1. Start the clock source used as the timer RD count source, before setting the TRD_CKSEL bit and the bits TCK2 to TCK0.

2. In the PWM3 mode, setting this value (the external signal input to the TRDCLK0 pin) is prohibited.

**Table 15-9 Available count sources for Timer RD in RL78/F14 (3/3)**

| CPU operation clock source ($f_{CLK}$) | Value of FRQSEL4 bit (Frequency of high-speed OCO) | Value of TRD_CKSEL | Value of bits TCK2 to TCK0 (Available count sources for Timer RD) (Note 1) |
|---|---|---|---|
| PLL clock $f_{MP} = f_{PLL}$ (CSS = 0) | 1: Either 64 MHz or 48 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{PLL} \leq 32$MHz |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | 0: Any of 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, or 1 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{CLK}$ |
| | | | ○ 001B: $f_{CLK}/2$ |
| | | | ○ 010B: $f_{CLK}/4$ |
| | | | ○ 011B: $f_{CLK}/8$ |
| | | | ○ 100B: $f_{CLK}/32$ |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: Setting prohibited |
| XT1 clock $f_{SL} (= f_{SUB})$ (CSS = 1) | 1: Either 64 MHz or 48 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | 000B: Setting prohibited |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | ○ 000B: $f_{SUB}$ |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | 0: Any of 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, or 1 MHz | 0: Either $f_{CLK}$ or $f_{MP}$ is selected | ○ 000B: $f_{CLK}$ |
| | | | ○ 001B: $f_{CLK}/2$ |
| | | | ○ 010B: $f_{CLK}/4$ |
| | | | ○ 011B: $f_{CLK}/8$ |
| | | | ○ 100B: $f_{CLK}/32$ |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |
| | | 1: $f_{SL}$ is selected | ○ 000B: $f_{SUB}$ |
| | | | 001B: Setting prohibited |
| | | | 010B: Setting prohibited |
| | | | 011B: Setting prohibited |
| | | | 100B: Setting prohibited |
| | | | 101B: External signal input to the TRDCLK0 pin (Note 2) |

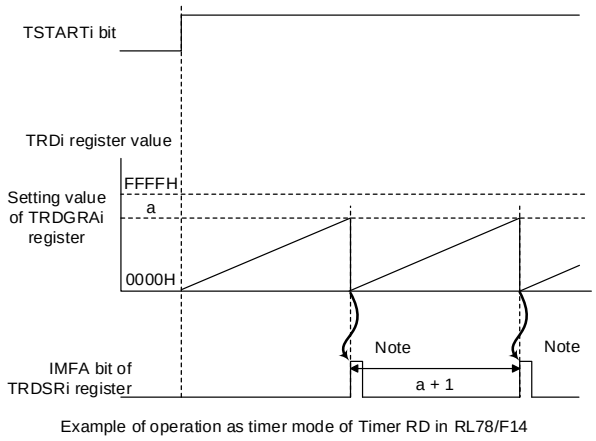
○: When this value is selected, the clock source of the Timer RD and that of the TAU ($f_{CLK}$) become the same.

Notes 1. Start the clock source used as the timer RD count source, before setting the TRD_CKSEL bit and the bits TCK2 to TCK0.

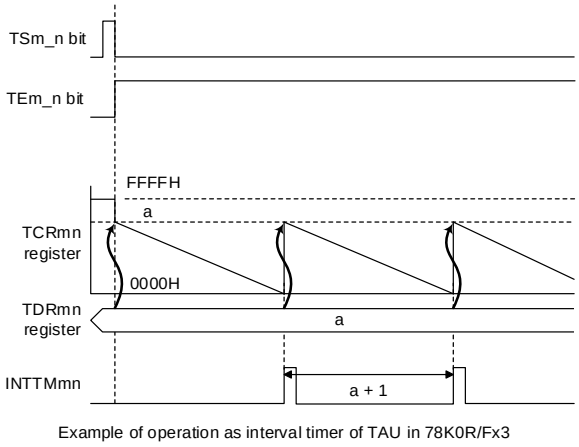
2. In the PWM3 mode, setting this value (the external signal input to the TRDCLK0 pin) is prohibited.

### 15.3.1 Porting code for TAU (interval timer) over to that for Timer RD (timer mode)

Figure 15-14 shows the comparison of the operation as the timer mode (the output compare function) in the RL78/F14 and that as the interval timer in the 78K0R/Fx3.




Example of operation as timer mode of Timer RD in RL78/F14




Example of operation as interval timer of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TRDGRAi register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSTARTi bit | TSm_n bit |
| Status of timer operation | - | TEm_n bit |
| Interrupt request | IMFA bit | INTTMmn |

Note Set to “0” by a program.

**Figure 15-14 Comparison of operation between timer mode in RL78/F14 and interval timer in 78K0R/Fx3**

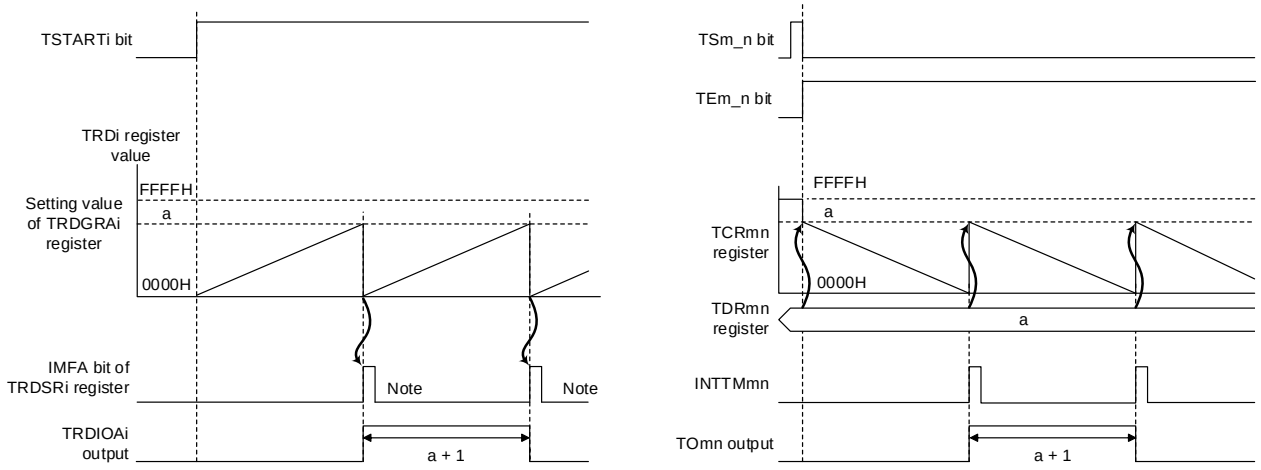
**<Key Points on Porting>**

- **Count mode**

Unlike the timer counter of the TAU in the 78K0R/Fx3, the Timer RD in the RL78/F14 operates as an up counter. Confirm that this difference would not lead to problems.

### 15.3.2 Porting code for TAU (square wave output function) over to that for Timer RD (timer mode)

Figure 15-15 shows the comparison of the operation as the timer mode (the output compare function) in the RL78/F14 and that as the square wave output in the 78K0R/Fx3.




Example of operation as timer mode of Timer RD in RL78/F14

Example of operation as square wave output of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TRDGRAi register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSTARTi bit | TSm_n bit |
| Status of timer operation | - | TEm_n bit |
| Interrupt request | IMFA bit | INTTMmn |
| Output pin | TRDIOAi pin | TOmn pin |

Note Set to “0” by a program.

**Figure 15-15 Comparison of operation between timer mode in RL78/F14 and square wave output in 78K0R/Fx3**

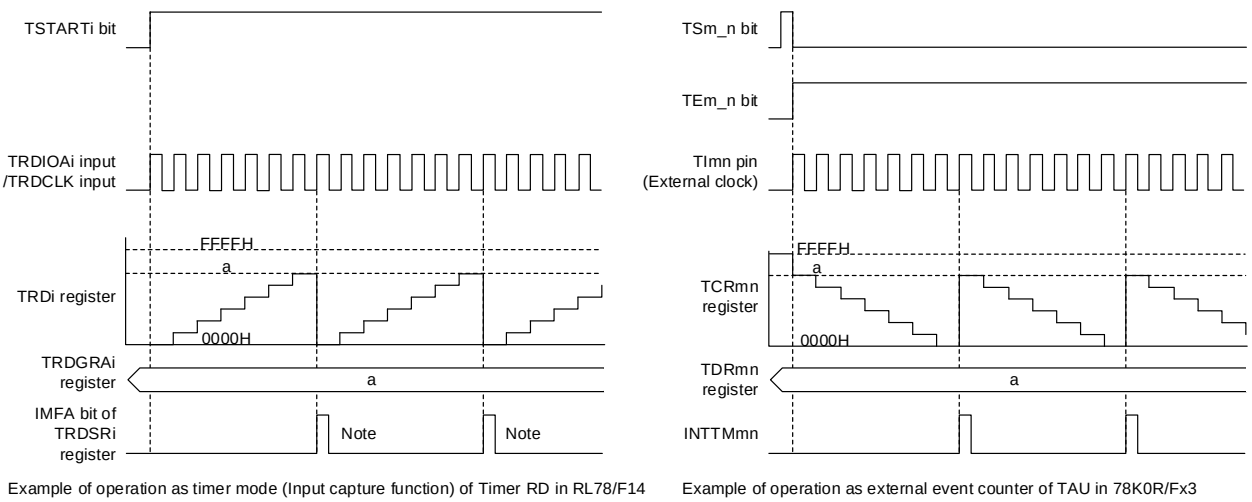
**<Key Points on Porting>**

**·Count mode**

Unlike the timer counter of the TAU in the 78K0R/Fx3, the Timer RD in the RL78/F14 operates as an up counter. Confirm that this difference would not lead to problems.

### 15.3.3 Porting code for TAU (external event counter) over to that for Timer RD (input capture function)

Figure 15-16 shows the comparison of the operation as the timer mode (the input capture function) in the RL78/F14 and that as the external event counter in the 78K0R/Fx3.




Example of operation as timer mode (Input capture function) of Timer RD in RL78/F14

Example of operation as external event counter of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TRDGRAi register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSTARTi bit | TSm_n bit |
| Status of timer operation | - | TEm_n bit |
| Interrupt request | IMFA bit | INTTMmn |
| External clock input pin | TRDCLK0 pin | TImn pin |

Note Set to “0” by a program.

**Figure 15-16 Comparison of operation between timer mode in RL78/F14 and external event counter in 78K0R/Fx3**

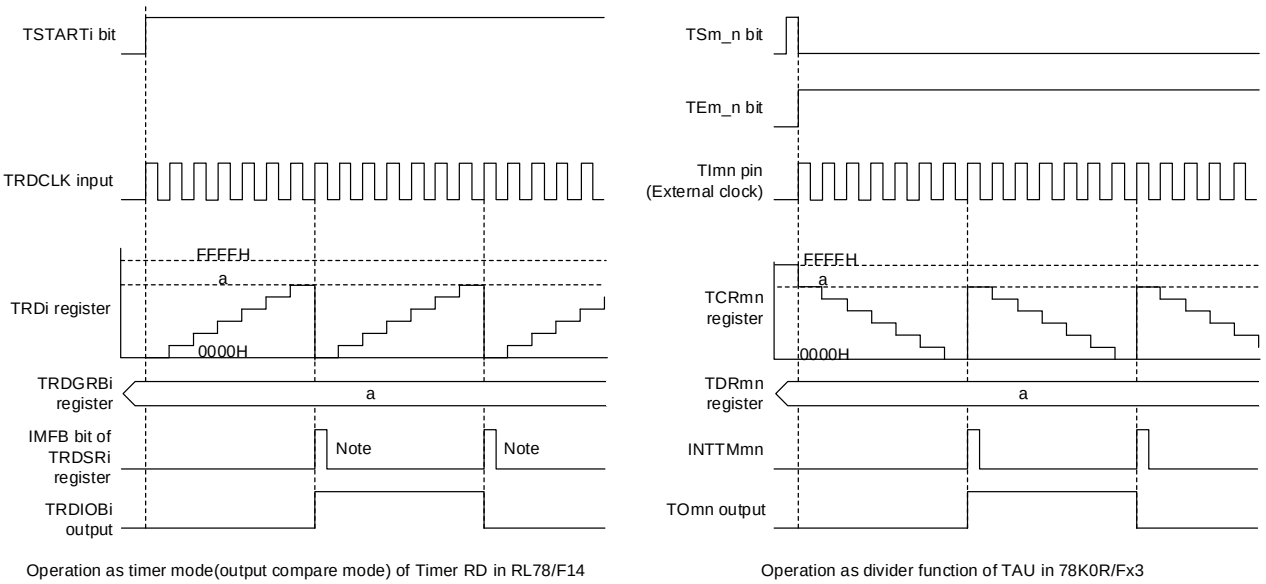
**<Key Points on Porting>**

**·Count mode**

Unlike the timer counter of the TAU in the 78K0R/Fx3, the Timer RD in the RL78/F14 operates as an up counter. Confirm that this difference would not lead to problems.

### 15.3.4 Porting code for TAU (divider function) over to that for Timer RD (output compare function)

Figure 15-17 shows the comparison of the operation as the timer mode (the output compare function) in the RL78/F14 and that as the divider function in the 78K0R/Fx3.




| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Count value setting | TRDGRBi register (16 bits) | TDRmn register (16 bits) |
| Counter start | TSTARTi bit | TSm_n bit |
| Status of timer operation | - | TEm_n bit |
| Interrupt request | IMFB bit | INTTMmn |
| External clock input pin | TRDCLK0 pin | TImn pin |
| Output pin | TRDIOBi pin | TOmn pin |

Note Set to “0” by a program.

**Figure 15-17 Comparison of operation between timer mode in RL78/F14 and divider function in 78K0R/Fx3**

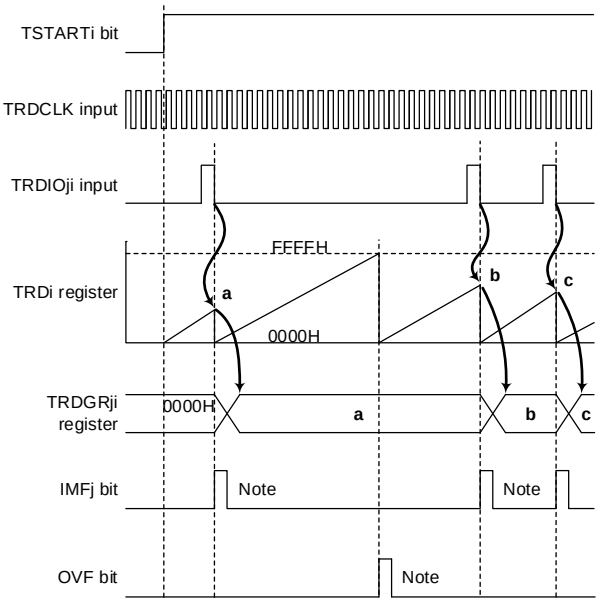
**<Key Points on Porting>**

**·Count mode**

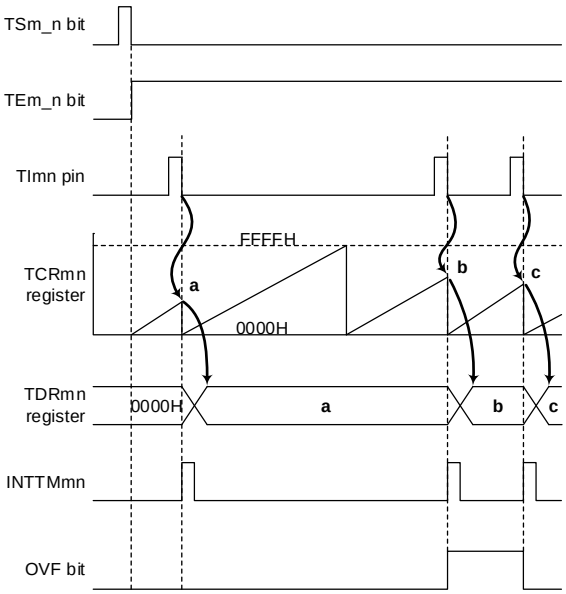
Unlike the timer counter of the TAU in the 78K0R/Fx3, the Timer RD in the RL78/F14 operates as an up counter. Confirm that this difference would not lead to problems.

### 15.3.5 Porting code for TAU (input pulse interval measurement function) over to that for Timer RD (input capture function)

Figure 15-18 shows the comparison of the operation as the timer mode (the input capture function) in the RL78/F14 and that as the input pulse interval measurement in the 78K0R/Fx3.




Example of operation as timer mode(input capture function) of Timer RD in RL78/F14




Example of operation as input pulse interval measurement of TAU in 78K0R/Fx3

(i = 0, 1, j = A, B, C, D)

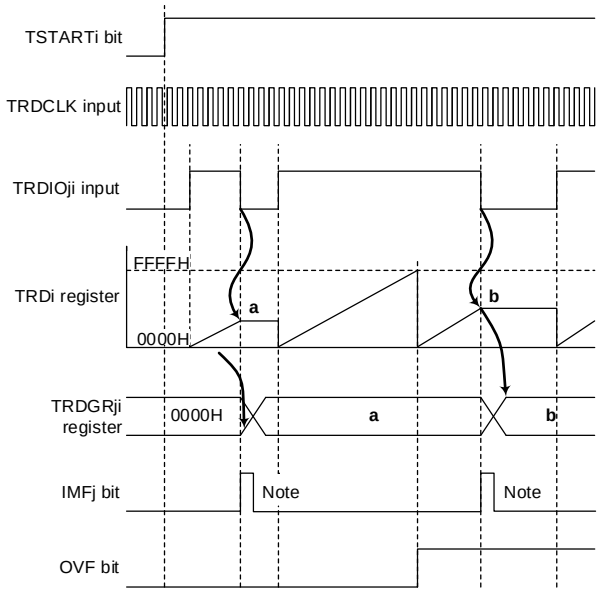
| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSTARTi bit | TSm_n bit |
| Status of timer operation | - | TEm_n bit |
| Measurement pulse input pin | TRDIOji pin | TImn pin |
| Storing measured value | TRDGRji register (16 bits) | TDRmn register (16 bits) |
| Interrupt request | IMFj bit | INTTMmn |
| Overflow flag | OVF bit | OVF bit |

Note Set to “0” by a program.

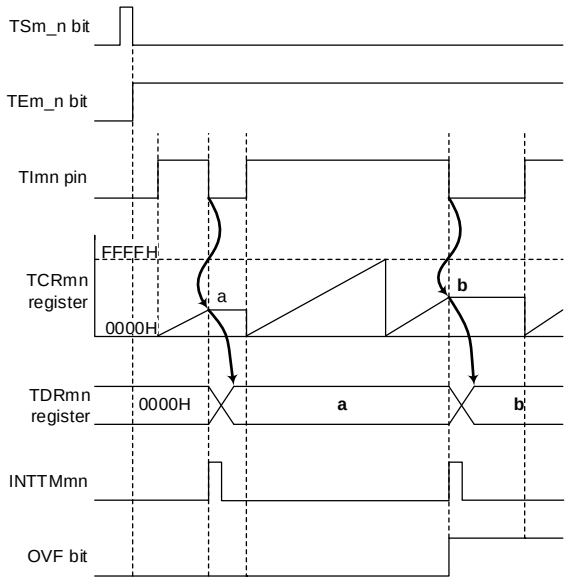
**Figure 15-18 Comparison of operation between timer mode in RL78/F14 and input pulse interval measurement in 78K0R/Fx3**

### 15.3.6 Porting code for TAU (input signal high-/low-level width measurement function) over to that for Timer RD (input capture function)

Figure 15-19 shows the comparison of the operation as the timer mode (the input capture function) in the RL78/F14 and that as the input signal high-/low-level width measurement in the 78K0R/Fx3.




Example of operation as timer mode(input capture function) of Timer RD in RL78/F14




Example of operation as input signal high-/low-level width measurement of TAU in 78K0R/Fx3.

(i = 0, 1, j = A, B, C, D)

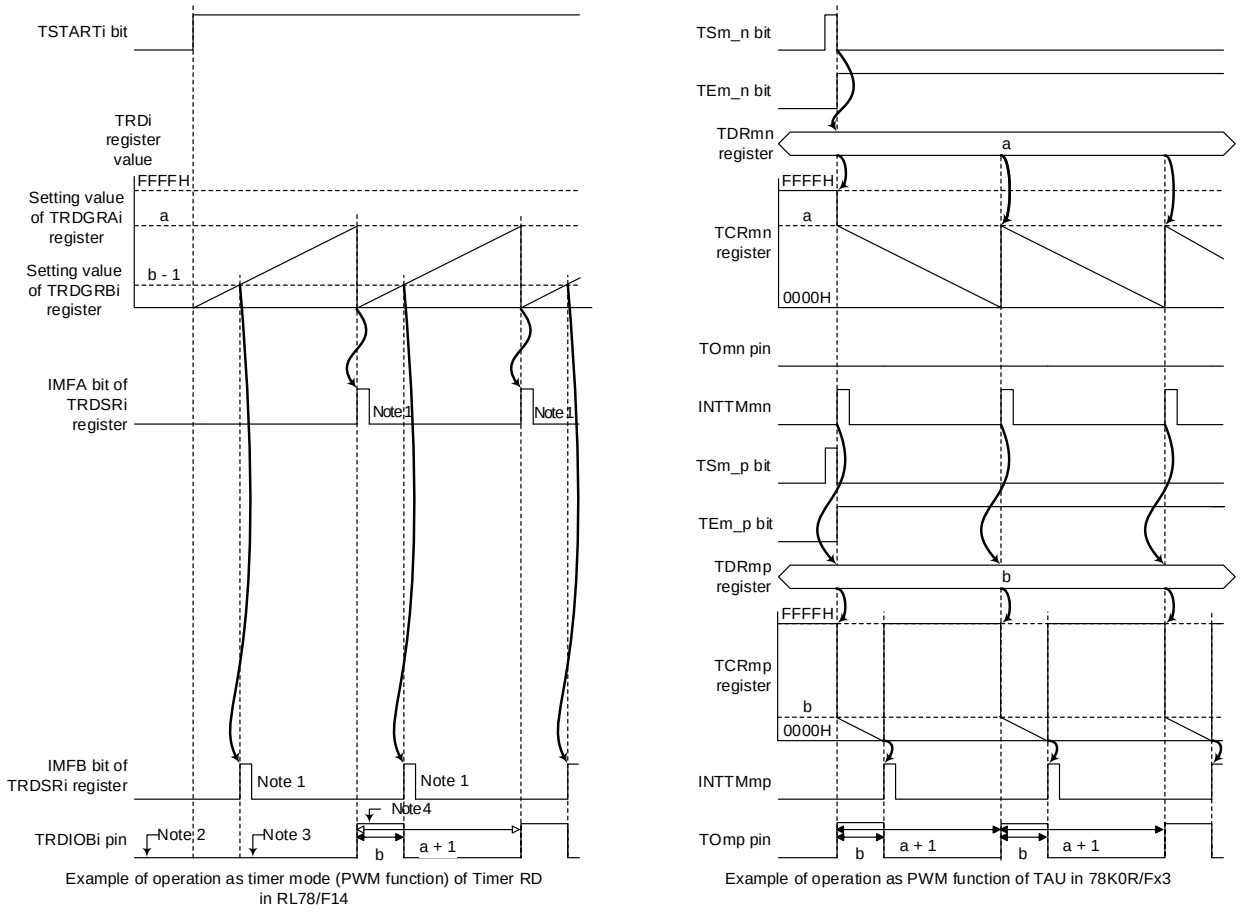
| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSTARTi bit | TSm_n bit |
| Status of timer operation | - | TEm_n bit |
| Measurement pulse input pin | TRDIOji pin | TImn pin |
| Storing measured value | TRDGRji register (16 bits) | TDRmn register (16 bits) |
| Interrupt request | IMFj bit | INTTMmn |
| Overflow flag | OVF bit | OVF bit |

Note Set to “0” by a program.

**Figure 15-19 Comparison of operation between timer mode in RL78/F14 and input signal high-/low-level width measurement in 78K0R/Fx3**

### 15.3.7 Porting code for TAU (PWM output) over to that for Timer RD (PWM function)

Figure 15-20 shows the comparison of the operation as the timer mode (the PWM function) in the RL78/F14 and that as the PWM function in the 78K0R/Fx3.




| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSTARTi bit | TSm_n bit<br>TSm_p bit |
| Status of timer operation | - | TEm_n bit<br>TEm_p bit |
| PWM period setting | TRDGRAi register (16 bits) | TDRmn register (16 bits) |
| PWM duty setting | TRDGRBi register (16 bits) | TDRmp register (16 bits) |
| Interrupt request | IMFA bit<br>IMFB bit | INTTMmn<br>INTTMmp |
| PWM output pin | TRDIOBi pin | TOmp pin |

Notes 1. Set to “0” by a program.
2. The initial output level remains unchanged until compare match.
(The initial output level is low in this figure)
3. Active level is low.
4. Inactive level is high.

**Figure 15-20 Comparison of operation between timer mode (PWM function) in RL78/F14 and PWM function in 78K0R/Fx3**

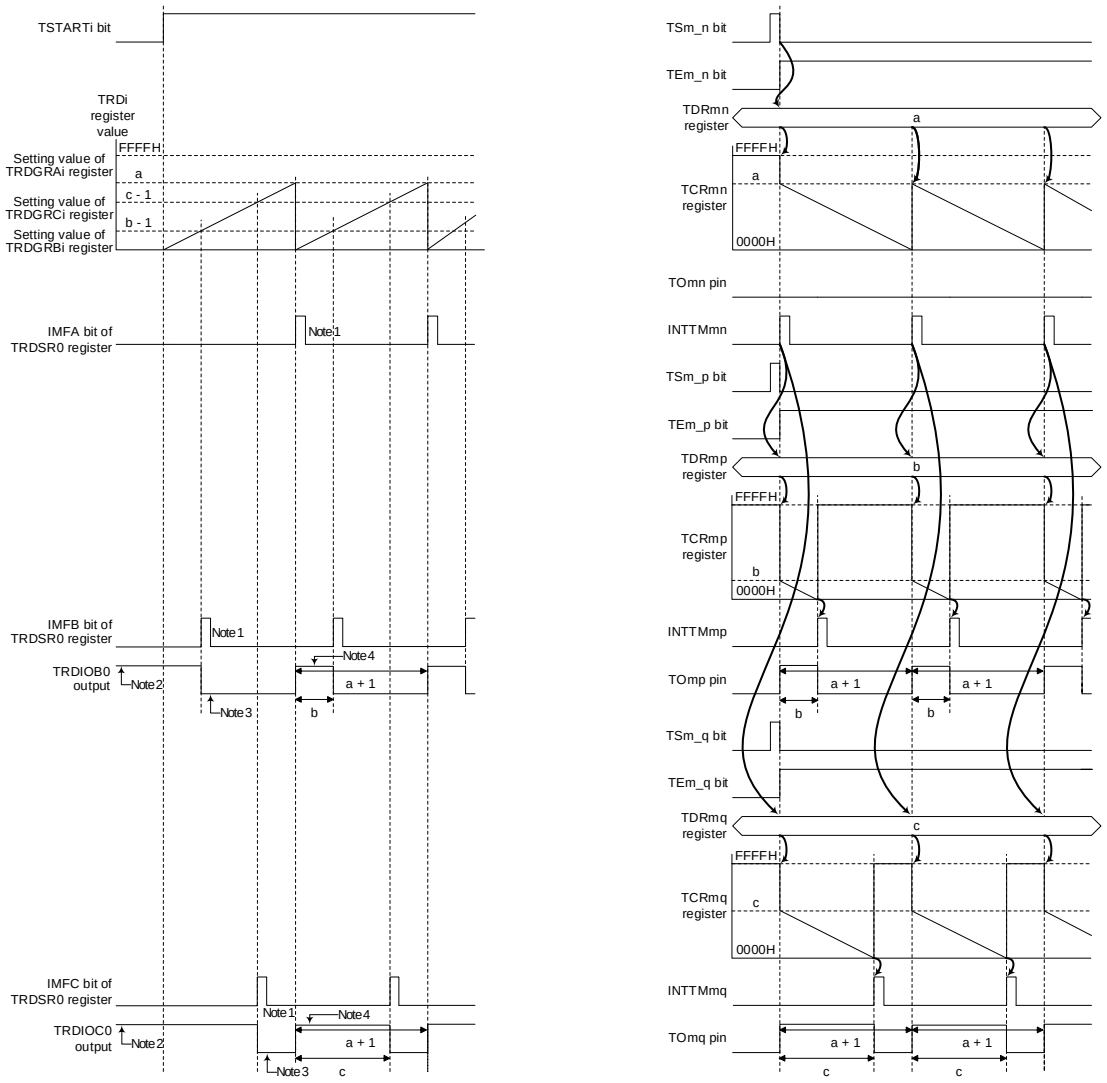
**<Key Points on Porting>**

·**Count mode**

Unlike the timer counter of the TAU in the 78K0R/Fx3, the Timer RD in the RL78/F14 operates as an up counter. Confirm that this difference would not lead to problems.

### 15.3.8 Porting code for TAU (multiple PWM output) over to that for Timer RD (PWM function)

Figure 15-21 shows the comparison of the operation as the timer mode (the PWM function) and that as the multiple PWM output function in the 78K0R/Fx3.




Example of operation as timer mode (PWM function) of Timer RD in RL78/F14 (i = 0, 1)

Example of operation as multiple PWM output function of TAU in 78K0R/Fx3

| Target items for setting | RL78/F14 | 78K0R/Fx3 |
|---|---|---|
| Counter start | TSTARTi bit | TSm_n bit<br>TSm_p bit<br>TSm_q bit |
| Status of timer operation | - | TEm_n bit<br>TEm_p bit<br>TEm_q bit |
| PWM period setting | TRDGRAi register (16 bits) | TDRmn register (16 bits) |
| PWM duty setting | TRDGRBi register (16 bits)<br>TRDGRCi register (16 bits) | TDRmp register (16 bits)<br>TDRmq register (16 bits) |
| Interrupt request | IMFA bit<br>IMFB bit<br>IMFC bit | INTTMmn<br>INTTMmp<br>INTTMmq |
| PWM output pin | TRDIOBi pin<br>TRDIOCi pin | TOmp pin<br>TOmq pin |

Notes 1. Set to “0” by a program.
2. The initial output level remains unchanged until compare match. (The intial output level is high in this figure.)
3. Active level is low.
4. Inactive level is high.

**Figure 15-21 Comparison of operation between timer mode (PWM function) in RL78/F14 and multiple PWM output function in 78K0R/Fx3**

**<Key Points on Porting>**

·**Count mode**

Unlike the timer counter of the TAU in the 78K0R/Fx3, the Timer RD in the RL78/F14 operates as an up counter. Confirm that this difference would not lead to problems.

# 16. Serial interface

The relationship between each communication mode of the serial interface in the RL78/F14 and that in the 78K0R/Fx3 is shown in Figure 16-1 to Figure 16-7, broken down by the number of pins for each product.

## 16.1 100-pin products

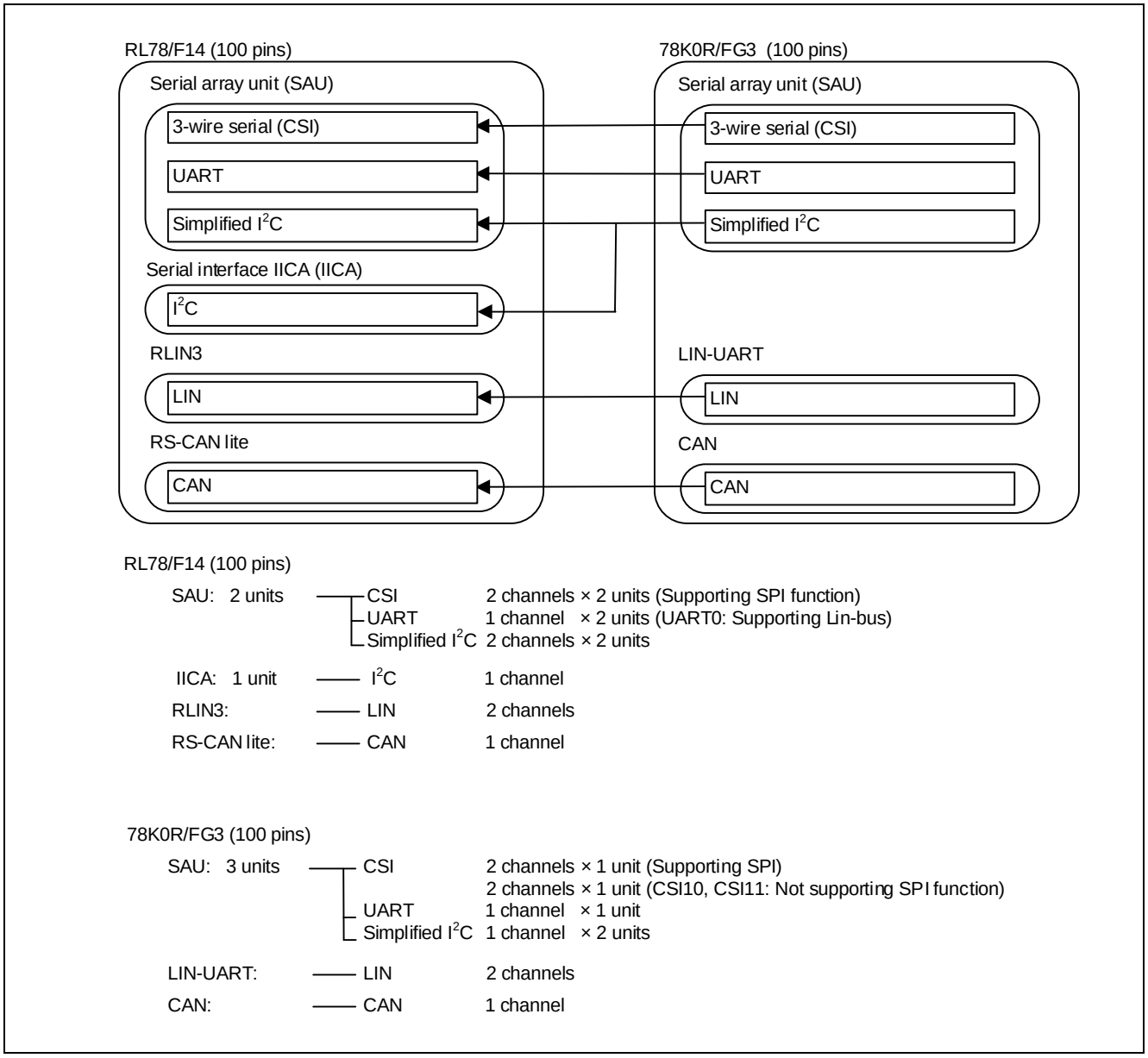
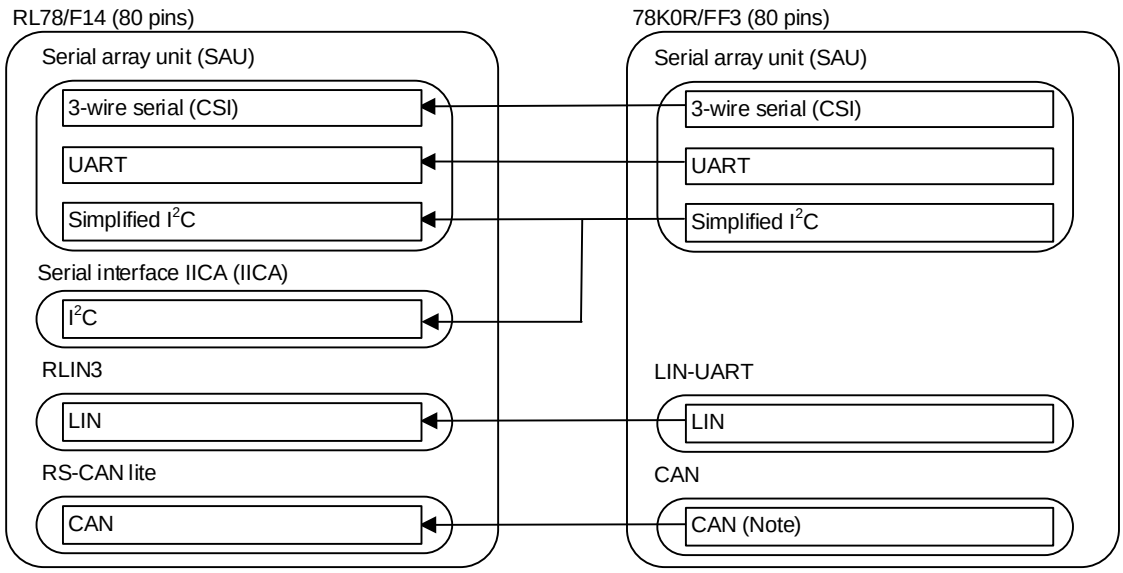



**Figure 16-1 Relationship between each communication mode of serial interface in RL78/F14 (100 pins) and that in 78K0R/FG3**

## 16.2 80-pin products




RL78/F14 (80 pins)

| | | | |
|---|---|---|---|
| SAU: 2 units | CSI | 2 channels × 2 units (Supporting SPI function) | |
| | UART | 1 channel × 2 units (UART0: Supporting Lin-bus) | |
| | Simplified $I^2C$ | 2 channels × 2 units | |
| IICA: 1 unit | $I^2C$ | 1 channel | |
| RLIN3: | LIN | Products with at least 128 Kbytes of code flash memory: | 2 channels |
| | | Products with up to 96 Kbytes of code flash memory: | 1 channel |
| RS-CAN lite: | CAN | 1 channel | |

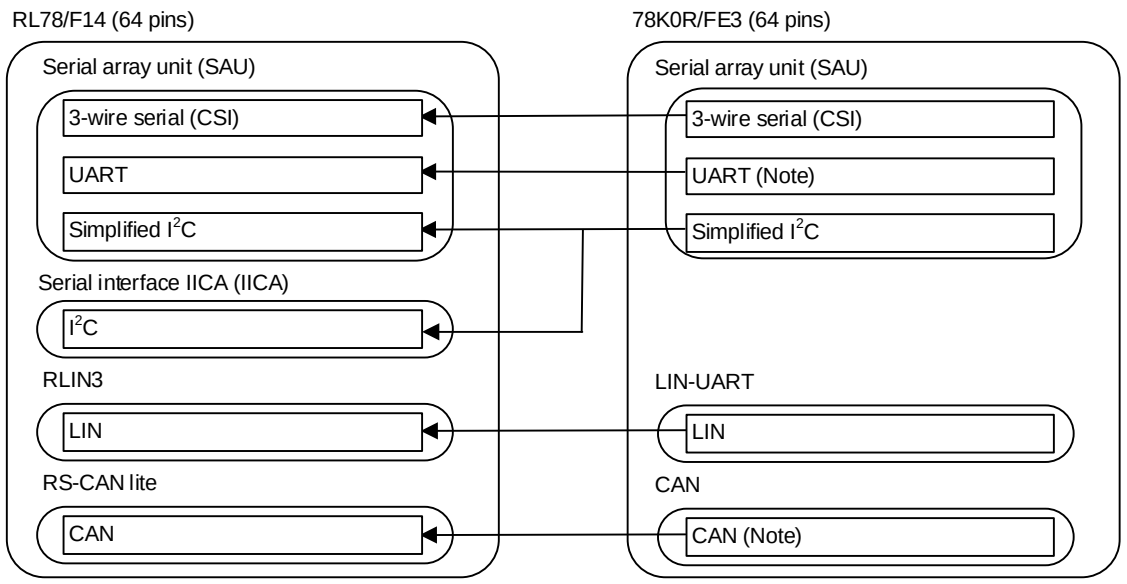
78K0R/FF3 (80 pins)

| | | | |
|---|---|---|---|
| SAU: 3 units | CSI | 2 channels × 1 unit (Supporting SPI) | |
| | | 1 channel × 1 unit (CSI10: Not supporting SPI function) | |
| | UART | 1 channel × 1 unit | |
| | Simplified $I^2C$ | 1 channel × 2 units | |
| LIN-UART: | LIN | 2 channels | |
| CAN: | CAN | 1 channel (Note) | |

Note This communication function is not provided for µPD78F1823-78F1825 products.

**Figure 16-2 Relationship between each communication mode of serial interface in RL78/F14 (80 pins) and that in 78K0R/FF3**

## 16.3 64-pin products




RL78/F14 (64 pins)

| | | | |
|---|---|---|---|
| SAU: 2 units | CSI | 2 channels × 2 units (Supporting SPI function) | |
| | UART | 1 channel × 2 units (UART0: Supporting Lin-bus) | |
| | Simplified $I^2C$ | 2 channels × 2 units | |
| IICA: 1 unit | $I^2C$ | 1 channel | |
| RLIN3: | LIN | Products with at least 128 Kbytes of code flash memory: | 2 channels |
| | | Products with up to 96 Kbytes of code flash memory: | 1 channel |
| RS-CAN lite: | CAN | 1 channel | |

78K0R/FE3 (64 pins)

[µPD78F1821, µPD78F1822, µPD78F1831 to 78F1835]

| | | |
|---|---|---|
| SAU: 3 units | CSI | 2 channels × 1 unit (Supporting SPI) |
| | | 1 channel × 1 unit (CSI10: Not supporting SPI function) |
| | UART | 1 channel × 1 unit |
| | Simplified $I^2C$ | 1 channel × 2 units |
| LIN-UART: | LIN | 2 channels |
| CAN: | CAN | 1 channel |

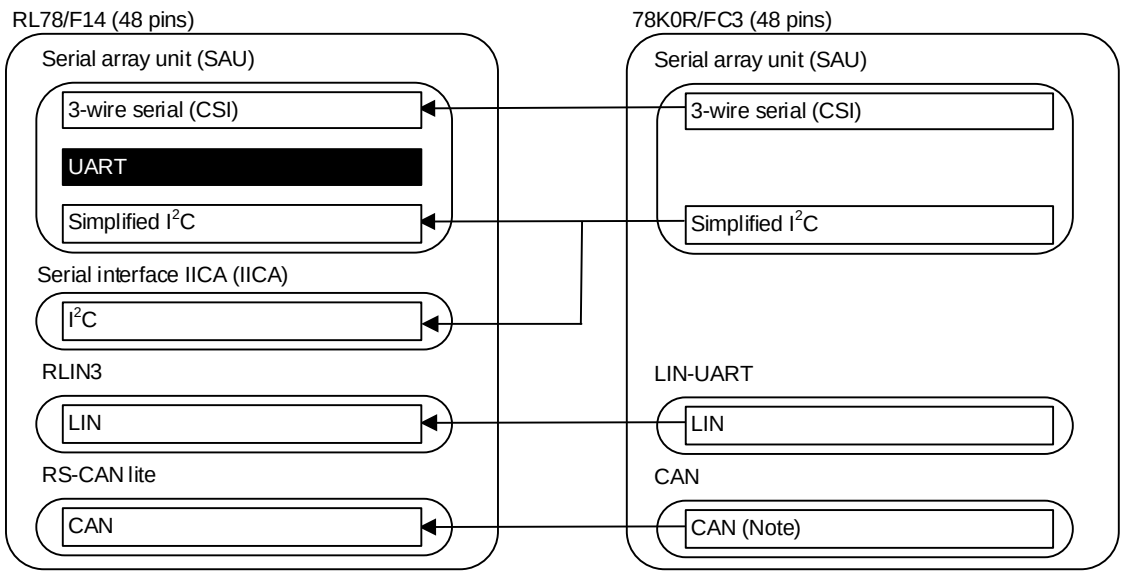
[µPD78F1818 to 78F1820]

| | | |
|---|---|---|
| SAU: 2 units | CSI | 2 channels × 1 unit (Supporting SPI) |
| | | 1 channel × 1 unit (CSI10: Not supporting SPI function) |
| | Simplified $I^2C$ | 1 channel × 1 unit |
| LIN-UART: | LIN | 2 channels |

Note This communication function is not provided for µPD78F1818-78F1820 products.

**Figure 16-3 Relationship between each communication mode of serial interface in RL78/F14 (64 pins) and that in 78K0R/FE3**

## 16.4 48-pin products




The outline characters on a black background indicate inapplicable functions for porting.

RL78/F14 (48 pins)

| | | | |
|---|---|---|---|
| SAU: 2 units | CSI | 2 channels × 2 units (Supporting SPI function) | |
| | UART | 1 channel × 2 units (UART0: Supporting Lin-bus) | |
| | Simplified I2C | 2 channels × 2 units | |
| IICA: 1 unit | I2C | 1 channel | |
| RLIN3: | LIN | Products with at least 128 Kbytes of code flash memory: | 2 channels |
| | | Products with up to 96 Kbytes of code flash memory: | 1 channel |
| RS-CAN lite: | CAN | 1 channel | |

78K0R/FC3 (48 pins)

| | | | |
|---|---|---|---|
| SAU: 2 units | CSI | 1 channel × 1 unit (Supporting SPI) | |
| | | 1 channel × 1 unit (CSI10: Not supporting SPI function) | |
| | Simplified I2C | 1 channel × 1 unit | |
| LIN-UART: | LIN | 2 channels | |
| CAN: | CAN | 1 channel (Note) | |

Note This communication function is not provided for µPD78F1812-78F1817 products.

**Figure 16-4 Relationship between each communication mode of serial interface in RL78/F14 (48 pins) and that in 78K0R/FC3 (48 pins)**

## 16.5 40-pin products

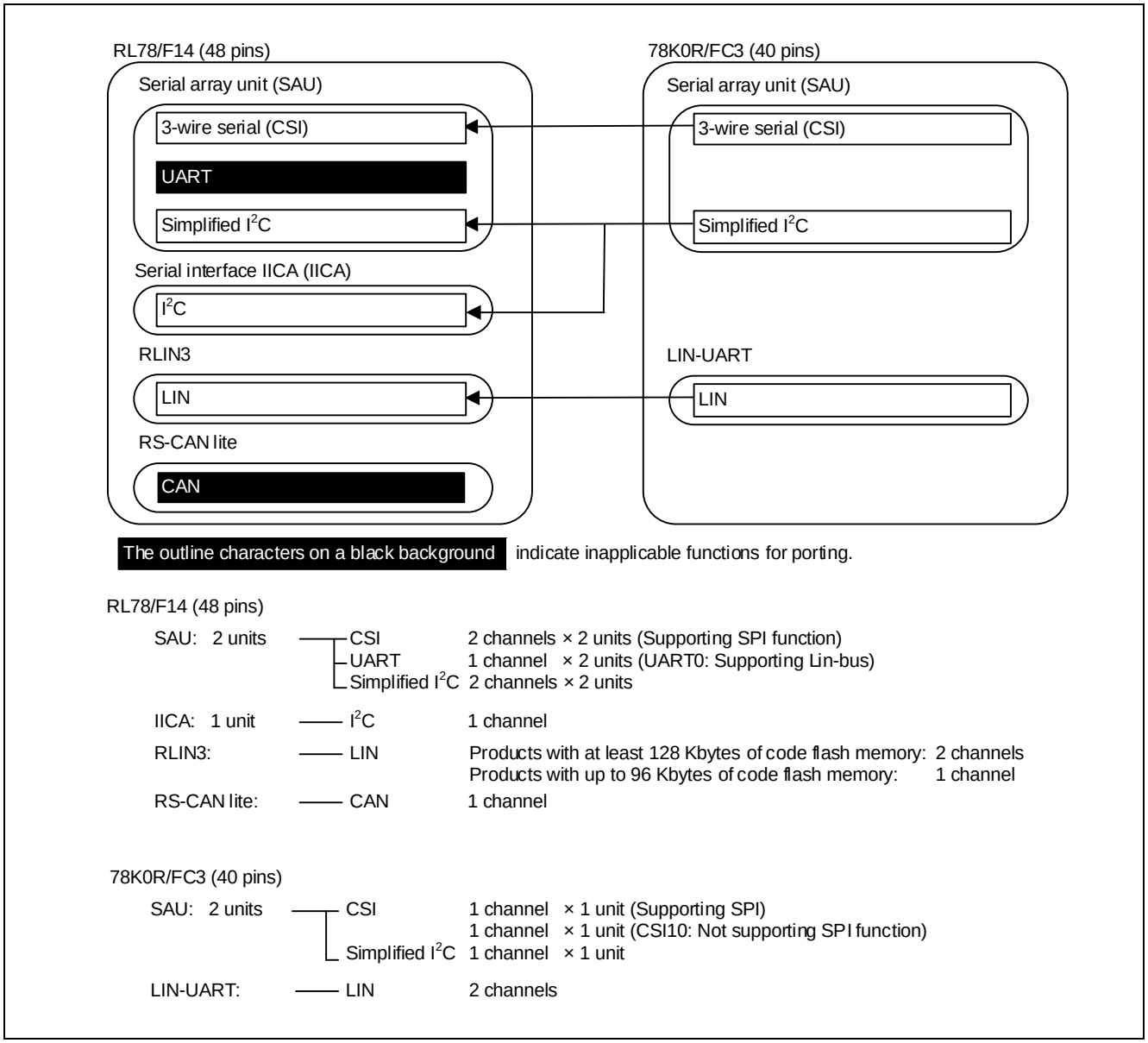
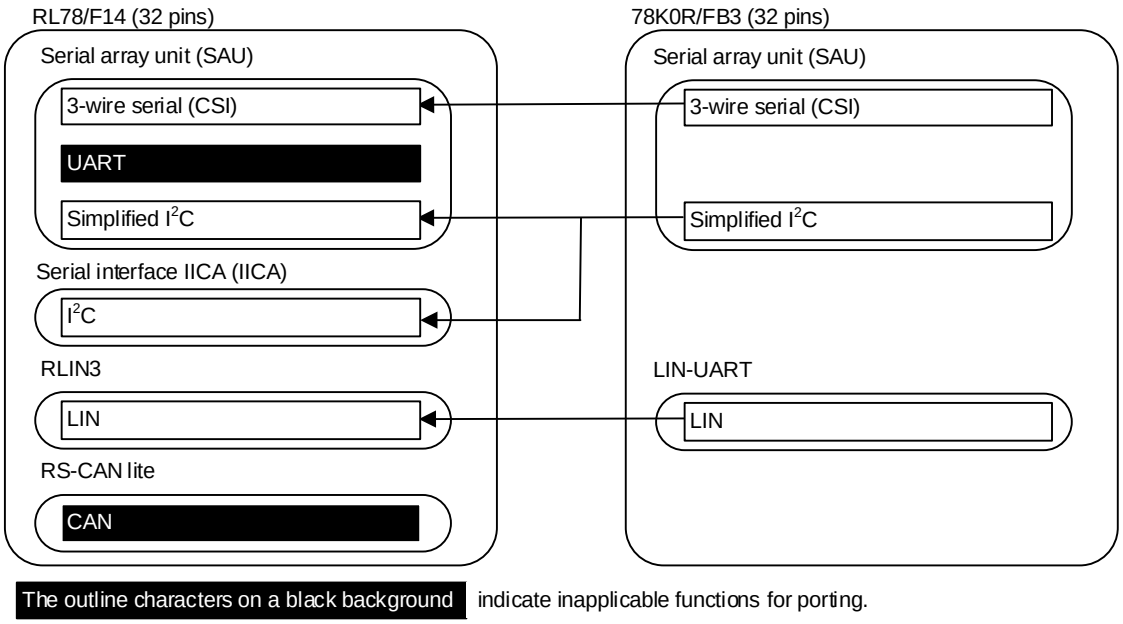



**Figure 16-5 Relationship between each communication mode of serial interface in RL78/F14 (48 pins) and that in 78K0R/FC3 (40 pins)**

## 16.6 32-pin products




The outline characters on a black background indicate inapplicable functions for porting.

RL78/F14 (32 pins)

| | | | |
|---|---|---|---|
| SAU: 2 units | CSI | 2 channels × 1 unit + 1 channel × 1 unit | (Supporting SPI function) |
| | UART | 1 channel × 2 units | (UART0: Supporting Lin-bus) |
| | Simplified $I^2C$ | 2 channels × 1 unit + 1 channel × 1 unit | |
| IICA: 1 unit | $I^2C$ | 1 channel | |
| RLIN3: | LIN | 1 channel | |
| RS-CAN lite: | CAN | 1 channel | |

78K0R/FB3 (32 pins)

| | | | |
|---|---|---|---|
| SAU: 2 units | CSI | 1 channel × 1 unit | (Supporting SPI) |
| | | 1 channel × 1 unit | (CSI10: Not supporting SPI function) |
| | Simplified $I^2C$ | 1 channel × 1 unit | |
| LIN-UART: | LIN | 2 channels | |

**Figure 16-6 Relationship between each communication mode of serial interface in RL78/F14 (32 pins) and that in 78K0R/FB3 (32 pins)**

## 16.7 30-pin products

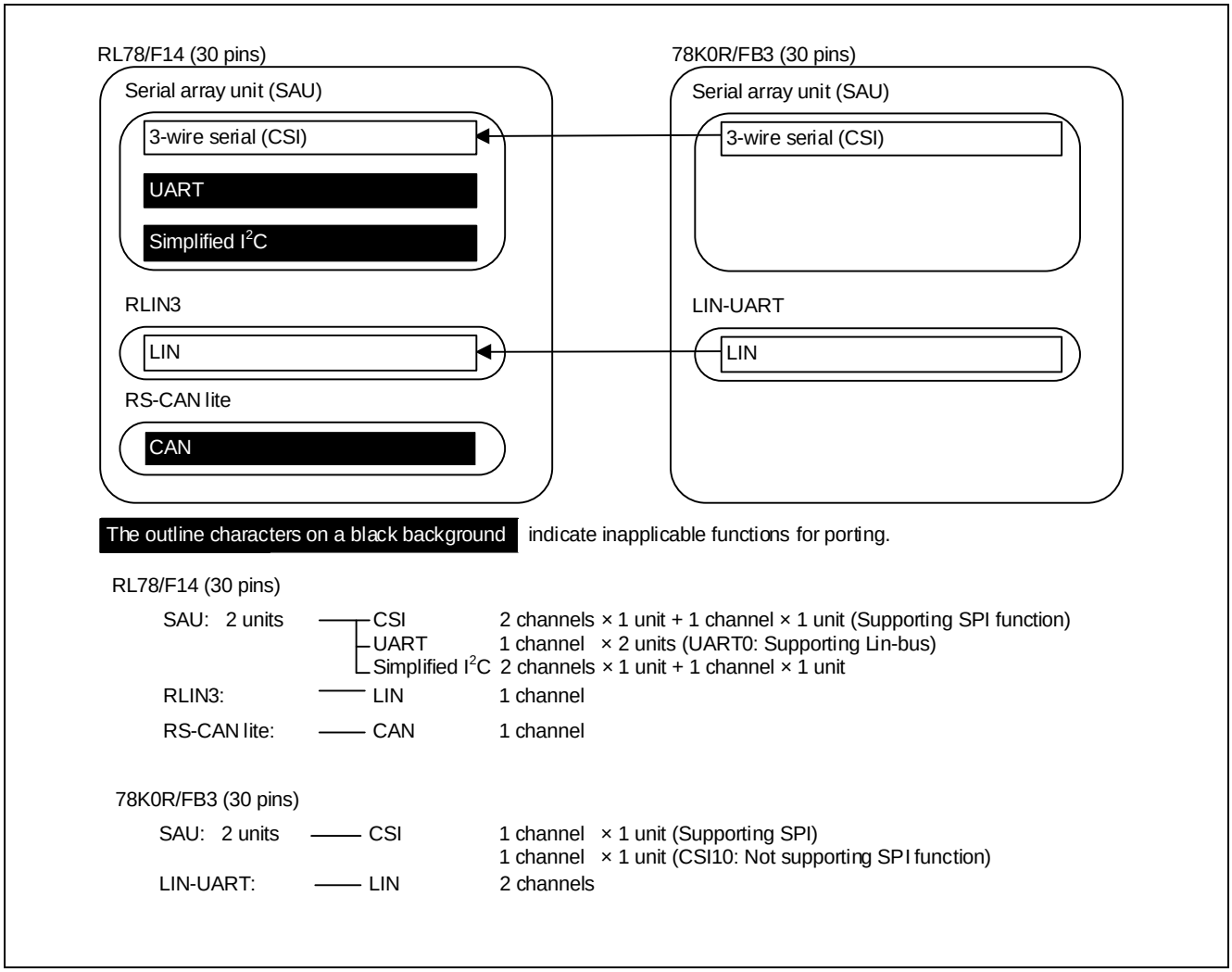
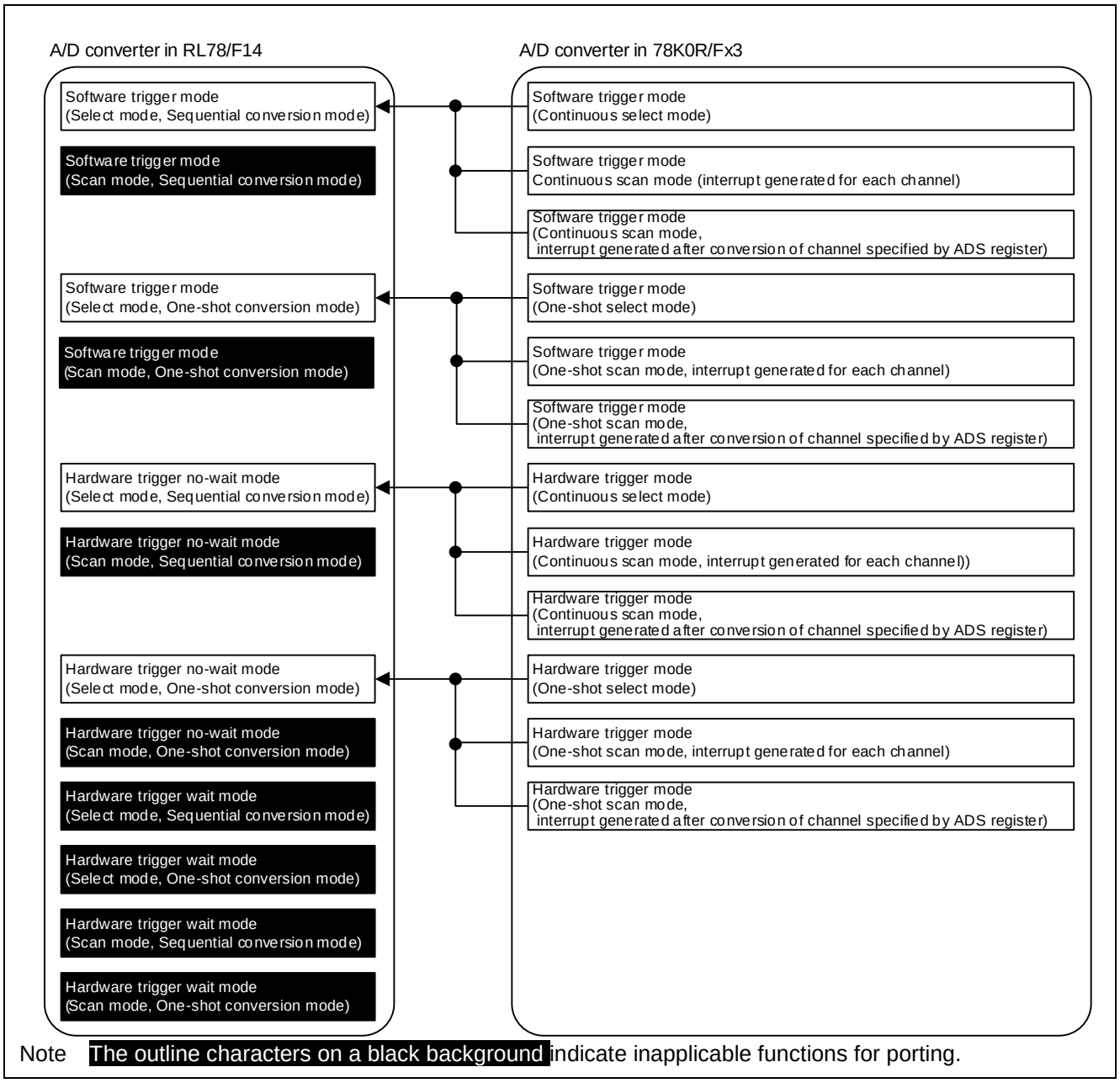



**Figure 16-7 Relationship between each communication mode of serial interface in RL78/F14 (30 pins) and that in 78K0R/FB3 (30 pins)**

## 17. A/D converter

Figure 17-1 shows the relationship between each mode of the A/D converter in the RL78/F14 and that in the 78K0R/Fx3. Also, Table 17-1 and Table 17-2 show the number of the channels and the provided analog input pins of the A/D converter in each product of the RL78/F14 and the 78K0R/Fx3, respectively.

Available channel configuration in the scan mode differs between the RL78/F14 and the 78K0R/Fx3. For this reason, we recommend that you use the select mode in the RL78/F14 when porting the code for the continuous scan mode or the one-shot scan mode in the 78K0R/Fx3.




Note The outline characters on a black background indicate inapplicable functions for porting.

**Figure 17-1 Relationship between each mode of A/D converter in RL78/F14 and that in 78K0R/Fx3**

**Table 17-1 Number of analog input channels and analog input pins of A/D converter in RL78/F14**

| | | 30 pins | 32 pins | 48 pins | | 64 pins | | 80 pins | | 100 pins |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Code flash memory | | Code flash memory | | Code flash memory | | |
| | | | | Up to 96 Kbytes | At least 128 Kbytes | Up to 96 Kbytes | At least 128 Kbytes | Up to 96 Kbytes | At least 128 Kbytes | |
| Number of channels | | 12 | 10 | 15 | 18 | 19 | 20 | 20 | 25 | 31 |
| Analog input pins (●: Provided, -: Not provided) | ANI0 (Note 1) | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI1 (Note 2) | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI2 (Note 3) | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI3 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI4 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI5 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI6 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI7 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI8 | ● | - | ● | ● | ● | ● | ● | ● | ● |
| | ANI9 | ● | - | ● | ● | ● | ● | ● | ● | ● |
| | ANI10 | - | - | ● | ● | ● | ● | ● | ● | ● |
| | ANI11 | - | - | ● | ● | ● | ● | ● | ● | ● |
| | ANI12 | - | - | ● | ● | ● | ● | ● | ● | ● |
| | ANI13 | - | - | - | - | ● | ● | ● | ● | ● |
| | ANI14 | - | - | - | - | ● | ● | ● | ● | ● |
| | ANI15 | - | - | - | - | ● | ● | ● | ● | ● |
| | ANI16 | - | - | - | - | - | ● | - | ● | ● |
| | ANI17 | - | - | - | - | - | - | - | ● | ● |
| | ANI18 | - | - | - | - | - | - | - | - | ● |
| | ANI19 | - | - | - | - | - | - | - | - | ● |
| | ANI20 | - | - | - | - | - | - | - | - | ● |
| | ANI21 | - | - | - | - | - | - | - | - | ● |
| | ANI22 | - | - | - | - | - | - | - | - | ● |
| | ANI23 | - | - | - | - | - | - | - | - | ● |
| | ANI24 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI25 | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| | ANI26 | - | - | - | ● | ● | ● | ● | ● | ● |
| | ANI27 | - | - | - | ● | - | - | ● | ● | ● |
| | ANI28 | - | - | - | ● | - | - | - | ● | ● |
| | ANI29 | - | - | - | - | - | - | - | ● | ● |
| | ANI30 | - | - | - | - | - | - | - | ● | ● |

Notes 1. The ANI0 pin shares the pin with $AV_{REFP}$ pin. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

2. The ANI1 pin shares the pin with $AV_{REFM}$ pin. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

3. The ANI2 pin shares the pin with ANO0 pin. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

**Table 17-2 Number of analog input channels and analog input pins of A/D converter in 78K0R/Fx3**

| | | 78K0R/FB3 | | 78K0R/FC3 | | 78K0R/FE3 | 78K0R/FF3 | 78K0R/FG3 |
|---|---|---|---|---|---|---|---|---|
| | | 30 pins | 32 pins | 40 pins | 48 pins | 64 pins | 80 pins | 100 pins |
| Number of channels | | 8 | 6 | 8 | 11 | 15 | 16 | 24 |
| Analog input pins (●: Provided, -: Not provided) | ANI0 | ● | ● | ● | ● | ● | ● | ● |
| | ANI1 | ● | ● | ● | ● | ● | ● | ● |
| | ANI2 | ● | ● | ● | ● | ● | ● | ● |
| | ANI3 | ● | ● | ● | ● | ● | ● | ● |
| | ANI4 | ● | ● | ● | ● | ● | ● | ● |
| | ANI5 | ● | ● | ● | ● | ● | ● | ● |
| | ANI6 | ● | - | ● | ● | ● | ● | ● |
| | ANI7 | ● | - | ● | ● | ● | ● | ● |
| | ANI8 | - | - | - | ● | ● | ● | ● |
| | ANI9 | - | - | - | ● | ● | ● | ● |
| | ANI10 | - | - | - | ● | ● | ● | ● |
| | ANI11 | - | - | - | - | ● | ● | ● |
| | ANI12 | - | - | - | - | ● | ● | ● |
| | ANI13 | - | - | - | - | ● | ● | ● |
| | ANI14 | - | - | - | - | ● | ● | ● |
| | ANI15 | - | - | - | - | - | ● | ● |
| | ANI16 | - | - | - | - | - | - | ● |
| | ANI17 | - | - | - | - | - | - | ● |
| | ANI18 | - | - | - | - | - | - | ● |
| | ANI19 | - | - | - | - | - | - | ● |
| | ANI20 | - | - | - | - | - | - | ● |
| | ANI21 | - | - | - | - | - | - | ● |
| | ANI22 | - | - | - | - | - | - | ● |
| | ANI23 | - | - | - | - | - | - | ● |

**<Key Points on Porting>**

**·Analog reference voltage and number of analog input pins**

The reference voltage input pin in the 78K0R/Fx3 is the $AV_{REF}$ pin, which is dedicated to the analog reference voltage input. On the other hand, in the RL78/F14, two pins are necessary for the analog reference voltage input, namely the $AV_{REFP}$ pin (a reference voltage (+ side) input pin) and the $AV_{REFM}$ pin (a reference voltage (- side) input pin). These two pins are also used as analog input pins, namely ANI0 and ANI1, respectively. In order to realize the A/D conversion accuracy with an acceptable error range of ±3 LSB in the RL78/F14, the reference voltage should be applied to the $AV_{REFM}$ pin and the $AV_{REFP}$ pin. In this case, ANI0 and ANI1 are not available, which means that the number of analog input pins with an acceptable error range of ±3 LSB decreases by 2. In the case of porting from the 78K0R/Fx3, the available number of the analog input pins is sufficient; however, the range of those pins differs so confirm that the difference would not lead to problems.

**·D/A converter and number of analog input pins**

In the RL78/F14, the pin which the D/A converter uses as the analog output pin (ANO0) is also used as the analog input pin (ANI2). The analog output performed by the D/A converter decreases the number of analog input pins with an acceptable error range of ±3 LSB by 1. Confirm that using the D/A converter would not lead to problems such as a shortage of analog input pins.

**·A/D conversion accuracy**

The analog pins in the RL78/F14 are classified as $V_{DD}$ system analog pins and $EV_{DD}$ system analog pins as shown in Table 17-3. Since the $EV_{DD}$ system analog pins have lower accuracy than the $V_{DD}$ system analog pins, the $V_{DD}$ system analog pins should be used for highly accurate conversion.

Table 17-4 shows the comparison of the A/D conversion accuracy between the RL78/F14 and the 78K0R/Fx3.

Since the products with up to 48 pins are not equipped with $EV_{DD0}$ pin or $EV_{DD1}$ pin, these products use $V_{DD}$ as power supply for the $EV_{DD}$ system analog pins. However the A/D conversion accuracy of the $EV_{DD}$ system analog pins remains ±4.5 LSB (MAX.: $4.0V \leq V_{DD} \leq 5.5V$) as shown in the user's manual.

**Table 17-3 $V_{DD}$ system analog pins and $EV_{DD}$ system analog pins in RL78/F14**

| Analog input pins | 30 pins | 32 pins | 48 pins | | 64 pins | | 80 pins | | 100 pins |
|---|---|---|---|---|---|---|---|---|---|
| | | | Code flash memory | | Code flash memory | | Code flash memory | | |
| | | | Up to 96 Kbytes | At least 128 Kbytes | Up to 96 Kbytes | At least 128 Kbytes | Up to 96 Kbytes | At least 128 Kbytes | |
| $V_{DD}$ system analog input pins | ANI0-ANI9 | ANI0-ANI7 | ANI0-ANI12 | ANI0-ANI12 | ANI0-ANI15 | ANI0-ANI16 | ANI0-ANI15 | ANI0-ANI17 | ANI0-ANI23 |
| $EV_{DD}$ system analog input pins | ANI24, ANI25 | ANI24, ANI25 | ANI24, ANI25 | ANI24-ANI28 | ANI24-ANI26 | ANI24-ANI26 | ANI24-ANI27 | ANI24-ANI30 | ANI24-ANI30 |

**Table 17-4 Comparison of A/D conversion accuracy between RL78/F14 and 78K0R/Fx3**

| | Reference voltage | A/D conversion accuracy | |
|---|---|---|---|
| | | $V_{DD}$ system analog pins (Note 1) | $EV_{DD}$ system analog pins (Note 1) |
| RL78/F14 | $AV_{REF}$ (+) = $AV_{REFP}$/ANI0<br>$AV_{REF}$ (-) = $AV_{REFM}$/ANI1 | ±3.0 LSB (Note 2) | ±4.5 LSB |
| | $AV_{REF}$ (+) = $V_{DD}$<br>$AV_{REF}$ (-) = $V_{SS}$ | ±5.0 LSB | ±6.5 LSB |
| 78K0R/Fx3 | $AV_{REF}$, $AV_{SS}$ | ±3.0 LSB | - |

Notes 1. For the $V_{DD}$ system analog input pins and the $EV_{DD}$ system analog input pins provided for each product of the RL78/F14, see **Table 17-3**.

2. The two pins used as the ANI0 and the ANI1 pin are also used as the $AV_{REFP}$ pin and the $AV_{REFM}$ pin, respectively. Under this condition, the ANI0 pin and the ANI1 pin are not available because these two pins are used as the A/D converter reference voltage input pins of the $AV_{REFP}$ pin and the $AV_{REFM}$ pin.

**·Porting code for continuous scan mode in 78K0R/Fx3 over to that for select mode in RL78/F14**

As shown in Table 17-5, the specified range of the ANI pins to be A/D converted in the scan mode differs between the RL78/F14 and the 78K0R/Fx3. Therefore we recommend that you determine the assignment of the analog input pins first when doing overall system pin assignment.

When porting code which uses the scan mode in the 78K0R/Fx3 over to that in the RL78/F14 is done, the A/D conversion time will increase when the range of ANI pins to be converted is not a multiple of 4. This is due to having to perform A/D conversion on the inputs of the unnessesary channels as well.

If such A/D conversion time leads to problems, examine a way of porting the code using the scan mode in the 78K0R/Fx3 over to that using the select mode in the RL78/F14.

**Table 17-5 Comparison of analog input channel specification registers between RL78/F14 and 78K0R/Fx3**

| | RL78/F14 (100 pins) | | | | | | | | | | | | | | | | | | | | | | | | | | | 78K0R/Fx3 (100 pins) | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS4-0 | Select mode | Scan mode | | | | | | | | | | | | | | | | | | | | | | | | | | Select mode | Scan mode | | | | | | | | | | | | | | | | | | | | | | | | |
| | | ANI0 (Note 1) | ANI1 (Note 2) | ANI2 (Note 3) | ANI3 | ANI4 | ANI5 | ANI6 | ANI7 | ANI8 | ANI9 | ANI10 | ANI11 | ANI12 | ANI13 | ANI14 | ANI15 | ANI16 | ANI17 | ANI18 | ANI19 | ANI20 | ANI21 | ANI22 | ANI23 | | ANI0 | ANI1 | ANI2 | ANI3 | ANI4 | ANI5 | ANI6 | ANI7 | ANI8 | ANI9 | ANI10 | ANI11 | ANI12 | ANI13 | ANI14 | ANI15 | ANI16 | ANI17 | ANI18 | ANI19 | ANI20 | ANI21 | ANI22 | ANI23 |
| 00000B | ANI0 (Note 1) | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 00001B | ANI1 (Note 2) | | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | | | ANI1 | ● | ● | | | | | | | | | | | | | | | | | | | | | | | |
| 00010B | ANI2 (Note 3) | | | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | | ANI2 | ● | ● | ● | | | | | | | | | | | | | | | | | | | | | | |
| 00011B | ANI3 | | | | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | ANI3 | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | | | | |
| 00100B | ANI4 | | | | | ● | ● | ● | ● | | | | | | | | | | | | | | | | | ANI4 | ● | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | | | |
| 00101B | ANI5 | | | | | | ● | ● | ● | ● | | | | | | | | | | | | | | | | ANI5 | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | | |
| 00110B | ANI6 | | | | | | | ● | ● | ● | ● | | | | | | | | | | | | | | | ANI6 | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | | | | | | |
| 00111B | ANI7 | | | | | | | | ● | ● | ● | ● | | | | | | | | | | | | | | ANI7 | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | | | | | |
| 01000B | ANI8 | | | | | | | | | ● | ● | ● | ● | | | | | | | | | | | | | ANI8 | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | | | | |
| 01001B | ANI9 | | | | | | | | | | ● | ● | ● | ● | | | | | | | | | | | | ANI9 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | | | |
| 01010B | ANI10 | | | | | | | | | | | ● | ● | ● | ● | | | | | | | | | | | ANI10 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | | |
| 01011B | ANI11 | | | | | | | | | | | | ● | ● | ● | ● | | | | | | | | | | ANI11 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | | |
| 01100B | ANI12 | | | | | | | | | | | | | ● | ● | ● | ● | | | | | | | | | ANI12 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | | |
| 01101B | ANI13 | | | | | | | | | | | | | | ● | ● | ● | ● | | | | | | | | ANI13 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | | |
| 01110B | ANI14 | | | | | | | | | | | | | | | ● | ● | ● | ● | | | | | | | ANI14 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | | |
| 01111B | ANI15 | | | | | | | | | | | | | | | | ● | ● | ● | ● | | | | | | ANI15 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | | |
| 10000B | ANI16 | | | | | | | | | | | | | | | | | ● | ● | ● | ● | | | | | ANI16 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | | |
| 10001B | ANI17 | | | | | | | | | | | | | | | | | | ● | ● | ● | ● | | | | ANI17 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | | |
| 10010B | ANI18 | | | | | | | | | | | | | | | | | | | ● | ● | ● | ● | | | ANI18 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | | |
| 10011B | ANI19 | | | | | | | | | | | | | | | | | | | | ● | ● | ● | ● | | ANI19 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | | |
| 10100B | ANI20 | | | | | | | | | | | | | | | | | | | | | ● | ● | ● | ● | ANI20 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | | |
| 10101B | ANI21 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI21 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | | |
| 10110B | ANI22 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI22 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | | |
| 10111B | ANI23 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI23 | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| 11000B | ANI24 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 11001B | ANI25 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 11010B | ANI26 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 11011B | ANI27 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 11100B | ANI28 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 11101B | ANI29 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| 11110B | ANI30 | - | | | | | | | | | | | | | | | | | | | | | | | | ANI0 | ● | | | | | | | | | | | | | | | | | | | | | | | | |

●: The analog input pins specified as the scan targets in the scan mode.

- : The setting conditions which are not supported by the target products on this application note.

Notes 1. The ANI0 pin shares the pin with $AV_{REFP}$ pin. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

2. The ANI1 pin shares the pin with $AV_{REFM}$ pin. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

3. The ANI2 pin shares the pin with ANO0 pin. Confirm that it would not lead to problems when you examine the specifications of your products or systems.

## 18. References

References documents for this application note are shown below. Be sure to obtain the latest version of each document from the website of Renesas Electronics Corporation when designing.

・RL78/ F13, F14 User's Manual: Hardware Rev. 2.10

・78K0R/Fx3 User's Manual: Hardware Rev. 6.00

・E1/E20/E2 Emulator, E2 Emulator Lite Additional Document for User's Manual

(Notes on Connection of RL78) Rev.7.00

・QB-MINI2 User's Manual Rev.6.00

・RL78 family User's Manual: Software Rev.2.20

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## Revision History

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| Rev. 1.10 | June 30, 2017 | | First edition issued |
| Rev. 2.00 | Oct. 31, 2017 | Throughout | Fully revised for expanding target devices: 78K0R/FB3 (30, 32 pins), 78K0R/FC3 (40, 48 pins), 78K0R/FE3 (64 pins), 78K0R/FF3 (80 pins), 78K0R/FG3 (100 pins), and RL78/F14 (30, 32, 48, 64, 80, 100 pins) |
| | | p.6 to p.19 | 1.1 to 1.7,<br>Tables added for comparing functions between RL78/F14 and 78K0R/Fx3, broken down by number of pins for each product |
| | | p.26 to p.38 | 3.2.1 to 3.2.7,<br>Tables added for comparing pin functions between RL78/F14 and 78K0R/Fx3, broken down by number of pins for each product |
| | | p.39 | Table 4-1 and Table 4-2 added for comparing memory size between each product of RL78/F14 and 78K0R/Fx3, respectively |
| | | p.42 | Table 5-1 modified for classifying each register status except "Held" when reset request is generated into "Cleared" or "Set" |
| | | p.57 to p.59 | 11.1.1 to 11.1.7,<br>Tables added for comparing I/O ports between RL78/F14 and 78K0R/Fx3, broken down by number of pins for each product |
| | | p.62 | Table 11-10 and Table 11-11 added for showing Pin I/O buffer power supplies for each product of RL78/F14 and 78K0R/Fx3, respectively |
| | | p.92 to p.94 | Description of counter source for Timer RD (Table 15-9) moved from 15.3.8 to 15.3 |
| | | p.103 | Figure 15-21 corrected for changing position of Note3 and Note 4 |
| | | p.105 to p.111 | 16.1 to 16.7,<br>Description added for showing relationship between each serial interface in RL78/F14 and that in 78K0R/Fx3, broken down by number of pins for each product |

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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**Renesas Electronics America Inc.**
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

**Renesas Electronics Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

**Renesas Electronics Taiwan Co., Ltd.**
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141




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