RL78/F13, F14, RL78/F15

Porting Guide from M16C/5M, 57 to RL78/F13, F14, F15

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Abstract

The RL78/F13, F14 and RL78/F15 products are the successors of the M16C/5M and M16C/57 groups. This application note provides information on porting from M16C/5M, 57 products that you are currently using to the RL78/F13, F14, F15 products that can replace the M16C/5M, 57 products. This application note also provides information on those functions of the RL78/F13, F14, F15 products that can replace the functions of the M16C/5M, 57 products.

For details on each product, refer to the user's manual of the product.

Target Devices

The 64-pin, 80-pin, and 100-pin products shown below are the target devices.

- M16C/5M, M16C/57
- RL78/F13, F14
- RL78/F15

Contents

1. Product Memory/Package Comparison

The lineup of the M16C/5M, 57 products is shown in Table 1-1, broken down by the pin count, memory size, and CAN channel count of each product. Also, the lineup of the RL78/F13, F14, F15 products that can replace the M16C/5M, 57 products is shown in Table 1-2 to Table 1-4.

1.1 M16C/5M, 57 Product Lineup

Table 1-1 M16C/5M, 57 Products and Replacement Products (RL78/F13, F14, F15) (1)

Memory				100-pin products		
Code flash	Data flash	E²dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
256 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	20 KB	R5F3571E	R5F35M1E	R5F35MAE
		-		R5F3576E	R5F35M6E	R5F35MDE
128 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	12 KB	R5F35716	R5F35M16	R5F35MA6
		-		R5F35766	R5F35M66	R5F35MD6
Replacement products				RL78/F14	RL78/F14	RL78/F15

Table 1-1 M16C/5M, 57 Products and Replacement Products (RL78/F13, F14, F15) (2)

Memory				80-pin products		
Code flash	Data flash	E²dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
256 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	20 KB	R5F3572E	R5F35M2E	R5F35MBE
		-		R5F3577E	R5F35M7E	R5F35MEE
128 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	12 KB	R5F35726	R5F35M26	R5F35MB6
		-		R5F35776	R5F35M76	R5F35ME6
96 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	8 KB	R5F35723	R5F35M23	R5F35MB3
		-		R5F35773	R5F35M73	R5F35ME3
Replacement products				RL78/F13, F14	RL78/F13, F14	RL78/F15

Table 1-1 M16C/5M, 57 Products and Replacement Products (RL78/F13, F14, F15) (3)

Memory				64-pin products		
Code flash	Data flash	E²dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
256 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	20 KB	R5F3573E	R5F35M3E	R5F35MCE
		-		R5F3578E	R5F35M8E	R5F35MFE
128 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	12 KB	R5F35736	R5F35M36	R5F35MC6
		-		R5F35786	R5F35M86	R5F35MF6
96 KB + 16 KB Note 1	4 KB × 2 Note 2	4 KB	8 KB	R5F35733	R5F35M33	R5F35MC3
		-		R5F35783	R5F35M83	R5F35MF3
Replacement products				RL78/F13, F14	RL78/F13, F14	RL78/F15

Notes: 1. Program ROM1 (256 KB/128 KB/ 96 KB) + Program ROM2 (16 KB)

2. Data flash in the M16C/5M, 57 products does not support the background operation (BGO) function.

1.2 Replacement Product Lineup (RL78/F13, F14, F15)

Table 1-2 Replacement Product Lineup (RL78/F13) (1)

Memory				80-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
128 KB	4 KB	-	8 KB	R5F10AMG	R5F10BMG	-
96 KB	4 KB	-	6 KB	R5F10AMF	R5F10BMF	-

Table 1-2 Replacement Product Lineup (RL78/F13) (2)

Memory				64-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
128 KB	4 KB	-	8 KB	R5F10ALG	R5F10BLG	-
96 KB	4 KB	-	6 KB	R5F10ALF	R5F10BLF	-

Table 1-3Replacement Product Lineup (RL78/F14) (1)

Memory				100-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
256 KB	8 KB	-	20 KB	-	R5F10PPJ	-
192 KB	8 KB	-	16 KB	-	R5F10PPH	-
128 KB	8 KB	-	10 KB	-	R5F10PPG	-

Table 1-3 Replacement Product Lineup (RL78/F14) (2)

Memory				80-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
256 KB	8 KB	-	20 KB	-	R5F10PMJ	-
192 KB	8 KB	-	16 KB	-	R5F10PMH	-
128 KB	8 KB	-	10 KB	-	R5F10PMG	-
96 KB	4 KB	-	8 KB	-	R5F10PMF	-

Table 1-3 Replacement Product Lineup (RL78/F14) (3)

Memory				64-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
256 KB	8 KB	-	20 KB	-	R5F10PLJ	-
192 KB	8 KB	-	16 KB	-	R5F10PLH	-
128 KB	8 KB	-	10 KB	-	R5F10PLG	-
96 KB	4 KB	-	8 KB	-	R5F10PLF	-

Table 1-4 Replacement Product Lineup (RL78/F15) (1)

Memory				100-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
512 KB	16 KB	-	32 KB	-	-	R5F113PL
384 KB	16 KB	-	26 KB	-	-	R5F113PK
256 KB	8 KB	-	20 KB	-	-	R5F113PJ
192 KB	8 KB	-	16 KB	-	-	R5F113PH
128 KB	8 KB	-	10 KB	-	-	R5F113PG

Table 1-4 Replacement Product Lineup (RL78/F15) (2)

Memory				80-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
512 KB	16 KB	-	32 KB	-	-	R5F113ML
384 KB	16 KB	-	26 KB	-	-	R5F113MK

Table 1-4 Replacement Product Lineup (RL78/F15) (3)

Memory				64-pin products		
Code flash	Data flash	E^2dataFlash	RAM	CAN: N/A	CAN: 1 ch	CAN: 2 ch
512 KB	16 KB	-	32 KB	-	-	R5F113LL
384 KB	16 KB	-	26 KB	-	-	R5F113LK

Remarks: 1. Data flash in the RL78/F13, F14, F15 products supports the background operation (BGO) function.
2. Besides the products listed above, the RL78/F13, F14, F15 products with different packages and memory size are also available. For details, refer to the User's Manual: Hardware of the applicable product.

2. Product Feature Comparison

Table 2-1 to Table 2-3 compare the features of the M16C/5M, 57 products with the counterparts of the RL78/F13, F14, F15 products, broken down by their packages. Please use it as a reference when porting. For details on each feature, refer to the user's manual.

2.1 100-pin Products

Table 2-1 Feature Comparison between 100-pin Products of M16C/5M, 57 and RL78/F14, F15

Items	M16C/5M, 57 (100 pins)	RL78/F14 (R5F10PPx)	RL78/F15 (R5F113Px)
CPU	M16C/60 CPU core, 32 MHz (Max.)	RL78 CPU core, 32 MHz (Max.) • Grade L: 32 MHz (Max.) • Grade K, Y: 24 MHz (Max.)	RL78 CPU core, 32 MHz (Max.) • Grade L: 32 MHz (Max.) • Grade K: 24 MHz (Max.)
Memory	Code flash: 256/128 KB Data flash: 4 KB × 2 E^2dataFlash: 4 KB/- RAM: 20/12 KB	Code flash: 256/192/128/96 Note/64 Note KB Data flash: 8/4 Note KB RAM: 20/16/10/8 Note/6 Note KB	Code flash: 512/384/256/192/128 KB Data flash: 16/8 KB RAM: 32/26/20/16/10 KB
Voltage detection	Power-on reset, Voltage detection circuit	Power-on reset, Voltage detection circuit	Power-on reset, Voltage detection circuit
I/O ports	CMOS I/O: 87 N-channel open drain: 1	CMOS I/O: 86 Input only: 5 Output only: 1	CMOS I/O: 86 Input only : 5 Output only: 1
Clock	XIN, XCIN, PLL, 40 MHz OCO, 125 kHz OCO	X1, PLL, High-speed OCO, XT1, Low-speed OCO	X1, PLL, High-speed OCO, XT1, Low-speed OCO
External interrupt inputs	$\overline{INT}$ × 8 ch, Key input × 4 ch	INTP × 14 ch, Key input × 8 ch	INTP × 14 ch, Key input × 8 ch
Watchdog timer	15-bit timer × 1 (with prescaler) (Selectable count source: Dedicated 125 kHz OCO or CPU clock)	17-bit timer × 1 (Count source: Dedicated low-speed OCO)	17-bit timer × 1 (Count source: Dedicated low-speed OCO)
DMA/DTC	DMA : 4 ch	DTC : 1 unit	DTC : 1 unit
Timer	Timer A: 16-bit timer × 5 ch (Timer mode, Event counter mode, One-shot timer mode, Pulse-width modulation (PWM) mode, Programmable output mode) Timer B: 16-bit timer × 6 ch (Timer mode, Event counter mode, Pulse frequency measurement mode, Pulse-width measurement mode) Three-phase motor control timer × 1 ch (Timers A1, A2, A4, and B2 used) Timer S: 16-bit timer × 1 ch (Input capture/Output compare: 8 ch) Task monitoring timer: 16-bit timer × 1 ch Real-time clock × 1 ch	TAU: 16-bit timer (8 ch × 2) (Interval timer, Square wave output, External event counter, Divider function, Input pulse interval measurement, Measurement of high-/low-level width of input signal, Delay counter, One-shot pulse output, PWM output, Multiple PWM output) Timer RJ: 16-bit timer × 1 (Timer mode, Pulse output mode, Event counter mode, Pulse width measurement mode, Pulse period measurement mode) Timer RD: 16-bit timer × 2 (Timer mode (Input capture/Output compare/PWM function), Reset synchronous PWM mode, Complementary PWM mode, PWM3 mode) Real-time clock × 1 ch	TAU: 16-bit timer (8 ch × 2) (Interval timer, Square wave output, External event counter, Divider function, Input pulse interval measurement, Measurement of high-/low-level width of input signal, Delay counter, One-shot pulse output, PWM output, Multiple PWM output) Timer RJ: 16-bit timer × 1 (Timer mode, Pulse output mode, Event counter mode, Pulse width measurement mode, Pulse period measurement mode) Timer RD: 16-bit timer × 2 (Timer mode (Input capture/Output compare/PWM function), Reset synchronous PWM mode, Complementary PWM mode, PWM3 mode) Real-time clock × 1 ch
Serial interface	UART0, 1, 3, 4 (UART mode, Clock synchronous serial I/O mode) UART2 (UART mode, Clock synchronous serial I/O mode, I^2C mode, IE mode, SIM mode) Multi-master I^2C-bus Interface: 1 ch Serial Bus Interface: 1 ch (Clock synchronous serial communication mode, 4-wire bus communication mode)	SAU: 2 units (CSI: 4 ch, UART: 2 ch, Simplified I^2C: 4 ch, LIN: 1 ch) Multi-master I^2C (IICA): 1 ch LIN/UART (RLIN3): 2 ch	SAU: 3 units (CSI: 6 ch, UART: 3 ch Simplified I^2C: 4 ch, LIN: 1 ch) Multi-master I^2C (IICA): 1 ch LIN/UART (RLIN3): 3 ch IEBus controller: 1 ch
LIN module	1 ch (Master only)	2 ch (Master/Slave)	3 ch (Master/Slave)
CAN module	2/1/0 ch	1 ch	2 ch
A/D converter	10-bit resolution: 26 ch	10-bit resolution: 31 ch	10-bit resolution: 31 ch
D/A converter	8-bit resolution: 1 ch	8-bit resolution: 1 ch	8-bit resolution: 1 ch
Comparator	-	1 ch	1 ch
Operating temperature	J-version: -40 to +85°C K-version:-40 to +125°C	Grade L: -40 to +105°C Grade K: -40 to +125°C Grade Y: -40 to +150°C	Grade L: -40 to +105°C Grade K: -40 to +125°C
Package	100-pin LQFP	100-pin LQFP	100-pin LQFP

Note: Not provided for the replacement products.

2.2 80-pin Products

Table 2-2 Feature Comparison between 80-pin Products of M16C/5M, 57 and RL78/F13, F14, F15

Items	M16C/5M, 57 (80 pins)	RL78/F13, F14 (R5F10AMx, R5F10BMx, R5F10PMx)	RL78/F15 (R5F113Mx)
CPU	M16C/60 CPU core, 32 MHz (Max.)	RL78 CPU core, 32 MHz (Max.) ● Grade L: 32 MHz (Max.) ● Grade K, Y: 24 MHz (Max.)	RL78 CPU core, 32 MHz (Max.) ● Grade L: 32 MHz (Max.) ● Grade K: 24 MHz (Max.)
Memory	Code flash: 256/128/96 KB Data flash: 4 KB × 2 E^2dataFlash: 4 KB/- RAM: 20/12/8 KB	Code flash: 256/192/128/96/64 Note KB Data flash: 8/4 KB RAM: 20/16/10/8/6/4 Note KB	Code flash: 512/384 KB Data flash: 16 KB RAM: 32/26 KB
Voltage detection	Power-on reset, Voltage detection circuit	Power-on reset, Voltage detection circuit	Power-on reset, Voltage detection circuit
I/O ports	CMOS I/O: 70 N-channel open drain: 1	CMOS I/O: 68 Input only: 5 Output only: 1	CMOS I/O: 68 Input only : 5 Output only: 1
Clock	XIN, XCIN, PLL, 40 MHz OCO, 125 kHz OCO	X1, PLL, High-speed OCO, XT1, Low-speed OCO	X1, PLL, High-speed OCO, XT1, Low-speed OCO
External interrupt inputs	$\overline{INT}$ × 6 ch, Key input × 4 ch	INTP × 14/12 ch, Key input × 8 ch	INTP × 14 ch, Key input × 8 ch
Watchdog timer	15-bit timer × 1 (with prescaler) (Selectable count source: Dedicated 125 kHz OCO or CPU clock)	17-bit timer × 1 (Count source: Dedicated low-speed OCO)	17-bit timer × 1 (Count source: Dedicated low-speed OCO)
DMA/DTC	DMA : 4 ch	DTC : 1 unit	DTC : 1 unit
Timer	Timer A: 16-bit timer × 5 ch (Timer mode, Event counter mode, One-shot timer mode, Pulse-width modulation (PWM) mode, Programmable output mode) Timer B: 16-bit timer × 3 ch (Timer mode, Event counter mode, Pulse frequency measurement mode, Pulse-width measurement mode) Three-phase motor control timer × 1 ch (Timers A1, A2, A4, and B2 used) Timer S: 16-bit timer × 1 ch (Input capture/Output compare: 8 ch) Task monitoring timer: 16-bit timer × 1 ch Real-time clock × 1 ch	TAU: 16-bit timer (8 ch × 2 / 8 ch + 4 ch) (Interval timer, Square wave output, External event counter, Divider function, Input pulse interval measurement, Measurement of high-/low-level width of input signal, Delay counter, One-shot pulse output, PWM output, Multiple PWM output) Timer RJ: 16-bit timer × 1 (Timer mode, Pulse output mode, Event counter mode, Pulse width measurement mode, Pulse period measurement mode) Timer RD: 16-bit timer × 2 (Timer mode (Input capture/Output compare/PWM function), Reset synchronous PWM mode, Complementary PWM mode, PWM3 mode) Real-time clock × 1 ch	TAU: 16-bit timer (8 ch × 2) (Interval timer, Square wave output, External event counter, Divider function, Input pulse interval measurement, Measurement of high-/low-level width of input signal, Delay counter, One-shot pulse output, PWM output, Multiple PWM output) Timer RJ: 16-bit timer × 1 (Timer mode, Pulse output mode, Event counter mode, Pulse width measurement mode, Pulse period measurement mode) Timer RD: 16-bit timer × 2 (Timer mode (Input capture/Output compare/PWM function), Reset synchronous PWM mode, Complementary PWM mode, PWM3 mode) Real-time clock × 1 ch
Serial interface	UART0, 1, 3, 4 (UART mode, Clock synchronous serial I/O mode) UART2 (UART mode, Clock synchronous serial I/O mode, I^2C mode, IE mode, SIM mode) Multi-master I^2C-bus Interface: 1 ch Serial Bus Interface: 1 ch (Clock synchronous serial communication mode, 4-wire bus communication mode)	SAU: 2 units (CSI: 4 ch, UART: 2 ch Simplified I^2C: 4 ch, LIN: 1 ch) Multi-master I^2C (IICA): 1 ch LIN/UART (RLIN3): 2/1 ch	SAU: 2 units (CSI: 4 ch, UART: 2 ch Simplified I^2C: 4 ch, LIN: 1 ch) Multi-master I^2C (IICA): 1 ch LIN/UART (RLIN3): 2 ch IEBus controller: 1 ch
LIN module	1 ch (Master only)	2/1 ch (Master/Slave)	2 ch (Master/Slave)
CAN module	2/1/0 ch	1/0 ch	2 ch
A/D converter	10-bit resolution: 27 ch	10-bit resolution: 25/20 ch	10-bit resolution: 25 ch
D/A converter	8-bit resolution: 1 ch	8-bit resolution: 1/0 ch	8-bit resolution: 1 ch
Comparator	-	1/0ch	1 ch
Operating temperature	J-version: -40 to +85°C K-version:-40 to +125°C	Grade L: -40 to +105°C Grade K: -40 to +125°C Grade Y: -40 to +150°C	Grade L: -40 to +105°C Grade K: -40 to +125°C
Package	80-pin LQFP	80-pin LQFP	80-pin LQFP

Note: Not provided for the replacement products.

2.3 64-pin Products

Table 2-3 Feature Comparison between 64-pin Products of M16C/5M, 57 and RL78/F13, F14, F15

Items	M16C/5M, 57 (64 pins)	RL78/F13, F14 (R5F10ALx, R5F10BLx, R5F10PLx)	RL78/F15 (R5F113Lx)
CPU	M16C/60 CPU core, 32 MHz (Max.)	RL78 CPU core, 32 MHz (Max.) ● Grade L: 32 MHz (Max.) ● Grade K, Y: 24 MHz (Max.)	RL78 CPU core, 32 MHz (Max.) ● Grade L: 32 MHz (Max.) ● Grade K: 24 MHz (Max.)
Memory	Code flash: 256/128/96 KB Data flash: 4 KB × 2 E^2dataFlash: 4 KB/- RAM: 20/12/8 KB	Code flash: 256/192/128/96/64 Note/ 48 Note/32 Note KB Data flash: 8/4 KB RAM: 20/16/10/8/6/4 Note/3 Note/2 Note KB	Code flash: 512/384 KB Data flash: 16 KB RAM: 32/26 KB
Voltage detection	Power-on reset, Voltage detection circuit	Power-on reset, Voltage detection circuit	Power-on reset, Voltage detection circuit
I/O ports	CMOS I/O: 54 N-channel open drain: 1	CMOS I/O: 52 Input only: 5 Output only: 1	CMOS I/O: 52 Input only : 5 Output only: 1
Clock	XIN, XCIN, PLL, 40 MHz OCO, 125 kHz OCO	X1, PLL, High-speed OCO, XT1, Low-speed OCO	X1, PLL, High-speed OCO, XT1, Low-speed OCO
External interrupt inputs	$\overline{INT}$ × 6 ch, Key input × 4 ch	INTP × 13/12/8 Note ch, Key input × 8 ch	INTP × 13 ch, Key input × 8 ch
Watchdog timer	15-bit timer × 1 (with prescaler) (Selectable count source: Dedicated 125 kHz OCO or CPU clock)	17-bit timer × 1 (Count source: Dedicated low-speed OCO)	17-bit timer × 1 (Count source: Dedicated low-speed OCO)
DMA/DTC	DMA : 4 ch	DTC : 1 unit	DTC : 1 unit
Timer	Timer A: 16-bit timer × 5 ch (Timer mode, Event counter mode, One-shot timer mode, Pulse-width modulation (PWM) mode, Programmable output mode) Timer B: 16-bit timer × 3 ch (Timer mode, Event counter mode, Pulse frequency measurement mode, Pulse-width measurement mode) Three-phase motor control timer × 1 ch (Timers A1, A2, A4, and B2 used) Timer S: 16-bit timer × 1 ch (Input capture/Output compare: 8 ch) Task monitoring timer: 16-bit timer × 1 ch Real-time clock × 1 ch	TAU: 16-bit timer (8 ch × 2 / 8 ch + 4 ch / 8 Note ch) (Interval timer, Square wave output, External event counter, Divider function, Input pulse interval measurement, Measurement of high-/low-level width of input signal, Delay counter, One-shot pulse output, PWM output, Multiple PWM output) Timer RJ: 16-bit timer × 1 (Timer mode, Pulse output mode, Event counter mode, Pulse width measurement mode, Pulse period measurement mode) Timer RD: 16-bit timer × 2 (Timer mode (Input capture/Output compare/PWM function), Reset synchronous PWM mode, Complementary PWM mode, PWM3 mode) Real-time clock × 1 ch	TAU: 16-bit timer (8 ch × 2) (Interval timer, Square wave output, External event counter, Divider function, Input pulse interval measurement, Measurement of high-/low-level width of input signal, Delay counter, One-shot pulse output, PWM output, Multiple PWM output) Timer RJ: 16-bit timer × 1 (Timer mode, Pulse output mode, Event counter mode, Pulse width measurement mode, Pulse period measurement mode) Timer RD: 16-bit timer × 2 (Timer mode (Input capture/Output compare/PWM function), Reset synchronous PWM mode, Complementary PWM mode, PWM3 mode) Real-time clock × 1 ch
Serial interface	UART0, 1, 3 (UART mode, Clock synchronous serial I/O mode) UART2 (UART mode, Clock synchronous serial I/O mode, I^2C mode, IE mode, SIM mode) Multi-master I^2C-bus Interface: 1 ch Serial Bus Interface: 1 ch (Clock synchronous serial communication mode, 4-wire bus communication mode)	SAU: 2/1 Note units (CSI: 4/2 Note ch, UART: 2/1 Note ch, Simplified I^2C: 4/2 Note ch, LIN: 1 ch) Multi-master I^2C (IICA): 1 ch LIN/UART (RLIN3): 2/1 ch	SAU: 2 units (CSI: 4 ch, UART: 2 ch, Simplified I^2C: 4 ch, LIN: 1 ch) Multi-master I^2C (IICA): 1 ch LIN/UART (RLIN3): 2 ch IEBus controller: 1 ch
LIN module	1 ch (Master only)	2/1 ch (Master/Slave)	2 ch (Master/Slave)
CAN module	2/1/0 ch	1/0 ch	2 ch
A/D converter	10-bit resolution: 16 ch	10-bit resolution: 20/19/12 Note ch	10-bit resolution: 20 ch
D/A converter	8-bit resolution: 1 ch	8-bit resolution: 1/0 ch	8-bit resolution: 1 ch
Comparator	-	1/0 ch	1 ch
Operating temperature	J-version: -40 to +85°C K-version:-40 to +125°C	Grade L: -40 to +105°C Grade K: -40 to +125°C Grade Y: -40 to +150°C	Grade L: -40 to +105°C Grade K: -40 to +125°C
Package	64-pin LQFP	64-pin LQFP	64-pin LQFP

Note: Not provided for the replacement products.

3. Product Pin Function Comparison

Table 3-1 compares the pin functions of the M16C/5M, 57 products with the counterparts of the RL78/F13, F14, F15 products. Please use it as a reference when porting. For details on each pin function, refer to the user's manual.

Table 3-1 Pin Function Comparison between M16C/5M, 57 and RL78/F13, F14, F15 (1)

M16C/5M, 57			RL78/F13, F14, F15		
Items	**Pins**	**I/O**	**Pins**	**I/O**	**Description of RL78/F13, F14, F15 pins**
Power supply	VCC	I	V_{DD}, EV_{DD0}, EV_{DD1}	I	Positive power supply pins. Connect the pins to have V_{DD} = EV_{DD}.
	VSS	I	V_{SS}, EV_{SS0}, EV_{SS1}	I	Ground potential pins. Connect the pins to have V_{SS} = EV_{SS}.
	-	-	REGC	O	Regulator output stabilization capacitance connection pin for internal operation Note 1
Analog power supply	AVCC	I	V_{DD}, EV_{DD0}, EV_{DD1}	I	Power supply pins for analog input pins
	AVSS	I	V_{SS}, EV_{SS0}, EV_{SS1}	I	Ground potential pins for analog input pins
Reset input	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$	I	External reset pin
Boot mode	CNVSS	I/O	TOOL0	I/O	Data I/O pin for a flash memory programmer/debugger
Main clock	XIN	I	X1	I	Resonator connection pin for the main system clock
	XOUT	O	X2/EXCLK	I/O	[X1 oscillation mode] Resonator connection pin for the main system clock (X2) [External clock input mode] External clock input pin for main system clock (EXCLK)
Sub Clock	XCIN	I	XT1	I	Resonator connection pin for the subsystem clock
	XCOUT	O	XT2/EXCLKS	I/O	[XT1 oscillation mode] Resonator connection pin for the subsystem clock (XT2) [External clock input mode] External clock input pin for the subsystem clock (EXCLKS)
Clock output	CLKOUT	O	PCLBUZ0	O	Clock/buzzer output pin
$\overline{\text{INT}}$ interrupt inputs	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	INTP0 to INTP13	I	External interrupt request input pins
$\overline{\text{NMI}}$ input	$\overline{\text{NMI}}$	I	-	-	An external interrupt (maskable interrupt) input to an INTPn pin can be used instead
Key input interrupts	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	KR0 to KR7	I	Key interrupt input pins
Timer A	TA0OUT to TA4OUT	I/O	TO00 to TO07, TO10 to TO17, TRJIO0, TRJO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	O	Timer output pins of TAU0, 1, Timer RJ, and Timer RD
	TA0IN to TA4IN	I	TI00 to TI07, TI10 to TI17, TRJIO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	I	Timer input pins of TAU0, 1, Timer RJ, and Timer RD
	ZP	I	TI00 to TI07, TI10 to TI17, TRJIO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	I	Timer input pins of TAU0, 1, Timer RJ, and Timer RD
Timer B	TB0IN to TB5IN	I	TI00 to TI07, TI10 to TI17, TRJIO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	I	Timer input pins of TAU0, 1, Timer RJ, and Timer RD
Three-phase motor control timer	U, V, W, $\overline{\text{U}}$, $\overline{\text{V}}$, $\overline{\text{W}}$	O	TRDIOB0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	O	Timer output pins of Timer RD
	IDU, IDW, IDV	I/O	TI00 to TI07, TI10 to TI17, TRJIO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	I	Timer input pins of TAU0, 1, Timer RJ, and Timer RD
	$\overline{\text{SD}}$	I	INTP0	I	Timer RD pulse output forced cutoff input pin
Real-time clock	RTCOUT	O	RTC1HZ	O	Real-time clock correction clock (1 Hz) output pin
Timer S	INPC1_0 to INPC1_7	I	TI00 to TI07, TI10 to TI17, TRJIO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	I	Timer input pins of TAU0, 1, Timer RJ, and Timer RD
	OUTC1_0 to OUTC1_7	O	TO00 to TO07, TO10 to TO17, TRJO0, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1	O	Timer output pins of TAU0, 1, Timer RJ, and Timer RD
	TSUDA, TSUDB	I	-	-	Two-phase pulse input is not provided for the RL78/F13, F14, F15 products

Table 3-1 in Function Comparison between M16C/5M, 57 and RL78/F13, F14, F15 (2)

M16C/5M, 57			RL78/F13, F14, F15		
Items	**Pins**	**I/O**	**Pins**	**I/O**	**Description of RL78/F13, F14, F15 pins**
Serial interface	CLK0 to CLK4	I/O	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21	I/O	Serial clock I/O pins of SAU0, 1, 2
	RXD0 to RXD4	I	RXD0, RXD1, RXD2, SI00, SI01, SI10, SI11, SI20, SI21, LRXD0, LRXD1, LRXD2	I	Serial data input pins of SAU0, 1, 2, and RLIN3
	TXD0 to TXD4	O	TXD0, TXD1, TXD2, SO00, SO01, SO10, SO11, SO20, SO21, LTXD0, LTXD1, LTXD2	O	Serial data output pins of SAU0, 1, 2, and RLIN3
	CTS0 to CTS3	I	SSI00, SSI01, SSI10, SSI11	I	Slave select input pins of SAU0, 1
	RTS0 to RTS3	O	-	-	I/O ports can be used instead
	SCL2 (Simplified I^2C)	I/O	SCL00, SCL01, SCL10, SCL11, SCLA0	I/O	Serial clock I/O pins of SAU0, 1, and IICA
	SDA2 (Simplified I^2C)	I/O	SDA00, SDA01, SDA10, SDA11, SDAA0	I/O	Serial data I/O pins of SAU0, 1, and IICA
	RXD2 (Simplified IEBus)	I	IERXD	I	IEBus serial data input pin
	TXD2 (Simplified IEBus)	O	IETXD	O	IEBus serial data output pin
Multi-master I^2C-bus	SCLMM	I/O	SCLA0	I/O	IICA serial clock I/O pin
	SDAMM	I/O	SDAA0	I/O	IICA serial data I/O pin
Serial bus interface	SSCK0	I/O	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21	I/O	Serial clock I/O pins of SAU0, 1, 2
	SSI0	I	SI00, SI01, SI10, SI11, SI20, SI21	I	Serial data input pins of SAU0, 1, 2
	SSO0	O	SO00, SO01, SO10, SO11, SO20, SO21	O	Serial data output pins of SAU0, 1, 2
	SCS0	I	SSI00, SSI01, SSI10, SSI11	I	Slave select input pins of SAU0, 1
LIN module	LIN0IN	I	LRXD0, LRXD1, LRXD2	I	LIN serial data input pins
	LIN0OUT	O	LTXD0, LTXD1, LTXD2	O	LIN serial data output pins
CAN Module	CRX0, CRX1	I	CRXD0, CRXD1	I	CAN serial data input pins
	CTX0, CTX1	O	CTXD0, CTXD1	O	CAN serial data output pins
A/D converter	VREF	I	AV_{REFP}	I	A/D converter reference voltage (+ side) input pin
	-	-	AV_{REFM}	I	A/D converter reference voltage (- side) input pin
	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN3_0 to AN3_2	I	ANI0 to ANI30	I	Analog input pins * A/D conversion accuracy depends on the power supply for the analog input pins. V_{DD} system analog pins achieve higher accuracy Power supply for: ・ANI0 to ANI23 Note 2: V_{DD} ・ANI24 to ANI30: EV_{DD0}, EV_{DD1}
	ADTRG	I	-	-	Combination of an external interrupt input to an INTPn pin and either DTC or ELC (provided only for the RL78/F14 and RL78/F15 products) can be used instead. (Software trigger when DTC selected/ Hardware trigger when ELC selected)
D/A converter	DA0	O	ANO0	O	D/A converter output pin
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 Note 3, P9_0 to P9_7, P10_0 to P10_7	I/O	P00 to P03, P10 to P17, P30 to P34, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, P120, P125 to P127, P140, P150 to P157	I/O	Pins with IOH1/IOL1 specification Note 4: P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97 Note 5, P106, P107, P120, P125 to P127, P140, P150 to P157 Pins with IOH2/IOL2 specification Note 4: P33, P34, P80 to P87, P90 to P97 Note 5, P100 to P105
Input-only ports	-	-	P121 to P124, P137	I	P121 to P124, P137 are input-only ports
Output-only port	-	-	P130	O	P130/RESOUT is an output-only port

Notes: 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 µF to 1 µF).
2. When the ANI0 to ANI23 pins are used as both analog input pins and digital I/O ports, the analog channel number should be configured in sequential ascending order. See 4.1.5(1) for details.
3. P8_5 output is N-channel open drain output.
4. The high-level output current (IOH1 or IOH2) and low-level output current (IOL1 or IOL2) vary from pin to pin. See 4.1.4(2) for details.
5. The high-level output current and low-level output current of P92 to P97, which are multiplexed with the analog input pin function, vary from product to product. See 4.1.4(2) for details.

4. Considerations

This chapter describes considerations that you need to take when porting from the M16C/5M, 57 products to the RL78/F13, F14, F15 products.

4.1 Considerations When Porting to RL78/F13, F14, F15

Make sure to refer to the user's manuals of the replacement products when porting from the M16C/5M, 57 products to the RL78/F13, F14, F15 products. Customers are required to sufficiently evaluate their products on their system.

4.1.1 Development Tools

The table below provides information on the development tools for the RL78/F13, F14, F15 products.

Table 4-1 Development Tools for RL78/F13, F14, F15

Tools	Description
e^2 studio	Renesas integrated development environment
CS+	Renesas integrated development environment (for RH850, V850, RX, RL78, 78K0R, 78K0)
CC-RL	C compiler package for RL78 Family
CA78K0R	C compiler package for RL78 Family and 78K0 Family
E2 emulator	On-chip debugging emulator and flash programmer
E2 emulator lite	On-chip debugging emulator and flash programmer
E1 emulator	On-chip debugging emulator and flash programmer
IECUBE	Full-spec emulator
PG-FP6	Flash memory programmer
Code Generator Plug-in	Tool that can automatically generate control programs for peripheral modules (bundled with CS+ and e^2 studio)
Applilet	Standalone tool for automatically generating device driver programs for peripheral modules
Data flash library	Library for reprogramming data flash memories
Code flash library	Library for reprogramming code flash memories

Remark: Besides the tools listed above, different development tools manufactured by Renesas partners are also available. For more information, please visit Renesas Electronics website or contact their customer support.

4.1.2 Noise

In order to eliminate unwanted noise, placing bypass capacitors (approximately 0.1 μF) between the V_{DD} and V_{SS} pins, between the EV_{DD0} and EV_{SS0} pins, and between the EV_{DD1} and EV_{SS1} pins is recommended. In addition, placing a capacitor (0.47 μF to 1 μF) between the REGC and V_{SS} pins is also recommended. Since the noise is affected by the board layout and software, customers are required to sufficiently evaluate the impact of the noise in their environments with their board layout and software.

4.1.3 Oscillator

Customers are required to consult the resonator manufacturer to determine the proper oscillation constant. In addition, customers are also required to sufficiently evaluate the oscillation in their environments.

4.1.4 I/O Ports

(1) Input-Only/Output-Only Ports

The RL78/F13, F14, F15 products are provided with input-only ports (P121 to P124, P137) and an output-only port (P130). Care must be taken when assigning pin functions.

(2) Port Output Current

The output current of the I/O ports in the RL78/F13, F14, F15 products varies from product to product and pin to pin. Care must be taken when assigning pin functions.

Table 4-2 Port Output Current of Each Product/Pin (Condition: V_{DD} = EV_{DD0} = EV_{DD1} = 4.0 V to 5.5 V)

Specification	Applicable pins		Port output current		
			Grade L	Grade K	Grade Y
IOH1/IOL1	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97 Note, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to 157, P160 to P167	Per pin	-5.0 mA/8.5 mA		
		Total of all pins	-50.0 mA/65.0 mA	-42.0 mA/65.0 mA	-32.0 mA/55.0 mA
IOH2/IOL2	P33, P34, P80 to P87, P90 to P97 Note, P100 to P105	Per pin	-0.1 mA/0.4 mA		
		Total of all pins	-2.0 mA/5.0 mA		

Note: The I/O buffer power supplies for P92 to P97 vary from product to product. The IOH1/IOL1 specification is applied to the pins whose power supply is EV_{DD0} or EV_{DD1}, whereas the IOH2/IOL2 specification is applied to the pins whose power supply is V_{DD}. The table below shows the output current specifications applied to P92 to P97 of each product.

Table 4-3 Port Output Current Specifications Applied to P92 to P97

Products	Port output current specifications applied to P92 to P97
Each product of RL78/F15	IOH2/IOL2 (P92 to P97)
RL78/F14 (100-pin products)	IOH2/IOL2 (P92 to P97)
RL78/F14 (80-pin products)	Products with 128 KB to 256 KB of code flash: IOH2/IOL2 (P92 to P97) Products with 64 KB to 96 KB of code flash: IOH2/IOL2 (P92 to P95), IOH1/IOL1 (P96, P97)
RL78/F14 (64-pin products)	Products with 128 KB to 256 KB of code flash: IOH2/IOL2 (P92 to P96) Products with 64 KB to 96 KB of code flash: IOH2/IOL2 (P92 to P95), IOH1/IOL1 (P96)
RL78/F14 (48-pin products)	IOH2/IOL2 (P92)
RL78/F13 (CAN and LIN incorporated) (80-pin products)	IOH2/IOL2 (P92 to P95), IOH1/IOL1 (P96, P97)
RL78/F13 (CAN and LIN incorporated) (64-pin products)	IOH2/IOL2 (P92 to P95), IOH1/IOL1 (P96)
RL78/F13 (CAN and LIN incorporated) (48-pin products)	IOH2/IOL2 (P92)
RL78/F13 (LIN incorporated) (80-pin products)	IOH2/IOL2 (P92 to P95), IOH1/IOL1 (P96, P97)
RL78/F13 (LIN incorporated) (64-pin products)	Products with 96 KB to 128 KB of code flash: IOH2/IOL2 (P92 to P95), IOH1/IOL1 (P96) Products with 32 KB to 64 KB of code flash: IOH1/IOL1 (P92 to P96)
RL78/F13 (LIN incorporated) (48-pin products)	Products with 96 KB to 128 KB of code flash: IOH2/IOL2 (P92) Products with 16 KB to 64 KB of code flash: IOH1/IOL1 (P92)

4.1.5 A/D Conversion

(1) ANI0 to ANI23 Pin Configuration as Analog Input Pins

In order to use some or all of the ANI0 to ANI23 pins as analog input pins, the analog channel number should be configured in sequential ascending order by the ADPC register. For example, when the ANI0 and ANI2 pins need to be used as analog input pins, the ANI1 pin cannot be used as a digital I/O port.

(2) A/D Conversion Accuracy

The A/D conversion accuracy in the RL78/F13, F14, F15 products depends on the pin and the power supply of the A/D converter. The analog input pins whose power supply is EV_{DD0} or EV_{DD1} (the ANI24 to ANI30 pins) have lower A/D conversion accuracy than the analog input pins whose power supply is V_{DD} (the ANI0 to ANI23 pins). For this reason, the ANI2 to ANI23 pins should be used as analog input pins and the AV_{REFP} and AV_{REFM} pins should be used as the reference voltage pins of the A/D converter to achieve higher conversion accuracy.

(3) A/D Conversion Result

The bit positions in the registers to which the A/D conversion results are written after the A/D conversion (10-bit A/D conversion) differ between the RL78/F13, F14, F15 products and M16C/5M, 57 products. Care must be taken when using the A/D conversion result to calculate a voltage or make a comparison.

[M16C/5M, 57] A/D Register (ADi)

b15						b8	b7	b0
0	0	0	0	0	0	Upper 2 bits	Lower 8 bits	

[RL78/F13, F14, F15] 10-Bit A/D Conversion Result Register (ADCR)

b15	b8	b7						b0
Upper 8 bits		Lower 2 bits	0	0	0	0	0	0

(4) Scan Mode

Although the scan mode in the RL78/F13, F14, F15 products is the counterpart of the single sweep mode and repeat sweep mode in the M16C/5M, 57 products, the number of analog input channels to be converted differs between these products.

- M16C/5M, 57: Selectable from 8 channels, 6 channels, 4 channels or 2 channels
- RL78/F13, F14, F15: 4 sequential channels of ANI0 to ANI23

Each of the RL78/F13, F14, F15 products is provided with only one A/D conversion result register. Therefore, the A/D conversion result register needs to be read each time a single channel is converted in the scan mode. As a side note, the DTC allows the conversion result to be stored in RAM without using the CPU.

5. References

The documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F13, F14 User's Manual: Hardware Rev. 2.10
- RL78/F15 User's Manual: Hardware Rev.1.00
- M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev.1.10

Alongside the RL78/F13, F14, F15 products described in this application note, the RH850 family Renesas 32-bit microcontrollers are worthy of consideration in terms of superior processing-performance (higher operation frequency) and many more peripheral functions in comparison with the M16C/5M, 57 products that you are currently using.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
Rev.1.00	Aug. 31, 2018		First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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