

# Application Note

## DA914x PCB Layout Recommendations

AN-PM-145

### Abstract

*This application note provides recommendations on how to place and route DA914x devices. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.*

**DA914x PCB Layout Recommendations**
**Contents**

<b>Abstract</b> .....	<b>1</b>
<b>Contents</b> .....	<b>2</b>
<b>Figures</b> .....	<b>2</b>
<b>Tables</b> .....	<b>3</b>
<b>1 Terms and Definitions</b> .....	<b>3</b>
<b>2 References</b> .....	<b>3</b>
<b>3 Introduction</b> .....	<b>4</b>
<b>4 Layout Recommendations</b> .....	<b>5</b>
4.1 DA914x Package Information .....	5
4.1.1 Ball Map .....	5
4.1.2 Package Information .....	6
4.1.3 Layout Guidelines .....	7
4.2 Buck Converter .....	7
4.2.1 DA914x Input .....	7
4.2.2 Ground Connections .....	9
4.2.3 LX Routing .....	11
4.2.4 Buck Output .....	12
4.2.5 Feedback Lines .....	12
4.3 Communication Interface (I <sup>2</sup> C) .....	13
4.4 GPIO Signals .....	13
<b>Appendix A Input Network Parameters</b> .....	<b>14</b>
A.1 AVDD to AGND Loop .....	14
A.2 FBP to FBN Loop .....	15
A.3 PVDD to PGND loop .....	15
<b>Revision History</b> .....	<b>16</b>

**Figures**

Figure 1: DA9141 Recommended Components and Connections .....	4
Figure 2: Ball Map .....	5
Figure 3: Package Outline Drawing .....	6
Figure 13: DA9141-A Footprint .....	7
Figure 4: Recommended Input Capacitor Placement and Routing (Layer 1) .....	8
Figure 5: Recommended Input Capacitor Placement and Routing (Layers 1 and 5) .....	9
Figure 6: Recommended Power Ground Traces .....	10
Figure 7: LX Node Pattern on DA9140 Evaluation Board (Layer 1) .....	11
Figure 8: LX Node Traces on DA9140 Evaluation Board (Layer 2) .....	12
Figure 9: Output Voltage Feedback Line Routing on DA9140 Evaluation Board (Layer 6) .....	13
Figure 10: AVDD to AGND Path Impedance Including Capacitor .....	14
Figure 11: FBP to FBN Path Impedance Including Capacitor .....	15
Figure 12: PVDD to PGND Path Impedance Including Capacitors .....	15

**Tables**

Table 1: DA9141 Recommended Components..... 4

**1 Terms and Definitions**

EVB	Customer evaluation board
FET	Field effect transistor
GND	Ground
GPIO	General purpose input or output
IC	Integrated circuit
PCB	Printed circuit board
FC-BGA	Flip chip, ball grid array

**2 References**

- [1] DA9141-A, DA9142-A Datasheets (for automotive applications), Renesas
- [2] DA9141, DA9142 Datasheet (for standard applications), Renesas
- [3] DA9140 Customer Evaluation Board Schematic, DA9140-30-A\_sch.pdf, Renesas
- [4] AN-PM-010, PCB Layout Guidelines for Dialog PMICs, Application Note, Renesas
- [5] UM-PM-061, DA9140 Quick Guide EVB, Renesas
- [6] UM-PM-062, DA9140 User Guide EVB, Renesas

**Note 1** References are for the latest published version, unless otherwise indicated.

### 3 Introduction

Renesas' DA9141 and DA9142 devices are power management ICs with integrated power FETs, see datasheets [1] and [2]. DA9141 is a single channel, quad-phase buck converter capable of driving up to 40 A loads, while the DA9142 is a dual-phase buck converter capable of driving up to 20 A loads.

The recommended components and connections for DA9141 are shown in Figure 1 and Table 1. Note that AEC-Q200 compliant components are required for Automotive applications.

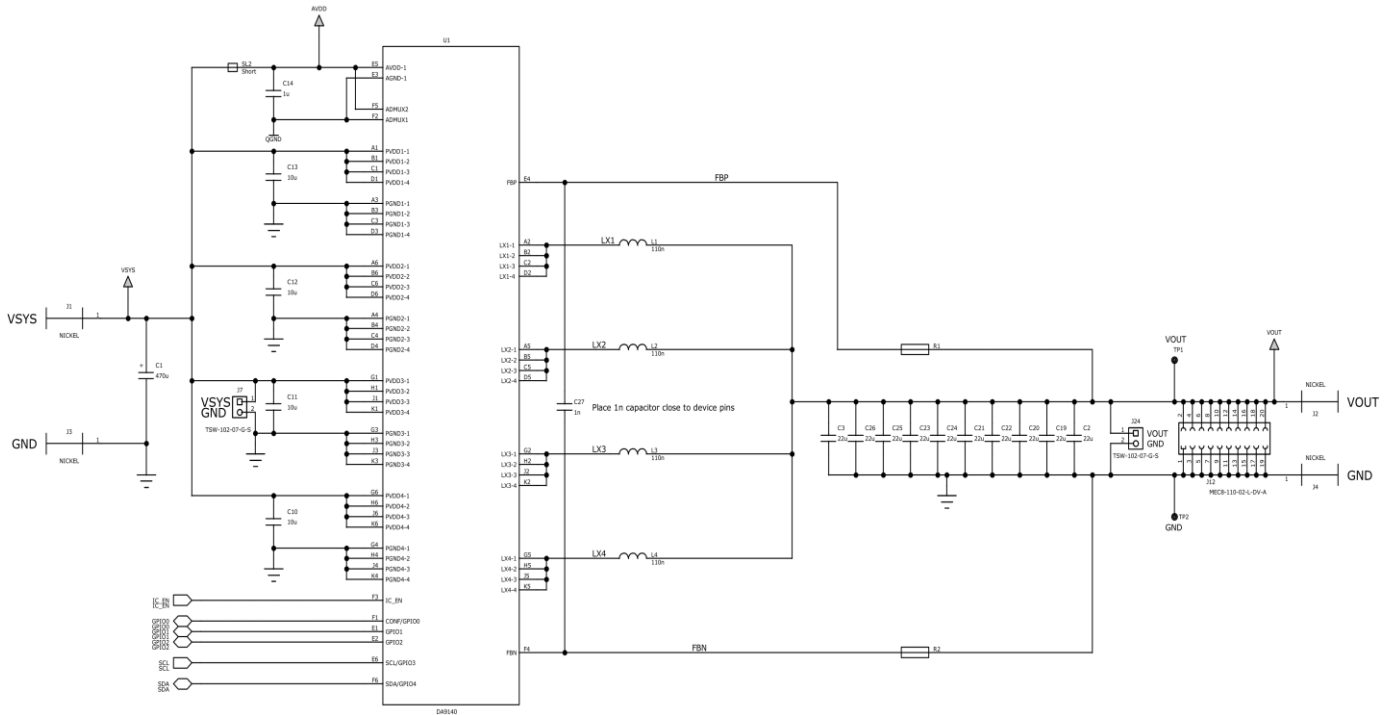


Figure 1: DA9141 Recommended Components and Connections

The details of the design reference can be obtained from the Customer Evaluation Board (EVB) schematics [3]. The EVB is described in the User Guides [5] and [6].

Details on recommended components are listed in Table 1.

Table 1: DA9141 Recommended Components

Application	Part Reference	Value	Part number
AVDD Bypass Capacitor	C14	1 µF	GCM188R71E105MA64
PVDD Bypass Capacitor	C10, C11, C12, C13	10 µF	GCM188D70J106ME36D
VOUT Bypass Capacitor	C2, C3, C19, C20, C21, C22, C23, C24, C25, C26	22 µF	GCM188E70E226M
FB Bypass Capacitor	C27	1 nF	GCD188R71H102KA01D
Output Inductor	L1, L2, L3, L4	112 nH	CLT3225AR11MI3

DA914x PCB Layout Recommendations

4 Layout Recommendations

DA914x is packaged in a 60-pin FC-BGA package with a 0.65 mm pitch.

At least a four-layer PCB stack-up should be used for best PCB layout design. However, the number of routing layers and other PCB parameters are also determined by the other devices in the system.

These recommendations are with reference to the DA9140 EVB, a six-layer PCB. General PMIC layout guidelines are provided in AN-PM-010 [4].

4.1 DA914x Package Information

4.1.1 Ball Map

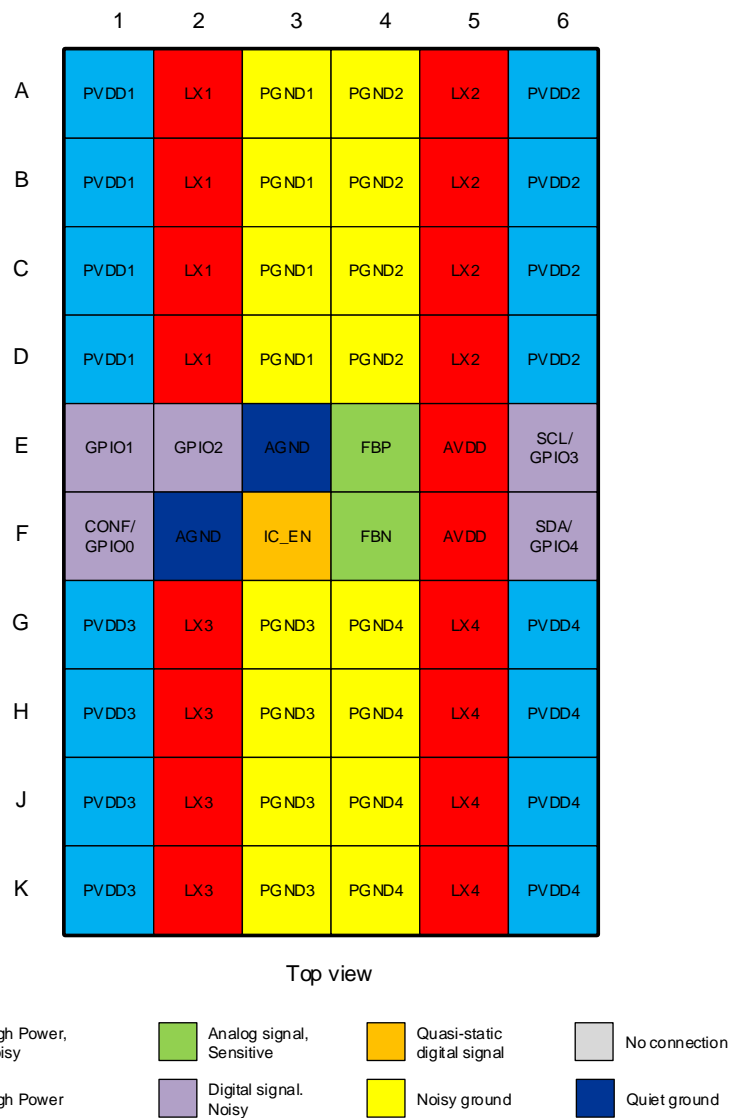
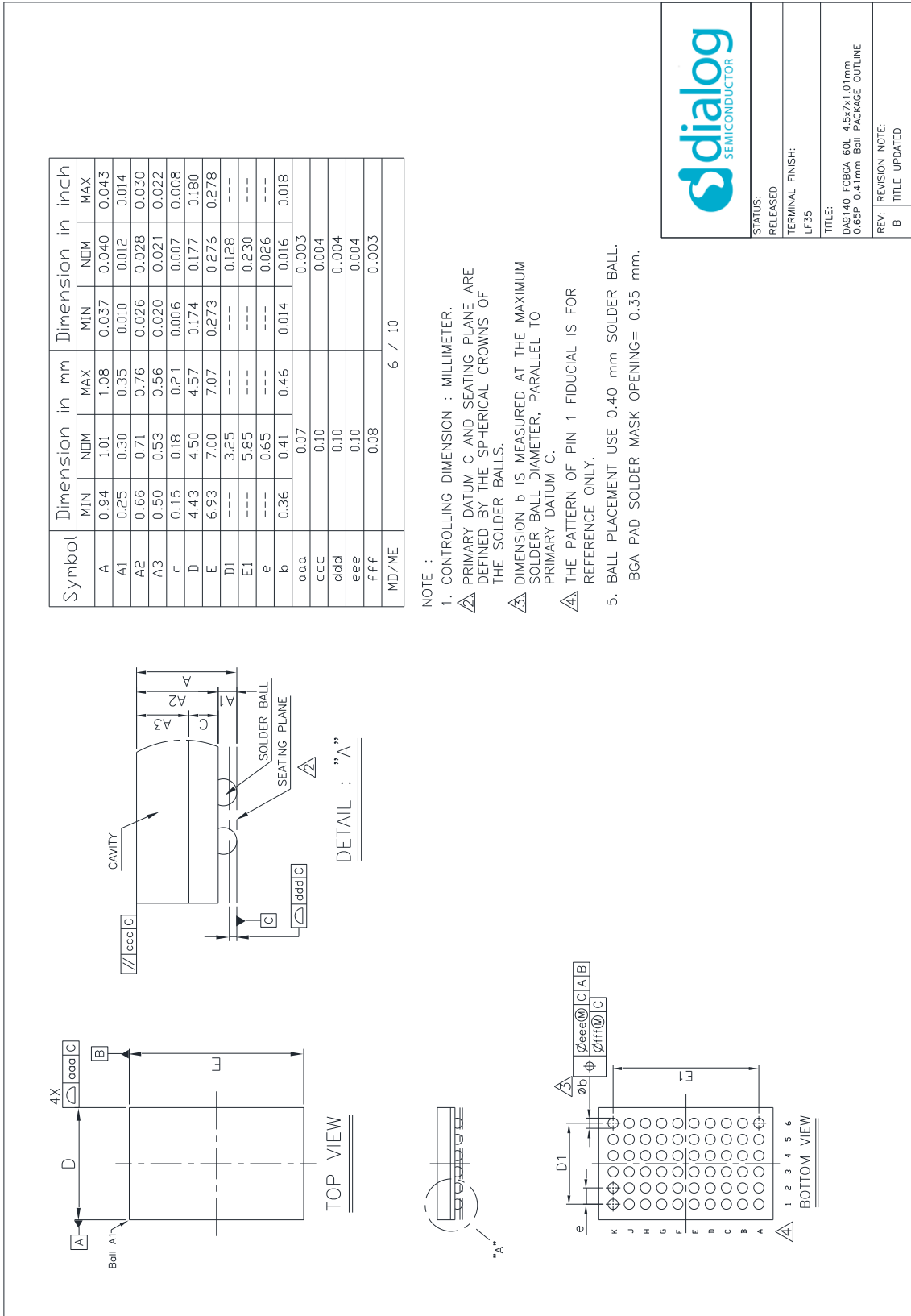


Figure 2: Ball Map

DA914x PCB Layout Recommendations

4.1.2 Package Information



STATUS:  
RELEASED

TERMINAL FINISH:  
LF35

TITLE:  
DA9140 FCBGA 60L 4.5x7x1.01mm  
0.65P 0.41mm Ball PACKAGE OUTLINE

REV: B  
REVISION NOTE:  
TITLE UPDATED

Figure 3: Package Outline Drawing

DA914x PCB Layout Recommendations

4.1.3 Layout Guidelines

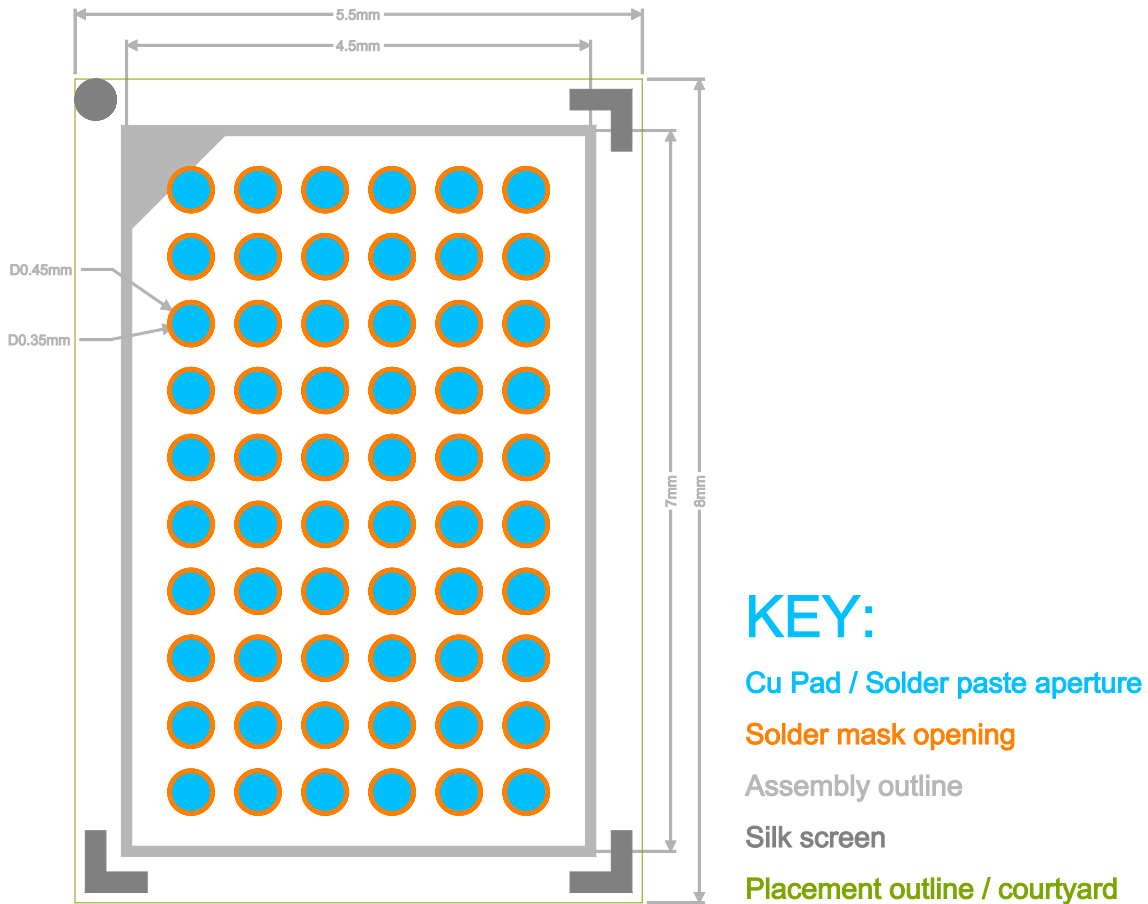


Figure 4: DA914x-A Footprint

4.2 Buck Converter

DA914x follows the standard buck layout procedure with output capacitors placed as close as possible to the load. Due to the device's ability to deliver high currents, a wide output trace for minimized parasitic impedance is recommended.

4.2.1 DA914x Input

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device's input and power GND pins to minimize the parasitic inductance.

In DA914x layout design, the input capacitor for each phase should be placed as close as possible to the PVDD<x> and PGND<x> pins, and on the same layer as the DA914x device.

If multiple layers are used, it is recommended to use at least four through-hole vias per phase (or at least twelve microvias per phase) to connect the input voltage (V<sub>SYS</sub>) between layers to minimize line resistance.

The DA914x has separate AVDD supply pins for the internal analog circuits. A 1 μF bypass capacitor (C14) should be placed close to the device's AVDD pin. The AVDD pin input and buck converter input (PVDD<x>) share the same net, but it is important to separate these traces. Do not connect both traces directly on the same layer.

### DA914x PCB Layout Recommendations

Ensure that the AVDD pin is connected to the input voltage (V<sub>SYS</sub>) plane far enough from the buck's input voltage plane so switching noise from the buck converter input (P<sub>VDD<x></sub>) is not injected to the AVDD pin.

Figure 5 shows the input capacitor placement and routing recommendation.

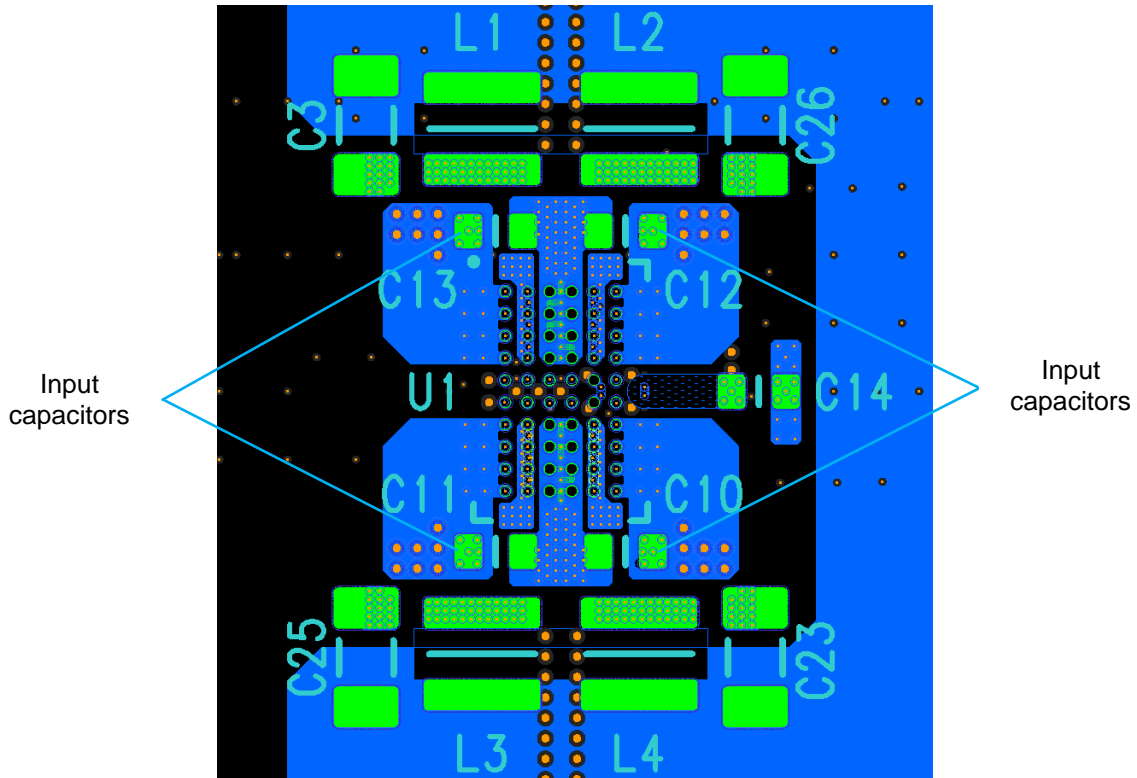
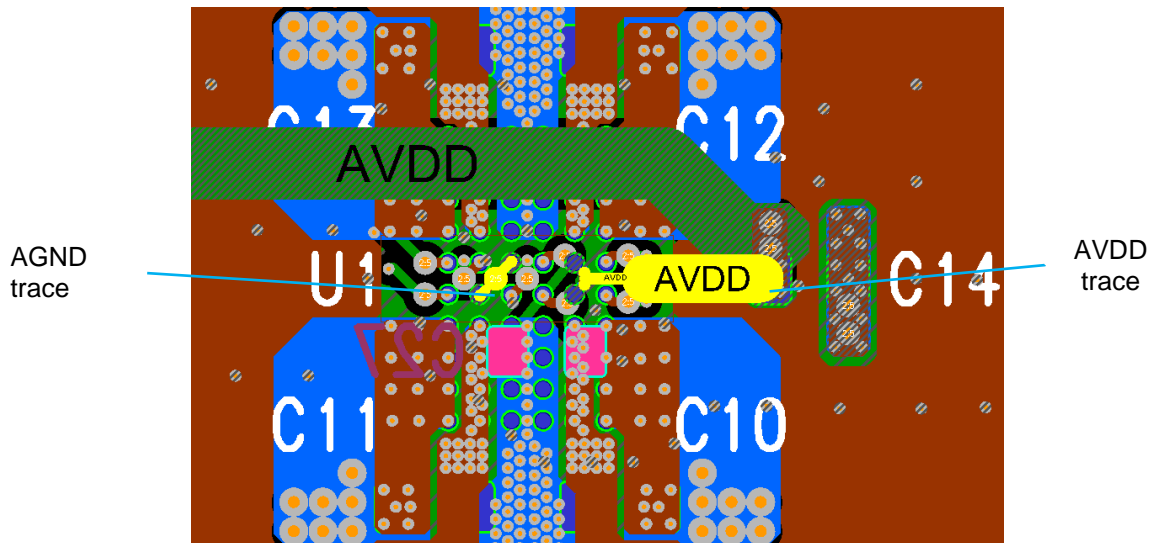


Figure 5: Recommended Input Capacitor Placement and Routing (Layer 1)

Figure 6 shows more details about the connection to the AVDD capacitor, connecting to a quiet ground plane on Layer 5 and a separate AVDD trace for connection to V<sub>SYS</sub> elsewhere on the board, far from the buck switching currents.



## DA914x PCB Layout Recommendations



**Figure 6: Recommended Input Capacitor Placement and Routing (Layers 1 and 5)**

### 4.2.2 Ground Connections

Special care should be taken with ground connections because of the high current capability of DA914x, and because of the device's high-performance requirements.

The power GND terminals (PGND<x>) of the DA914x are placed between each phase's LX pin.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (PGND<x>) and to connect them at a single point.

AGND is isolated from the power GND terminals (PGND<x>) at the top layer (component layer) and connected at a single point on the bottom layer. [Figure 6](#) shows more details about the AGND connection to the quiet ground plane on Layer 5.

Layer 2 can be used as a return power GND plane, where the device's PGND pins and output capacitor GND can be connected. It is recommended to minimize the line impedance of the PGND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

An example of how to connect the GND terminals is illustrated in [Figure 7](#).

#### NOTE

It is recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

DA914x PCB Layout Recommendations

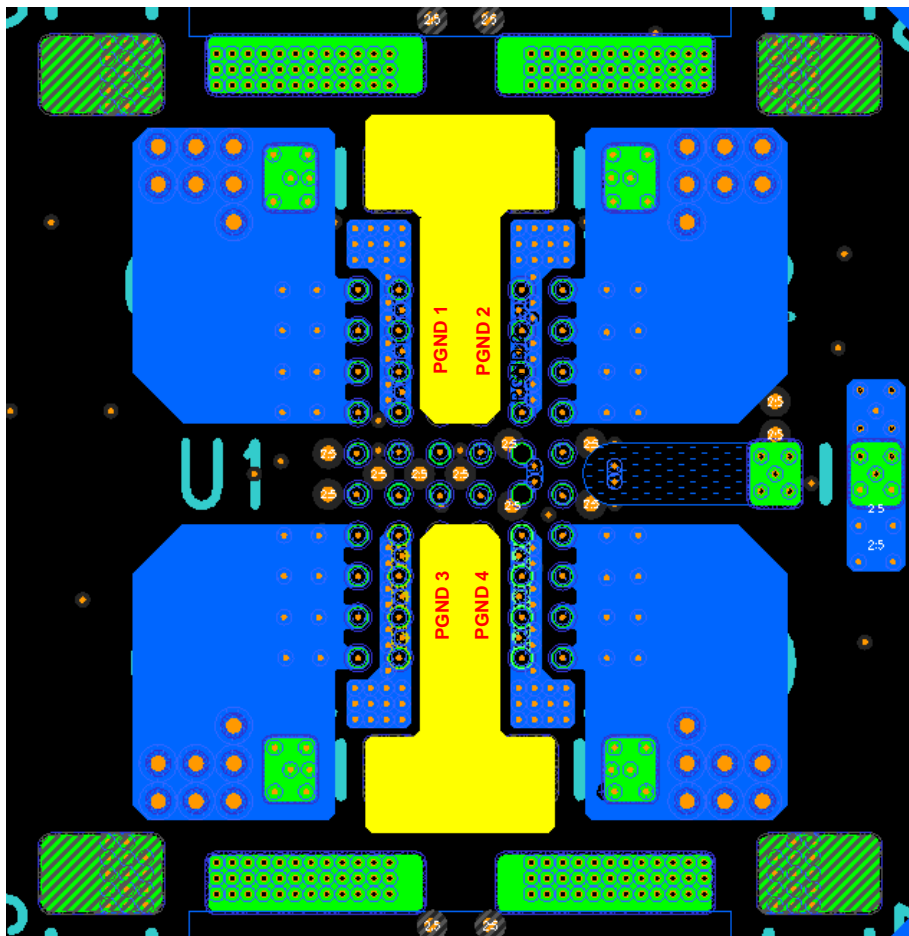


Figure 7: Recommended Power Ground Traces

DA914x PCB Layout Recommendations

4.2.3 LX Routing

Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converter stability. Very high current will flow through this trace and so the width of trace used for this LX node must be considered. Also, ensure that there are enough vias to deliver the current.

The LX node patterns on the DA9140 Evaluation Board are shown in the top level view in [Figure 8](#).

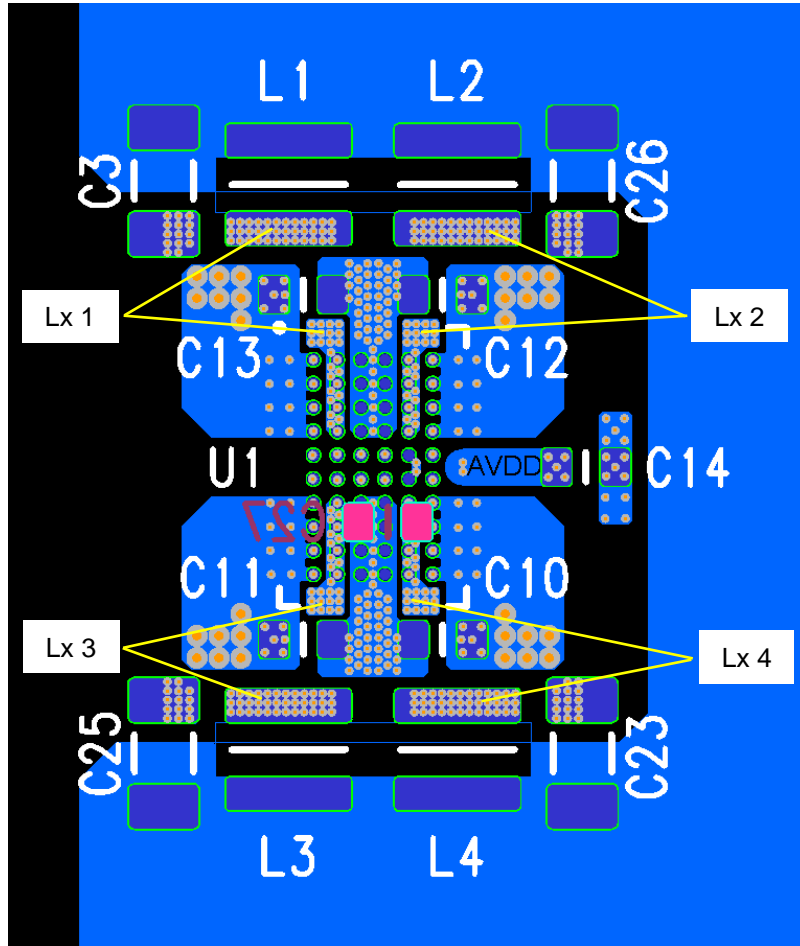


Figure 8: LX Node Pattern on DA9140 Evaluation Board (Layer 1)

On the bottom side in red the FB Bypass Capacitor C27 is visible. [Figure 9](#) on the next page shows the traces of the Lx nodes of layer 2.

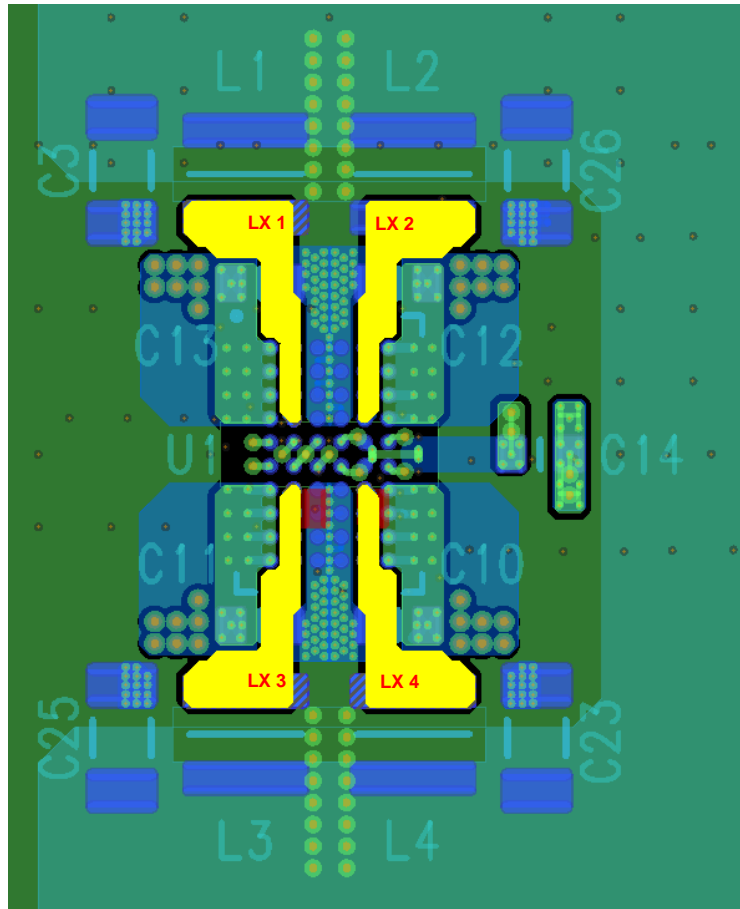


Figure 9: LX Node Traces on DA9140 Evaluation Board (Layer 2)

#### 4.2.4 Buck Output

Output capacitors should be placed as close as possible to the load. However, minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors (the load) is also important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces since the output peak current can be up to 40 A for DA9141.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

#### 4.2.5 Feedback Lines

Feedback lines must be routed as a differential pair far from any noise source (for example, output inductors, or LX node). It is strongly recommended to place a bypass capacitor (typically 1 nF) between the positive and negative sides of the differential feedback. The bypass capacitor should be placed as close as possible to the IC. It is useful for filtering noise which may be injected to the feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other devices in the system).

Ensure that the feedback lines are not overlapping any noisy node traces (for example, the LX node trace) without an insulation plane in between. If DA914x is assembled on the top layer, it is recommended to route the feedback lines on Layer 4 or below when the traces are near to the IC and the switch node areas. It is also recommended that the feedback lines are shielded by a quiet ground on their routing layer to avoid lateral coupling to other signals.

## DA914x PCB Layout Recommendations

### NOTE

- The negative feedback trace is at ground potential and care should be taken not to connect any part of the trace to the ground plane.
- The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Dialog DA9140 Evaluation Board, are shown in [Figure 10](#).

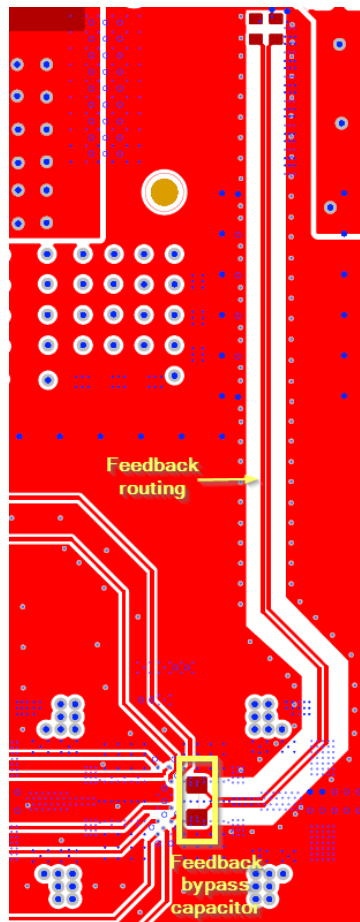


Figure 10: Output Voltage Feedback Line Routing on DA9140 Evaluation Board (Layer 6)

### 4.3 Communication Interface (I<sup>2</sup>C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

### 4.4 GPIO Signals

Generally, GPIOs have the lowest routing priority. Any layer can be used for routing these signals.

However, care must be taken regarding the noise produced by the GPIOs in order to avoid coupling to the sensitive analog references and feedbacks.

## Appendix A Input Network Parameters

The examples in this section are provided for reference. They use an evaluation board that follows the guidelines set by this document and can be taken as a target specification if the exact guidelines cannot be followed.

### A.1 AVDD to AGND Loop

Figure 11 shows the impedance plot for the AVDD to AGND path including a GRM155R61A105KE15D capacitor. The effective inductance at 1 GHz should be kept below 250 pH.

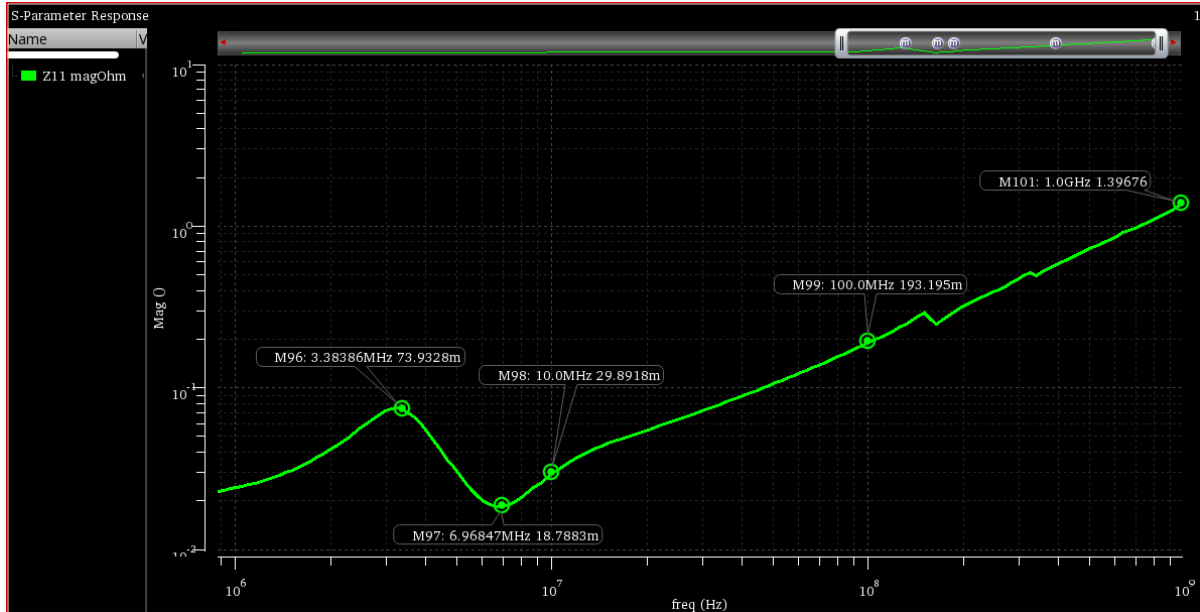


Figure 11: AVDD to AGND Path Impedance Including Capacitor

### DA914x PCB Layout Recommendations

#### A.2 FBP to FBN Loop

Figure 12 shows the impedance plot for the FBP to FBN path including a GRM155R71H102KA01D capacitor.

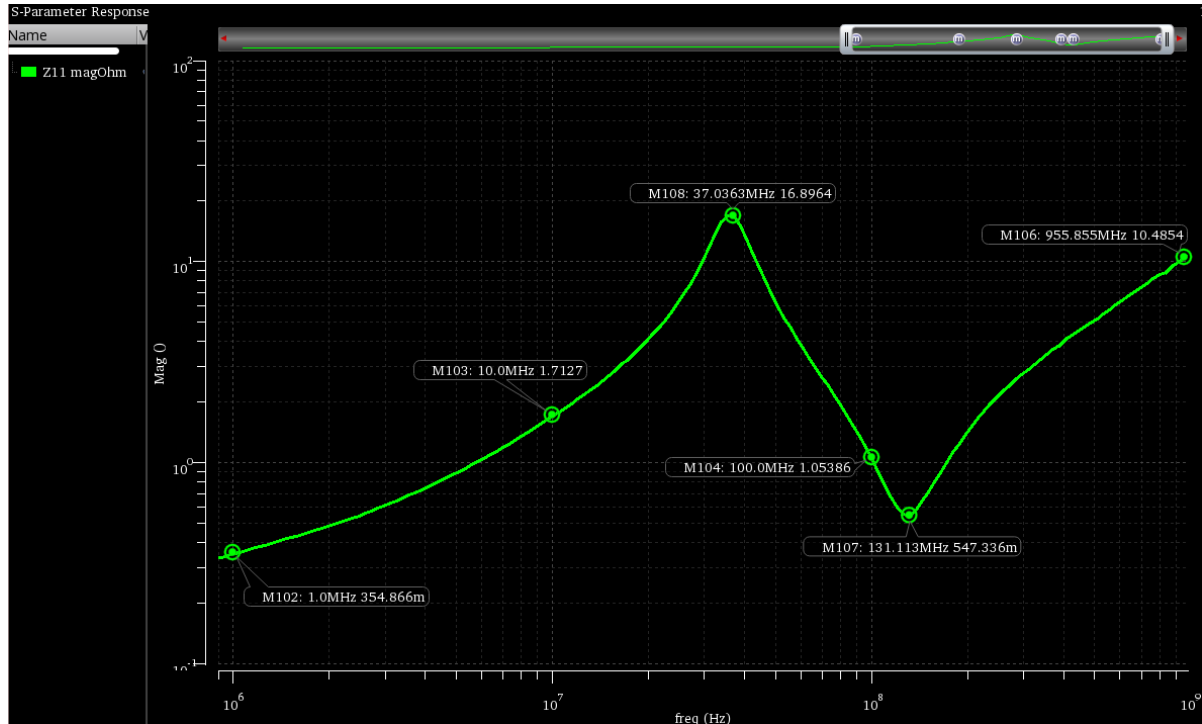


Figure 12: FBP to FBN Path Impedance Including Capacitor

#### A.3 PVDD to PGND loop

Figure 13 shows the impedance plot for the path from a single phase PVDD to its own PGND including two GRM188R61E106MA73 capacitors. The effective inductance at 1 GHz should be kept below 200 pH.

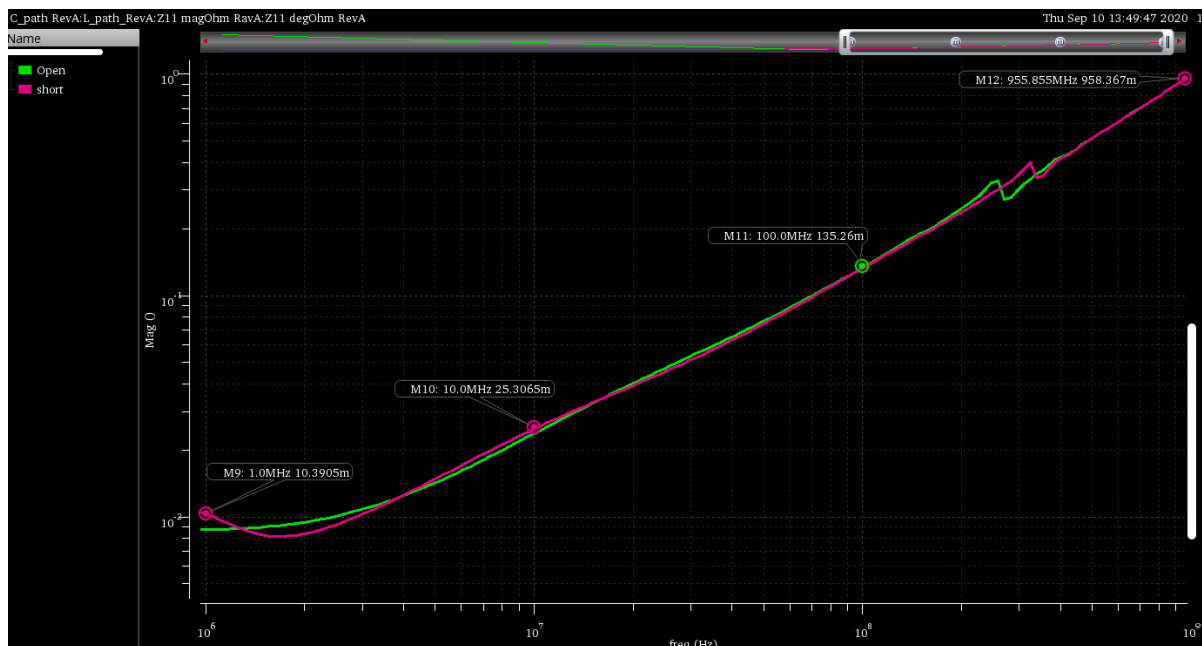


Figure 13: PVDD to PGND Path Impedance Including Capacitors

**Revision History**

Revision	Date	Description
1.1	06-Mar-2023	Added PCB Footprint
1.0	04-Feb-2022	Initial version.

**Status Definitions**

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

**RoHS Compliance**

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.



---

## DA914x PCB Layout Recommendations

### Important Notice and Disclaimer

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

[www.renesas.com](http://www.renesas.com)

Contact Information

<https://www.renesas.com/contact/>