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SH7280 Group

MTU2: Output of Complementary Pairs of PWM Signals in Three Phases (Complementary PWM Mode)

Introduction

This application note describes an example of setting up multi-function timer pulse unit 2 (MTU2) for the output of complementary pulse width modulation (PWM) waveforms in three phases with a non-overlapping relationship between states of the positive and inverse signals.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

The sample program employs MTU2 in complementary PWM mode for the three-phase output of complementary PWM waveforms. Figure 1 shows an overview.

1. Channels 3 and 4 of MTU2 are used to make settings for complementary PWM mode (complementary PWM mode 3). The output pins for the positive PWM signals are TIOC3B, TIOC4A, and TIOC4B. The corresponding inverse signals are output on pins TIOC3D, TIOC4C, and TIOC4D. The low level is selected as active for PWM output.
2. For both the positive and inverse signals, MTU2 outputs PWM waveforms with a dead time (interval for preventing short-circuits) in which the state transitions of the positive and inverse signals do not overlap. The duration of the dead time is set to 4 µs.
3. PWM carrier cycle is set to 400 µs.
4. The PWM duty cycle is incremented or decremented by an interrupt signal generated every PWM cycle.
5. Waveforms are output by toggling the level on the TIOC3A pin in synchronization with half cycles of the PWM carrier.

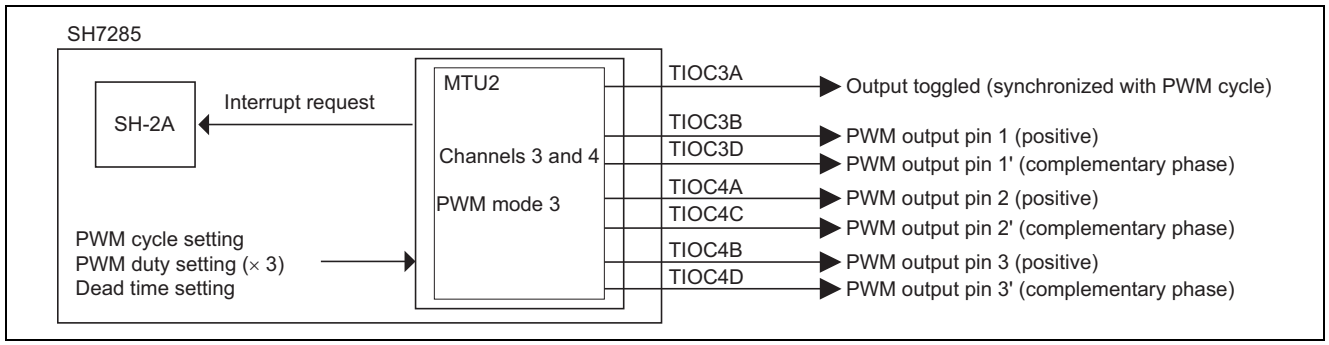


Figure 1 Three-Phase Output of Complementary PWM (Complementary PWM Mode 3)

1.2 Module Used

Channels 3 and 4 of MTU2

1.3 Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
MCU	SH7285 [R5F72856]	
Operating frequency	Internal clock:	Iϕ = 100 MHz
	Bus clock:	Bϕ = 50 MHz
	Peripheral clock:	Pϕ = 50 MHz
	MTU2S clock:	Mϕ = 50 MHz
	AD clock:	Aϕ = 50 MHz
MCU operating mode	Single-chip	
Compiler	SuperH RISC engine C/C++ Compiler Ver.9.01.01 from Renesas Technology	
C compiler options	Default settings of the C compiler	

2. Description of the Sample Application

In this sample program, MTU2 is used in complementary PWM mode.

2.1 Operational Overview of Module Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

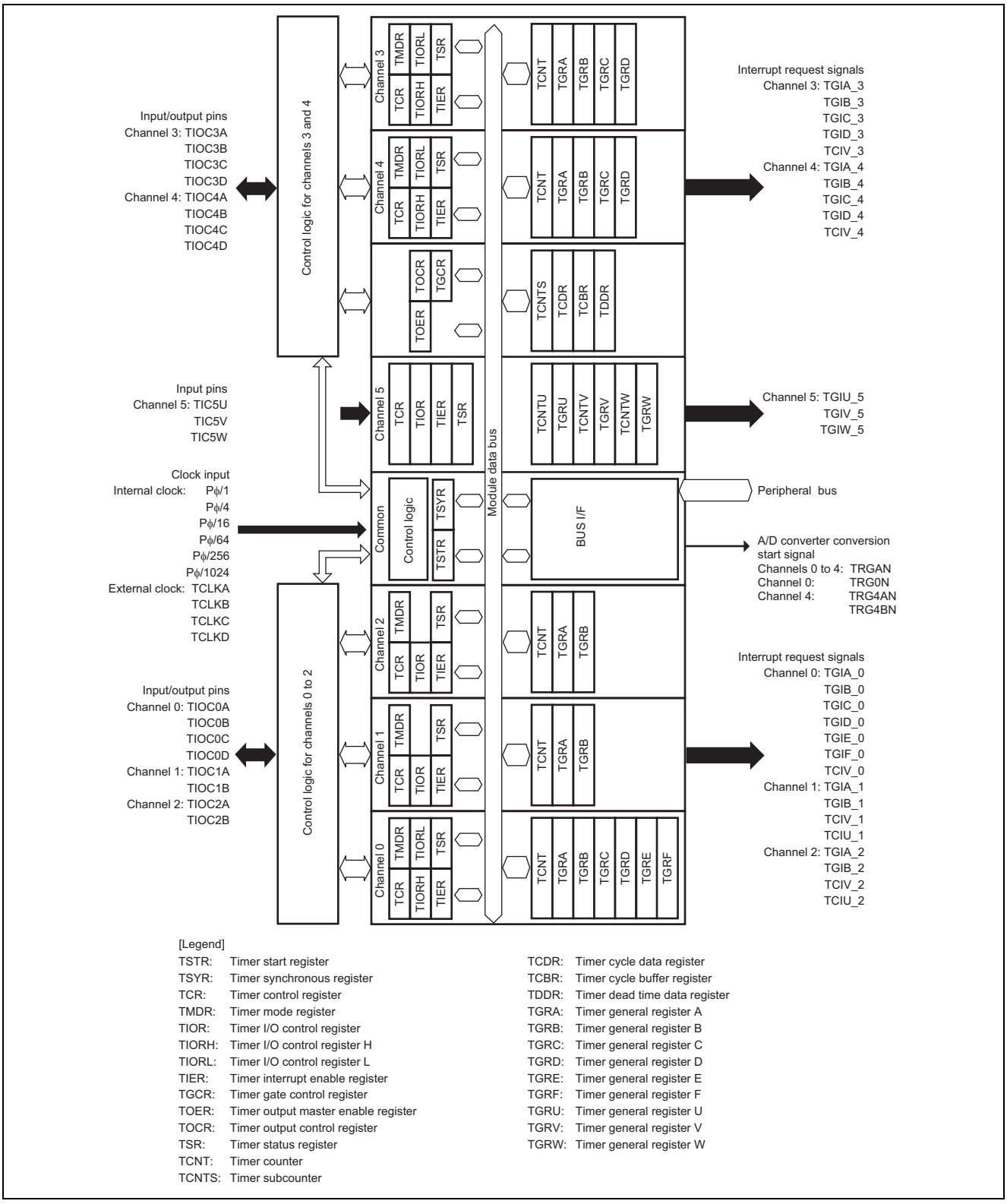
MTU2 is a multi-functional timer unit that has six 16-bit timer channels. Settings for compare-match function, input-capture function, etc. can be made for each channel. Settings for complementary PWM mode and reset-synchronized PWM mode are made for channels 3 and 4, enabling the control of six PWM output lines.

For details on MTU2, see the section on MTU2 in the *SH7280 Group Hardware Manual* (REJ09B0393).

Table 2 gives an overview of MTU2 and figure 2 is a block diagram of MTU2.

Table 2 Overview of MTU2

Item	Description
Number of channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clock	The clock signal for counter input can be selected from among 8 different input clock signals (except for channel 5, with only 4 different clock signals available).
Operation of channels 0 to 5	• Waveform output on compare match • Input capture function • Counter clearing • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Input to and output from registers are synchronized with counter operation. • PWM output in up to 12 phases in combination with synchronous operation
Triggers for A/D converter	• A/D converter start trigger can be generated. • In complementary PWM mode, interrupts at the crest and trough of the counter value and A/D converter start triggers can be skipped.
Buffered operation	• Settings for buffered operation of registers can be made to channels 0, 3, and 4.
Operating modes	• Settings for PWM mode can be made on channels 0 to 4. • Settings for phase counting mode can be set for each of channels 1 and 2 individually. • Waveform output in a total of six phases, including the positive and inverse signals for three phases, is possible in reset-synchronized PWM mode or complementary PWM mode.
Interrupt requests	• 28 different interrupt sources (interrupt generation by compare match, input capture, etc.)
Others	• Cascade-connection operation • High-speed access by internal 16-bit bus • Automatic transfer of register data is enabled. • Module standby mode can be set. • Dead time compensation counter is available in channel 5.



[Legend]

TSTR:	Timer start register	TCDR:	Timer cycle data register
TSYR:	Timer synchronous register	TCBR:	Timer cycle buffer register
TCR:	Timer control register	TDDR:	Timer dead time data register
TMDR:	Timer mode register	TGRA:	Timer general register A
TIOR:	Timer I/O control register	TGRB:	Timer general register B
TIORH:	Timer I/O control register H	TGRC:	Timer general register C
TIORL:	Timer I/O control register L	TGRD:	Timer general register D
TIER:	Timer interrupt enable register	TGRE:	Timer general register E
TGCR:	Timer gate control register	TGRF:	Timer general register F
TOER:	Timer output master enable register	TGRU:	Timer general register U
TOCR:	Timer output control register	TGRV:	Timer general register V
TSR:	Timer status register	TGRW:	Timer general register W
TCNT:	Timer counter		
TCNTS:	Timer subcounter		

Figure 2 Block Diagram of MTU2

2.1.2 Complementary PWM Mode

Complementary PWM mode can be set up for the combination of channels 3 and 4 of MTU2. In complementary PWM mode, PWM waveforms are output in three phases with a non-overlapping relationship between the states of the positive and inverse signals. The output of PWM waveforms which do not have the non-overlapping time (interval for preventing short circuits) can also be set up. PWM output pins for complementary PWM mode are pins TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D. Furthermore, toggling of the output level in synchronization with the PWM cycle can be set up on the TIOC3A pin.

Figure 3 is a block diagram of channels 3 and 4 of MTU2 in complementary PWM mode.

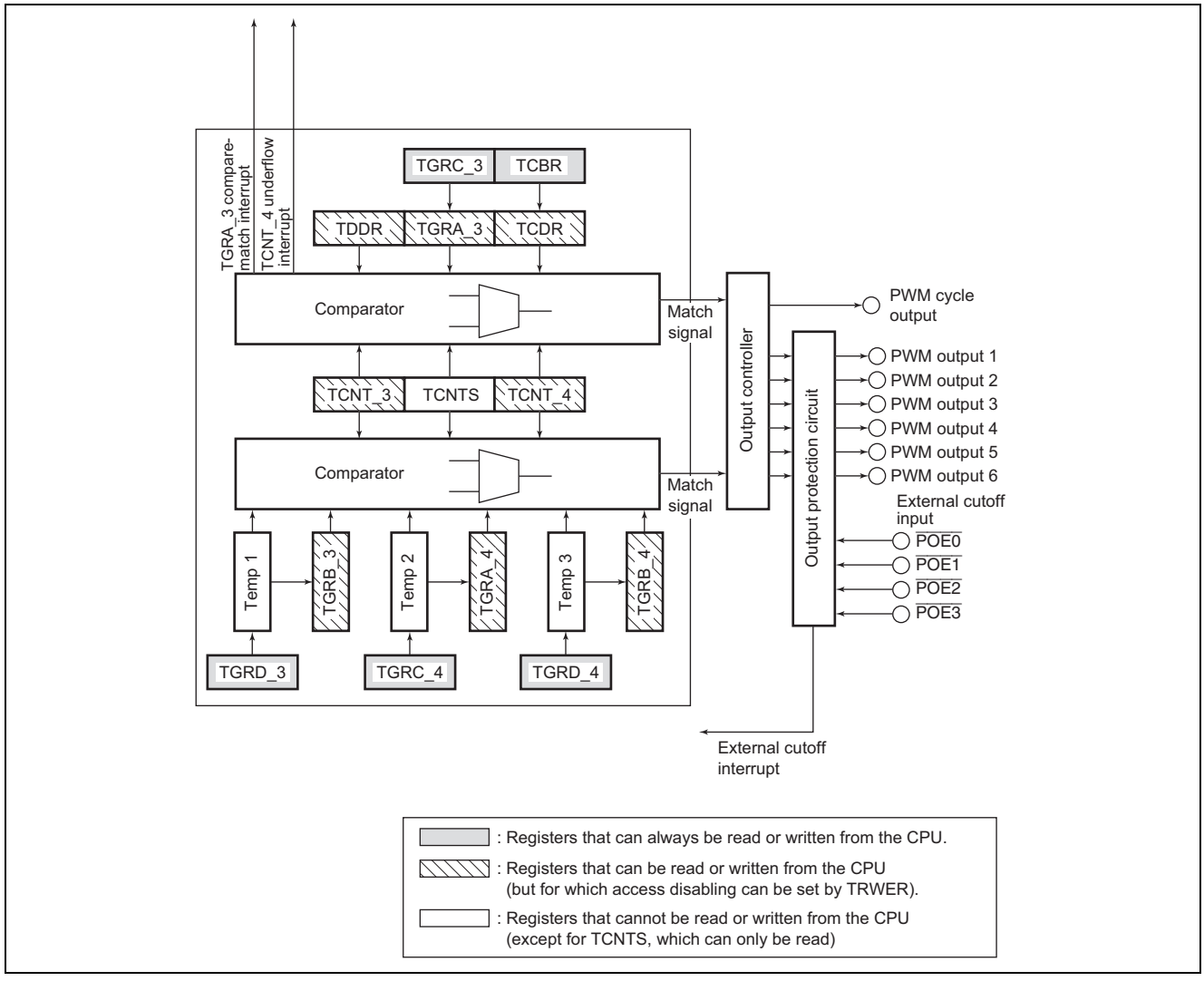


Figure 3 Block Diagram of Channels 3 and 4 in Complementary PWM Mode

- Timer general register A_3 (TGRA_3)
  TGRA_3 functions as a compare match register. The upper limit (1/2 carrier cycle + dead time) for counting is set here. Moreover, when the value in this register is changed during timer operation, the new value is that set in timer general register C_3 (TGRC_3).
- Timer general register B_3 (TGRB_3)
  TGRB_3 functions as a comparison register. The duty cycle of the PWM waveforms which are output from pins TIOC3B and TIOC3D is set by the values in this register. Moreover, when the value in this register is changed during timer operation, the new value is that set in timer general register D_3 (TGRD_3).
- Timer general register C_3 (TGRC_3)
  TGRC_3 functions as the buffer register for TGRA_3. During timer operation, the values set in this register are written to TGRA_3.
- Timer general register D_3 (TGRD_3)
  TGRD_3 functions as the buffer register for TGRB_3. During timer operation, the values set in this register are written to TGRB_3.
- Timer general register A_4 (TGRA_4)
  TGRA_4 functions as a comparison register. The duty cycle of PWM the waveforms which are output from pins TIOC4A and TIOC4C are set in this register. Moreover, when the value in this register is changed during timer operation, the value is that set in the timer general register C_4 (TGRC_4).
- Timer general register B_4 (TGRB_4)
  TGRB_4 functions as a comparison register. The duty cycle of the PWM waveforms which are output from pins TIOC4B and TIOC4D are set in this register. Moreover, when the value in this register is changed during timer operation, the value to be changed is set in the timer general register D_4 (TGRD_4).
- Timer general register C_4 (TGRC_4)
  TGRC_4 functions as a buffer register for TGRA_4. During timer operation, the values set in this register are written to TGRA_4.
- Timer general register D_4 (TGRD_4)
  TGRD_4 functions as a buffer register for TGRB_4. During timer operation, the values set in this register are written to TGRB_4.
- Temporary registers 1, 2, and 3 (Temp1, 2, and 3)
  Temporary registers 1, 2, and 3 are between the respective buffer and comparison registers. Data written in a buffer register are transferred to the corresponding temporary register and then to the comparison register. The temporary registers cannot be accessed by the CPU.
- Timer counter _3 (TCNT_3)
  TCNT_3 is a 16-bit counter. TCNT_3 decrementation on compare matches with TGRA_3, and incrementation on compare matches with the timer dead-time data register (TDDR).
- Timer counter _4 (TCNT_4)
  TCNT_4 is a 16-bit counter. TCNT_4 decrementation on compare matches with the timer cycle data register (TCDR), and incrementation when timer counting reaches H'0000.
- Timer dead time data register (TDDR)
  The TDDR is a 16-bit readable and writable register. The dead time for the PWM waveforms is set in this register.
- Timer cycle data register (TCDR)
  The TCDR is a 16-bit register. The setting in this register defines half of the cycle for the PWM carrier.
- Timer cycle buffer register (TCBR)
  The TCBR functions as the buffer register for the TCDR. During timer operation, the values set in this register are written to TCDR.

2.2 Operation of the Sample Program

2.2.1 Settings for Operation of the Sample Program

In this sample program, the output of complementary PWM waveforms in three phases on channels 3 and 4 of MTU2 is obtained by selecting complementary PWM mode 3. An output level is also toggled in synchronization with the PWM carrier cycle. Table 3 gives the setting conditions for operation in complementary PWM mode in this sample program. Figure 4 shows a sample of output waveforms in complementary PWM mode.

Table 3 Setting for Operation in Complementary PWM Mode

Item	Description
Channels in use	3 and 4
Operating mode	Complementary PWM mode 3 (data transfer at the crest and trough of the counter value)
Functions of pins	• TIOC3A pin: Output toggled in synchronization with the PWM cycle • TIOC3B pin: PWM output 1 (positive waveform) • TIOC3D pin: PWM output 1' (inverse waveform for PWM output 1) • TIOC4A pin: PWM output 2 (positive waveform) • TIOC4C pin: PWM output 2' (inverse waveform for PWM output 2) • TIOC4B pin: PWM output 3 (positive waveform) • TIOC4D pin: PWM output 3' (inverse waveform for PWM output 3)
Active level	• Output of positive signal: Active low • Output of inverse signal: Active low
Counter clock	12.5 MHz (Pϕ clock frequency divided by 4)
PWM carrier cycle	400 µs (carrier frequency: 2.5 kHz)
Short-circuit prevention interval (dead time)	4 µs
PWM duty cycle	• Initial duty cycle for PWM outputs 1, 2, 3: 50% PWM duty cycle value is updated every time the TGRA_3 interrupt is generated (setting is incremented or decremented).
Interrupt	• Compare match interrupt for TGRA_3 A TGRA_3 compare match is generated once per PWM-carrier cycle.

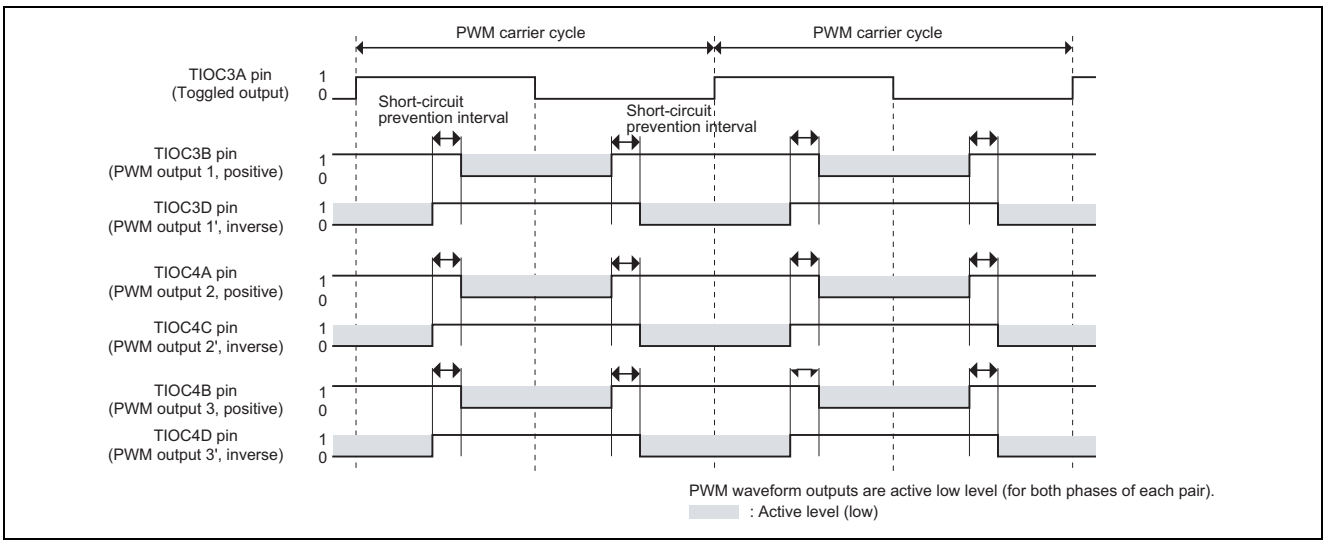


Figure 4 Output Waveforms in Complementary PWM Mode Operation

2.2.2 Description of Operation by the Sample Program

1. Operation of Timer Counters

   Figure 5 shows the operation of two timer counters in complementary PWM mode. Counters TCNT_3 and TCNT_4 of channels 3 and 4 count up and then down. The initial setting of the TCNT_3 counter is the same as the value set in the TDDR. The initial setting of the TCNT_4 counter is H'0000. Timer counting starts simultaneously on channels 3 and 4.

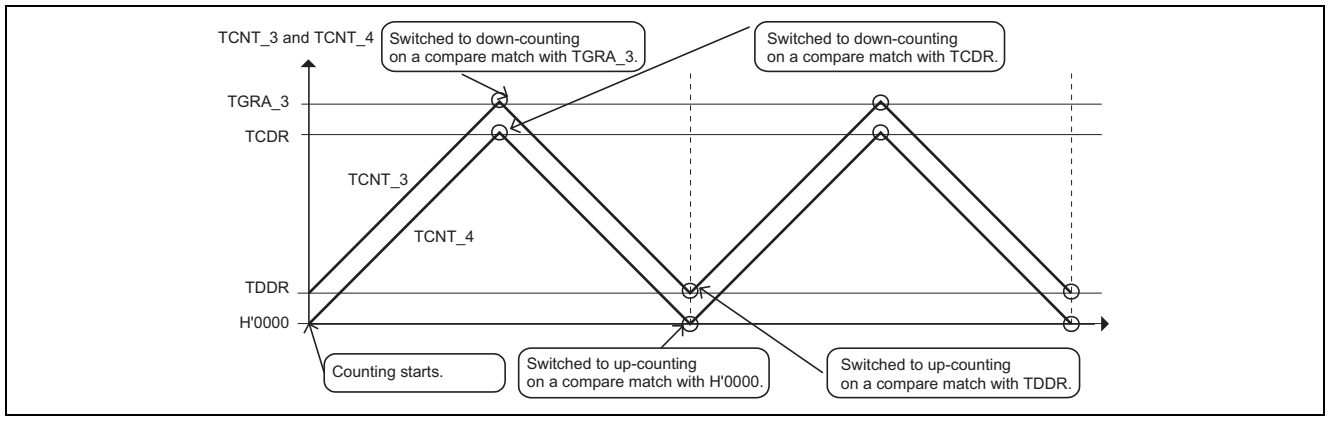


Figure 5 Operation of Timer Counters

2. PWM Waveform Output

   Figure 6 shows the output of PWM waveforms in complementary PWM mode. The counters for PWM output are constantly compared with the comparison registers (TGRB_3, TGRA_4, and TGRB_4). When the counter values match the values of these registers, the output levels of the positive and inverse PWM signals are switched according to the values of bits OLSN and OLSP in the timer output control register (TOCR).

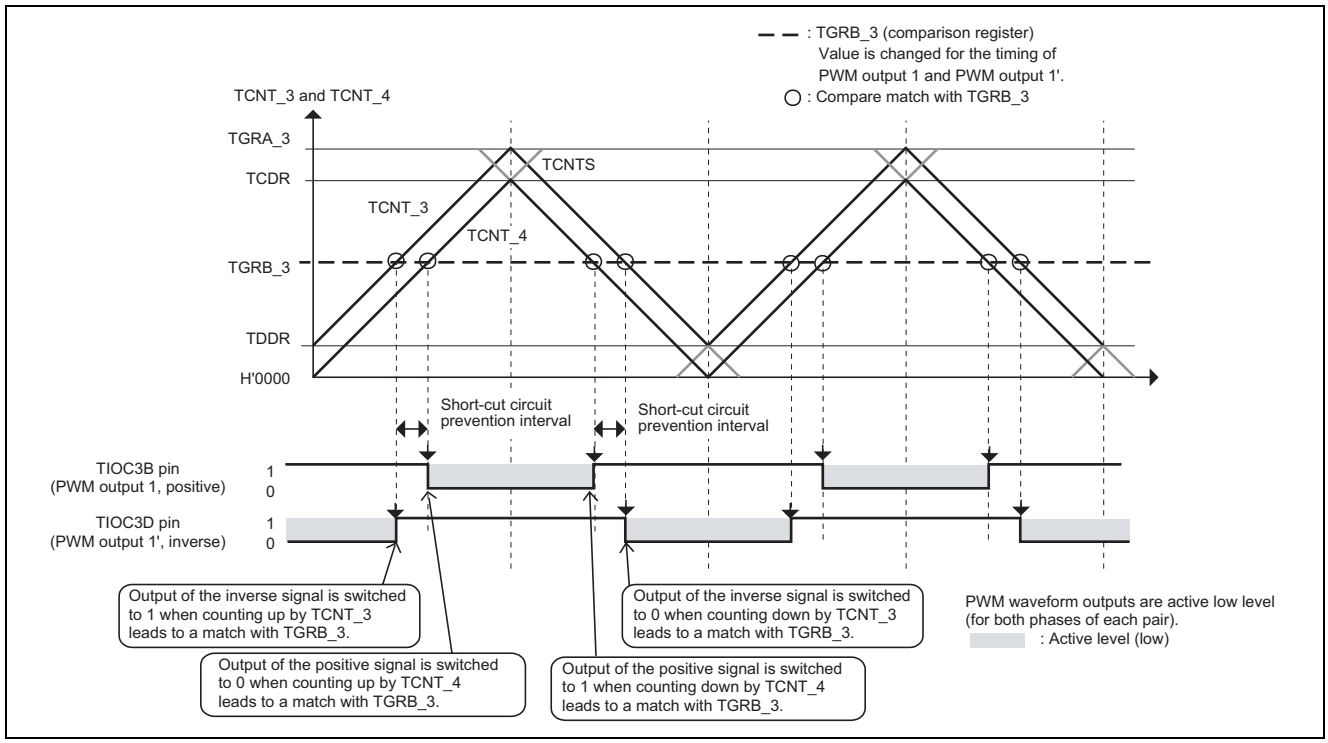


Figure 6 Output of PWM Waveforms in Complementary PWM Mode

3. Changes to PWM Duty Cycle
   Figure 7 shows the timing of updating values for the PWM duty cycle. In this sample program, the register settings for PWM duty cycle are incremented or decremented from the handler for a compare-match interrupt with TGRA_3 (that generated at the highest counter value). Changes to three buffer registers TGRD_3, TGRC_4, and TGRD_4 are used to increment or decrement the values of PWM duty cycle. When the duty cycle is changed, make sure that the last setting to be made is that for TRGR_4. Furthermore, if the value in TGRD_4 is neither incremented nor decremented, make sure that a value is written to TGRD_4 after the registers with values to be incremented or decremented have been updated.

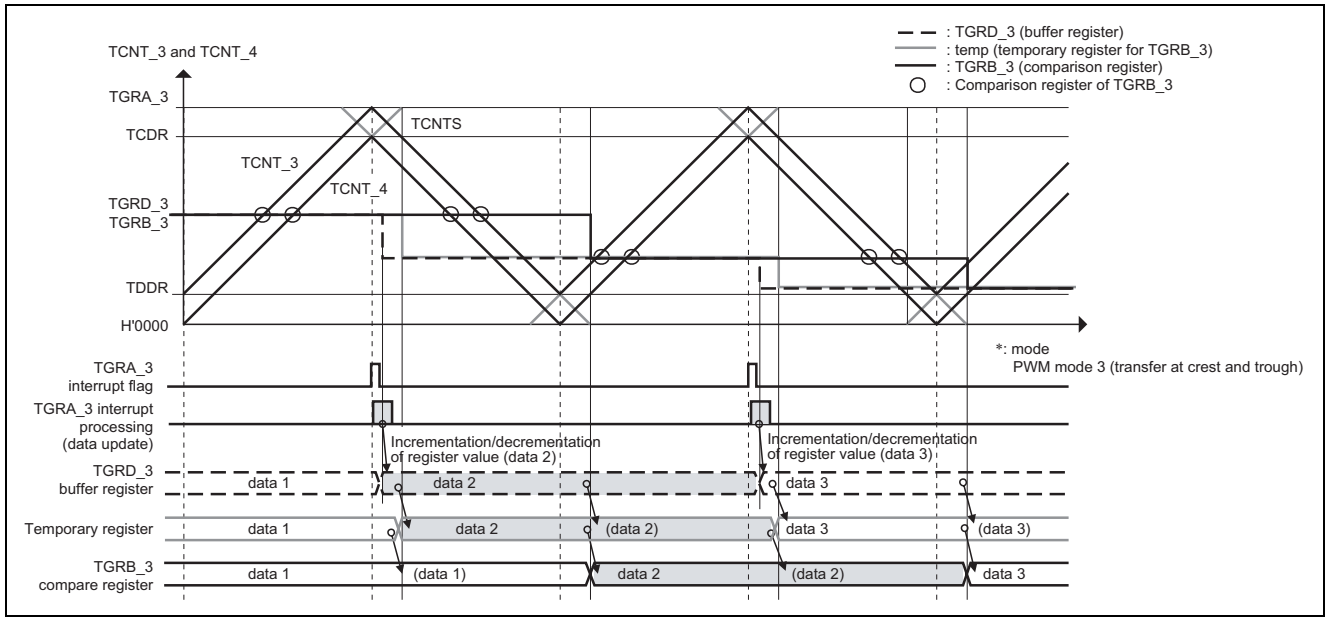


Figure 7 Timing of Updating the PWM Duty Cycle

4. Output Toggling in Synchronization with the PWM Cycle
   Figure 8 shows the operations for toggling of an output level in synchronization with the PWM cycle. The PSYE bit in the timer output control register (TOCR) is set to 1 to select toggling of an output in synchronization with the PWM carrier cycle. Toggling is of the signal on the TIOC3A pin. The initial value for output is 1.

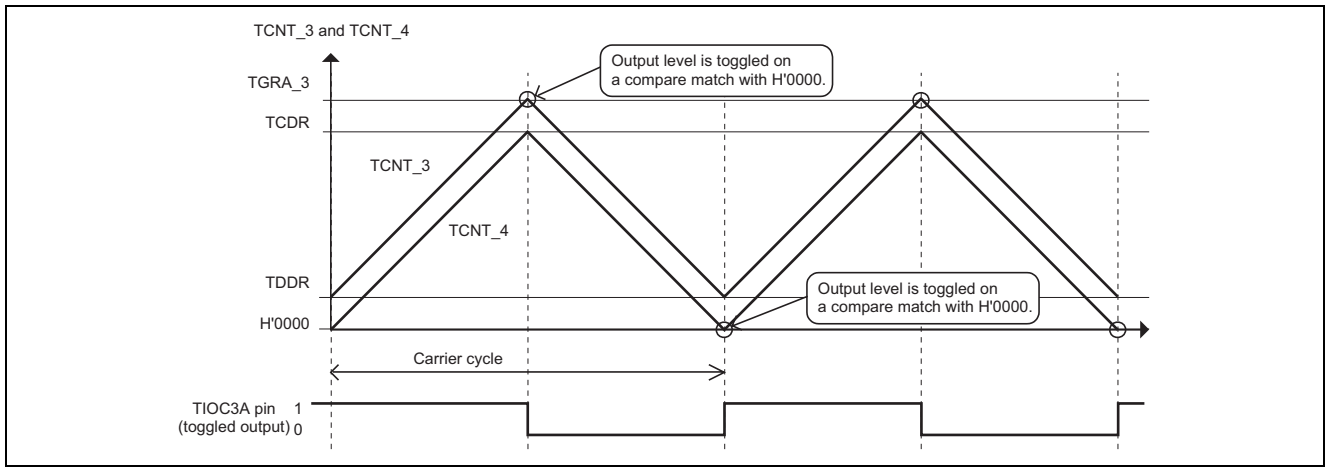


Figure 8 Operation for Toggling an Output in Synchronization with the PWM Cycle

2.2.3 Examples of Output with Desired PWM Duty Cycles

Table 4 gives relations between register settings for PWM duty cycle and the behavior of the positive and inverse waveforms. In complementary PWM mode, when the value in a comparison register (TGRB_3, in this sample program) is H'0000, the positive output remains ON while the inverse output remains OFF; i.e. the output levels are fixed. Furthermore, when the value in the comparison register is greater than or equal to the value in the TGRA_3 register, the level of the positive signal is fixed to the OFF state while the level of the inverse signal is fixed to the ON state.

Figures 9 and 10 shows examples of output waveforms of the positive and inverse signals. When changing the PWM duty cycle, make sure that the values are set in the corresponding buffer registers rather than directly in the comparison registers.

Table 4 Examples of Setting that Control the PWM Duty Cycle and Output Waveforms

	Output Waveforms*[1]		
Value in TGRB_3	**Positive output (TIOC3B pin)**	**Inverse output (TIOC3D pin)**	**Waveform Chart**
TGRB_3 ≥TGRA_3	Fixed to the OFF state (high)	Fixed to the ON state (low)	Figure 9 (a)
Between TGRA_3 and TCDR	Fixed to the OFF state (high)	Output of the OFF waveform (pulse)	—
TGRB_3 = TCDR	Fixed to the OFF state (high)	Output of the OFF waveform (to be a pulse twice the width of the short-circuit prevention interval)	Figure 9 (b)
Between (TCDR – Td) and TCDR	Output of the ON waveform (pulse)	Output of the OFF waveform	—
TGRB_3 = (TCDR – Td)	Output of the ON waveform (to be a pulse twice the width of the short-circuit prevention interval)	Output of the OFF waveform (to be a pulse four times the width of the short-circuit prevention interval)	Figure 9 (c)
Between (TDDR × 2) and (TCDR – Td)	Output of complementary PWM waveforms		—
TGRB_3 = (TDDR × 2)	Output of the OFF waveform (to be a pulse four times the width of the short-circuit prevention interval)	Output of the ON waveform (to be a pulse twice the width of the short-circuit prevention interval)	Figure 10 (a)
Between TDDR and (TDDR × 2)	Output of the OFF waveform	Output of the ON waveform (pulse)	—
TGRB_3 = TDDR	Output of the OFF waveform (to be a pulse twice the width of the short-circuit prevention interval)	Fixed to the OFF state (high)	Figure 10 (b)
Between H'0000 and TDDR	Output of the OFF waveform (pulse)	Fixed to the OFF state (high)	—
TGRB_3 = H'0000	Fixed to the ON state (low)	Fixed to the OFF state (high)	Figure 10 (c)

Note: 1. The active level of the PWM output is set to low. The descriptions of the output waveforms refer to the positive and inverse signals for a single complementary pair.

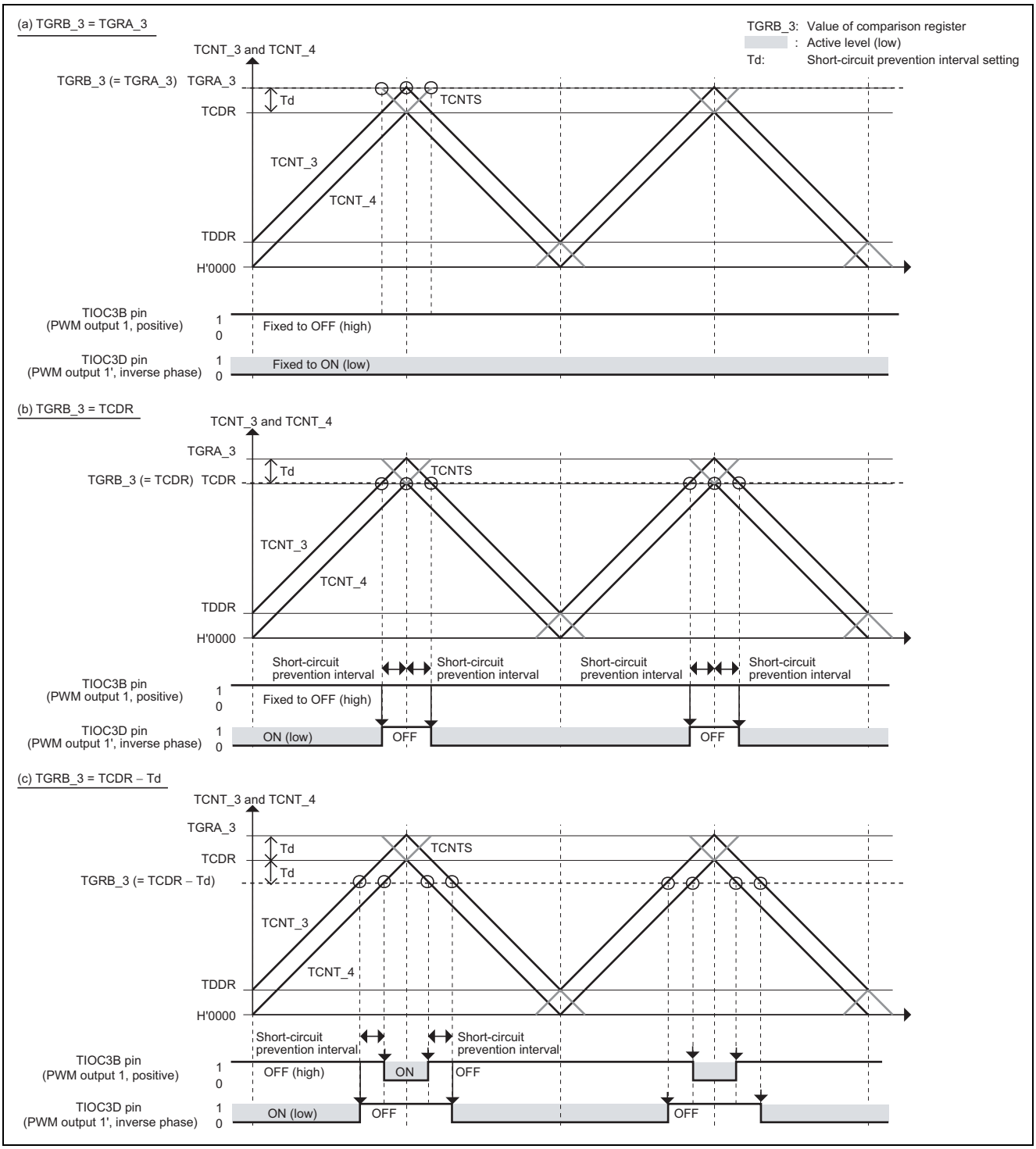


Figure 9 Examples of PWM Waveform Output (1)

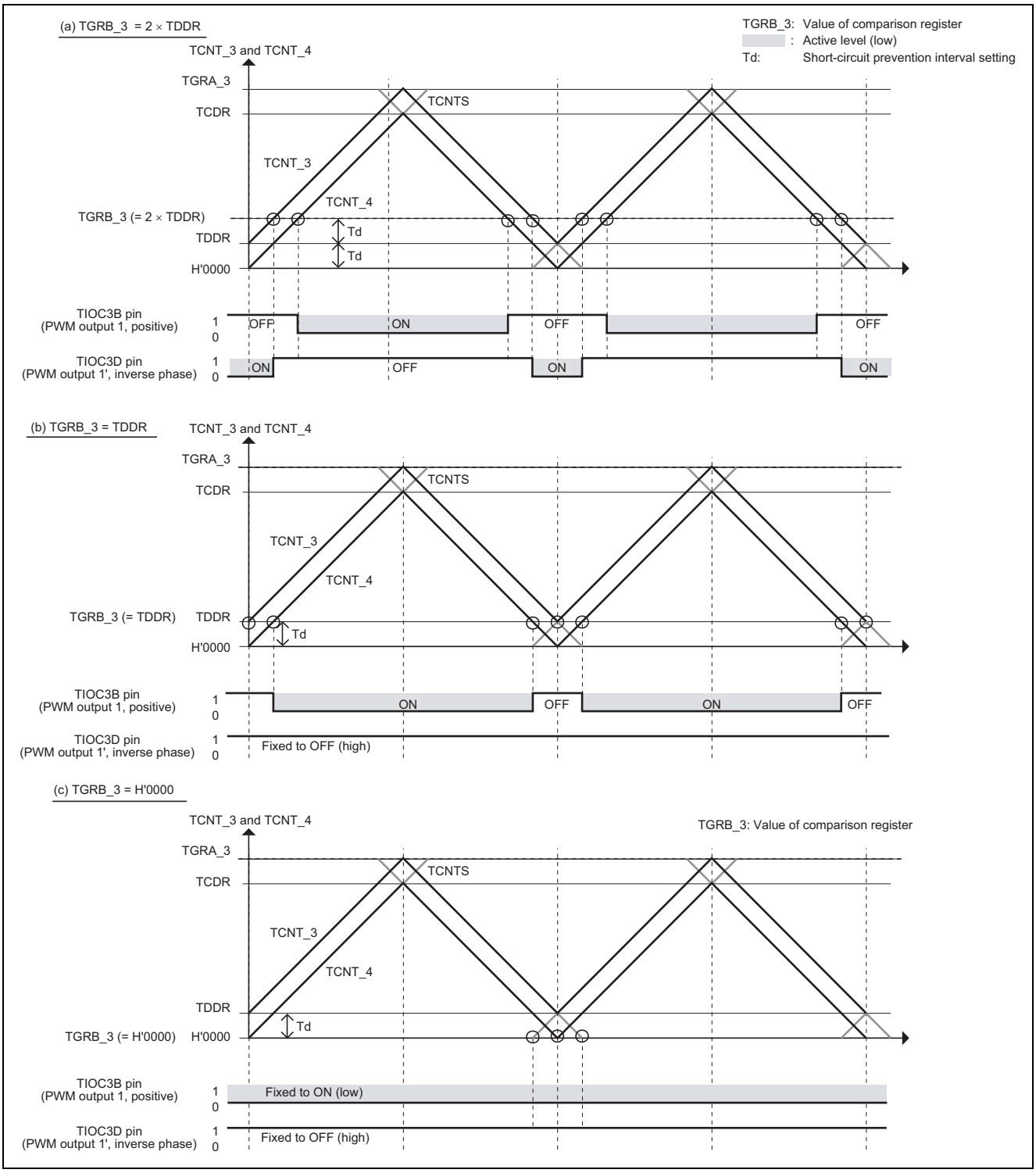


Figure 10 Examples of PWM Waveform Output (2)

2.3 Configuration of the Sample Program

2.3.1 Description of Functions

Table 5 lists functions used in this sample program.

Table 5 Functions Used

Function Name	Label	Description
Main	main ()	Initializes other modules and makes settings for timers of MTU2
Standby setting	stbcr_init ()	Makes setting to release MTU2 from standby
Initialization of MTU2	mtu2_init ()	Initializes MTU2 (channels 3 and 4) Places channels 3 and 4 in complementary PWM mode 3
Initialization of PFC	pfc_init ()	Initializes the pin function controller (PFC) Selects the required MTU2-related pin functions, so that the pins function as timer pins
TGRA_3 interrupt	int_mtu2_tgia3 ()	Handles the TGRA_3 compare match interrupt from MTU2 (channel 3) Increments or decrements the setting to control the three-phase PWM duty cycle Generates an interrupt for every cycle of the PWM carrier cycle (400 μs)

2.3.2 Variable Usage

Table 6 gives a list of variables used in the sample program.

Table 6 Variable Usage

Label Name	Description	Name of Employing Module
Dead_time	Setting for dead time (value set in the TDDR)	mtu2_init ()
C_cycle	1/2 the PWM carrier cycle (value set in the TCBR)	
Pul_cycle	1/2 the PWM carrier cycle + value of dead time (value set in the TGRC_3)	
Pul_pwm_duty1	PWM duty-cycle setting for the PWM1 output (pins TIOC3B and TIOC3D) (value set in the TGRD_3)	mtu2_init () int_mtu2_tgia3 ()
Pul_pwm_duty2	PWM duty-cycle setting for the PWM2 output (pins TIOC4A and TIOC4C) (value set in the TGRC_4)	
Pul_pwm_duty3	PWM duty-cycle setting for the PWM3 output (pins TIOC4B and TIOC4D) (value set in the TGRD_4)	

2.4 Procedure for Setting the Module Used

The following subsections describe the flow of processing by the sample program.

2.4.1 Main Function

Figure 11 shows the flow of processing by the main function.

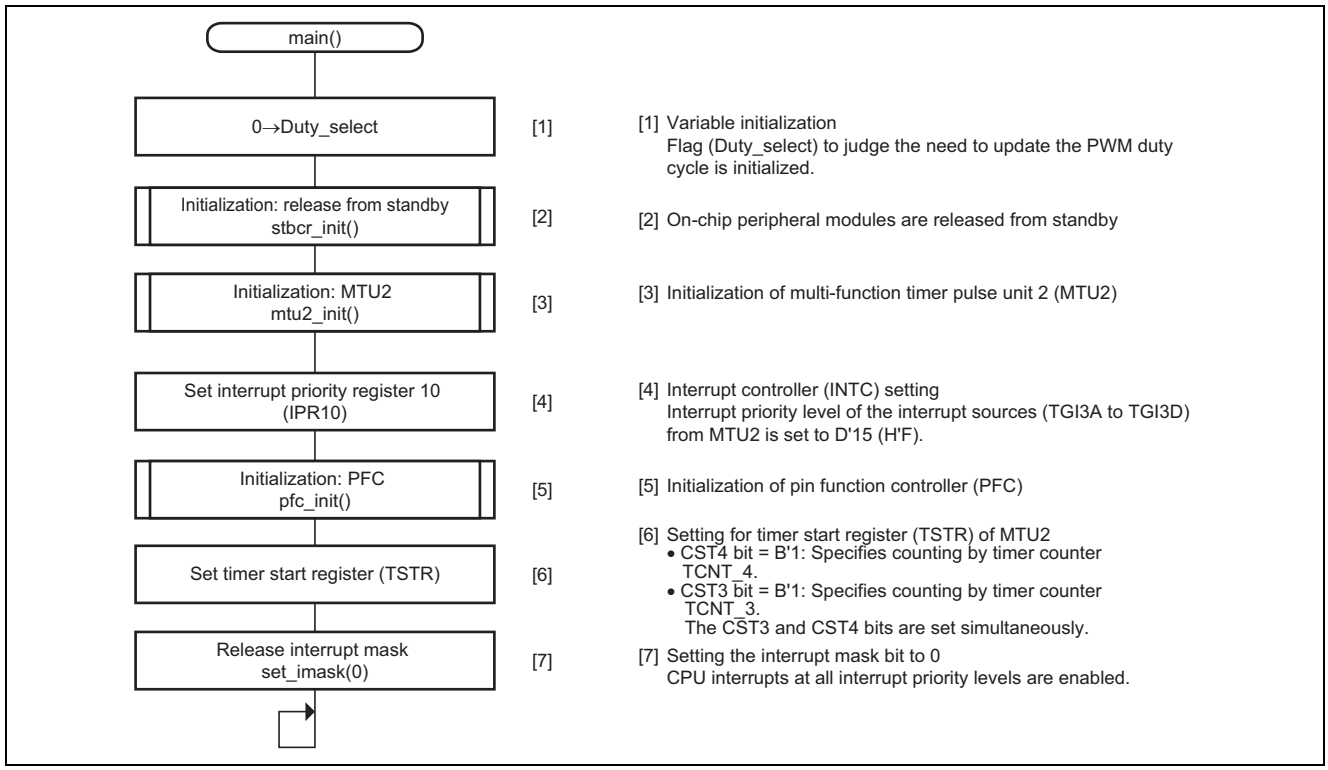


Figure 11 Processing by Function main

2.4.2 Initialization for Standby

Figure 12 shows the flow of processing for standby processing.

Figure 12 Initialization: Release from Standby

2.4.3 Initialization of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 13 shows the flow for initialization of MTU2. Settings are made to set up complementary PWM mode 3 on channels 3 and 4.

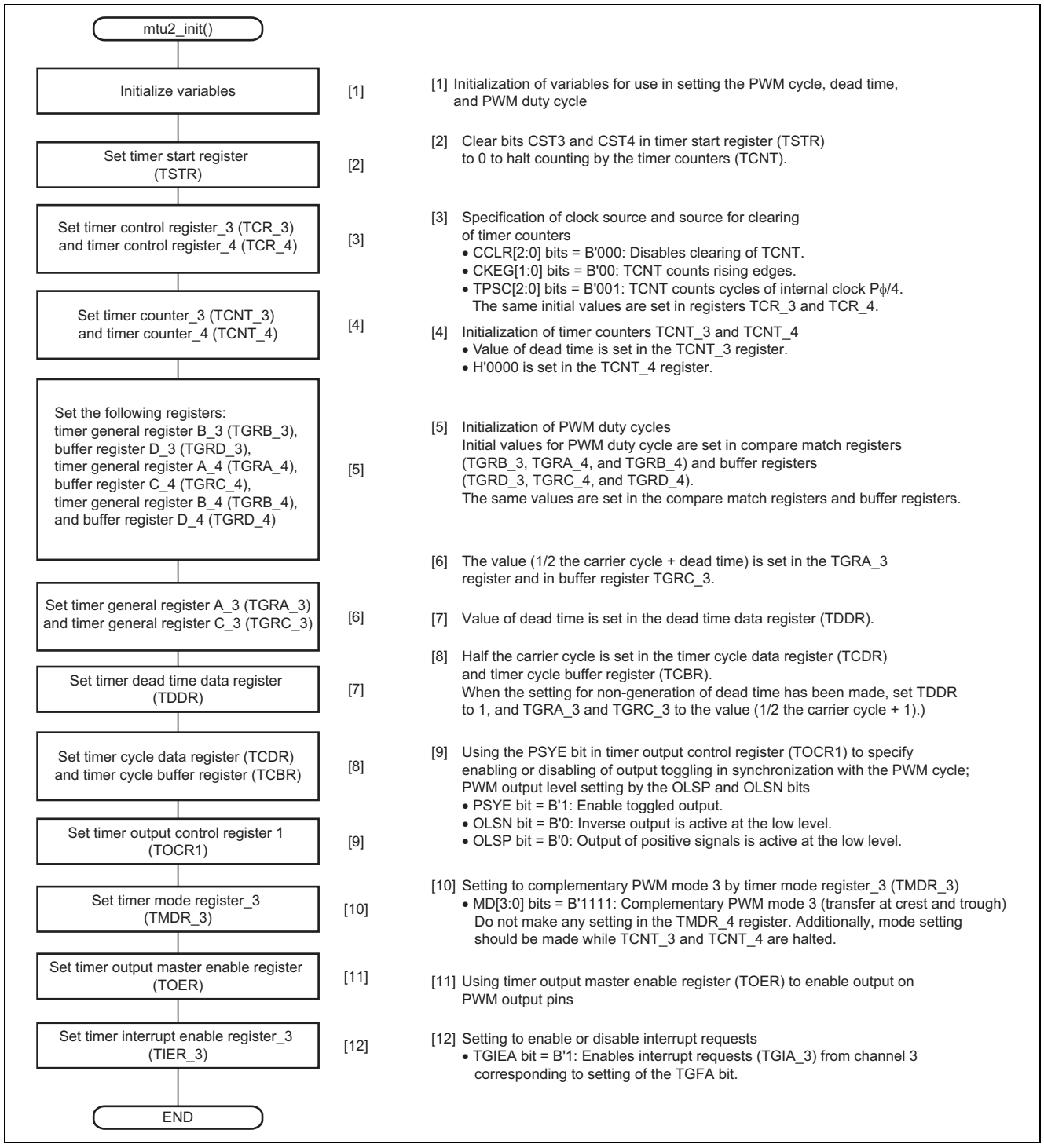


Figure 13 Initialization of MTU2

2.4.4 Initialization of Pin Function Controller (PFC)

Figure 14 shows the flow for initialization of the PFC.

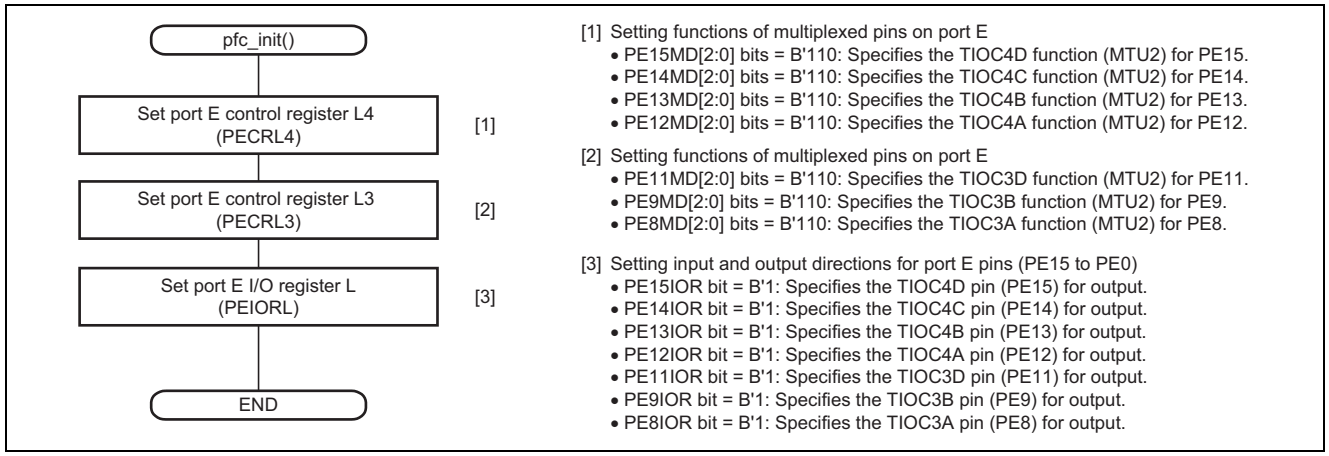


Figure 14 Initialization of Pin Function Controller (PFC)

2.4.5 Handling of the Compare Match Interrupt

Figure 15 shows the flow for handling the compare match interrupt (TRRA_3) from MTU2.

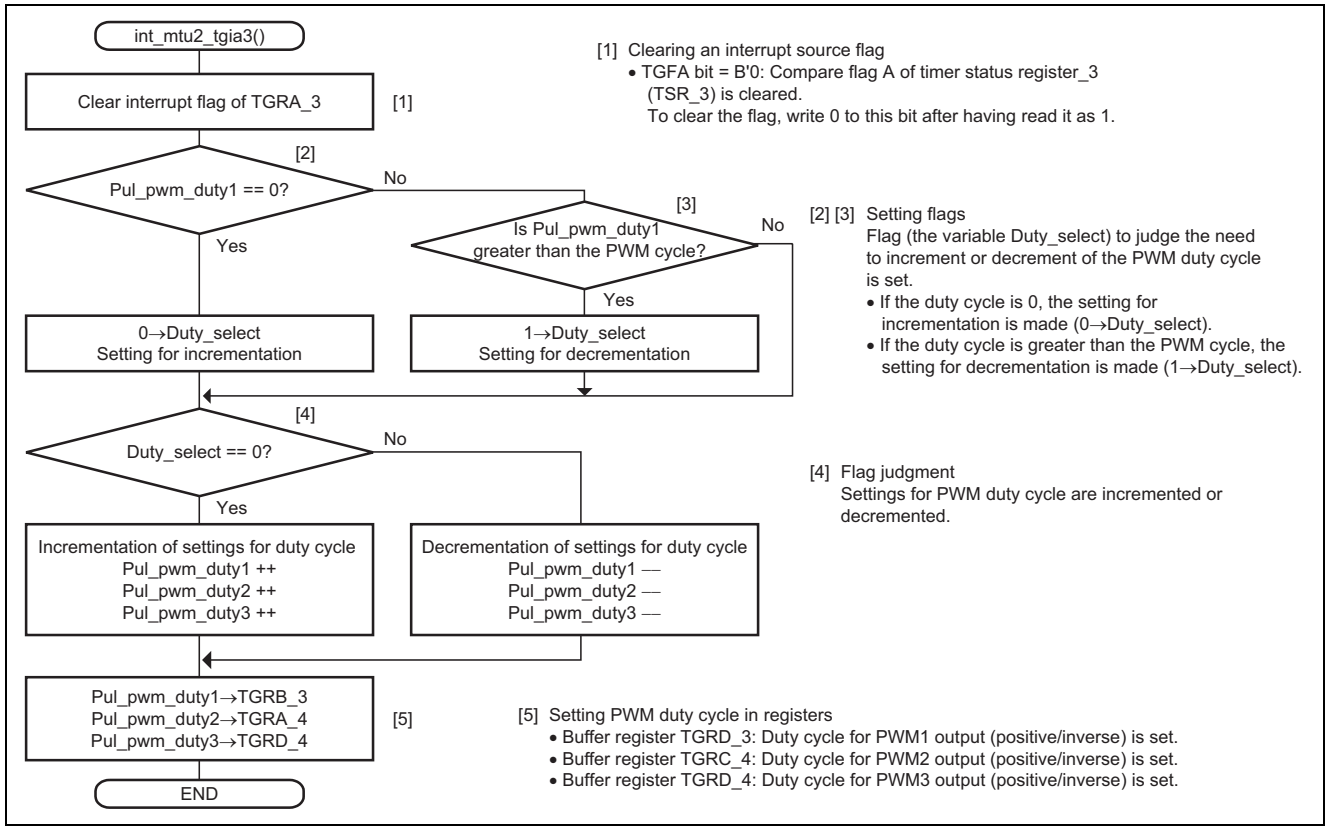


Figure 15 Interrupt Handling

2.5 Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

2.5.1 Clock Pulse Generator (CPG)

Table 7 gives a list of settings for registers of the clock pulse generator (CPG).

Table 7 Clock Pulse Generator (CPG)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	Specifies division ratios for operating frequency • STC[2:0] = B'001: Bus clock (Bϕ) frequency division ratio, × 1/2 • IFC[2:0] = B'000: Internal clock (Iϕ) frequency division ratio, × 1 • PFC[2:0] = B'001: Peripheral clock (Pϕ) frequency division ratio, × 1/2
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	Specifies clock for MTU2S • MSSCS[1:0] = B'01: The PLL output clock is selected as the source clock. • MSDIVS[1:0] = B'01: Division ratio for the source clock = 1/2
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	Specifies clock for A/D converter • ASSCS[1:0] = B'01: The PLL output clock is selected as the source clock. • ASDIVS[1:0] = B'01: Division ratio for the source clock = 1/2

2.5.2 Power-Down Modes

Table 8 gives register settings related to low-power modes.

Table 8 Power-Down Modes

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFE 0408	H'5E	Settings for the operation of various modules • HIZ = B'0: Pin states are held in software standby mode. • MSTP36 = B'1: Clock supply to MTU2S halted. • MSTP35 = B'0: MTU2 runs. • MSTP34 = B'1: Clock supply to POE2 halted. • MSTP33 = B'1: Clock supply to IIC3 halted. • MSTP32 = B'1: Clock supply to ADC0 halted.

2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 9 gives a list of settings for registers of multi-function timer pulse unit 2 (MTU2).

Table 9 Multi-Function Timer Pulse Unit 2 (MTU2)

Register Name	Address	Setting	Description
Timer control register_3 (TCR_3)	H'FFFE 4200	H'01	Sets details of TCNT control. • CCLR[2:0] = B'000: TCNT clearing disabled • CKEG[1:0] = B'00: TCNT counts rising edge. • TPSC[2:0] = B'001: TCNT counts cycles of internal clock Pϕ/4.
Timer control register_4 (TCR_4)	H'FFFE 4201	H'01	Sets details of TCNT control. • CCLR[2:0] = B'000: TCNT clearing disabled • CKEG[1:0] = B'00: TCNT counts rising edge. • TPSC[2:0] = B'001: TCNT counts cycles of internal clock Pϕ/4.
Timer counter_3 (TCNT_3)	H'FFFE 4210	D'50	16-bit counter For complementary PWM mode, the initial value is the same as that of the timer dead time data register (TDDR).
Timer counter_4 (TCNT_4)	H'FFFE 4212	H'0000	16-bit counter Initial value is set to H'0000.
Timer general register A_3 (TGRA_3)	H'FFFE 4218	D'2550	For complementary PWM mode, the setting is the upper limit (1/2 carrier cycle + dead time) on the value of TCNT_3 is set.
Timer general register C_3 (TGRC_3)	H'FFFE 4224		In complementary PWM mode, the same value set in TGRA_3 is set for initialization of the TGRA_3 buffer register.
Timer general register B_3 (TGRB_3)	H'FFFE 421A	D'1275	For complementary PWM mode, this is the comparison register for PWM output 1, and its setting determines the PWM duty cycle (initial output value).
Timer general register D_3 (TGRD_3)	H'FFFE 4226		In complementary PWM mode, the same value set in TGRB_3 is set for initialization of the TGRB_3 buffer register. Incremented or decremented value of PWM duty cycle is set in this register
Timer general register A_4 (TGRA_4)	H'FFFE 421C	D'1275	For complementary PWM mode, this is the comparison register for PWM output 2, and its setting determines the PWM duty cycle (initial output value).
Timer general register C_4 (TGRC_4)	H'FFFE 4228		In complementary PWM mode, the same value set in TGRA_4 is set for initialization of the TGRA_4 buffer register. Incremented or decremented value of PWM duty cycle is set in this register.

Register Name	Address	Setting	Description
Timer general register B_4 (TGRB_4)	H'FFFE 421E	D'1275	For complementary PWM mode, this is the comparison register for PWM output 3, and its setting determines the PWM duty cycle (initial output value).
Timer general register D_4 (TGRD_4)	H'FFFE 422A		In complementary PWM mode, the same value set in TGRB_4 is set for initialization of the TGRB_4 buffer register. Incremented or decremented value of PWM duty cycle is set in this register
Timer dead time data register (TDDR)	H'FFFE 4216	D'50	16-bit register used only in complementary PWM mode The setting is the offset value (value that determines the dead time) for TCNT_4 and TCNT_3.
Timer cycle data register (TCDR)	H'FFFE 4214	D'2500	Register used only in complementary PWM mode The setting is the upper limit on the value (1/2 the carrier cycle) of TCNT_4.
Timer cycle buffer register (TCBR)	H'FFFE 4222		Register used only in complementary PWM mode Buffer register for the TCDR The setting is the same as that of the TCDR.
Timer output control register 1 (TOCR1)	H'FFFE 420E	H'40	Sets output operation in complementary PWM mode. • PSYE = B'1: Toggled output in synchronization with the PWM cycle is enabled. • TOCL = B'0: Writing to the TOCS, OLSN, and OLSP bits is enabled. • TOCS = B'0: Selects use of the TOCR1 setting • OLSN = B'0: Selects levels for inverse output in complementary PWM mode. Initial output = high, active level = low • OLSP = B'0: Selects levels for output of positive signals in complementary PWM mode. Initial output = high, active level = low
Timer mode register_3 (TMDR_3)	H'FFFE 4202	H'3F	Sets operation mode (channel 3). • BFB = B'1: TGRB and TGRD are used together (buffered operation) • BFA = B'1: TGRA and TGRC are used together (buffered operation) • MD[3:0] = B'1111: Complementary PWM mode 3 (transfer at crest and trough)

Register Name	Address	Setting	Description
Timer mode register_4 (TMDR_4)	H'FFFE 4203	—	Sets operation mode (channel 4). Note: When channel 3 is set to complementary PWM mode, settings made for channel 4 are ineffective (operation is automatically in accord with the settings of channel 3). No setting is made; the register is left at its initial value.
Timer output master enable register (TOER)	H'FFFE 420A	H'FF	Specifies enabling or disabling of output through the MTU2 output pins. • OE4D = B'1: MTU2 output on the TIOC4D pin is enabled. • OE4C = B'1: MTU2 output on the TIOC4C pin is enabled. • OE3D = B'1: MTU2 output on the TIOC3D pin is enabled. • OE4B = B'1: MTU2 output on the TIOC4B pin is enabled. • OE4A = B'1: MTU2 output on the TIOC4A pin is enabled. • OE3B = B'1: MTU2 output on the TIOC3B pin is enabled.
Timer interrupt enable register_3 (TIER_3)	H'FFFE 4208	H'01	Specifies enabling or disabling of interrupt requests. • TGIEA = B'1: Interrupt requests (TGIA) corresponding to setting of the TGFA bit are enabled.
Timer start register (TSTR)	H'FFFF 4280	H'C0	Selects operation or stoppage of TCNT for channels 0 to 4. • CST4 = B'1: TCNT_4 counts • CST3 = B'1: TCNT_3 counts Counting by TCNT_2 to TCNT_0 is stopped. Bit settings for counting by TCNT_4 and TCNT_3 should be made at the same time.

2.5.4 Interrupt Controller (INTC)

Table 10 gives a list of settings for registers of the interrupt controller (INTC).

Table 10 Interrupt Controller (INTC)

Register Name (	Address	Setting	Description
Interrupt priority registers 10 (IPR10)	H'FFFE 0C08	H'00F0	Selects interrupt priority (level 0 to 15). • Bit 15 to 12 = B'0000: MTU2 (TGI2A and TGI2B) interrupt level = 0 • Bit 11 to 8 = B'0000: MTU2 (TCI2V and TCI2U) interrupt level = 0 • Bit 7 to 4 = B'1111: MTU3 (TGI3A to TGI3D) interrupt level = 15 • Bit 3 to 0 = B'0000: MTU3 (TCI3V) interrupt level = 0 In this sample program, TGI3A interrupt is used.

2.5.5 Pin Function Controller (PFC)

Table 11 gives a list of settings for registers of the pin function controller (PFC).

Table 11 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port E control register L4 (PECRL4)	H'FFFE 3A10	H'6666	Specifies functions of multiplexed pins on port E. • PE15MD[2:0] = B'110: Specifies the TIOC4D I/O (MTU2) for PE15. • PE14MD[2:0] = B'110: Specifies the TIOC4C I/O (MTU2) for PE14. • PE13MD[2:0] = B'110: Specifies the TIOC4B I/O (MTU2) for PE13. • PE12MD[2:0] = B'110: Specifies the TIOC4A I/O (MTU2) for PE12.
Port E control register L3 (PECRL3)	H'FFFE 3A12	H'6066	Specifies functions of multiplexed pins on port E. • PE11MD[2:0] = B'110: Specifies the TIOC3D I/O (MTU2) for PE11. • PE10MD[2:0] = B'000: Specifies the PE10 I/O (port) for PE10. • PE9MD[2:0] = B'110: Specifies the TIOC3B I/O (MTU2) for PE9. • PE8MD[2:0] = B'110: Specifies the TIOC3A I/O (MTU2) for PE8.
Port E I/O register L (PEIORL)	H'FFFE 3A06	H'FB00	Specifies input and output directions for port E pins. • PE15IOR = B'1: Specifies the TIOC4D pin (PE15) for output. • PE14IOR = B'1: Specifies the TIOC4C pin (PE14) for output. • PE13IOR = B'1: Specifies the TIOC4B pin (PE13) for output. • PE12IOR = B'1: Specifies the TIOC4A pin (PE12) for output. • PE11IOR = B'1: Specifies the TIOC3D pin (PE11) for output. • PE10IOR = B'0: Specifies the PE10 (port) for input. • PE9IOR = B'1: Specifies the TIOC3B pin (PE9) for output. • PE8IOR = B'1: Specifies the TIOC3A pin (PE8) for output. • PE7IOR to PE0IOR all set to B'0: PE7 to PE0 are input pins.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7280 Group Hardware Manual (REJ09B0393)
  The most up-to-date version of this document is available on the Renesas Technology Website.

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