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April 1st, 2010
Renesas Electronics Corporation

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H8/300L Super Low Power Series

Measuring Pulse Frequency by Event Counting

Introduction

Using the Timer C 8-bit event counter function, this function measures the pulse frequency input through Timer C Event Input Pin (TMIC).

Target Device

H8/38024

Contents

1. Specifications

1. Using the Timer C 8-bit event counter function, this function measures the pulse frequency input through Timer C Event Input Pin (TMIC).
2. Counting rising edge detection operations of a pulse input through TMIC input pin for 1 s, this function stores the pulse count for 1 s into the RAM.
3. The 1-s measurement time is measured using the Timer A clock time-base function.
4. The Timer Counter C (TCC) is set to the up-counter controlled by hardware with UD pin which is connected to GND.

2. Description of Functions Used

1. In this task sample, the Timer C 8-bit event counter function is used to measure the frequency of a pulse input at TMIC input pin.
   a. The block diagram of the Timer C 8-bit event counter function is shown in figure 1 and is described below .
      - Timer Mode Register C (TMC) is an 8-bit read/write register which selects the interval function, controls up/down for Timer Counter C (TCC), and selects the input clock. It can be selected whether TCC up/down control is performed by hardware using UD pin input, or whether TCC functions as an up-counter or a down-counter set by software control.
      - Timer Counter C (TCC) is an 8-bit read-only counter which is counted up/down by an internal clock/external event which is input. The input clock can be selected from a total of eight clocks, namely, clocks obtained by dividing the system clock by 8192, 2048, 512, 64, 16 and 4, and subclock/4, and an external clock. In this sample task, TCC is set to up-counter controlled by hardware, and edge detection of TMIC input pin is selected as the TCC input clock.
      - Timer C Interrupt Request Flag (IRRTC) is set to 1 when TCC overflows. A Timer C interrupt is accepted and Timer C interrupt handling is started when IRRTC is set to 1, Timer C interrupt enable (IENTC) in Interrupt Enable Register 2 (IENR2) is set to 1, and the I bit in Condition Code Register (CCR) is cleared to 0.
      - Timer C Event Input Pin (TMIC) functions as the input pin of a pulse whose frequency is measured.

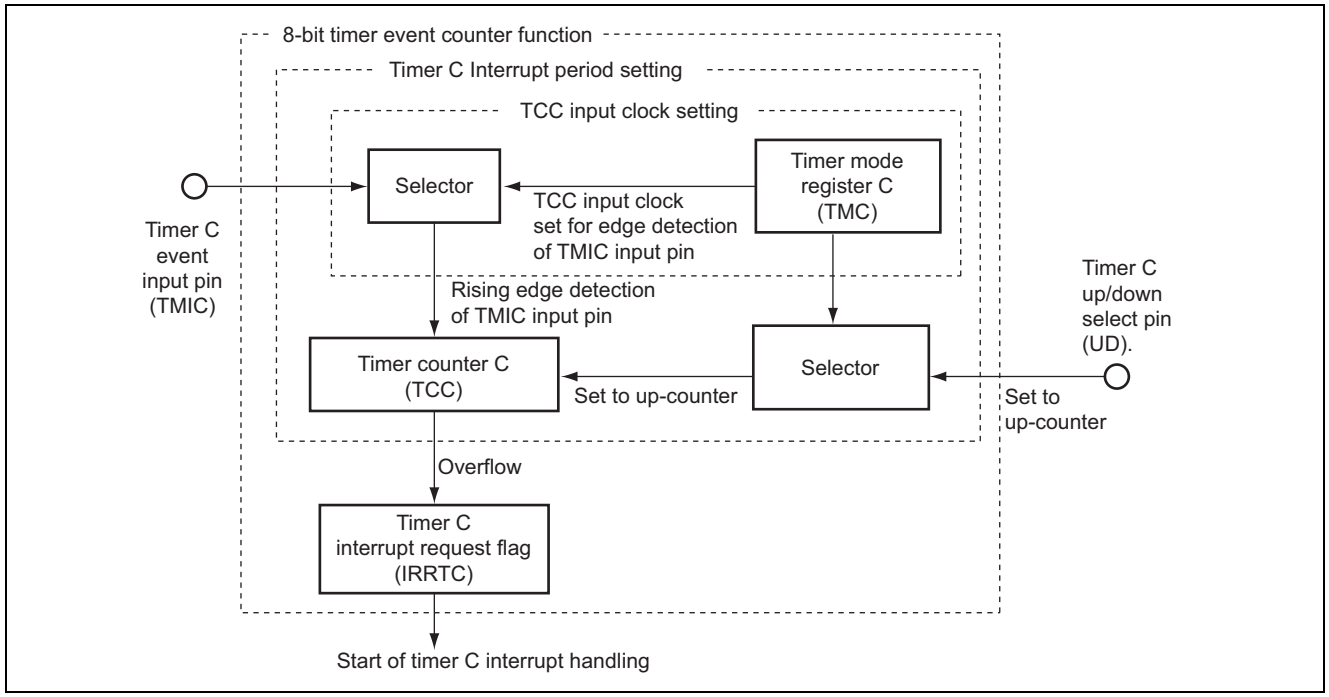


Figure 1 Block Diagram of Timer C Event Counter Function

b. The method to measure frequencies is described below.
- Inputting 256 rising edges to TMIC input pin, TCC overflows to generate a Timer C interrupt.
- The value of the 8-bit counter cnt1 is incremented during Timer C interrupt handling.
- When 1 s has elapsed, the TCC count value is stored in cnt2 and TCC counting up the pulse frequency at the TMIC input pin is completed.
- Frequencies of pulses input to TMIC pin is given by the equation below:

$$\text{Input pulse frequency (Hz)} = (\text{Timer C interrupts}) \times 256 + (\text{Counter value of TCC after 1 s})$$
$$= (\text{cnt1 value}) \times 256 + (\text{cnt2 value})$$

- The counter (cnt1) to count Timer C interrupts is an 8-bit counter, so frequencies of input pulses that can be measured should be 65.535 kHz maximum.
- When the 8-bit counter (cnt1) to count Timer C interrupts overflows, frequency measurement will be stopped immediately and operation ends by writing H'00 in cnt1 and the register (cnt2) which stores the counter value of TCC when 1 s has elapsed.

2. Table 1 shows function assignment in this sample task. The functions are assigned as shown in table 1 and frequencies are measured by the Timer C event counter function.

Table 1 Assignment of Functions

Function	Assignment
PSW	A 5-bit counter using a clock obtained by dividing 32.768 kHz by 4 as input
TMA	Selects PSW and sets the TCA overflow period.
TCA	An 8-bit counter using a clock obtained by dividing 32.768 kHz by 128 as input
TMC	Sets interval function, sets TCC to up-counter by hardware, and sets TCC input clock as edge detection of TMIC input pin
TCC	An 8-bit counter using edge detection of TMIC input pin as input
TLC	Sets reload value of TCC overflow to H”00
$\overline{\text{IRQ1}}$	Sets PB3/AN3/$\overline{\text{IRQ1}}$ pin to TMIC input pin
IEG1	Sets input sense of the TMIC pin to rising edge detection.
IENTA	Enables Timer A interrupt requests
IENTC	Enables Timer C interrupt requests
IRRTA	Indicates whether or not a Timer A interrupt is requested.
IRRTC	Indicates whether or not a Timer C interrupt is requested.
TMIC	Input pin of pulses whose frequency is measured.
UD pin	An input pin to set TCC to up-counter

3. Principle of Operation

1. Figure 2 illustrates the principle of operation of this sample task. As shown in figure 2, the pulse frequency is measured using Timer C 8-bit event counter function by hardware processing and software processing.

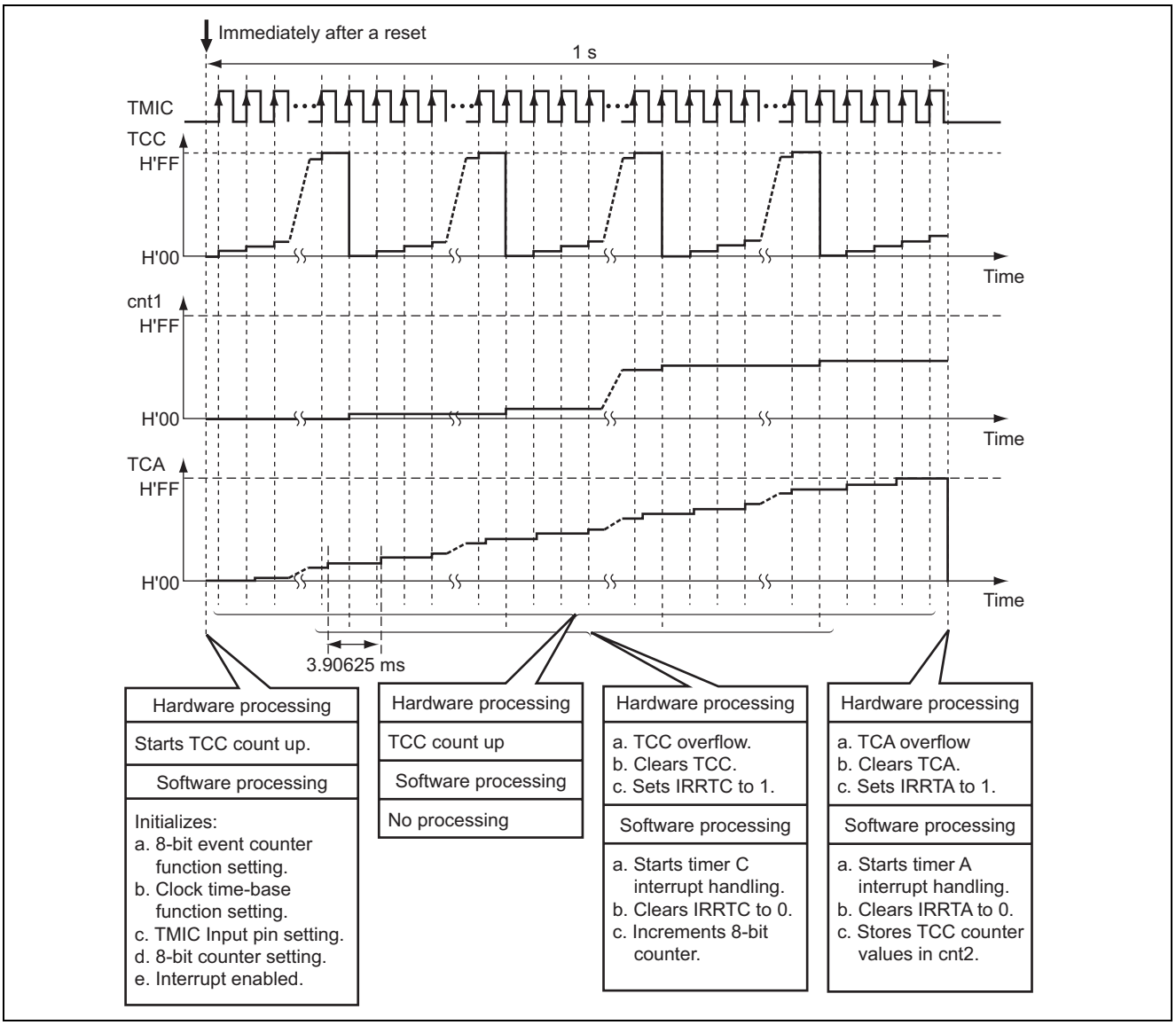


Figure 2 Operation Principle of Frequency Measurement by Timer C 8-bit Event Counter Function

4. Description of Software

4.1 Modules

Table 2 describes the modules in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main Routine	main	Sets Timer C 8-bit event counter function, clock time-base function, the 8-bit counter, enables interrupts, and initializes Timer C after completing measurement.
After 1s	taint	Disables interrupts and stores TCC counter value in cnt2 during Timer A interrupt handling after 1s.
8-Bit Counter	tcint	Increments the 8-bit counter value and processes for cnt1 overflow during Timer C interrupt handling.

4.2 Arguments

Arguments used in this sample task are described in table 3.

Table 3 Description of Internal Registers

Argument	Function	Used in	Data Length	Input/ Output
cnt1	Stores counter value of 8-bit counter after 1 s.	8-bit counter	1 byte	Output
cnt2	Stores TCC counter value after 1 s.	After 1 s	1 byte	Output

4.3 Internal Registers

Table 4 describes the internal registers in this sample task.

Table 4 Description of Internal Registers

Register		Function	Address	Setting
TMA		Timer Mode Register A When TMA = H'18, the Timer A function is set to clock time-base function, TCA input clock source is set to PSW and TCA overflow period to 1s.	H'FFB0	H'18
TCA		Timer Counter A An 8-bit up-counter using a clock obtained by dividing 32.768 kHz by 128 as input	H'FFB1	H'00
TMC		Timer Mode Register C When TMC = H'7F, the Timer C function is set to the interval function, TCC is set to up-counter controlled by hardware, and the TCC input clock is set to input edge detection of TMIC pin.	H'FFB4	H'7F
TCC		Timer Counter C An 8-bit up-counter using input edge detection of TMIC pin as input	H'FFB5	H'00
TLC		Timer Load Register C When TLC = H'00, TCC starts counting up from H'00 and when TCC overflows, H'00 is loaded to TCC.	H'FFB5	H'00
PMR3	UD	Port Mode Register 3 (P30/UD pin switch) When UD = 0, P30/UD functions as P30 input/output pin. When UD = 1, P30/UD functions as UD input pin.	H'FFCA Bit 0	1
PMRB	IRQ1	Port Mode Register B (PB3/AN3/$\overline{\text{IRQ1}}$ pin switch) When $\overline{\text{IRQ1}}$ = 0, PB3/AN3/$\overline{\text{IRQ1}}$ functions as PB3/AN3 input pin. When $\overline{\text{IRQ1}}$ = 1, PB3/AN3/$\overline{\text{IRQ1}}$ functions as $\overline{\text{IRQ1}}$/TMIC input pin.	H'FFEE Bit 3	1
IEGR	IEG1	IRQ Edge Select Register (IRQ1 Edge Select) When IEG1 = 0, edge detection of TMIC input pin is set to falling edge detection. When IEG1 = 1, edge detection of TMIC input pin is set to rising edge detection.	H'FFF2 Bit 1	1
IENR1	IENTA	Interrupt Enable Register 1 (Timer A Interrupt Enable) When IENTA = 0, Timer A interrupt request is disabled. When IENTA = 1, Timer A interrupt request is enabled.	H'FFF3 Bit 7	1
IENR2	IENTC	Interrupt Enable Register 2 (Timer C Interrupt Enable) When IENTC = 0, Timer C interrupt request is disabled. When IENTC = 1, Timer C interrupt request is enabled.	H'FFF4 Bit 1	1
IRR1	IRRTA	Interrupt Request Register 1 (Timer A Interrupt Request Flag) When IRRTA = 0, Timer A interrupt is not requested. When IRRTA = 1, Timer A interrupt is requested.	H'FFF6 Bit 7	0
IRR2	IRRTC	Interrupt Request Register 2 (Timer C Interrupt Request Flag) When IRRTC = 0, Timer C interrupt is not requested. When IRRTC = 1, Timer C interrupt is requested.	H'FFF7 Bit 1	0

4.4 RAM

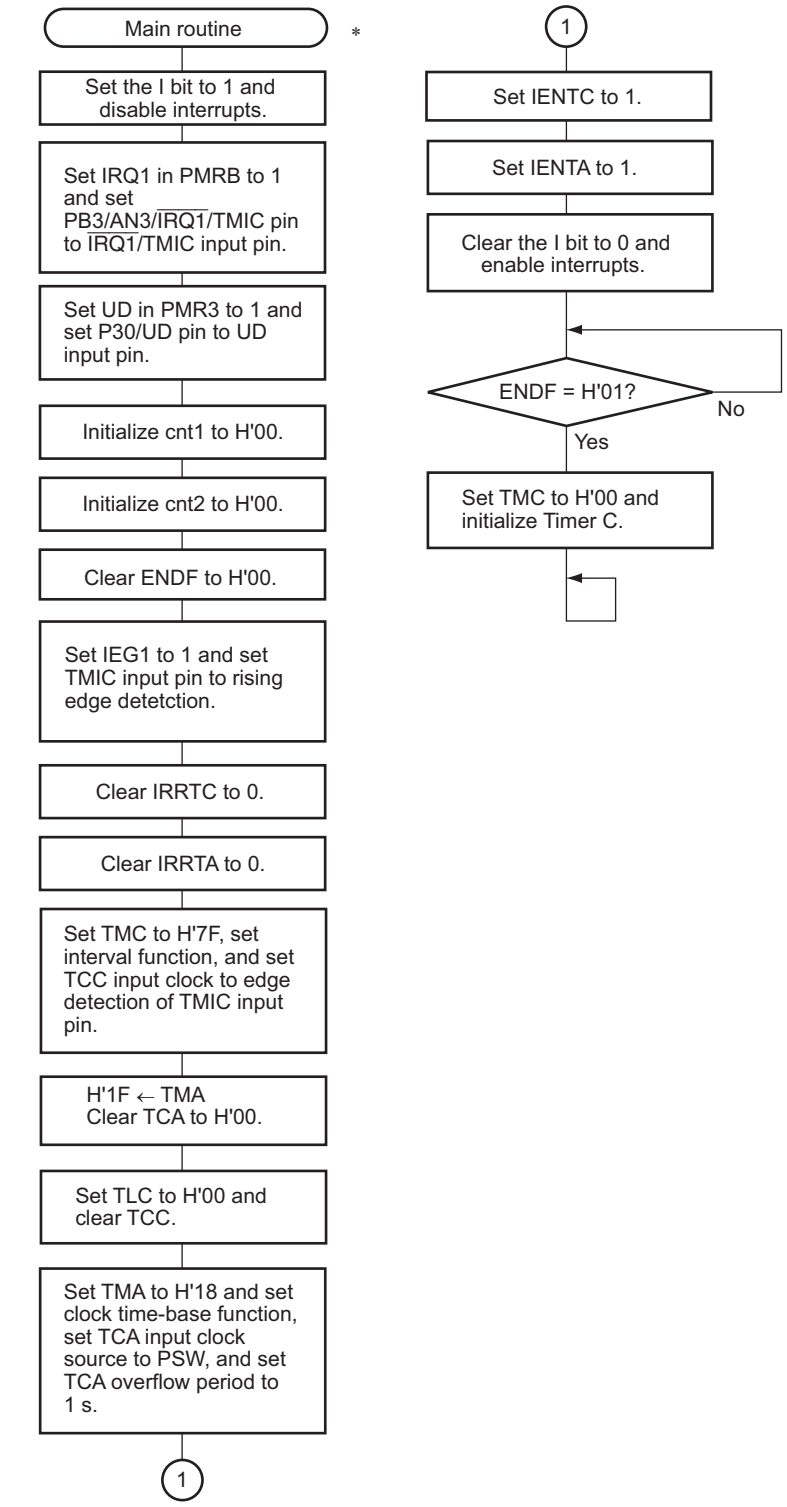
Table 5 describes the RAMs used in this sample task.

Table 5 Description of RAM Used

Label	Function	Address	Used in
cnt1	Stores the counter value of 8-bit counter after 1 s.	H'FB80	8-bit Counter
cnt2	Stores the counter value of TCC after 1 s.	H'FB81	After 1 s
ENDF	Data to indicate whether or not input pulse frequency measurement is completed. When measuring time is under 1 s and cnt1 < H'FF, ENDF = H'00 When 1 s has elapsed in measuring or cnt1 == H'FF, ENDF = H'01	H'FB82	Main Routine 8-bit Counter After 1 s

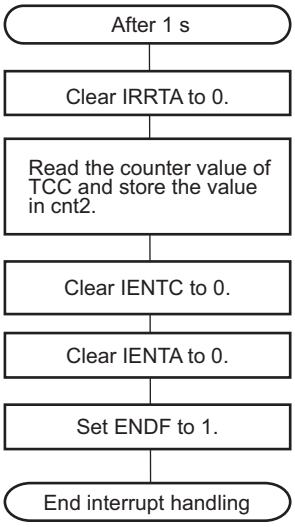
5. Flowchart

1. Main routine

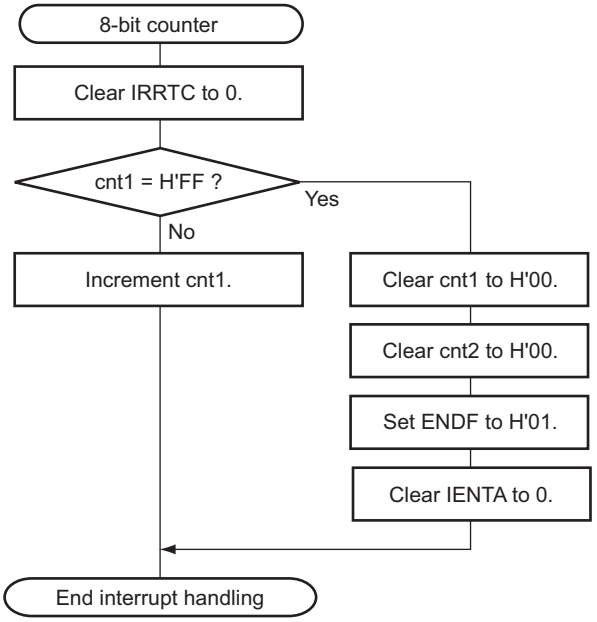


Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer A interrupt handling routine



3. Timer C interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
  .EXPORT    _INIT
  .IMPORT    _main
;
  .SECTION   P,CODE
_INIT:
  MOV.W      #H'FF80,R7
  LDC.B      #B'10000000,CCR
  JMP        @_main
;
  .END
```

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300L Super Low Power Series                                                              */
/*      -H8/38024 Series-                                                                       */
/*  Application Note                                                                            */
/*                                                                                              */
/*  'Pulse Frequency Measurement by Event                                                       */
/*   Counter Function'                                                                          */
/*                                                                                              */
/*  Function                                                                                    */
/*  :Timer C 8bit Event Counter                                                                 */
/*                                                                                              */
/*  External Clock :  10MHz                                                                     */
/*  Internal Clock :  5MHz                                                                      */
/*  Sub Clock :       32.768kHz                                                                 */
/*                                                                                              */
/************************************************************************************************/

#include     <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char     b7:1;       /* bit7 */
    unsigned char     b6:1;       /* bit6 */
    unsigned char     b5:1;       /* bit5 */
    unsigned char     b4:1;       /* bit4 */
    unsigned char     b3:1;       /* bit3 */
    unsigned char     b2:1;       /* bit2 */
    unsigned char     b1:1;       /* bit1 */
    unsigned char     b0:1;       /* bit0 */
};
```

```
#define      TMA         *(volatile unsigned char *)0xFFB0   /* Timer Mode Register A            */
#define      TCA         *(volatile unsigned char *)0xFFB1   /* Timer Counter A                  */
#define      TMC         *(volatile unsigned char *)0xFFB4   /* Timer Mode Register C            */
#define      TCC         *(volatile unsigned char *)0xFFB5   /* Timer Counter C                  */
#define      TLC         *(volatile unsigned char *)0xFFB5   /* Timer Load Register C            */
#define      PMR3_BIT    (*(struct BIT *)0xFFCA)             /* Port Mode Register 3             */
#define      UD          PMR3_BIT.b0                         /* Port Mode Register 3 bit0        */
#define      PMRB_BIT    (*(struct BIT *)0xFFEE)             /* Port Mode Register B             */
#define      IRQ1        PMRB_BIT.b3                         /* Port Mode Register B bit3        */
#define      IEGR_BIT    (*(struct BIT *)0xFFF2)             /* Interrupt Edge Select Register 1 */
#define      IEG1        IEGR_BIT.b1                         /* IRQ1 Edge Select                 */
#define      IENR1_BIT   (*(struct BIT *)0xFFF3)             /* Interrupt Enable Register 1      */
#define      IENTA       IENR1_BIT.b7                        /* Timer A Interrupt Enable         */
#define      IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2      */
#define      IENTC       IENR2_BIT.b1                        /* Timer C Interrupt Enable         */
#define      IRR1_BIT    (*(struct BIT *)0xFFF6)             /* Interrupt Request Register 1     */
#define      IRRTA       IRR1_BIT.b7                         /* Timer A Interrupt Request Flag   */
#define      IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2     */
#define      IRRTC       IRR2_BIT.b1                         /* Timer C Interrupt Request Flag   */

#pragma interrupt        (taint)
#pragma interrupt        (tcint)
/************************************************************************************************/
/*  Function                                                                                    */
/************************************************************************************************/
extern void  INIT ( void );                                  /* SP Set                           */
void         main ( void );
void         taint ( void );
void         tcint ( void );

/************************************************************************************************/
/*  RAM define                                                                                  */
/************************************************************************************************/
unsigned char            cnt1;                               /* 8bit Counter                     */
unsigned char            cnt2;                               /* 8bit Counter                     */
unsigned char            ENDF;                               /* End Data                         */

/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section          V1                                  /* Vector Section                   */
void (*const VEC_TBL1[])(void) = {                           /* 0x0000 - 0x000F                  */
    INIT                                                     /* 0x0000 Reset Vector              */
};
#pragma section          V2                                  /* Vector Section Set               */
void (*const VEC_TBL2[])(void) = {
    taint                                                    /* 0x0016 Timer A Interrupt Vector  */
};
#pragma section          V3                                  /* Vector Section Set               */
void (*const VEC_TBL3[])(void) = {
    tcint                                                    /* 0x001A Timer C Interrupt Vector  */
};

#pragma section                                              /* P                                */
```

```
/*****************************************************************************************/
/*  Main Program                                                                         */
/*****************************************************************************************/
void main ( void )
{
    set_imask_ccr(1);                           /* Interrupt Disable                    */

    IRQ1 = 1;                                   /* TMIC Input Select                    */
    UD   = 1;                                   /* UD Input Select                      */

    cnt1 = 0;                                   /* Initialize 8bit  Counter             */
    cnt2 = 0;                                   /* Initialize 8bit  Counter             */
    ENDF = 0;                                   /* Clear END Flag                       */

    IEG1 = 1;                                   /* TMIC Select                          */
    IRRTC = 0;                                  /* Clear IRRTC                          */
    IRRTA = 0;                                  /* Clear IRRTC                          */

    TMC = 0x7F;                                 /* Initialize 8bit Event Counter Function */
    TMA = 0x1F;                                 /* Initialize Timer Counter A           */
    TLC = 0x00;                                 /* Clear TCC                            */
    TMA = 0x18;                                 /* Initialize Clock Time Base Function  */

    IENTC = 1;                                  /* Timer C Interrupt Enable             */
    IENTA = 1;                                  /* Timer A Interrupt Enable             */

    set_imask_ccr(0);                           /* Interrupt Enable                     */

    while (ENDF =  = 0);

    TMC = 0;                                    /* Initialize Timer C Function          */

    while (1) {
        ;
    }
}

/*****************************************************************************************/
/*  Timer A Interrupt                                                                    */
/*****************************************************************************************/
void taint ( void )
{
    IRRTA = 0;                                  /* Clear IRRTA                          */

    cnt2  = TCC;                                /* Store TCC                            */

    IENTC = 0;                                  /* Timer C Interrupt Disable            */

    IENTA = 0;                                  /* Timer A Interrupt Disable            */

    ENDF  = 1;                                  /* Set ENDF                             */
}
```

```
/*****************************************************************************************************/
/*  Timer C Interrupt                                                                                */
/*****************************************************************************************************/
void tcint ( void )
{
    IRRTC = 0;                                          /* Clear IRRTC                  */

    if ( cnt1 ==  0xff ) {                              /* 8bit Counter = 0xff?         */
        cnt1 = 0;                                       /* Clear cnt1                   */
        cnt2 = 0;                                       /* Clear cnt2                   */
        ENDF = 1;                                       /* ENDF                         */
        IENTA = 0;                                      /* Timer A Interrupt Disable    */
    }
    else {
        cnt1++;                                         /* cnt1 Increment               */
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0016
CV3	H'001A
P	H'0100
B	H'FB80

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		Description	
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