M32C/84, 85, 87, 88 Groups

Searching Unused Areas and Programming the Flash Memory

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Abstract

This document describes a method of searching unused areas (data value is FFFFh) and programming data to the flash memory.
CPU rewrite mode (EW1 mode) is used for rewriting the flash memory.

Products

M32C/84 Group
M32C/85 Group
M32C/87 Group
M32C/88 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

In this document, a search is performed of unused areas (data value is FFFFh), and the flash memory is programmed.

Assuming 1 record is 64 words (128 bytes), at a reset start, a search is performed for an empty record (record where all data values are FFFFh) in block A (data flash) of the flash memory, and record data is programmed when a trigger occurs. When record data is programmed, if there are no empty records, the data flash is block erased and then the record data is programmed.

Table 1.1 lists the Peripheral Functions and Their Applications.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Flash memory	Execute program and block erase operations
INT0 interrupt	Request record data programming

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	M30879FLGP (M32C/87 Group)
Operating frequencies	• XIN clock: 10 MHz • PLL clock: 30 MHz • CPU clock (= bus clock): 30 MHz during normal operation 10 MHz during flash memory rewrite • Peripheral clock: 30 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09
C compiler	Renesas Electronics Corporation M32C Series Compiler V.5.42 Release 00
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir “$(CONFIGDIR)” The default setting is used in the integrated development environment.
Operating mode	Single-chip mode
Sample code version	1.00
Board used	Renesas Starter Kit for M32C/87 (device part no.: R0K330879S001BE)

3. Reference Application Note

The application note associated with this application note is listed below. Refer to this application note for additional information.

- M32C/84, 85, 87, 88 Groups
  Example of Rewriting the User ROM Area Using EW1 Mode (REJ05B1424-0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1 Pin Used and Its Function

Pin Name	I/O	Function
P8_2/$\overline{\text{INT0}}$	Input	Request record data programming

5. Software

5.1 Operation Overview

In the sample code accompanying this application note, the data flash is divided into record units, where each area has 32 records (record 0 to record 31).
At a reset start, a search is performed for an empty record (all data values are FFFFh). When an empty record is found, the start address of the empty record is set as the data write address.
When a falling edge of the $\overline{\text{INT0}}$ signal is detected, record data is programmed to the empty record, and the start address of the next record is set as the data write address.
When programming record data, if the data write address is not within the address range of the data flash, it is determined that there are no empty records, the data flash is erased, record data is programmed to record 0, and the data write address is set to the start address of record 1.
CPU rewrite mode (EW1 mode) is used for rewriting the flash memory.

Figure 5.1 shows the Relation Between the Data Flash and the Record.

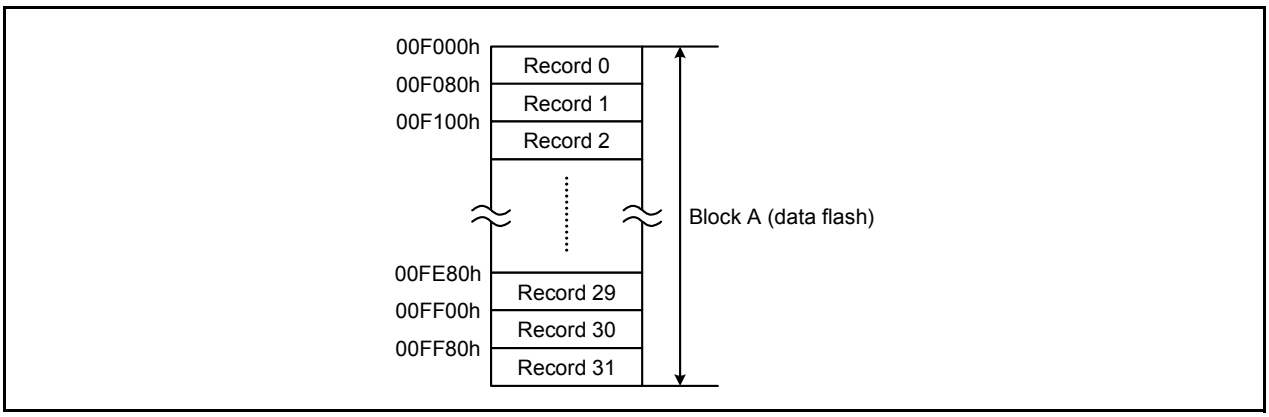


Figure 5.1 Relation Between the Data Flash and the Record

The procedure for searching an empty record and setting the data write address is shown below.

(1) In order to search an empty record, set the data write address to the start address of the data flash (Figure 5.2).

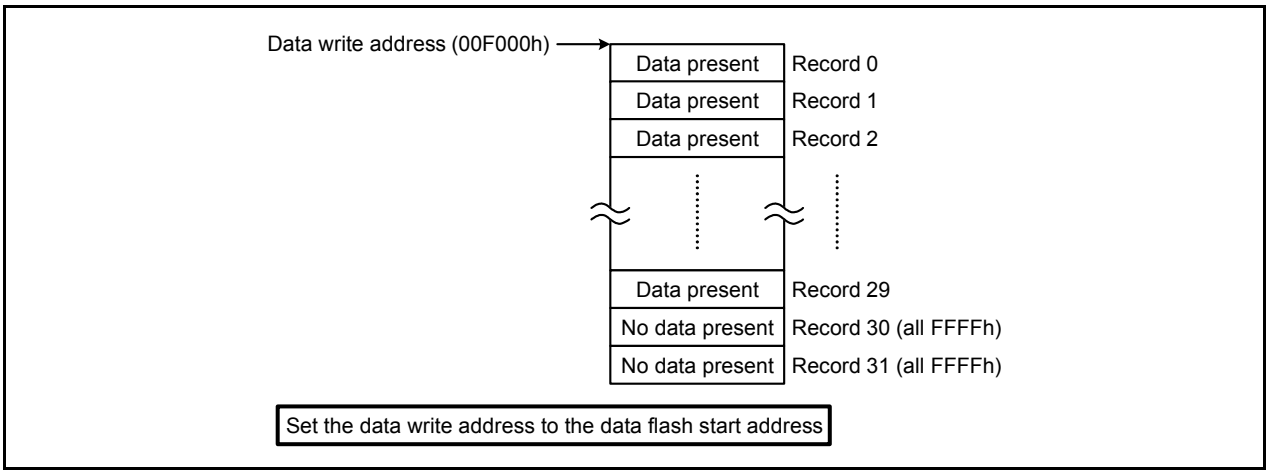


Figure 5.2 Setting the Data Write Address to the Data Flash Start Address

(2) A check is performed to see if the record for the data write address is empty or not. To be more precise, the check is to confirm whether or not all data in one record from the data write address are unused (all FFFFh).

(3) When the record is not empty, the data write address is updated to the start address of the next record (Figure 5.3).

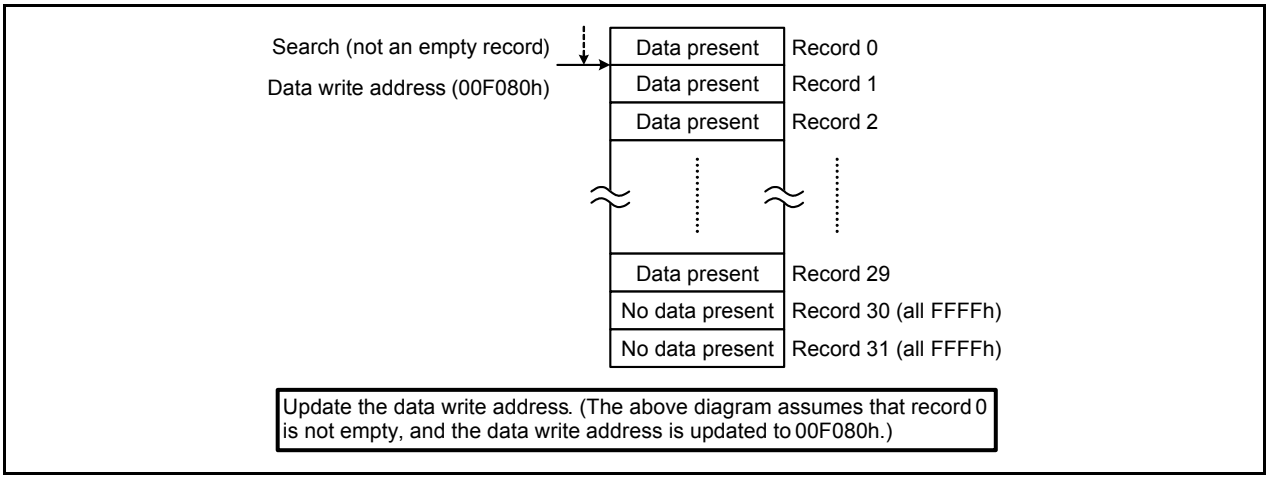


Figure 5.3 Updating the Data Write Address

(4) Steps (2) and (3) are repeated until an empty record is found or the data write address becomes bigger than the end address of the data flash.

(5) If empty records are found, search processing is completed (Figure 5.4).

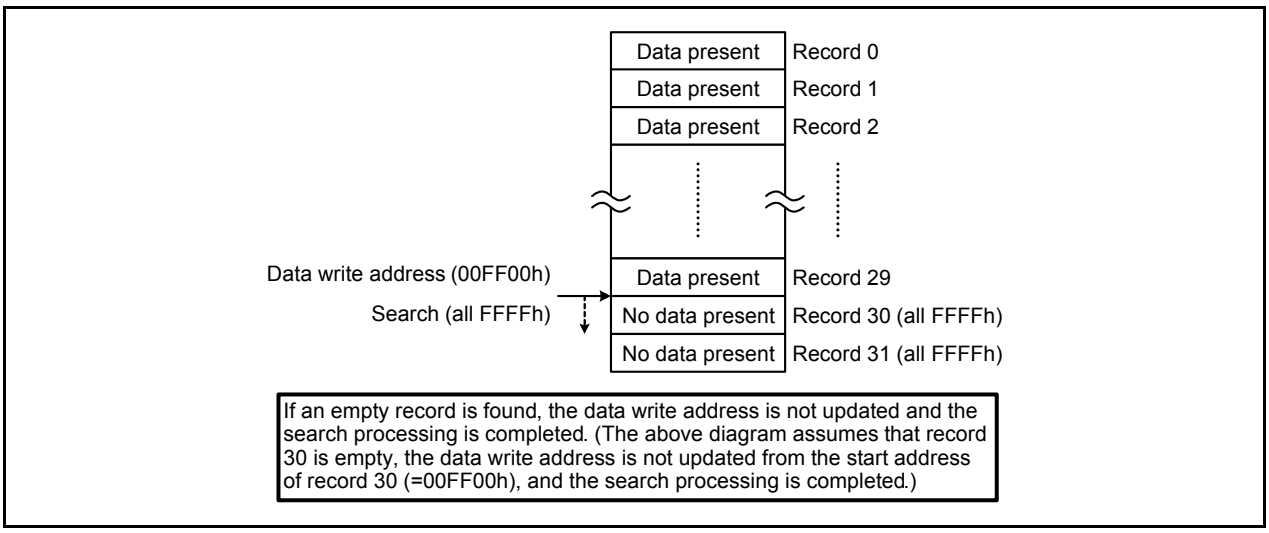


Figure 5.4 Search Completion

(6) If empty records are not found, and the data write address is bigger than the end address of the data flash, set an address that is bigger than the end address (10000h) as the data write address.
When programming record data, as the data write address is not within the data flash address range, it is determined that there are no empty records.

5.2 Constants

Table 5.1 lists the Constants Used in the Sample Code.

Table 5.1 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
COMPLETE	(0)	Normal completion
ERR_PROGRAM	(-1)	Program error
ERR_ERASE	(-2)	Block erase error
TOP_DATAFLASH	(0xF000)	Data flash start address
END_DATAFLASH	(0xFFFF)	Data flash end address
RECORDED_SIZE_WORD	(0x40)	Record size (number of words)

5.3 Variables

Table 5.2 lists the Global Variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
uint16_t	record_data[]	1 record worth of data to program to the data flash	main
uint16_t	*pwrite_address	Data write address	write_address_init, write_record, FLASH_program_record

5.4 Functions

Table 5.3 lists the Functions.

Table 5.3 Functions

Function Name	Outline
main	Main processing
write_address_init	Data write address initialization
make_data	Record data creation
write_record	Data write control processing
FLASH_block_erase	Data flash erase
FLASH_program_record	Record data programming
FLASH_ew1_start	EW1 mode start processing
FLASH_ew1_end	EW1 mode end processing

5.5 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	The system clock is initialized, maskable interrupts are enabled, the data write address is initialized, and the program waits for a record data programming request (INT0). The following processes are performed in the main loop: (1) Record data creation (2) Data write control processing In the sample code accompanying this application note, return processing from a block erase error and return processing from a program error (error processing) are not performed. Add error processing when necessary.
Argument	None
Returned value	None

write_address_init	
Outline	Data write address initialization
Header	None
Declaration	static void write_address_init(void)
Description	A search is performed for an empty record starting from the start address of the data flash, and the start address of the empty record is set as the data write address.
Argument	None
Returned value	None

make_data	
Outline	Record data creation
Header	None
Declaration	static void make_data(uint16_t *pdata)
Description	Record data is created to program to the data flash. In this application note, a sequence from 0 to 127 is created and stored in the address indicated in pdata. Change the processing according to the content of the record data programmed.
Argument	uint16_t *pdata: Pointer to the area where the record data that was created is stored
Returned value	None

write_record	
Outline	Data write control processing
Header	None
Declaration	static int8_t write_record(uint16_t *pwrite_data)
Description	Confirmation is made that the data write address is within the address range of the data flash. If the data write address is not within the address range of the data flash, the data flash is erased and the start address of record 0 is set as the data write address. After the data write address is set, record data is programmed. If a block erase error occurs during data flash erase processing, “block erase error (ERR_ERASE)” is returned. If a program error occurs while programming the record data, “program error (ERR_PROGRAM)” is returned. If processing is completed normally, “processing completed normally (COMPLETE)” is returned.
Argument	uint16_t *pwrite_data: Pointer to the record data to be programmed
Returned value	Processing results: COMPLETE: Processing completed normally ERR_PROGRAM: Program error ERR_ERASE: Block erase error

FLASH_block_erase	
Outline	Data flash erase
Header	None
Declaration	static int8_t FLASH_block_erase(void)
Description	The data flash is erased (block erase). If an error occurs during block erase processing, “block erase error (ERR_ERASE)” is returned. If processing is completed normally, “block erase completed normally (COMPLETE)” is returned.
Argument	None
Returned value	Block erase results: COMPLETE: Block erase completed normally ERR_ERASE: Block erase error

FLASH_program_record	
Outline	Record data programming
Header	None
Declaration	static int8_t FLASH_program_record(uint16_t *pwrite_data)
Description	Record data designated by the argument is programmed from the data write address. If an error occurs during the program, “program error (ERR_PROGRAM)” is returned. If processing is completed normally, “program completed normally (COMPLETE)” is returned.
Argument	uint16_t *pwrite_data: Pointer to the record data to be programmed
Returned value	Program results: COMPLETE: Program completed normally ERR_PROGRAM: Program error

FLASH_ew1_start	
Outline	EW1 mode start processing
Header	None
Declaration	static void FLASH_ew1_start(void)
Description	Maskable interrupts are disabled. After the CPU clock and internal memory wait are set, the MCU enters EW1 mode of CPU rewrite mode.
Argument	None
Returned value	None

FLASH_ew1_end	
Outline	EW1 mode end processing
Header	None
Declaration	static void FLASH_ew1_end(void)
Description	After CPU rewrite mode is disabled, the CPU clock and internal memory wait are restored to their previous states, and maskable interrupts are enabled.
Argument	None
Returned value	None

5.6 Flowcharts

5.6.1 Main Processing

Figure 5.5 shows the Main Processing.

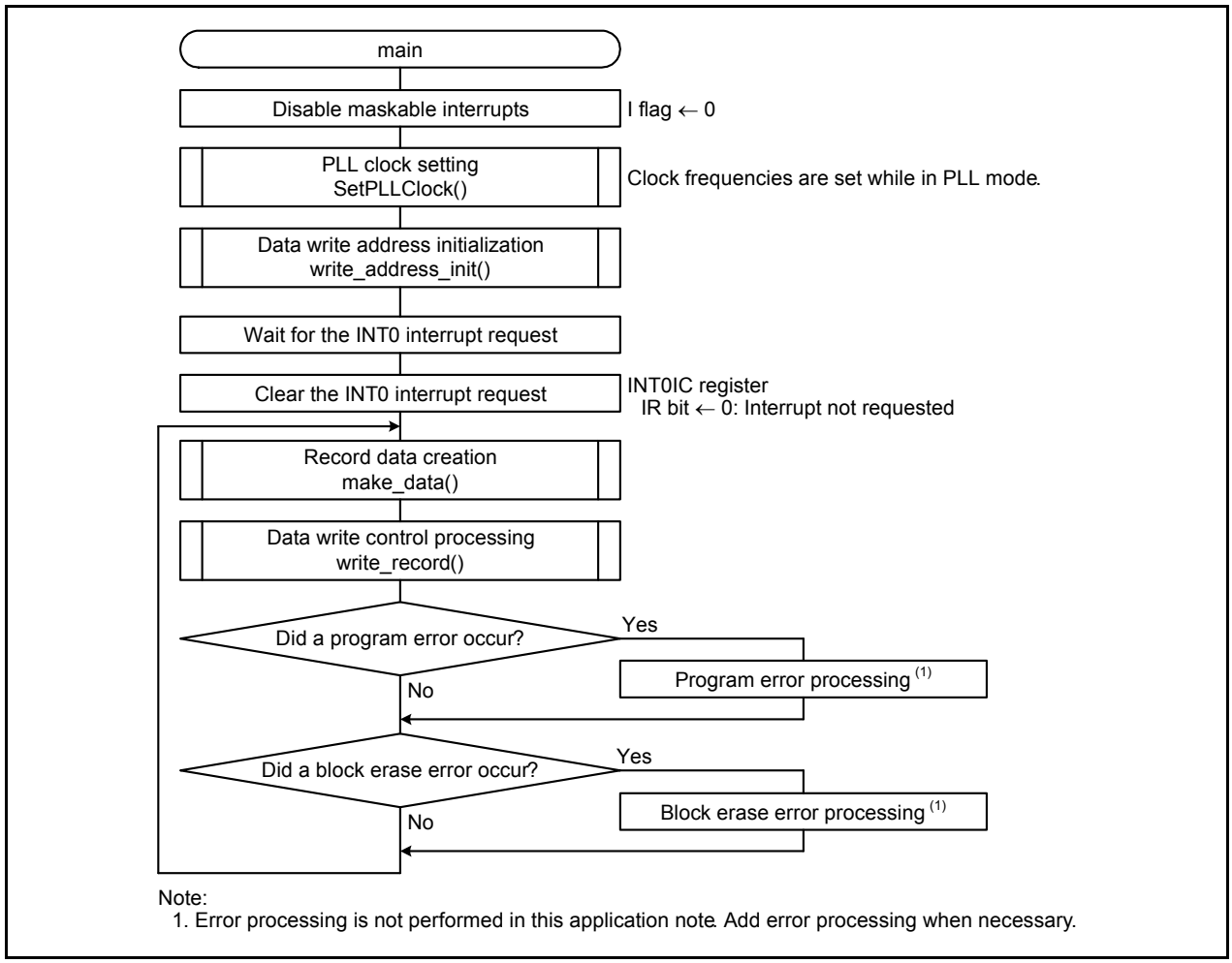


Figure 5.5 Main Processing

5.6.2 Data Write Address Initialization

Figure 5.6 shows Data Write Address Initialization.

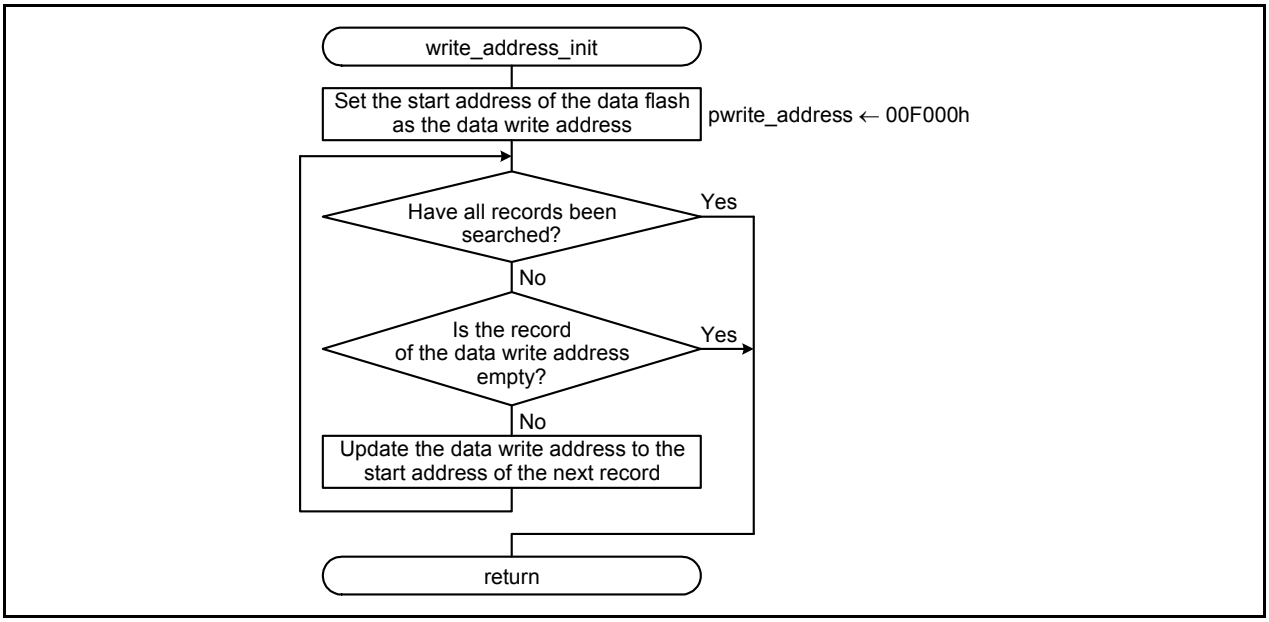


Figure 5.6 Data Write Address Initialization

5.6.3 Record Data Creation

Figure 5.7 shows Record Data Creation.

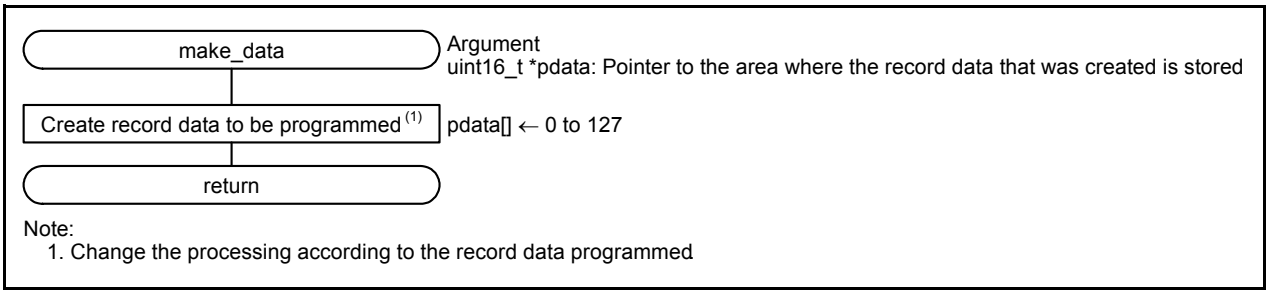


Figure 5.7 Record Data Creation

5.6.4 Data Write Control Processing

Figure 5.8 shows Data Write Control Processing.

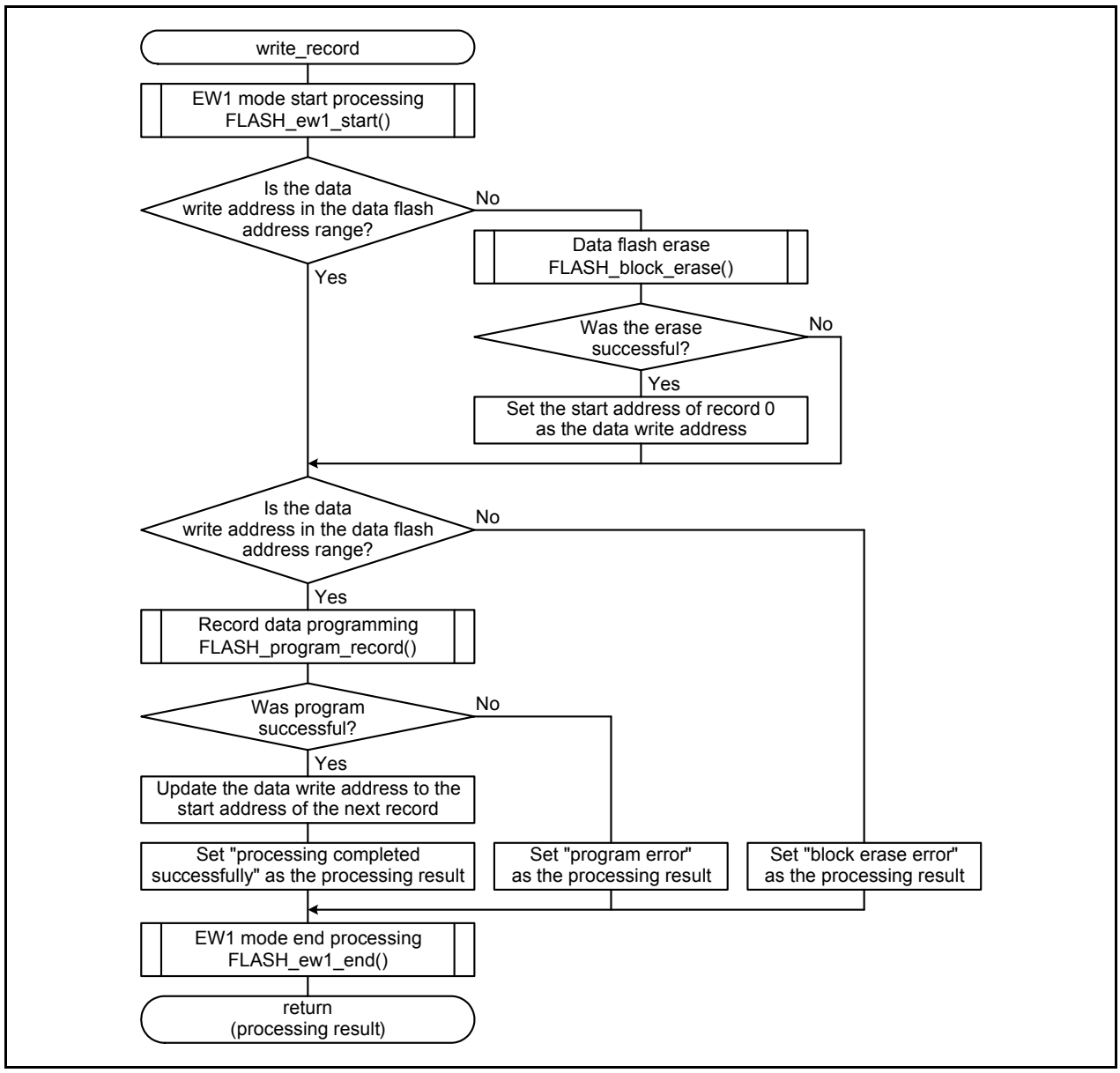


Figure 5.8 Data Write Control Processing

5.6.5 Data Flash Erase

Figure 5.9 shows Data Flash Erase.

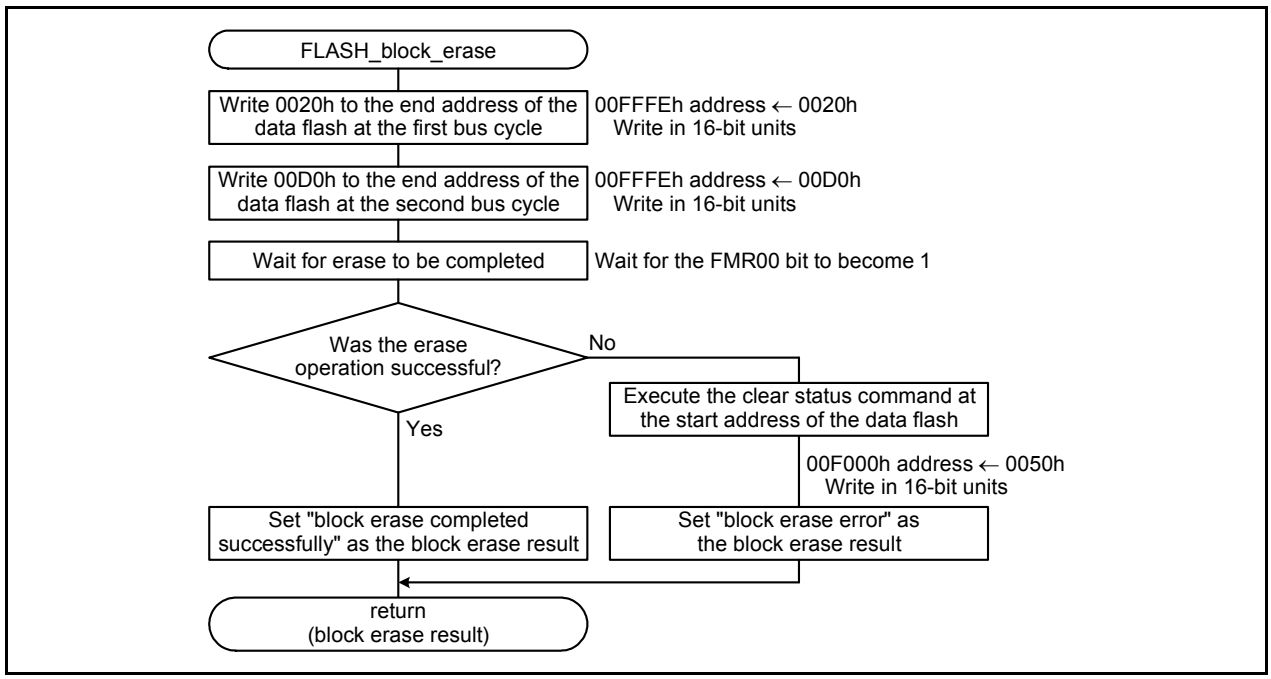


Figure 5.9 Data Flash Erase

5.6.6 Record Data Programming

Figure 5.10 shows Record Data Programming.

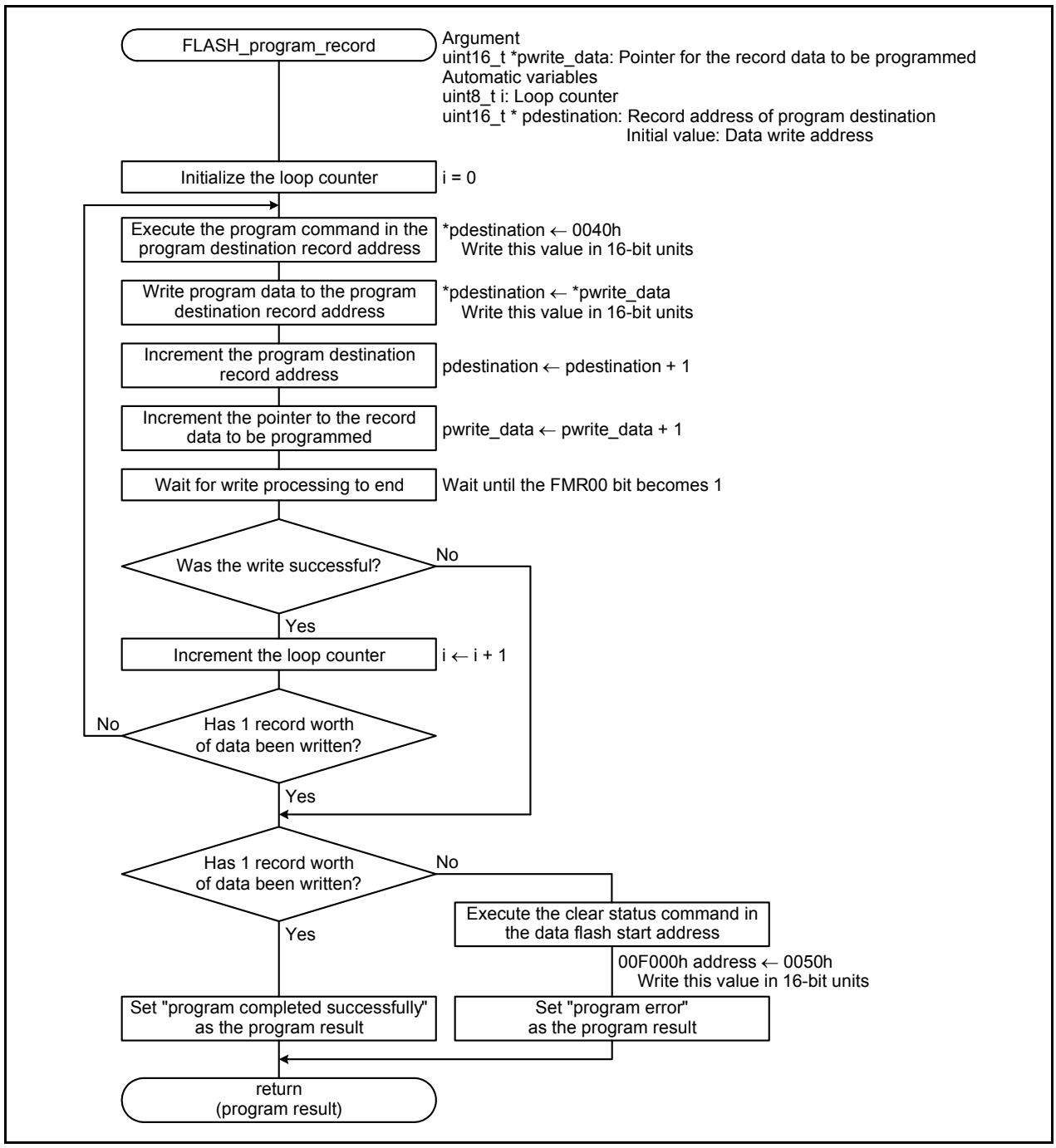
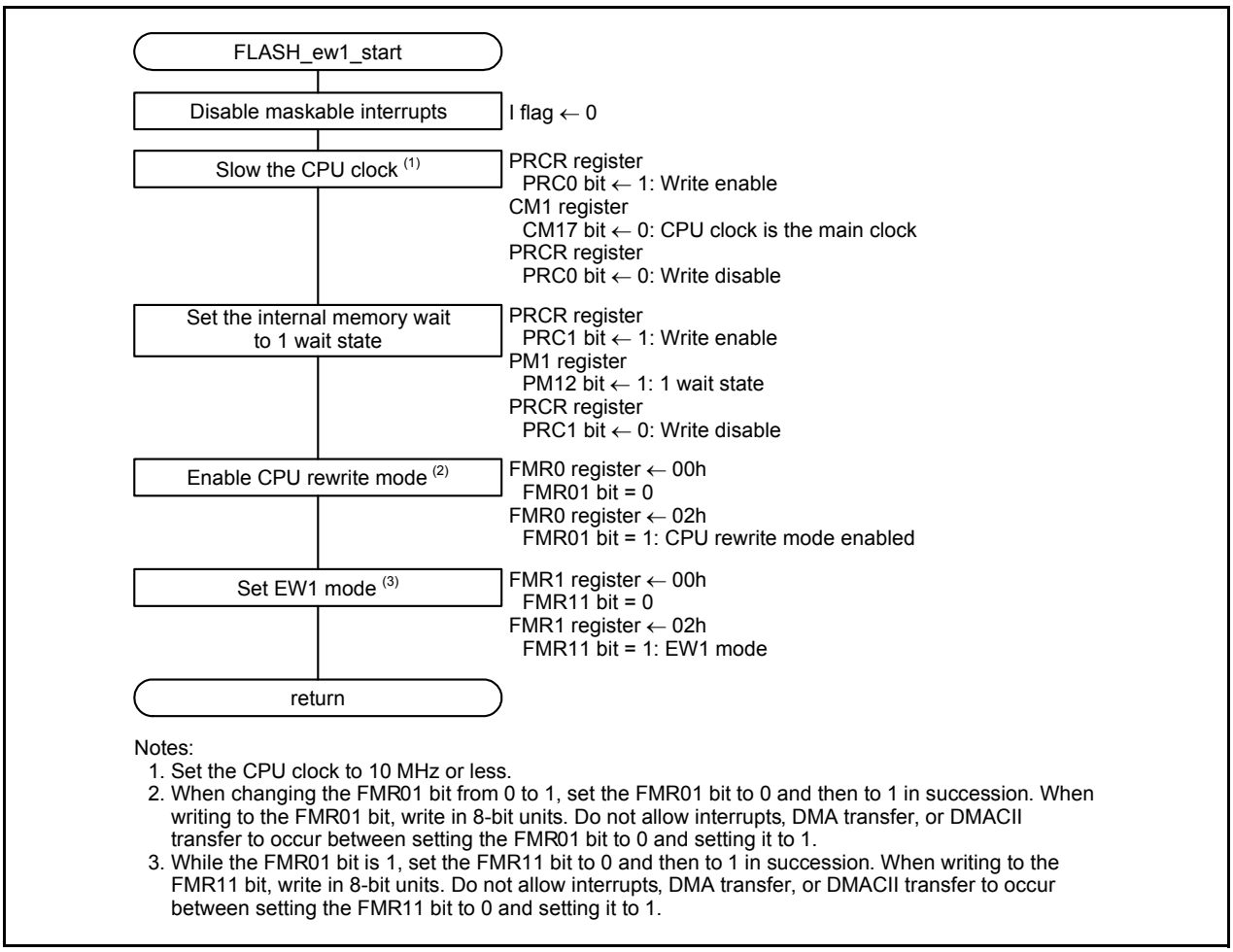


Figure 5.10 Record Data Programming

5.6.7 EW1 Mode Start Processing

Figure 5.11 shows EW1 Mode Start Processing.



Notes:
1. Set the CPU clock to 10 MHz or less.
2. When changing the FMR01 bit from 0 to 1, set the FMR01 bit to 0 and then to 1 in succession. When writing to the FMR01 bit, write in 8-bit units. Do not allow interrupts, DMA transfer, or DMACII transfer to occur between setting the FMR01 bit to 0 and setting it to 1.
3. While the FMR01 bit is 1, set the FMR11 bit to 0 and then to 1 in succession. When writing to the FMR11 bit, write in 8-bit units. Do not allow interrupts, DMA transfer, or DMACII transfer to occur between setting the FMR11 bit to 0 and setting it to 1.

Figure 5.11 EW1 Mode Start Processing

5.6.8 EW1 Mode End Processing

Figure 5.12 shows EW1 Mode End Processing.

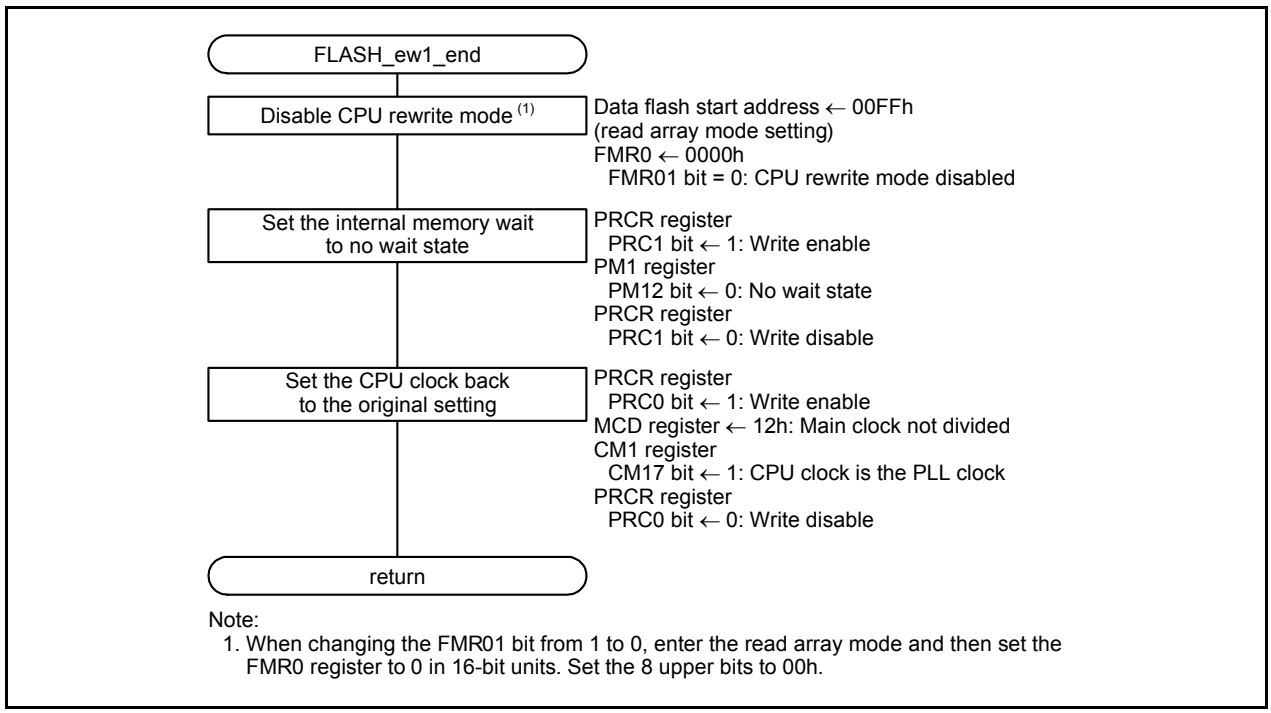


Figure 5.12 EW1 Mode End Processing

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M32C/84 Group (M32C/84, M32C/84T) Hardware Manual Rev.1.01
M32C/85 Group (M32C/85, M32C/85T) Hardware Manual Rev.1.03
M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual Rev.1.51
M32C/88 Group (M32C/88T) Hardware Manual Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M32C Series C Compiler Package V.5.42
C Compiler User's Manual Rev.2.00
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Revision History	M32C/84, 85, 87, 88 Groups Searching Unused Areas and Programming the Flash Memory

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 30, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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