

## M16C/63, M16C/64A, and M16C/65 Groups

Example of Pulse Width Modulator

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## 1. Abstract

This application notes describes the setting method and example for the pulse width modulator in the M16C/63, M16C/64A, and M16C/65 Groups.

# 2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

• MCUs: M16C/63 Group M16C/64A Group M16C/65 Group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the user's manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.



## 3. Application Example

This section describes using PWM0 to output a waveform from port P9\_3.

### 3.1 Application Example Settings

PWM0 cycle and high-level width are set to approximately 3.0 ms and 100  $\mu$ s, and output. When an INTO interrupt is generated, the duty is changed to 50% (high-level width is approximately 1.5 ms). Table 3.1 lists the Application Example Settings.

#### Table 3.1 Application Example Settings

Item	Setting		
Quitout ping	✓ Output PWM0 signal from P9_3		
Output pins	Output PWM0 signal from P4_6 <sup>(1)</sup>		
	✓ f1 divided by 2		
PWM count sources	f1 divided by 4		
F WW Count Sources	f1 divided by 8		
	f1 divided by 16		

Note:

1. Neither the P4\_6 nor P4\_7 pin exists in the M16C/63 Group 80-pin package.



#### 3.2 Application Example Waveform

Figure 3.1 shows the Sample Output Waveform, and Figure 3.2 shows the PWMPRE0 and PWMREG0 Register Settings.

Peripheral clock (f1) is set to the main clock (XIN = 8 MHz) no division.

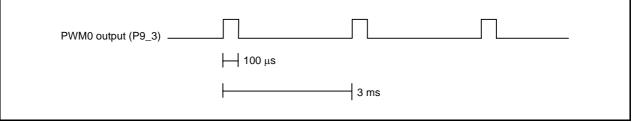
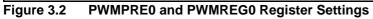


Figure 3.1 Sample Output Waveform

	the PWM cycle width and high-level width are set to 3 ms and 100 $\mu s$ corresponding to $_{2}$ 3.1 Sample Output Waveform:
Relati	onship between related registers and PWM cycle, and high-level width is as follows:
	$PWM cycle = \frac{(2^8 - 1) \times (m + 1)}{fj}  (unit: s)$
	High-level width = $\frac{(m + 1) \times n}{fj}$ (unit: s)
	fj: Frequency of count source (unit: Hz) m: PWMPRE0 register setting value n: PWMREG0 register setting value
Whe	en the frequency of the count source is set to f1 divided by 2:
	PWM cycle (approximately 3 ms) = $\frac{(256 - 1) \times (m + 1)}{(8 \times 10^6) / 2}$
	PWMPRE0 register setting value m = 46.
	High-level width (approximately 100 $\mu$ s) = $\frac{(46 + 1) \times n}{(8 \times 10^6) / 2}$
PWI	uming the formulas above: MPRE0 register setting value m = 46 MREG0 register setting value n = 9





### 3.3 Flowchart

Figure 3.3 shows the Main Program Flowchart.

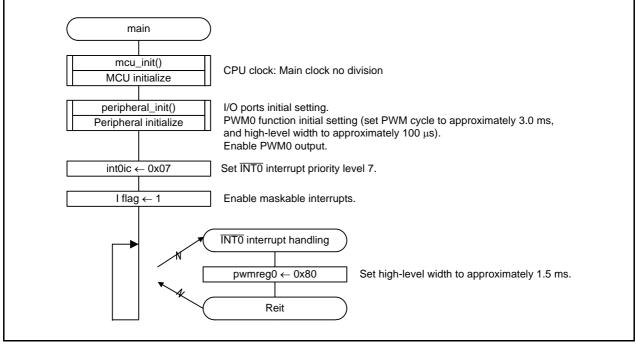


Figure 3.3 Main Program Flowchart



### 3.4 Sample Program Operation Example

The value written to the PWMREG0 register during PWM0 output is not reflected until the next cycle of PWM0 output begins.

The PWM output signal is low immediately after the MCU is reset. Then the associated waveform output starts. Figure 3.4 shows the PWM0 Output Example of the Sample Program.

		Set to 1 (PW	VM output enabled) by a	program.	
PWMEN0 bit in the PWMCON1 register			,,.,.,.,.,.,,.,		
INTO pin					
PWM0 prescaler prelatch	00h	2Ęh			
Reset valu		t registers PWMF VMREG0 by a pro			PWMREG0 register by a m in INTO interrupt handling.
PWM0 register prelatch	00h X	09h \		:V X 80h	
PWM0 prescaler latch	00h		2EI	1	
PWM0 register	↑ Reset	value			
latch	00h	)	Rewritten reset value PWM0 output enable the second cycle of F	but before d is reflected in	X 80h Value rewritten during PWM output is reflected in the next cycle. (2Eh + 1) × 80h
PWM0 output		i√ output i←→	(2Eh + 1) × 09h (8 × 10 <sup>6</sup> ) / 2	[	(8 × 10 <sup>6</sup> ) / 2 (8 × 1
	-		$\frac{(2^8 - 1) \times (2Eh + 1)}{(8 \times 10^6) / 2}$ low-level signal is st cycle after reset.		$\frac{(2^8 - 1) \times (2Eh + 1)}{(8 \times 10^6) / 2}$
The above diagram	m assumes t	the PWMPORT0	bit in the PWMCON1 re	egister is 1 (PWN	l output).

Figure 3.4 PWM0 Output Example of the Sample Program



### 3.5 Register Settings

Figure 3.5 to Figure 3.7 show Register Settings.

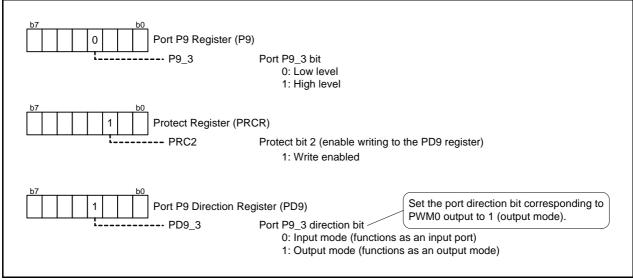


Figure 3.5 Register Settings (1)



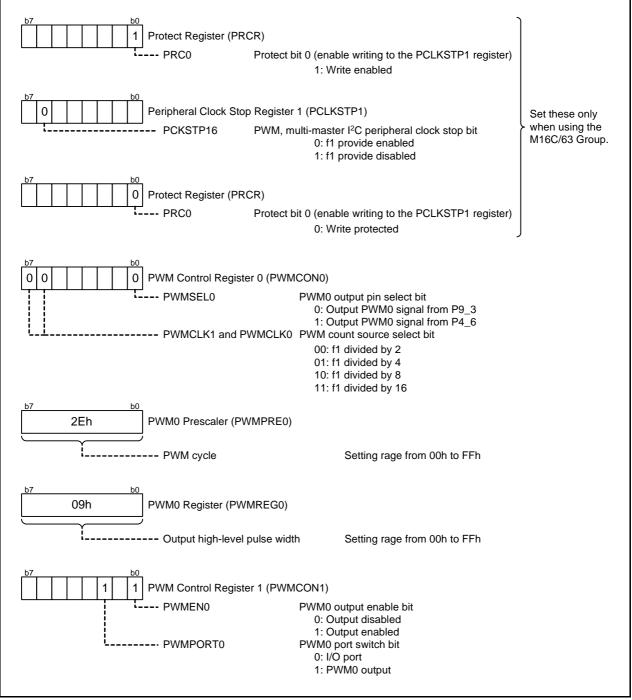


Figure 3.6Register Settings (2)



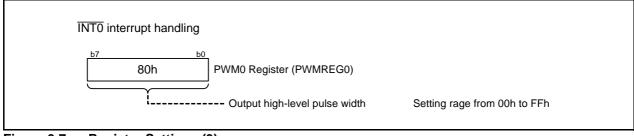


Figure 3.7 Register Settings (3)



## 4. Sample Program

A sample program can be downloaded from the Renesas Electronics website. To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

## 5. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.1.00 M16C/64A Group User's Manual: Hardware Rev.1.10 M16C/65 Group User's Manual: Hardware Rev.1.10 The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News The latest information can be downloaded from the Renesas Electronics website.

C Compiler User's Manual M16C Series, R8C Family C Compiler Package V.5.45 C Compiler User's Manual Rev.2.00 The latest version can be downloaded from the Renesas Electronics website.

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## M16C/63, M16C/64A, and M16C/65 Groups Example of Pulse Width Modulator

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### General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
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  accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

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