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SH7764 Group

LCD Controller TFT-LCD Interfacing Example

Introduction

This application note shows the TFT-LCD interfacing example using the SH7764 Microcontrollers (MCUs) on-chip LCD Controller (LCDC).

Target Device

SH7764 (R0K507764E001BR from Renesas Technology Corp.)

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1. Preface

1.1 Specifications

The SH7764 MCU on-chip LCD controller (LCDC) is connected with a TFT-LCD panel to display the graphic image.

1.2 Module Used

- LCD controller (LCDC)
- General-purpose I/O ports (GPIO)

1.3 Applicable Conditions

- MCU SH7764
- Operating frequency

CPU clock:	324 MHz
SuperHyway clock:	108 MHz
Peripheral clock:	54 MHz
Bus clock:	108 MHz
- Integrated development environment

from Renesas Technology Corp.

- C compiler

SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03 Release00
from Renesas Technology Corp.
- Compiler options

Default settings of the High-performance Embedded Workshop
-cpu=sh4a -endian=little -include="\$(WORKSPDIR)\inc"
-object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -optimize=0
-gbr=auto -chginclpath -errorpath
-global_volatile=0 -opt_range=all -infinite_loop=0
-del_vacant_loop=0 -struct_alloc=1 -nologo

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7764 Group Application Note: SH7764 Example of Initialization (REJ06B0919)

2. Description of the Sample Application

This application note shows the pin connection example and configuration example to display the graphic image by the LCDC. The specifications of the TFT-LCD panel used in this application note are shown in 2.2.

2.1 LCDC Operation

2.1.1 Overview

A unified memory architecture is adopted for the LCD controller (LCDC) so that the image data for display is stored in system memory. The LCDC module reads data from system memory, uses the palette memory to determine the colors, then puts the display on the LCD panel. It is possible to connect the LCDC to the LCD module* other than microcomputer bus interface types and NTSC/PAL types and those that apply the LVDS interface.

Note: * LCD module can be connected to the LVDS interface by using the LSI with LVDS conversion LSI.

2.1.2 Features

Table 1 lists the LCDC features. Figure 1 shows a block diagram of LCDC.

Table 1 LCDC Features

Item	Function
Panel interface	Serial interface method
Type of LCD	STN/dual-STN/TFT panels
Panel data formats	8/12/16/18-bit bus width
Color modes	4/8/15/16-bpp
Grayscale modes	1/2/4/6-bpp
Panel sizes	16 × 1 to 1024 × 1024 dots
Color palette	24-bit
Display in neutral colors for STN/DSTN panels	24-bit space-modulation FRC with 8-bit RGB values for reduced flicker
VRAM	A certain area of the synchronous DRAM (CS1 or CS2) is used as VRAM.
Line buffer	2.4-kbyte
Signal polarity	Programmable
Data formats	The endian of bytes is set. A packed pixel method is available.
Interrupt	An interrupt can be generated at a user-specified position.

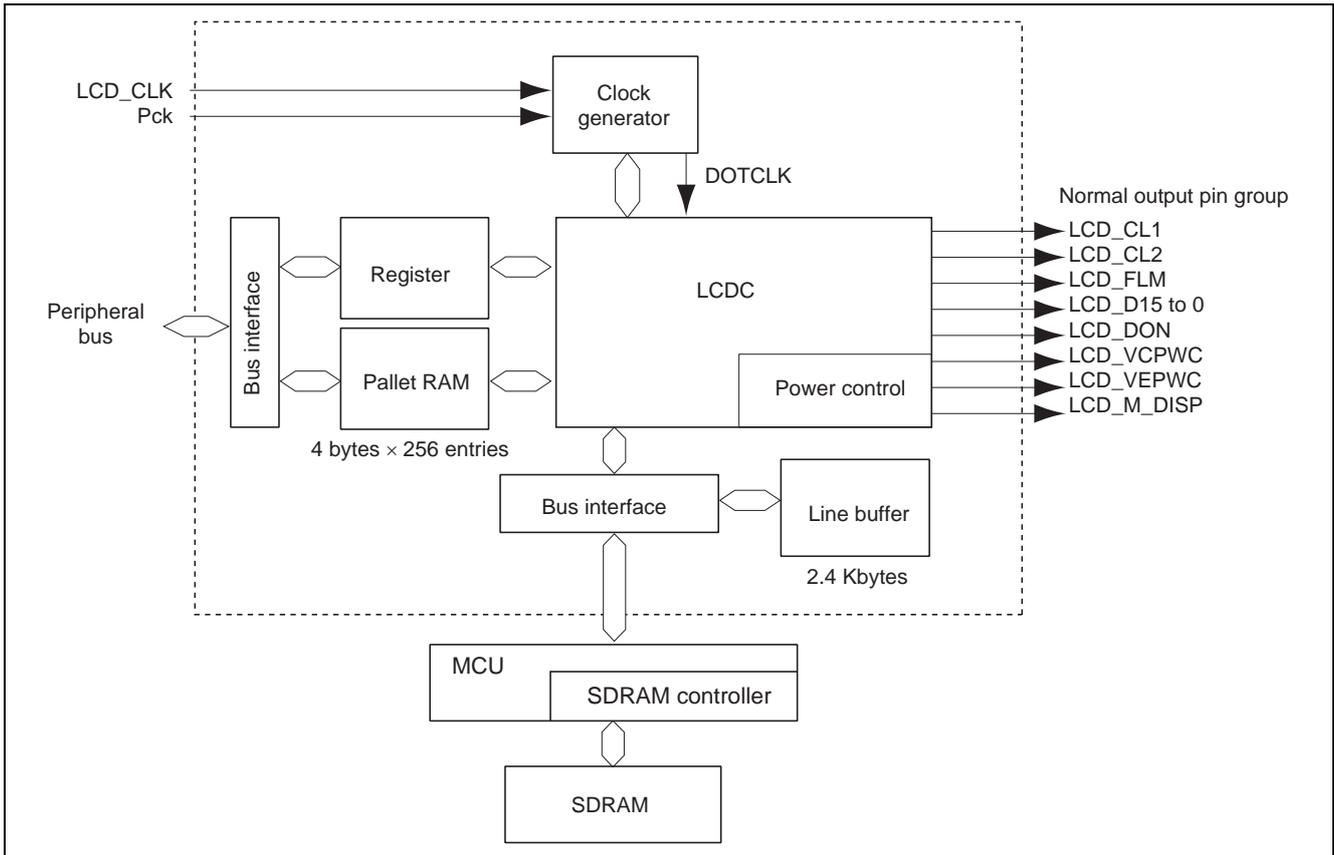


Figure 1 LCDC Block Diagram

2.1.3 I/O Pins

Table 2 lists the LCDC I/O pins.

Table 2 LCDC I/O Pins

Pin Name	I/O	Function
LCD_D15 to 0	Output	Data for LCD panel
LCD_DON	Output	Display-on signal (DON)
LCD_CL1	Output	Shift-clock 1 (STN/DSTN)/horizontal sync signal (HSYNC)
LCD_CL2	Output	Shift-clock 2 (STN/DSTN)/dot clock (DOTCLK)
LCD_M_DISP	Output	LCD current-alternating signal/DISP signal
LCD_FLM	Output	First line marker/vertical sync signal (VSYNC) (TFT)
LCD_VCPWC	Output	LCD-module power control (VCC)
LCD_VEPWC	Output	LCD-module power control (VEE)
LCD_CLK	Input	LCD clock-source input

2.1.4 LCD Module Sizes which can be Displayed

This LCDC is capable of controlling displays with up to 1024 × 1024 dots and 16 bpp (bits per pixel). The image data for display is stored in VRAM, which is shared with the CPU. This LCDC should read the data from VRAM before display.

This LSI has a maximum 16-burst (32-bit bus width) memory read operation and a 2.4-Kbyte line buffer, so although a complete breakdown of the display is unlikely, there may be some problems with the display depending on the combination. A recommended size at the frame rate of 60 Hz is 320 × 240 dots in 16 bpp or 640 × 480 dots in 8 bpp.

As a rough standard, the bus occupation ratio shown below should not exceed 40%. The overhead coefficient becomes 2.000 when the CL2 SDRAM is connected to a 32-bit data bus and 1.825 when connected to a 64-bit data bus. The each value is ideal value under the best condition.

$$\text{Bus occupation ratio (\%)} = \frac{\text{Overhead coefficient} \times \text{Total number of display pixels } ((\text{HDCN} + 1) \times 8 \times (\text{VDLN} + 1)) \times \text{Frame rate (Hz)} \times \text{Number of colors (bpp)}}{\text{CLKOUT (Hz)} \times \text{Bus width (= 32 bits)}} \times 100$$

Example) Total number of display pixels = H480 × V640, Frame rate = 60 Hz,
Number of colors 16 bits, Overhead coefficient = 2.00, Bus clock = 108 MHz

$$\text{Bus occupation ratio} = \frac{2.00 \times 480 \times 640 \times 60 \times 16}{108 \times 10^6 \times 32} \times 100 = 17.06\%$$

Figure 2 shows the valid display and the retrace period.

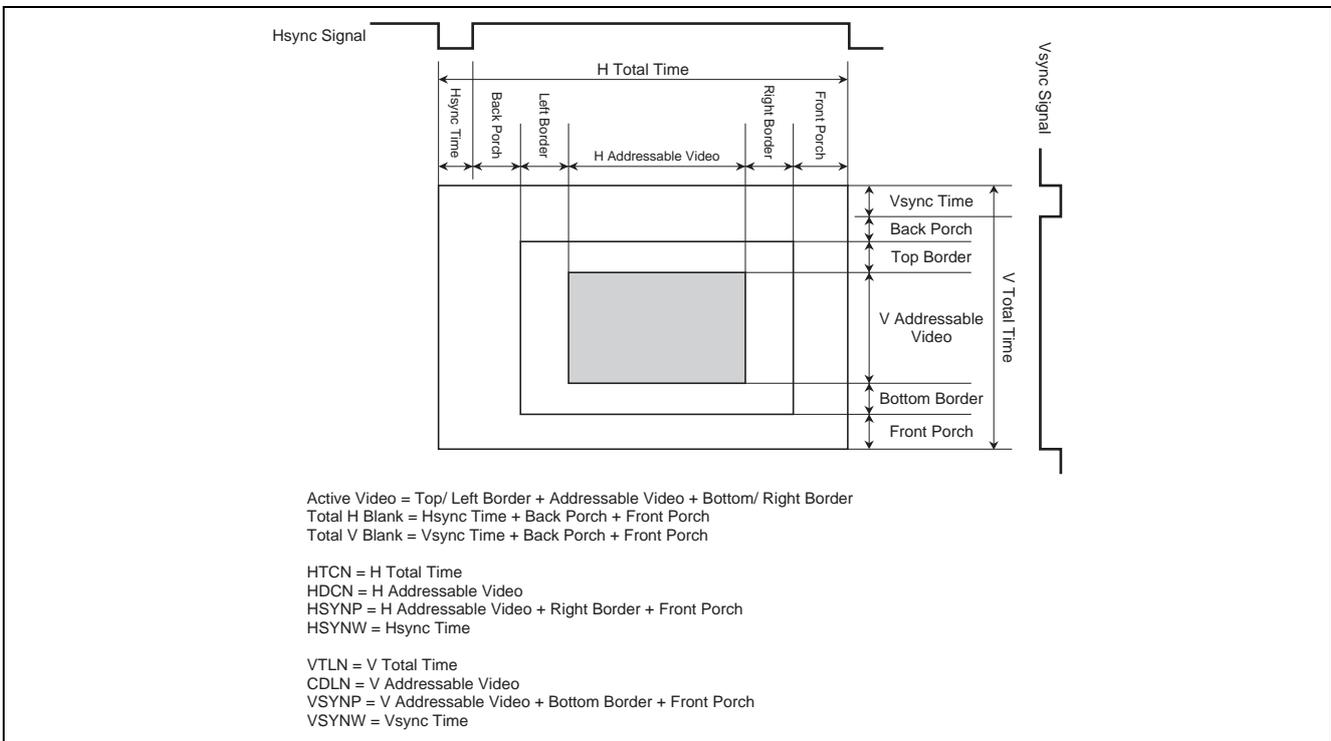


Figure 2 Valid Display and the Retrace Period

2.1.5 Color Palette

Color palette registers are not set in the sample application. If a color palette is to be used, please refer to the *SH7764 Group Hardware Manual* (REJ09B0360). It gives an outline in this section.

This LCDC has a color palette which outputs 24 bits of data per entry and is able to simultaneously hold 256 entries. The color palette thus allows the simultaneous display of 256 colors chosen from among 16-M colors.

The procedure below may be used to set up color palettes at any time.

1. The PALEN bit in the LDPALCR is 0 (initial value); normal display operation
2. Access LDPALCR and set the PALEN bit to 1; enter color-palette setting mode after three cycles of peripheral clock.
3. Access LDPALCR and confirm that the PALS bit is 1.
4. Access LDPR00 to LDPRFF and write the required values to the PALD00 to PALDFF bits.
5. Access LDPALCR and clear the PALEN bit to 0; return to normal display mode after a cycle of peripheral clock.

Figure 3 shows the data format for a color-palette entry.

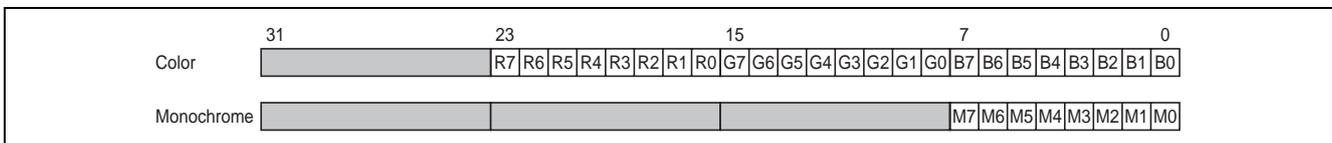


Figure 3 Data Format for Color-Palette Entry

2.1.6 Clock and LCD Data Signal Example

Figure 4 shows the LCD data signal example.

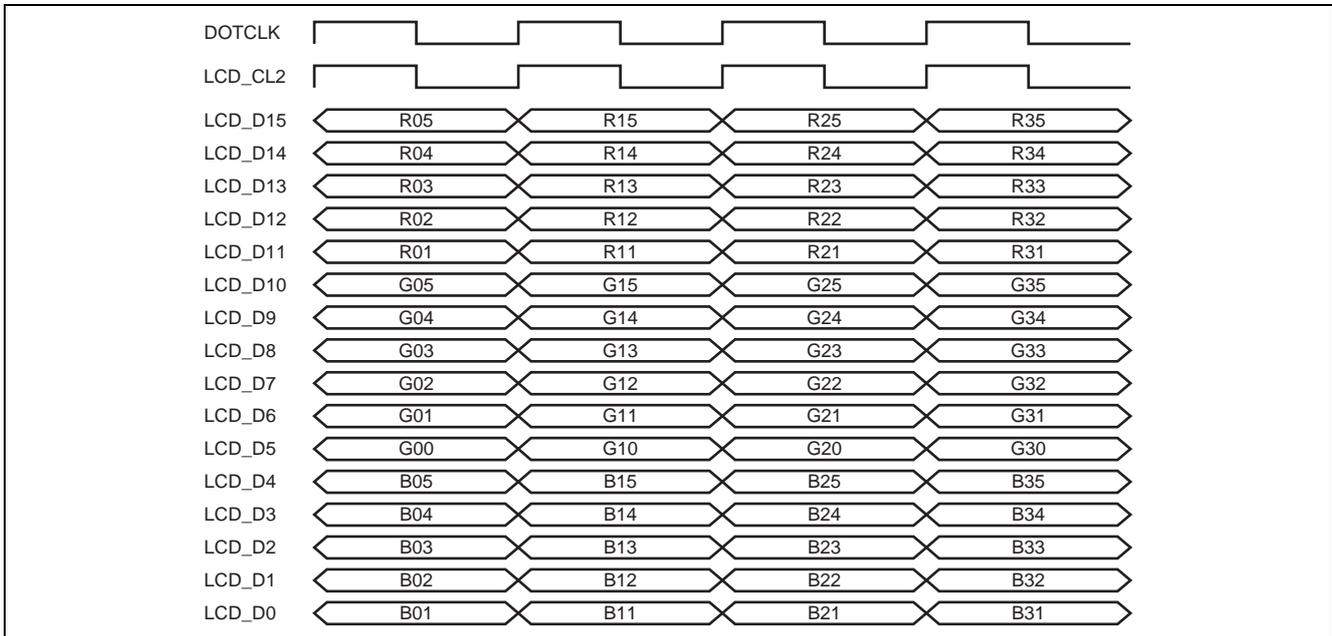


Figure 4 Clock and LCD Data Signal Example (TFT Color 16-Bit Data Bus Module)

2.1.7 Power-Supply Control Sequence

An LCD module normally requires a specific sequence for processing to do with the cutoff of the input power supply. Settings in LDPMMR, LDPSPR, and LDCNTR, in conjunction with the LCD power-supply control pins (LCD_VCPWC, LCD_VEPWC, and LCD_DON), are used to provide processing of power-supply control sequences that suits the requirements of the LCD module.

If LCD module power-supply control-sequence processing is in use by the LCDC or the supply of power is cut off while the LCDC is in its display-on mode, normal operation is not guaranteed. In the worst case, the connected LCD module may be damaged.

Figure 5 is timing charts that show outlines of power-supply control sequences and table 3 is a summary of available power-supply control sequence periods.

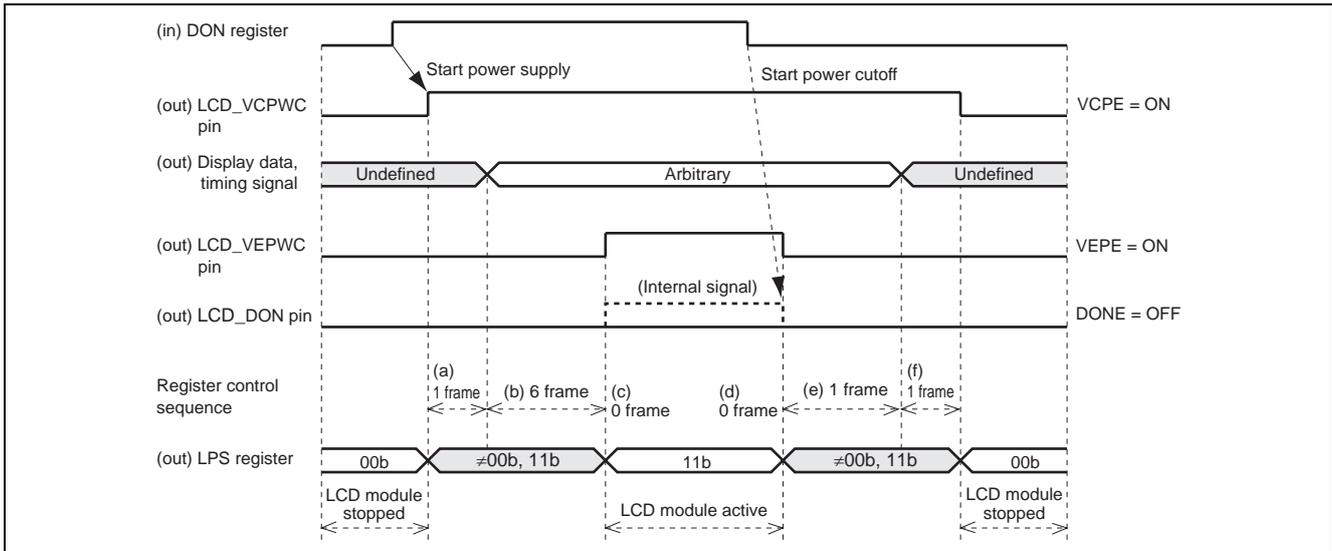


Figure 5 Power-Supply Control Sequence and States of the LCD Module

Table 3 Available Power-Supply Control-Sequence Periods at Typical Frame Rates

ONX, OFFX Register Value	Frame Rate	
	120 Hz	60 Hz
H'F	$(-1+1)/120 = 0.00$ (ms)	$(-1+1)/60 = 0.00$ (ms)
H'0	$(0+1)/120 = 8.33$ (ms)	$(0+1)/60 = 16.67$ (ms)
H'1	$(1+1)/120 = 16.67$ (ms)	$(1+1)/60 = 33.33$ (ms)
H'2	$(2+1)/120 = 25.00$ (ms)	$(2+1)/60 = 50.00$ (ms)
.	.	.
.	.	.
.	.	.
H'D	$(13+1)/120 = 116.67$ (ms)	$(13+1)/60 = 233.33$ (ms)
H'E	$(14+1)/120 = 125.00$ (ms)	$(14+1)/60 = 250.00$ (ms)

2.2 TFT-LCD Panel Specifications

Table 4 lists the specification of the TFT-LCD panel to use in this application. The specifications of the TFT-LCD panel used for this application note (LS037V7DW01, manufactured by Sharp Corporation) are listed in the table below. As detailed specifications differ with the TFT-LCD panel, be sure to check the data sheet for the product you will be using.

2.2.1 General Specifications

Table 4 lists the general specifications of the TFT-LCD panel to use in this application.

Table 4 TFT-LCD Panel General Specifications (Excerpt from Datasheet)

Item	Specifications
Resolution	VGA or QVGA
Number of pixels	H 480 × V 640 (Number of dots: H (480 × 3) × V 640)
Pixel configuration	R, G, B vertical stripes
Number of colors	260,000 colors
Input signal	CMOS RGB (6 bits each digital)

2.2.2 Pin Functions

Table 5 lists the pin functions of the TFT-LCD panel used in this application.

Table 5 TFT-LCD Panel Pin Functions (Excerpt from Datasheet)

Symbol	Description
RESB	Reset signal
INI	Power-on control
DEN	Display-on signal
HSYNC	Horizontal sync signal
VSYNC	Vertical sync signal
CLKIN	Dot clock
R5-0	Red data signal (MSB: R5)
G5-0	Green data signal (MSB: G5)
B5-0	Blue data signal (MSB: B5)

2.2.3 Interface Timing

Figure 6 and figure 7 shows the interface timing of the TFT-LCD panel used in this application. Table 6 lists the timing characteristics.

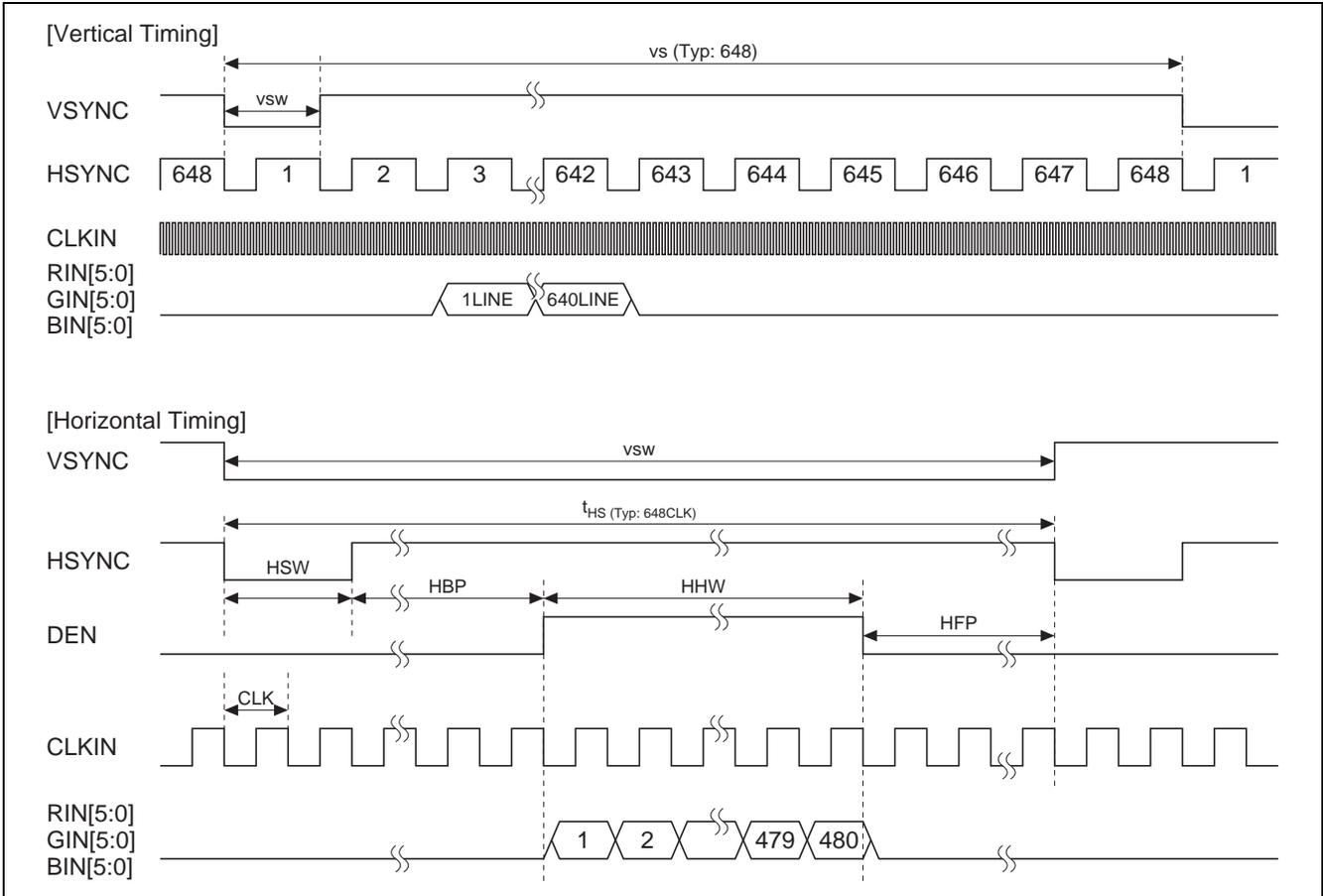


Figure 6 TFT-LCD Panel Interface Timing Example (Excerpt from Datasheet)

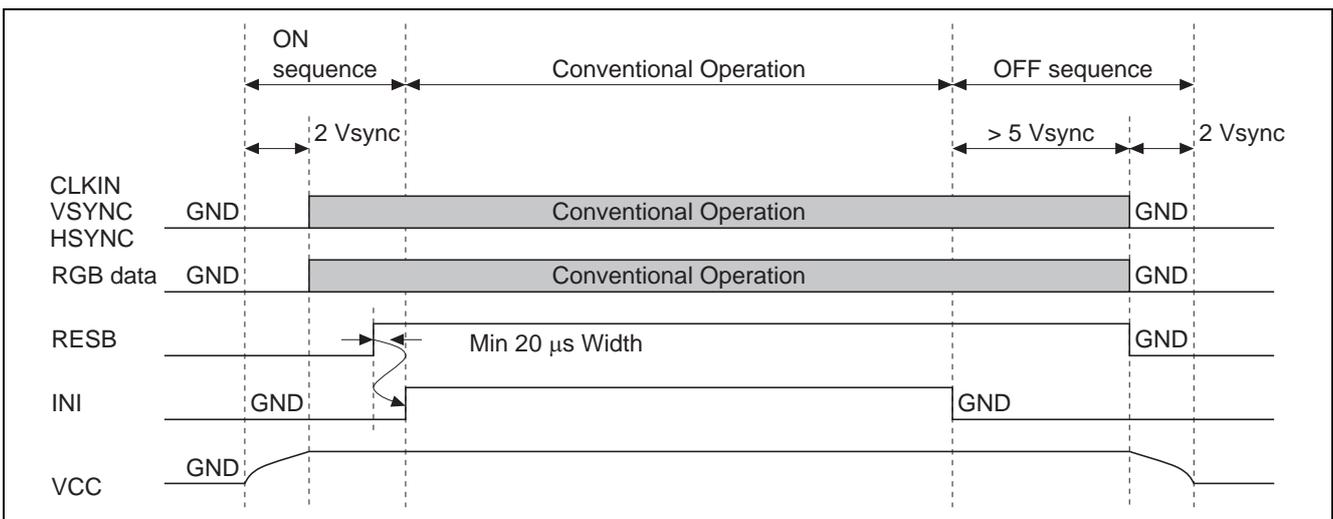


Figure 7 TFT-LCD Panel Power-Supply Sequence (Excerpt from Datasheet)

Table 6 TFT-LCD Panel Timing Characteristics (Excerpt from Datasheet)

Item		MODE	Symbol	Min	Typ	Max	Unit
CLK	Cycle time	VGA	t_{CLK}	38	39.7	41.7	ns
		QVGA		152	158.8	167	
Hsync	Cycle time	VGA	t_{HS}	—	648	—	CLK
		QVGA		—	324	—	
	Valid width		t_{HSW}	—	2	—	
Vsync	Cycle time	VGA	t_{VS}	—	648	—	HCYC
		QVGA		—	324	—	
	Valid width		t_{VSW}	—	1	—	
DEN	Horizontal back porch time	VGA	t_{HBP}	28	78	166	t_{CLK}
		QVGA		14	38	82	
	Horizontal front porch time	VGA	t_{HFP}	0	88	138	t_{CLK}
		QVGA		0	44	68	
Valid width		t_{HHW}	—	480	—	t_{CLK}	

2.3 TFT-LCD Panel Circuit Example

2.3.1 Pin Connection Example

Figure 8 shows the TFT-LCD panel hardware connection in this application.

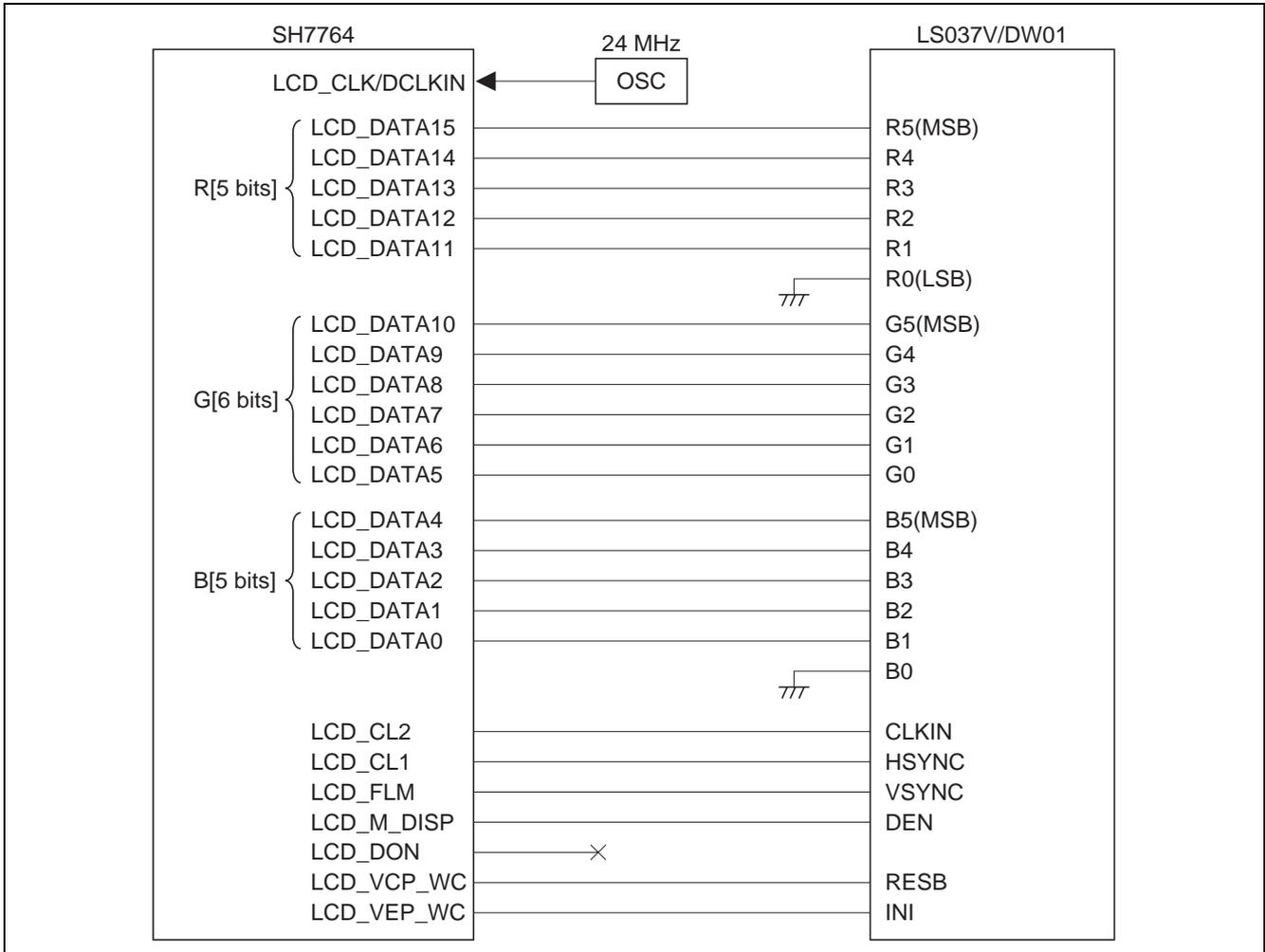


Figure 8 TFT-LCD Panel Hardware Connection

2.4 Sample Program Specifications

This section describes the specifications of the sample program and shows the flow chart of each processing.

2.4.1 Specifications

- Outputs the graphic image to the VGA size (V 480 x H 640) TFT-LCD panel.
- Red, green, and blue bars are displayed on the panel.

2.4.2 Main Flow Chart of the Sample Program

Figure 9 shows the main flow chart of the sample program. Initialization of the LCDC by the sample program is shown in figures 10 to 12, and the display is turned on after execution of the processing shown in figure 13. After graphics have been displayed on the TFT-LCD panel over a certain period, the display is turned off following execution of the processing shown in figure 14.

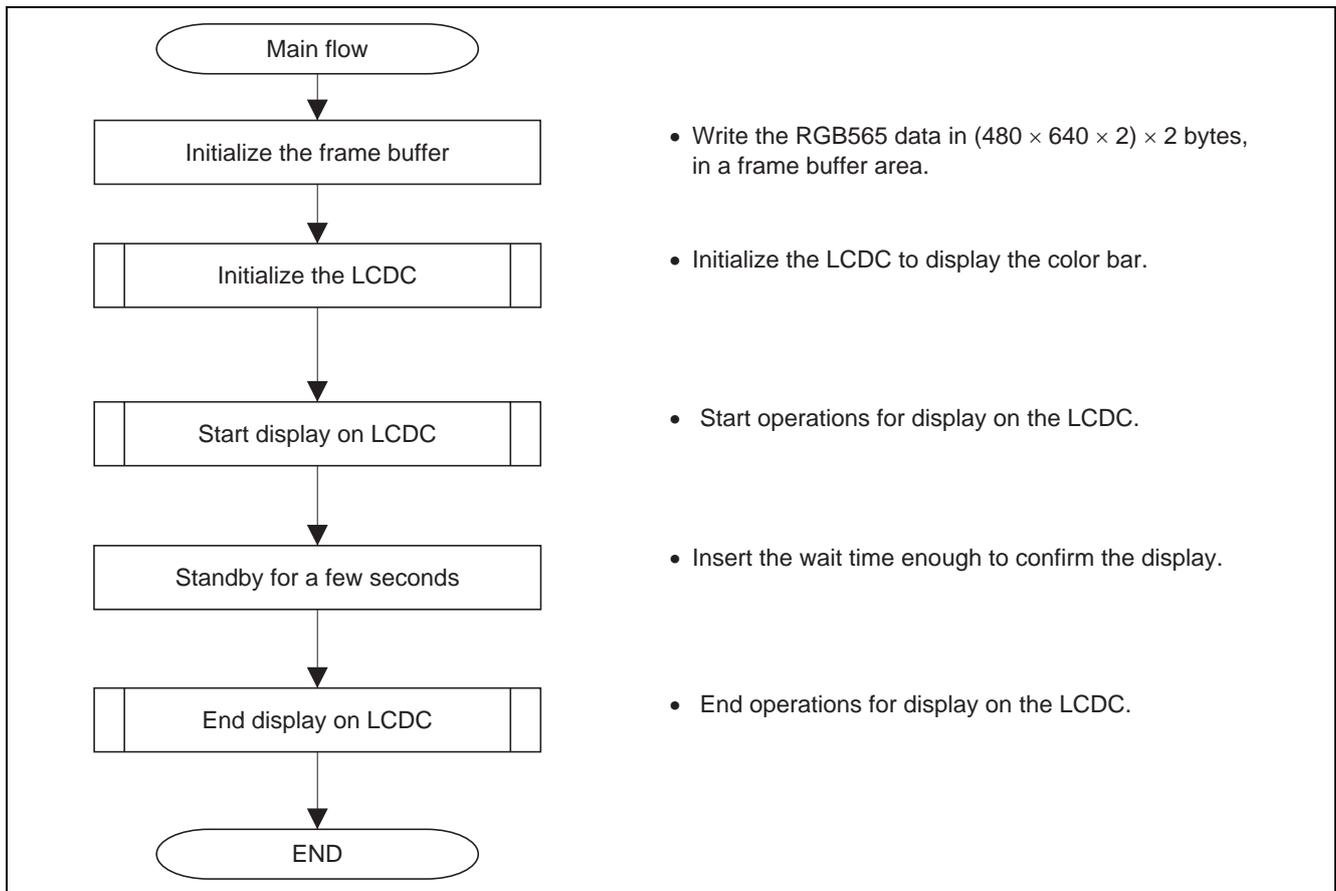


Figure 9 Sample Program Main Flow

2.4.3 Initialization of the LCDC

Figure 10 shows the flow for initialization of the LCDC.

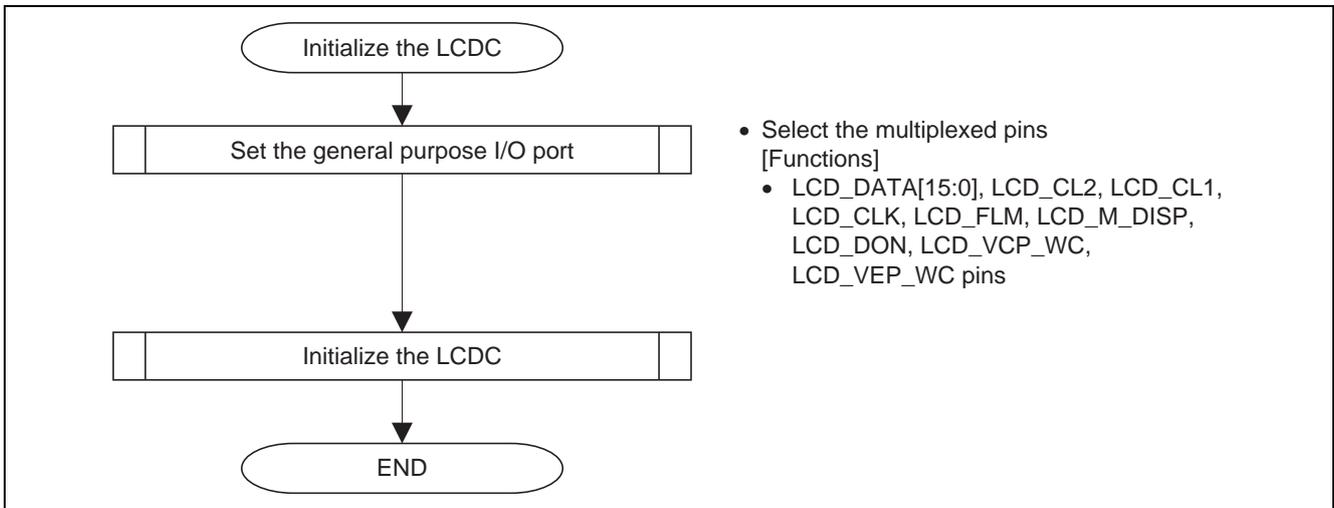


Figure 10 Flow for Initialization of the LCDC

2.4.4 Setting the LCDC

Figure 11 and figure 12 show the setting examples of the LCDC. Follow this procedure to set the control signal output for the TFT-LCD panel. Values listed in figure 11 and figure 12 are set according to the TFT-LCD panel specifications described in section 2.2.

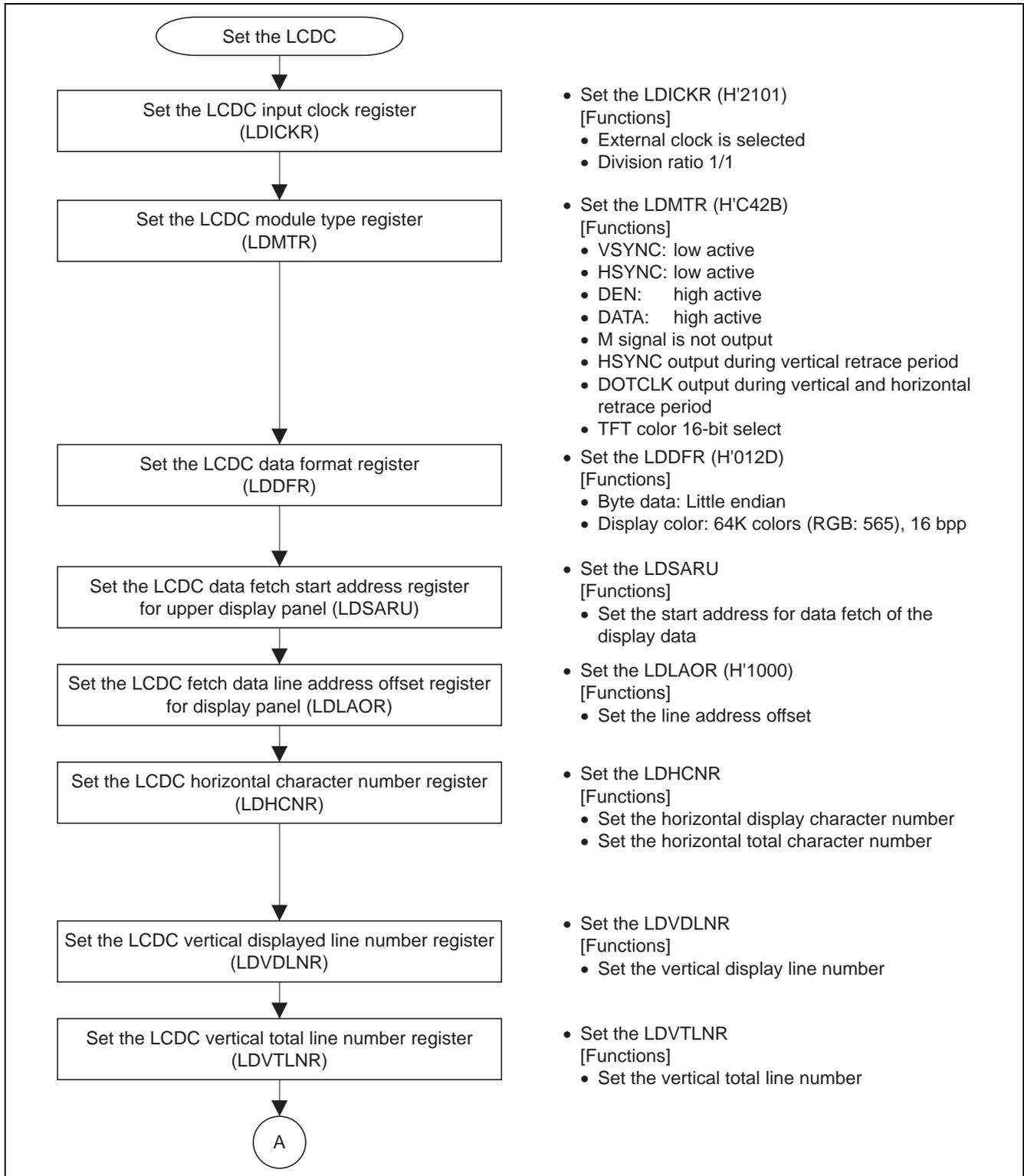


Figure 11 Setting Examples of the LCDC (1)

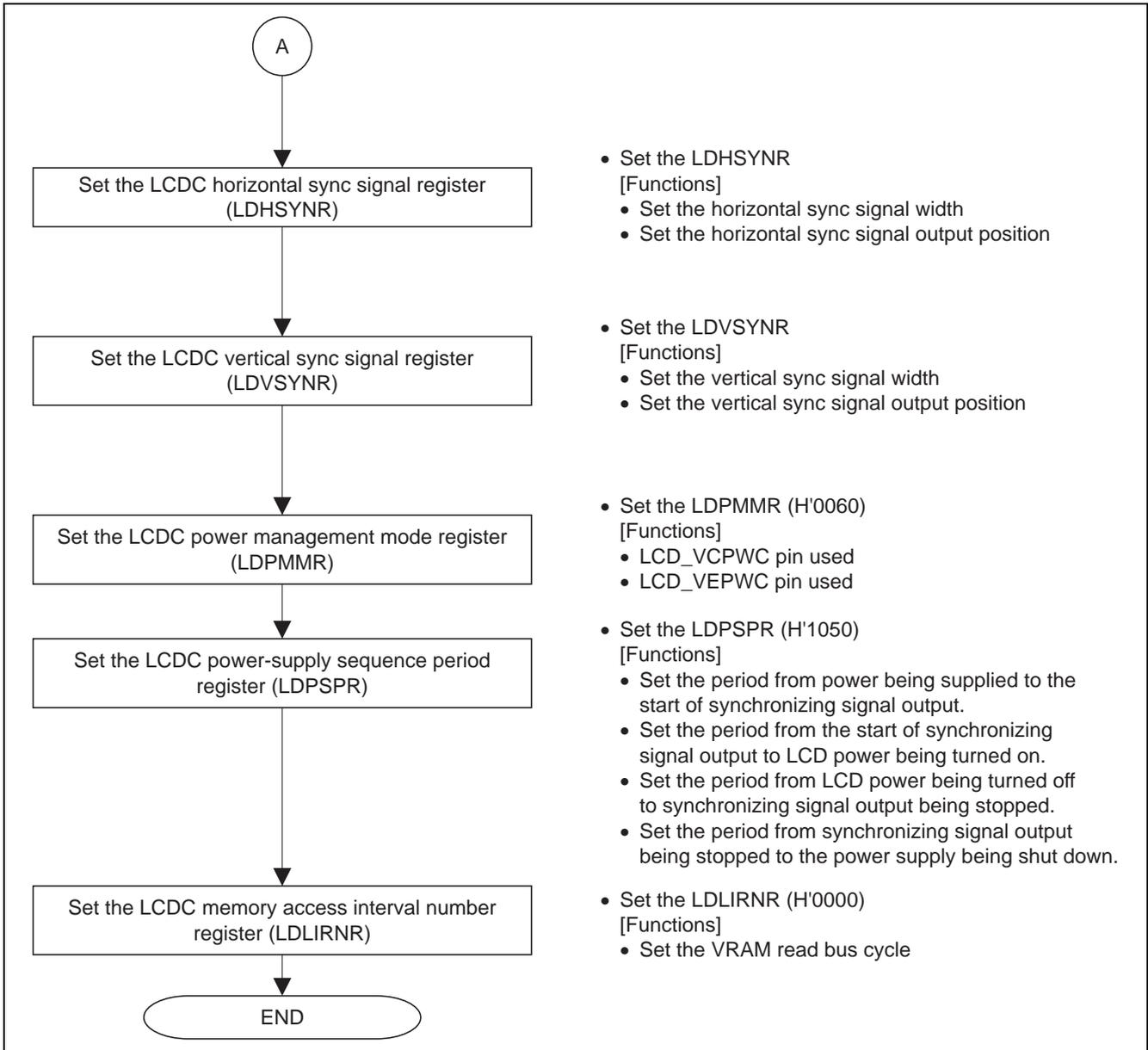


Figure 12 Setting Examples of the LCDC (2)

2.4.5 Setting the LCDC Starts Display and LCDC Stops Display

Figure 13 shows the setting example of the LCDC starts display, and figure 14 shows the setting example of the LCDC stops display.

When 1s are written to the DON2 bit and the DON bit, the LCDC starts display. When 0 is written to the DON bit, the LCDC stops display.

When display starts or ends, LCDC operation must be in accord with the power-control sequences specified in section 2.4.4, Setting the LCDC. The DON bit must not be manipulated until the given sequence is complete.



Figure 13 Setting Examples of the Start of LCDC Display

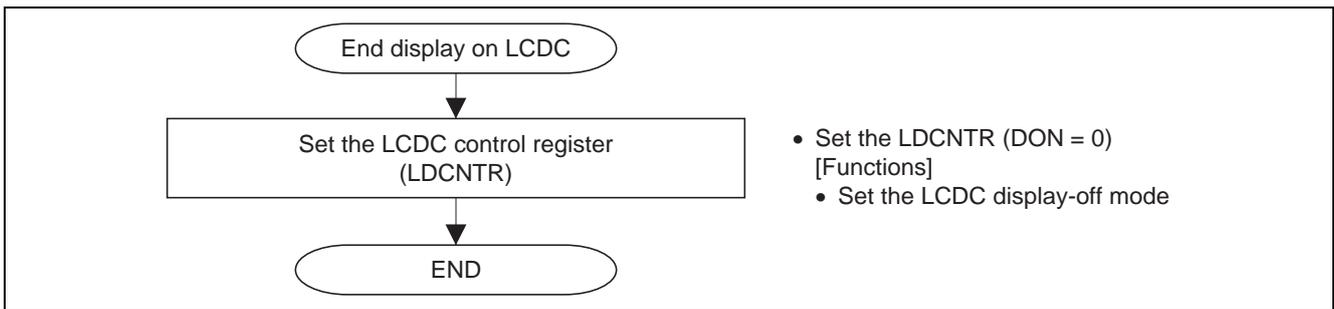


Figure 14 Setting Examples of the Stop of LCDC Display

3. Sample Program "lcdc.c"

3.1 Listings of Sample Program "Macro definition"

```

1  /*"FILE COMMENT"***** Technical reference data *****
2  *
3  *   System Name : SH7764 Sample Program
4  *   File Name   : lcdc.c
5  *   Abstract    : VDC2 TFT-LCD Panel Display Example
6  *   Version     : 1.00.00
7  *   Device      : SH7764
8  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.05.01).
9  *               : C/C++ compiler package for the SuperH RISC engine family
10 *               :                               (Ver.9.03 Release00).
11 *   OS          : none
12 *   H/W Platform: R0K507764E001BR
13 *   Disclaimer  :
14 *               <Note>
15 *               This sample program is provided only as a reference and
16 *               its operation is not guaranteed.
17 *               Use this sample program as a technical reference when
18 *               developing software.
19 *
20 *   The information described here may contain technical inaccuracies or
21 *   typographical errors. Renesas Technology Corporation and Renesas Solutions
22 *   assume no responsibility for any damage, liability, or other loss rising
23 *   from these inaccuracies or errors.
24 *
25 *   Copyright (C) 2009 Renesas Technology Corp. All Rights Reserved
26 *   AND Renesas Solutions Corp. All Rights Reserved
27 *
28 *   History     : June.01,2009 Ver.1.00.00
29 *"FILE COMMENT END"*****
30 #include "iodefine.h"
31
32 /* ==== Macro definition ==== */
33 /* ---- TFT panel display module ---- */
34 #define TFT_TOTAL_CLOCK 648 /* Width including the blanking interval */
35 #define TFT_TOTAL_LINE 648 /* Height including the blanking interval */
36 #define TFT_PANEL_CLOCK 480 /* Number of pixels in horizontal direction */
37 #define TFT_PANEL_LINE 640 /* Number of pixels in vertical direction */
38 #define TFT_H_FRONT_PORCH 88 /* Horizontal front porch */
39 #define TFT_HSYNC_START (TFT_PANEL_CLOCK + TFT_H_FRONT_PORCH)
40 /* Display start position in horizontal direction */
41 #define TFT_HSYNC_WIDTH 8 /* Hsync pulse width (min = 8 dots) */
42 #define TFT_VSYNC_WIDTH 1 /* Vsync pulse width */
43 #define LINE_OFFSET 2048 /* Line offset */
44
45 /* ==== Function prototype declaration ==== */
46 void lcdc_main(void);
47 void lcdc_initial(void);
48 void lcdc_port_set(void);
49 void lcdc_control_initial(void);
50 void lcdc_enable(void);
51 void lcdc_disable(void);
52 void fill_rect(unsigned int x, unsigned int y,
53 unsigned int w, unsigned int h, unsigned short color,
54 unsigned int base_address, unsigned int line_offset);
55 void delay(void);
56
57 /* ==== Variable definition ==== */
58 #pragma section _LCD_FRAME_BUFFER /* Places on a 512-byte boundary in the cache disabled area */
59 unsigned short frame_buffer[TFT_PANEL_CLOCK][TFT_PANEL_LINE];
60 #pragma section

```

3.2 Listings of Sample Program "Display main"

```

61  /* "FUNC COMMENT"*****
62  * ID      :
63  * Outline : Display main
64  *-----
65  * Include :
66  *-----
67  * Declaration : void lcdc_main(void);
68  *-----
69  * Function   :
70  *-----
71  * Argument   : void
72  *-----
73  * Return Value: void
74  * "FUNC COMMENT END"*****/
75  void lcdc_main(void)
76  {
77      /* ---- Initializes the frame buffer ---- */
78      fill_rect(0,0,TFT_PANEL_CLOCK / 3,TFT_PANEL_LINE,0xF800,
79              (unsigned int)frame_buffer,LINE_OFFSET);
80      fill_rect(TFT_PANEL_CLOCK / 3,0,(TFT_PANEL_CLOCK / 3) * 2,TFT_PANEL_LINE,0x07E0,
81              (unsigned int)frame_buffer,LINE_OFFSET);
82      fill_rect((TFT_PANEL_CLOCK / 3) * 2,0,TFT_PANEL_CLOCK,TFT_PANEL_LINE,0x001F,
83              (unsigned int)frame_buffer,LINE_OFFSET);
84      /* Draws a color bar in the frame buffer */
85
86      /* ---- Initializes the LCDC module ---- */
87      lcdc_initial();
88
89      /* ---- Outputs the color bar on the TFT-LCD ---- */
90      lcdc_enable();
91      delay(); /* Waits for several seconds */
92      lcdc_disable();
93  }

```

3.3 Listings of Sample Program "LCDC initialization"

```

94  /* "FUNC COMMENT"*****
95  * ID      :
96  * Outline : LCDC initialization
97  *-----
98  * Include :
99  *-----
100 * Declaration : void lcdc_initial(void);
101 *-----
102 * Function   :
103 *-----
104 * Argument   : void
105 *-----
106 * Return Value: void
107 * "FUNC COMMENT END"*****/
108 void lcdc_initial(void)
109 {
110     lcdc_port_set();    /* I/O pin setting */
111     lcdc_control_initial(); /* LCDC setting */
112 }

```

3.4 Listings of Sample Program "I/O pin setting"

```

113 /* "FUNC COMMENT"*****
114 * ID      :
115 * Outline : I/O pin setting
116 *-----
117 * Include :
118 *-----
119 * Declaration : void lcdc_port_set(void);
120 *-----
121 * Function   : Sets I/O pins for the LCDC.
122 *-----
123 * Argument   : void
124 *-----
125 * Return Value: void
126 * "FUNC COMMENT END"*****/
127 void lcdc_port_set(void)
128 {
129     /* ---- LCD_DATA15,14,13,12,11,10,9,8 ---- */
130     GPIO.PTSEL_G.WORD = 0x0000;
131
132     /* ---- LCD_CL2,LCD_DON,LCD_VCP_WC,LCD_VEP_WC ---- */
133     GPIO.PTSEL_H.BIT._PTSEL_H3 = GPIO.PTSEL_H.BIT._PTSEL_H2 =
134     GPIO.PTSEL_H.BIT._PTSEL_H1 =GPIO.PTSEL_H.BIT._PTSEL_H0 = 0;
135
136     /* ---- LCD_DATA7,6,5,4,3,2,1 ---- */
137     GPIO.PTSEL_I.WORD = 0x0000;
138
139     /* ---- LCD_DATA0,LCD_CL1,LCD_CLK,LCD_FLM,LCD_M_DISP --- */
140     GPIO.PTSEL_K.BIT._PTSEL_K4 = GPIO.PTSEL_K.BIT._PTSEL_K3 =
141     GPIO.PTSEL_K.BIT._PTSEL_K2 = GPIO.PTSEL_K.BIT._PTSEL_K1 =
142     GPIO.PTSEL_K.BIT._PTSEL_K0 = 0;
143 }

```

3.5 Listings of Sample Program "LCDC initialization"

```

144 /*"FUNC COMMENT"*****
145 * ID      :
146 * Outline : LCDC initialization
147 *-----
148 * Include :
149 *-----
150 * Declaration : void lcdc_control_initial(void);
151 *-----
152 * Function   : Initializes the LCDC.
153 *-----
154 * Argument   : void
155 *-----
156 * Return Value: void
157 *"FUNC COMMENT END"*****/
158 void lcdc_control_initial(void)
159 {
160     /* ---- Clock selection and divider setting ---- */
161     LCDC.LDICKR.WORD = 0x2101;
162     /* bit13:12(ICKSEL)=01 uses LCD_CLK (external pin) */
163     /* bit5:0(DCDR)=000001 divider 1/1 */
164
165     /*---- Pin polarity selection ---- */
166     LCDC.LDMTR.WORD = 0xC42B;
167     /* bit15(FLMPOL)=1      Vsync is "L" active */
168     /* bit14(CL1POL)=1     Hsync is "L" active */
169     /* bit13(DISPPOL)=0    DEN is "H" active */
170     /* bit12(DPOL)=0      DATA is "H" active */
171     /* bit10(MCNT)=1      M signal is not output */
172     /* bit9(CL1CNT)=0     Hsync is output during the vertical interval */
173     /* bit8(CL2CNT)=0    DotCLK is output during the vertical interval */
174     /* bit5:0(MIFTYP)=101011 TFT color-16bit */
175
176     /* ---- Data format setting ---- */
177     LCDC.LDDFR.WORD = 0x012D;
178     /* bit8(PABD)=1      Little endian */
179     /* bit6:0(DSPCOLOR)=0101101 64k-Color RGB:5-6-5 */
180
181     /* Setting for reading images from external memory ---- */
182     LCDC.LDSARU = (unsigned long *)frame_buffer;
183
184     /* ---- Line offset setting ----*/
185     LCDC.LDLAOR = LINE_OFFSET * sizeof(short);
186
187     /* ---- Settings of the horizontal display character and the total number of characters ---- */
188     LCDC.LDHCCR.BIT._HDCN = (TFT_PANEL_CLOCK / 8) - 1;
189     LCDC.LDHCCR.BIT._HTCN = (TFT_TOTAL_CLOCK / 8) - 1;
190
191     /* ---- Settings of the vertical display line and the total number of lines ---- */
192     LCDC.LDVCLNR.BIT._VDLN = TFT_PANEL_LINE - 1;
193     LCDC.LDVCLNR.BIT._VTLN = TFT_TOTAL_LINE - 1;
194
195     /* ---- Horizontal/vertical sync signal timing settings ---- */
196     LCDC.LDHSYNR.BIT._HSYNW = (TFT_HSYNC_WIDTH / 8) - 1;
197     LCDC.LDHSYNR.BIT._HSYNP = (TFT_HSYNC_START / 8) - 1;
198     LCDC.LDVSYNR.BIT._VSYNW = TFT_VSYNC_WIDTH - 1;
199     LCDC.LDVSYNR.BIT._VSYNP = (TFT_TOTAL_LINE - TFT_VSYNC_WIDTH) - 2;
200
201     /* ---- Power control pin setting ---- */
202     LCDC.LDPMMR.WORD = 0x0060;
203     /* bit[6](VCPE) = 1      uses the LCD_VCPWC pin */
204     /* bit[5](VEPE) = 1      uses the LCD_VEPWC pin */

```

```

205     LCDC.LDPSPR.WORD = 0x1050;
206     /* bit[15:12](ONA) = 0001 Power-on to start of the sync signal (33.33ms) */
207     /* bit[11:8](ONB) = 0000 Start of the sync signal to LCD power-on (16.67ms) */
208     /* bit[7:4](OFFE) = 0101 LCD power-off to end of the sync signal (100ms) */
209     /* bit[3:0](OFFF) = 0000 End of the sync signal to power-off (16.67ms) */
210
211     /* ---- VRAM read clock cycle interval setting ---- */
212     LCDC.LDLIRNR.WORD = 0x0000;
213 }

```

3.6 Listings of Sample Program "Start LCDC display operation, Stop LCDC display operation"

```

214 /*"FUNC COMMENT"*****
215 * ID      :
216 * Outline : Start LCDC display operation
217 *-----
218 * Include :
219 *-----
220 * Declaration : void lcdc_enable(void);
221 *-----
222 * Function    : Starts the display operation.
223 *-----
224 * Argument    : void
225 *-----
226 * Return Value: void
227 /*"FUNC COMMENT END"*****/
228 void lcdc_enable(void)
229 {
230     /* ---- Starts the LCDC display operation ---- */
231     LCDC.LDCNTR.BIT._DON2 = 1;
232     LCDC.LDCNTR.BIT._DON = 1;
233     /* bit[4](DON2) = 1 Starts the LCDC display operation */
234     /* bit[0](DON)  = 1 Display-on mode */
235 }
236
237 /*"FUNC COMMENT"*****
238 * ID      :
239 * Outline : Stop LCDC display operation
240 *-----
241 * Include :
242 *-----
243 * Declaration : void lcdc_disable(void);
244 *-----
245 * Function    : Stops the display operation.
246 *-----
247 * Argument    : void
248 *-----
249 * Return Value: void
250 /*"FUNC COMMENT END"*****/
251 void lcdc_disable(void)
252 {
253     /* ---- Stops the LCDC display operation ---- */
254     LCDC.LDCNTR.BIT._DON = 0;
255     /* bit[0](DON)  = 0 Display-off mode */
256 }

```

4. Documents for Reference

- Hardware Manual
SH7764 Group Hardware Manual (REJ09B0360)
The most up-to-date version of this document is available on the Renesas Technology Website.
- Software Manual (REJ09B0003)
SH-4A Software Manual
The most up-to-date version of this document is available on the Renesas Technology Website.

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