To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8SX Family

Input-Capture Operation Employing Multiplexed TPU and I/O Pin Functions

Introduction

Previously, measuring the period and width at high level of an input pulse waveform was only possible by feeding the same pulse to two separate TIOC pins and using the input capture functions. On this device, PFCR9 register settings for a pin can be used to place the required multiplexed TPU and input/output pin functions on a single TIOC pin, allowing measurement of the period and width at high level of an input pulse waveform with a single input port pin.

Target Device

H8SX/1663F

Contents

1. Specification

By employing multiplexed TPU and I/O pin functions, along with the input capture function of a timer, a single TIOC input pin is used to measure the period and width at high level of an input pulse waveform.

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating Frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Description of Functions Used

By setting the PFCR9 register so that a single port pin is shared between its TIOCA0 and TIOCB0 functions, the pin can be employed to measure the width at high level and period of a pulse waveform. Figure 1 is a block diagram of input-capture operation using the multiplexed TPU and I/O pin functions. Descriptions of the TPU and PFCR9 registers are given below the figure.

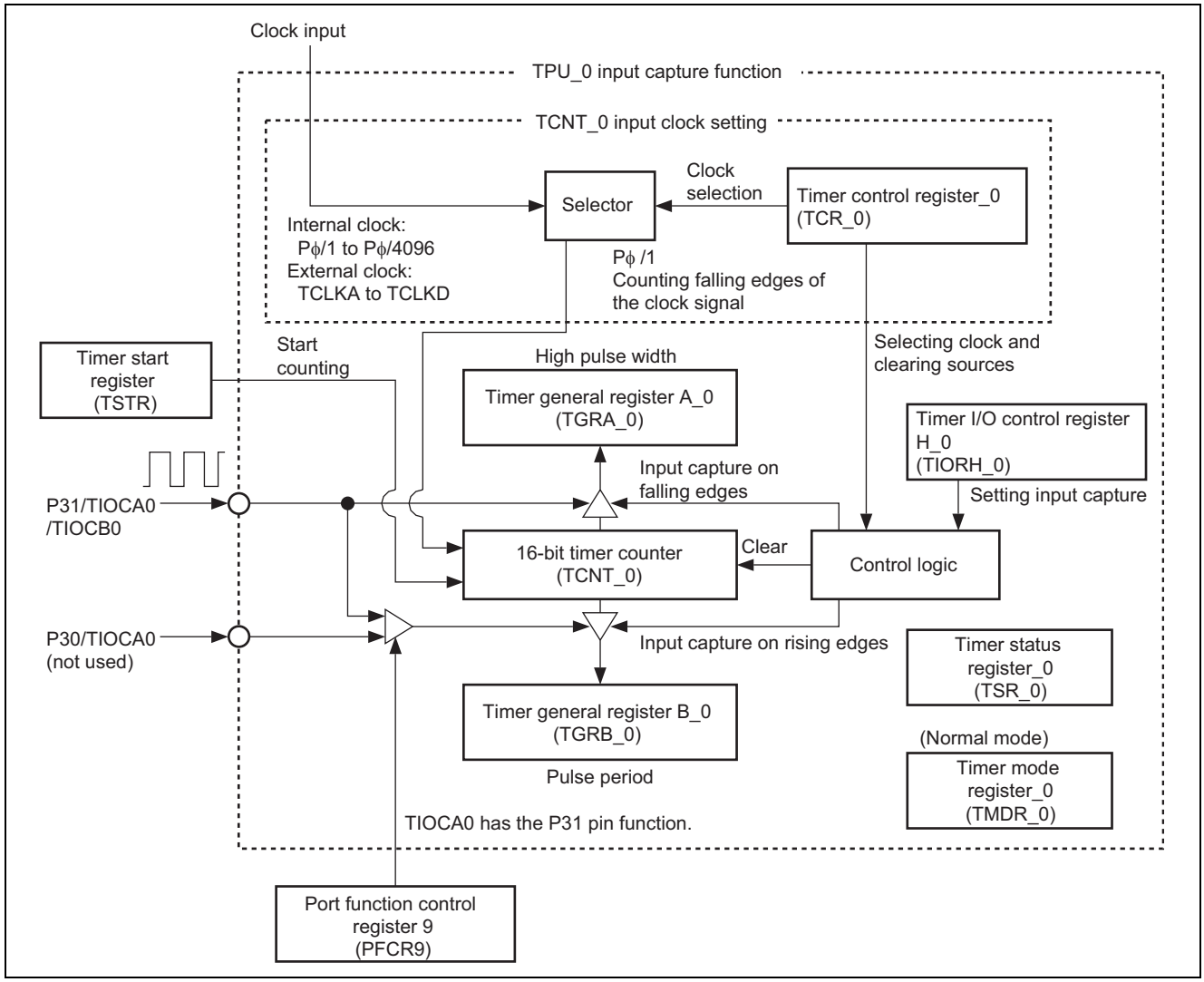


Figure 1 Block Diagram of Input Capture Operation with Multiplexed TPU and I/O Pin Functions

- Timer Start Register (TSTR)

TSTR starts or stops operation of channels 0 to 5. Stop the TCNT counter before setting the operating mode in TMDR or the clock for counting in TCR.

- Timer Control Register_0 (TCR_0)

TCR controls the TCNT operation for each channel. The TPU has a total of six TCR registers, one for each channel. TCR register settings should only be made while TCNT operation is stopped.

- Timer I/O Control Register H_0 (TIORH_0)

TIOR controls TGR. The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.

To designate the input capture pin in TIOR, the DDR bit and ICR bit for the corresponding pin should be set to 0 and 1, respectively.

- Timer Counter_0 (TCNT_0)

TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel. TCNT is initialized to H'0000 by a reset or in hardware standby mode. TCNT cannot be accessed in 8-bit units. TCNT must always be accessed in 16-bit units.

- Timer General Register A_0 (TGRA_0)
- Timer General Register B_0 (TGRB_0)

TGR is a 16-bit readable/writable register and has a dual function as an output compare or input capture register. The TPU has 16 TGR registers, four each for channels 0 and 3 and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated for operation as buffer registers.
The TGR registers cannot be accessed in 8-bit units; they must always be accessed in 16-bit units. Combinations of TGR and buffer for buffer operation are TGRA and TGRC, TGRB and TGRC.

- Timer Mode Register_0 (TMDR_0)

TMDR sets the operating mode for each channel. In this sample task, TPU_0 is set for normal operation.

- Timer Status Register_0 (TSR_0)

TSR indicates the status of each channel.

- Port Function Control Register_9 (PFCR_9)

PFCR9 selects the functions for pins with multiplexed TPU and I/O pin functions. In this sample task, the input pin for input capture in TIOCA0 can be set to operate as the P31, TIOCA0, or TIOCB0 pin.

4. Principles of Operation

Period of input pulse and high width can be measured from a TIOC input pin by using the multiplexed TPU and I/O pin functions, and the input-capture function.

4.1 Multiplexed TPU and I/O Pin Functions

Figures 2 and 3 illustrate examples of connection for conventional pulse measurement and connection for pulse measurement by using multiplexed TPU and I/O pin functions, respectively. Setting the PFCR9 bit for the multiplexed TPU and I/O pin functions to 1 makes TIOCA (C), the input pin for TGRA (C), the same port pin as TIOCB (D). Therefore, input capture to TGRA (C) and TGRB (D) can be accomplished with a single pin that functions as both TIOCB (D) and TIOCA (C).

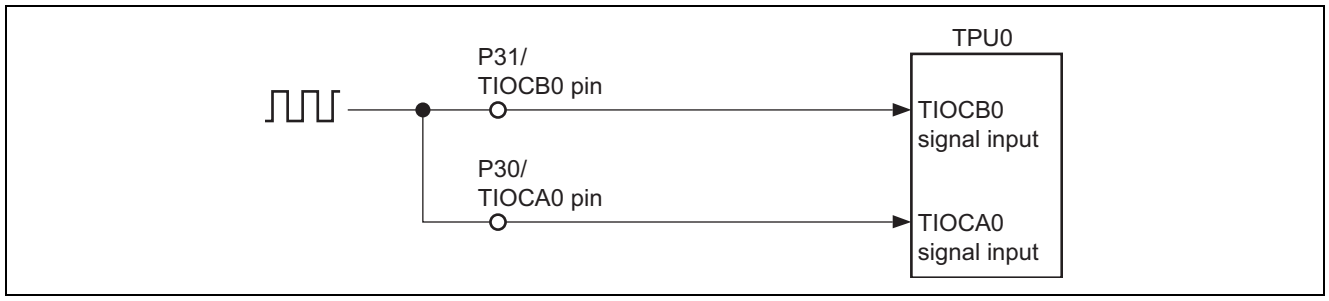


Figure 2 Example of Connection for Conventional Pulse Measurement

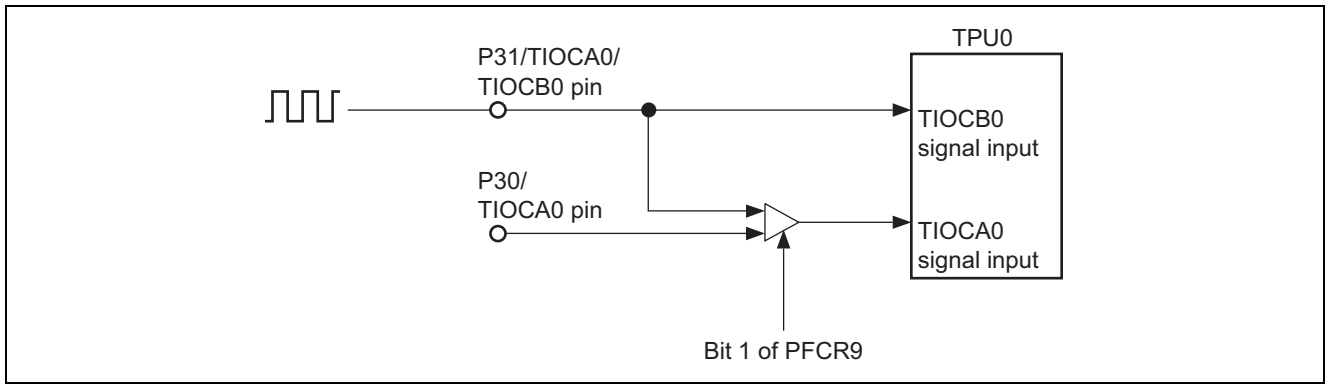
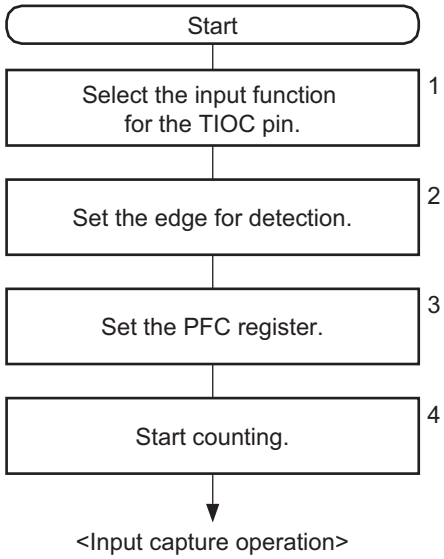


Figure 3 Example of Connection for Pulse Measurement by Using Multiplexed TPU and I/O Pin Functions

4.2 Example of Setting Procedure

Figure 4 illustrates an example of settings for measuring the period and high width of a pulse waveform by using multiplexed TPU and I/O pin functions.

1. Use TIOCA and TIOCB or TIOCC and TIOCD as a pair.
2. Use the corresponding TIOR to set the TGRs as input capture registers. Then, set the triggers for input capture to the registers so that one is rising edge and the other is falling edge.
3. Set the corresponding bit in PFCR9 to 1.
4. Set the CST bit in TSTR to 1, making the timer start counting.



Note: Usage of multiple TPU and I/O pin functions is only possible with inputs.
When a pin with a multiplexed TIOC function is set as an output, the pin cannot be shared among functions.

Figure 4 Example of Settings for Measurement of Pulse Period and High Width by Using Multiplexed TPU and I/O Pin Functions

4.3 Example of Measuring Pulse Period and High Width

Figure 5 illustrates the operation of measuring pulse period and high width. Also, table 2 describes hardware and software processing.

In this sample task, the P31/TIOCA0/TIOCB0 pin is set to multiple pin functions. Falling edges are selected for input capture as the TIOCA0 input pin. Rising edges are selected for input capture as the TIOCB0 input pin. Input capture by a single pin as TIOCB0 and TIOCA is selected by setting bit 1 in the PFCR9 register to 1. Clearing of the TCNT_0 counter is by input-capture events generated for TGRB_0.

With the above settings the number reached by the counter during the period over which the input pulse is high will be transferred to TCRA_0. The number reached by the counter during one period of the input pulse will be transferred to TGRB_0.

The period and width at high level of the input pulse waveform can then be calculated from the period of the clock signal that drives counting by TCNT_0 and the values of TGRA_0 and TGRB_0.

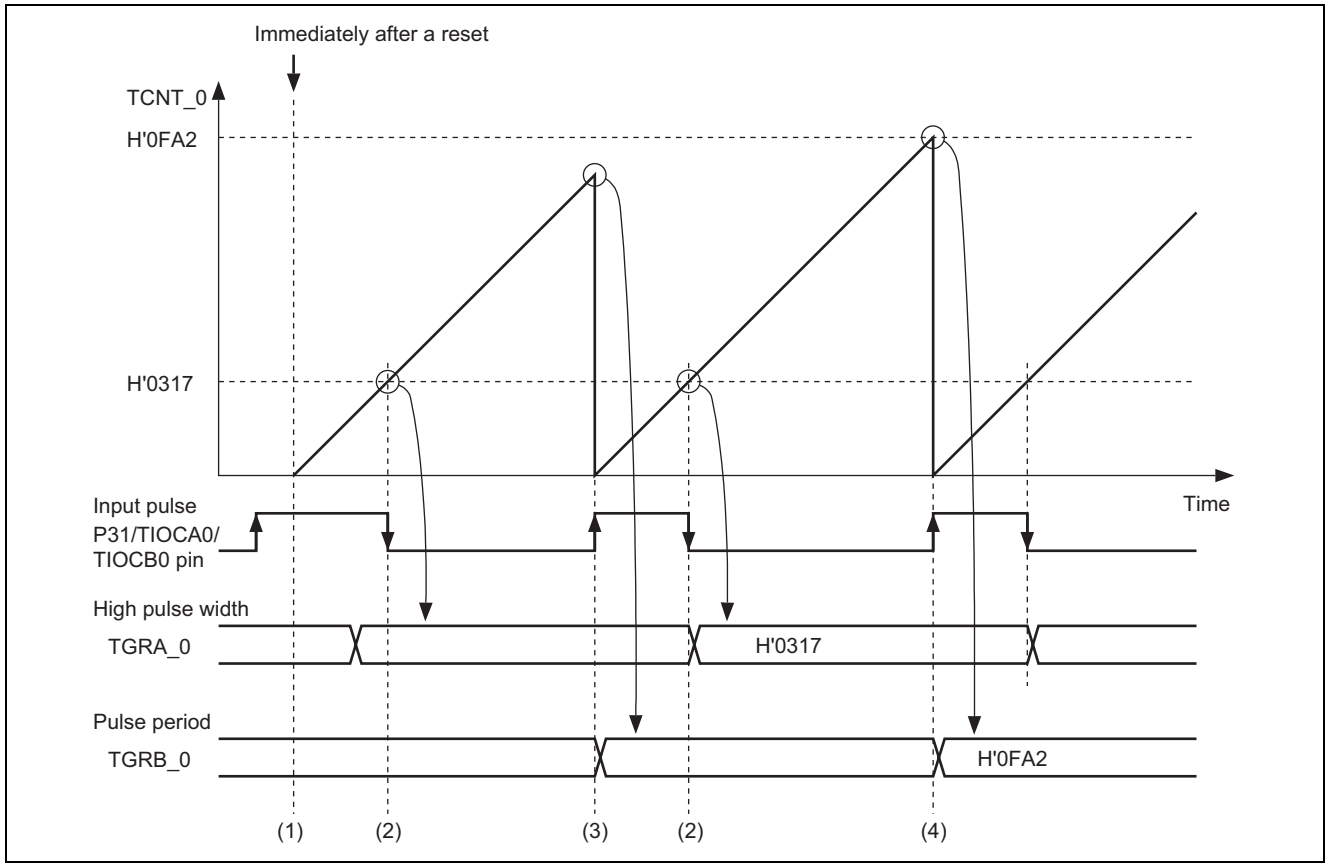


Figure 5 Example of Operation when Using Multiplexed TPU and I/O Pin Functions to Measure Period and Width at High Level of a Pulse Signal

Table 2 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial setting*
(2)	(a) Input capture in TGRA_0 (b) Transfer value in TCNT_0 to TGRA_0. (c) Set TGFB bit in TSR_0 to 1.	No processing
(3)	(a) Input capture in TGRB_0 (b) Transfer value in TCNT_0 to TGRB_0. (c) Set TGFB bit in TSR_0 to 1.	(a) Clear TGFA and TGFB bits in TSR_0 to 0.
(4)	(a) Input capture in TGRB_0. (b) Transfer value in TCNT_0 to TGRB_0. (c) Set TGFB bit in TSR_0 to 1.	(a) Copy pulse width (TGRA_0) to RAM (plshigh). (b) Copy pulse period (TGRB_0) to RAM (plsperiod).

Note *: Initial settings
(a) The rising edge of the signal on the TIOCB0 pin is the trigger for input capture by TGRB_0 of the value in TCNT_0. The falling edge of the signal on the TIOCA0 pin is the trigger for input capture by TGRA_0 of the value in TCNT_0.
(b) Clear TCNT_0 by input capture in TGRB_0.
(c) Input capture in TGRA_4 is generated by a compare match of TGRA_3.
(d) Clear the status flags of TGRA/TGRB/TPU.
(e) Start counting by TCNT_0.

5. Description of Software

5.1 Operating Environment

Table 3 Operating environment

Item	Description
Development tool	High-performance Embedded Workshop Ver.4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.01 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	B	Non-initialized data area (RAM area)

Table 5 Vector Table for Interrupt Exception Processing

Exception Processing Source	Vector No.	Vector Table Address	Destination Function
Reset	0	H'000000	init

5.2 List of Functions

Table 6 List of Functions

Function Name	Function
init	Initialization routine Sets the CCR and configures the clocks, releases modules from the module stop mode, and calls the main function.
main	Main routine Selects the multiplexed TPU and I/O pin functions, sets up TPU_0, and measures pulses.

5.3 RAM Usage

Table 7 RAM Usage

Type	Name of Variable	Description	Used in Function
unsigned short	plshigh	Pulse width Holds the width (high level) of the input pulse waveform.	main
unsigned short	plsperiod	pulse period Holds the period of the input pulse waveform.	main

5.4 Formulae for Calculating Measured Values for the Pulse Waveform

The period and width of the pulse waveform are calculated with the following formulae.

When Pϕ = 24 MHz and TGRB_0 = H'0FA2,

Pulse period = TGRB_0 + 1/Pϕ = H'0FA2 +1/24 MHz
= 166.79 … ≅ 166.8 µs

When Pϕ = 24 MHz and TGRA_0 = H'0317,

High pulse width = TGRA_0 +1/Pϕ = H'0317 + 1/24 MHz
= 33 µs

5.5 Description of Functions

5.5.1 init Function

1. Functional overview

Initialization routine which releases the modules from module stop mode, configures the clocks, and calls the main function.

2. Arguments

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latch is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by the mode pins (MD2 to MD0; see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latch is released by a reset.
10	MDS2	Undefined*	R	
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 8 Values of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select These bits select the frequency of the system clock provided to the CPU, DMAC, and DTC. 000: Input clock × 4
9	ICK1	0	R/W	
8	ICK0	0	R/W	
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select These bits select the frequency of the peripheral module clock. 001: Input clock × 2
5	PCK1	0	R/W	
4	PCK0	1	R/W	
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select These bits select the frequency of the external bus clock. 000: Input clock × 4
1	BCK1	0	R/W	
0	BCK0	0	R/W	

- MSTPCRA, MSTPCRB, and MSTPCRC control the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode. 1: Enabled all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

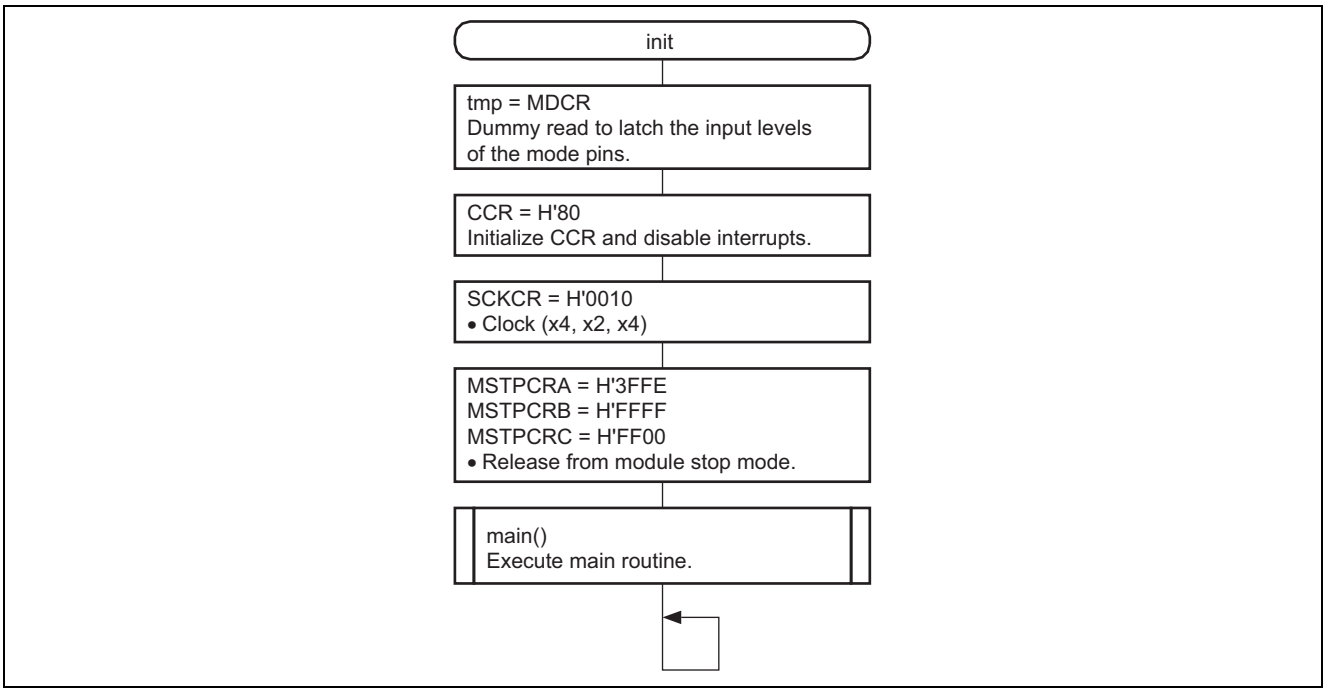
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input levels
of the mode pins.
CCR = H'80
Initialize CCR and disable interrupts.
SCKCR = H'0010
• Clock (x4, x2, x4)
MSTPCRA = H'3FFE
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release from module stop mode.
main()
Execute main routine.

5.5.2 main Function

1. Functional overview

Selects the multiplexed TPU and I/O pin functions, sets up TPU_0 and measures pulses.

2. Arguments

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 3 data direction register (P3DDR) Number of bits: 8 Address: H'FFFB82

Bit	Bit Name	Setting	R/W	Description
1	P31DDR	0	R/W	0: Sets P31 as an input pin. 1: Sets P31 as an output pin.

- Port 3 input buffer control register (P3ICR) Number of pins: 8 Address: H'FFFB92

Bit	Bit Name	Setting	R/W	Description
1	P31ICR	1	R/W	0: Disables input buffer for pin P31. Input signal is fixed to high level. 1: Enables input buffer for pin P31. Reflects the state of the pin on the peripheral module side.

- Port function control register 9 (PFCR9) Number of bits: 8 Address: H'FFFBC9

Bit	Bit Name	Setting	R/W	Description
1	TPUMS0A	1	R/W	Multiplexed TPU and I/O Pin Functions Select Selects TIOCA0 function. 0: Specifies P30 as an output-compare output and an input-capture input. 1: Specifies P31 as an input-capture input and P30 as an output-compare output.

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	0	R/W	Counter start 5 to 0 Selects operation or stoppage for TCNT. 0: Stops counting by TCNT_5 to TCNT_0. 1: Counting by TCNT_5 to TCNT_0 proceeds.
4	CST4	0	R/W	
3	CST3	0	R/W	
2	CST2	0	R/W	
1	CST1	0	R/W	
0	CST0	1	R/W	

- Timer control register_0 (TCR_0) Number of bits: 8 Address: H'FFFFC0

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter clear 2 to 0
6	CCLR1	1	R/W	Select the trigger for clearing of counter TCNT_0.
5	CCLR0	0	R/W	010: TCNT_0 cleared on compare match of/input capture in TGRB_0.
4	CKEG1	0	R/W	Clock edge 1 and 0
3	CKEG0	0	R/W	Select the input clock edge. 00: Counts falling edges
2	TPSC2	0	R/W	Timer prescaler 2 to 0
1	TPSC1	0	R/W	Select the TCNT_3 counter clock.
0	TPSC0	0	R/W	000: Counts cycles of the internal clock Pϕ/1.

- Timer mode register_0 (TMDR_0) Number of bits: 8 Address: H'FFFFC1

Bit	Bit Name	Setting	R/W	Description
3	MD3	0	R/W	Mode 3 to 0
2	MD2	0	R/W	Set the timer operating mode.
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer I/O control register H_0 (TIORH_0) Number of bits: 8 Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Description
7	IOB3	1	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	Specify the function of TGRB_0.
5	IOB1	0	R/W	1000: TGRB_0 functions as an input capture register. Input
4	IOB0	0	R/W	capture on rising edges of the signal on the P31/TIOCA0/TIOCB0 pin.
3	IOA3	1	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	Specify the function of TGRA_0.
1	IOA1	0	R/W	1001: TGRA_0 functions as an input capture register. When
0	IOA0	1	R/W	TPUMS0A in PFCR9 is set to 1, input capture is on falling edges of the signal on the P31/TIOCA0/TIOCB0 pin.

- Timer status register_0 (TSR_0) Number of bits: 8 Address: H'FFFFC5

Bit	Bit Name	Setting	R/W	Description
1	TGFB	0	R/(W)*	Input Capture/Output Compare Flag B When TGRB_0 is functioning as an input capture register, the following conditions apply. [Setting condition] Transfer of the value in TCNT_0 to TGRB_0 triggered by the input capture signal [Clearing condition] Writing of 0 in TGFB_0 after having read TGFB when TGFA is set to 1.
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_1 is functioning as an input capture register, the following conditions apply. [Setting condition] Transfer of the value in TCNT_0 to TGRA_0 triggered by the input capture signal [Clearing condition] Writing of 0 in TGFA_0 after having read TGFA when TGFA is set to 1.

Note: * Only 0 can be written here, to clear the flag.

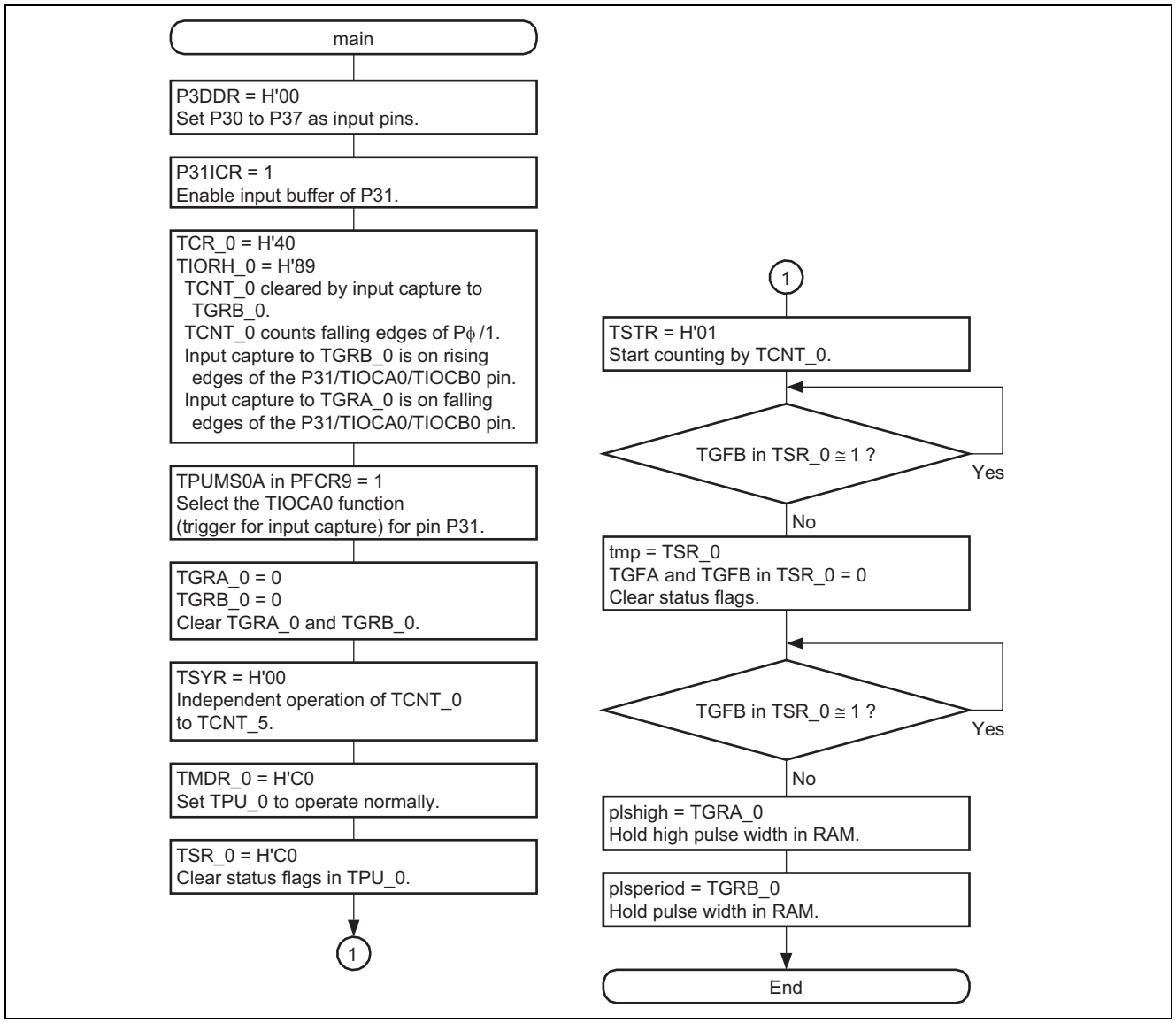
- Timer general register A_0 (TGRA_0) Number of bits: 16 Address: H'FFFFC8

Function: Input capture register in this application
Setting value: H'0000

- Timer general register B_0 (TGRB_0) Number of bits: 16 Address: H'FFFFCA

Function: Input capture register in this application
Setting value: H'0000

5. Flowchart


main
P3DDR = H'00
Set P30 to P37 as input pins.
P31ICR = 1
Enable input buffer of P31.
TCR_0 = H'40
TIORH_0 = H'89
TCNT_0 cleared by input capture to TGRB_0.
TCNT_0 counts falling edges of Pϕ/1.
Input capture to TGRB_0 is on rising edges of the P31/TIOCA0/TIOCB0 pin.
Input capture to TGRA_0 is on falling edges of the P31/TIOCA0/TIOCB0 pin.
TPUMS0A in PFCR9 = 1
Select the TIOCA0 function
(trigger for input capture) for pin P31.
TGRA_0 = 0
TGRB_0 = 0
Clear TGRA_0 and TGRB_0.
TSYR = H'00
Independent operation of TCNT_0 to TCNT_5.
TMDR_0 = H'C0
Set TPU_0 to operate normally.
TSR_0 = H'C0
Clear status flags in TPU_0.
1
1
TSTR = H'01
Start counting by TCNT_0.
TGFB in TSR_0 ≅ 1 ?
Yes
No
tmp = TSR_0
TGFA and TGFB in TSR_0 = 0
Clear status flags.
TGFB in TSR_0 ≅ 1 ?
Yes
No
plshigh = TGRA_0
Hold high pulse width in RAM.
plsperiod = TGRB_0
Hold pulse width in RAM.
End

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun.18.07	—	First edition issued

Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life

   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.