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H8SX Family

PPG Non-Overlapping (Unit 1) – DTC Transfer –

Introduction

This application note describes using the non-overlapping operation mode of the programmable pulse generator (PPG) function to produce pulse output. In addition, the data transfer controller (DTC) is used to transfer the next unit of data as pulse output.

Coordinated operation with the DTC reduces the load on the CPU, enabling transfer of the next unit of data as the pulse output.

Target Devices

H8SX/1648 Group, H8SX/1648A Group, H8SX/1648L Group, H8SX/1648G Group, H8SX/1648H Group

Preface

This program can be used with other H8SX Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed.

Check the latest version of the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

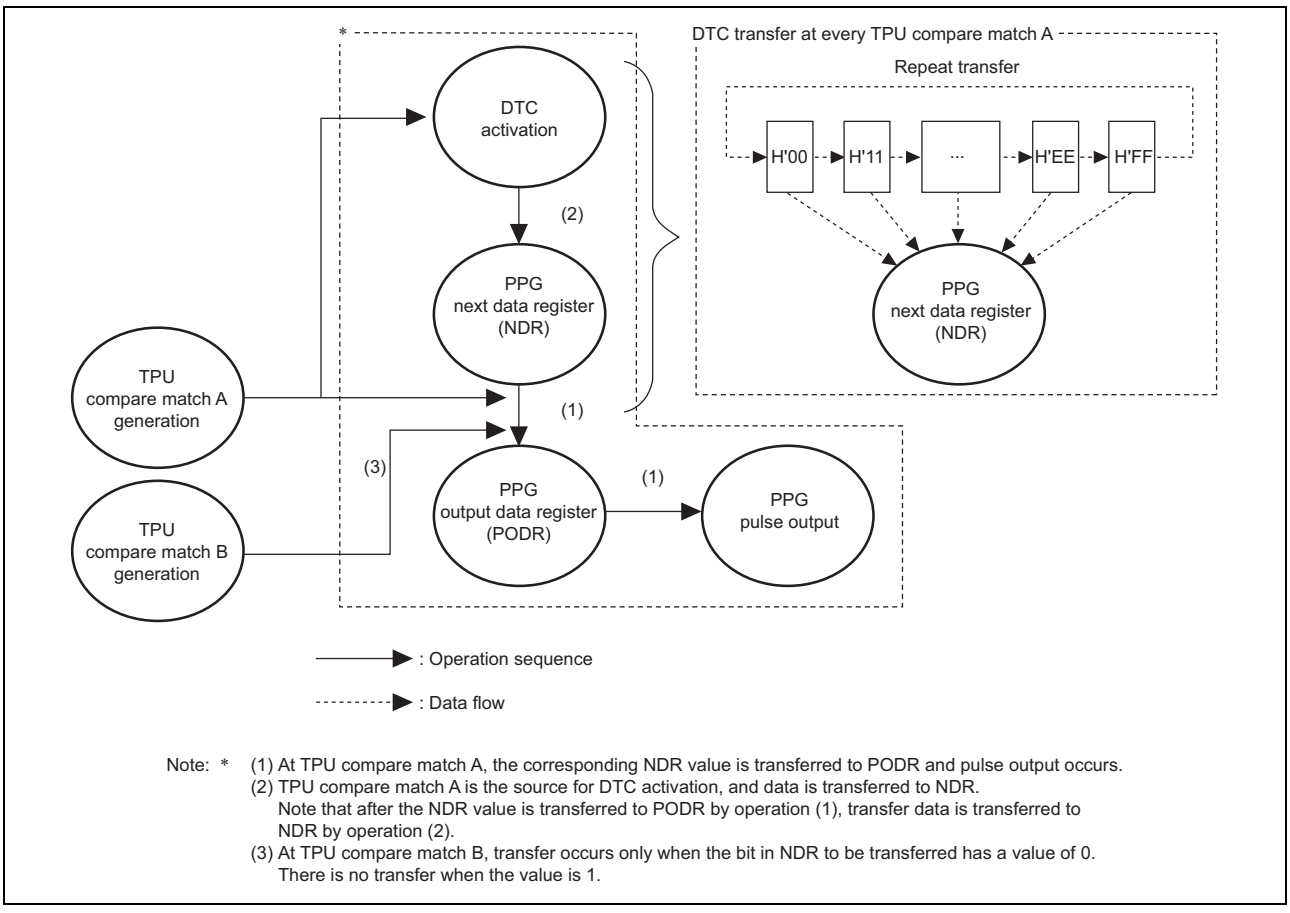
Contents

1. Specifications

The specifications of this application note cover using the PPG function and DTC transfer to generate pulse output for 16 bytes of data. Then the DTC performs a repeat transfer and pulse output is generated for 16 bytes of data a second time.

Figure 1 shows an overview of the operations described in this application note. The detailed specifications for the perations described in this application note are listed below.

- The PPG pulse output group used is group 4 (pins PO16 to PO19).
- Non-overlapping operation in direct output mode is used for PPG pulse output.
- The 16-bit timer pulse unit (TPU) channel 6 compare match is used as the PPG activation source.
- The TPU compare match A period is set to 20 µs.
- The TPU compare match B period is set to 40 µs.
- The TPU output compare match A is used as the DTC activation source.
- The repeat transfer mode of the DTC is used to transfer 16 bytes of data to the next data register (NDR) of the PPG.
- The data transferred by the DTC consists of 16 bytes as follows: H'00, H'11, H'22, …, H'DD, H'EE, H'FF.



Note: * (1) At TPU compare match A, the corresponding NDR value is transferred to PODR and pulse output occurs.
(2) TPU compare match A is the source for DTC activation, and data is transferred to NDR.
Note that after the NDR value is transferred to PODR by operation (1), transfer data is transferred to NDR by operation (2).
(3) At TPU compare match B, transfer occurs only when the bit in NDR to be transferred has a value of 0.
There is no transfer when the value is 1.

Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 12.5 MHz System clock(Iϕ): 50 MHz (12.5 MHz multiplied by 4) Peripheral module clock (Pϕ): 25 MHz (12.5 MHz multiplied by 2) External bus clock (Bϕ): 50 MHz (12.5 MHz multiplied by 4)
Operating voltage	3.3V
Operating mode	Mode 7 (MD2 = 1, MD1 = 1, MD0 = 1)
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01
C/C++ compiler	Renesas Technology H8S/300, H8/300 C/C++ Compiler (V6.02.00)
Compile options	-cpu = H8SXA:24MD, -optimize = 1
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V9.03.00)
Linker options	start = start = PResetPRG,PIntPRG/0400, P,C$DSEC,C$BSEC,D/0800, CDTCV/02690 B,R/0FF2000, S/0FFBE00

3. Functions Used

3.1 Programmable Pulse Generator

The programmable pulse generator (PPG) generates pulse output by using the 16-bit timer pulse unit (TPU) as a time base. The PPG comprises 4-bit units (groups 7 to 0) that can operate either simultaneously or independently.

Figure 2 shows a schematic diagram of the PPG. PPG pulse output is enabled when the corresponding bits in the next data enable register (NDER) are set to 1. An initial output value is determined by its corresponding the output data register (PODR) initial setting. When the compare match event specified by the PPG output control register PCR occurs, the corresponding the next data register (NDR) bit contents are transferred to PODR to update the output values. Sequential output of data of up to 16 bits is possible by writing new output data to NDR before the next compare match.

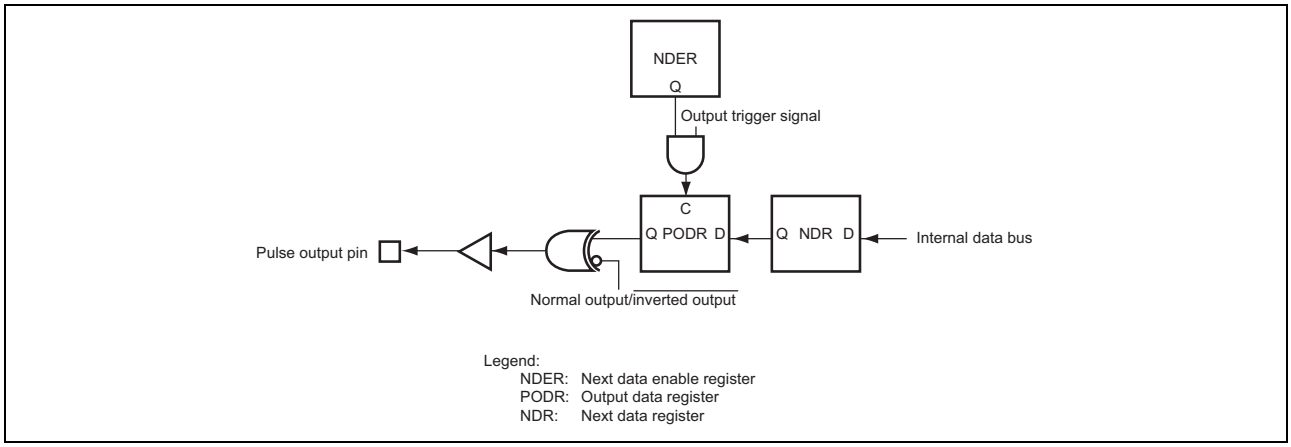


Figure 2 Schematic Diagram of PPG

3.2 Non-Overlapping Pulse Output

During non-overlapping operation, transfer from NDR to PODR is performed as follows:

- At compare match A, the NDR bits are always transferred to PODR.
- At compare match B, the NDR bits are transferred only if their value is 0. The NDR bits are not transferred if their value is 1.

Figure 3 illustrates the non-overlapping pulse output operation.

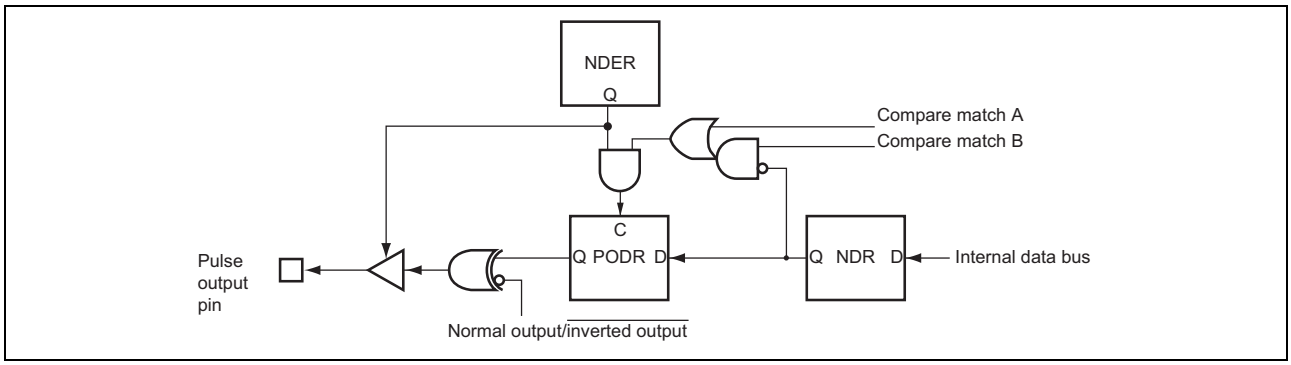


Figure 3 Non-Overlapping Pulse Output

Therefore, 0 data can be transferred ahead of 1 data by making compare match B occur before compare match A.

The NDR contents should not be altered during the interval from compare match B to compare match A (the non-overlapping margin).

This can be accomplished by having the TGIA interrupt handling routine write the next data in NDR, or by having the TGIA interrupt activate the DTC or DMAC. Note, however, that the next data must be written before the next compare match B occurs.

Figure 4 shows the timing of this operation.

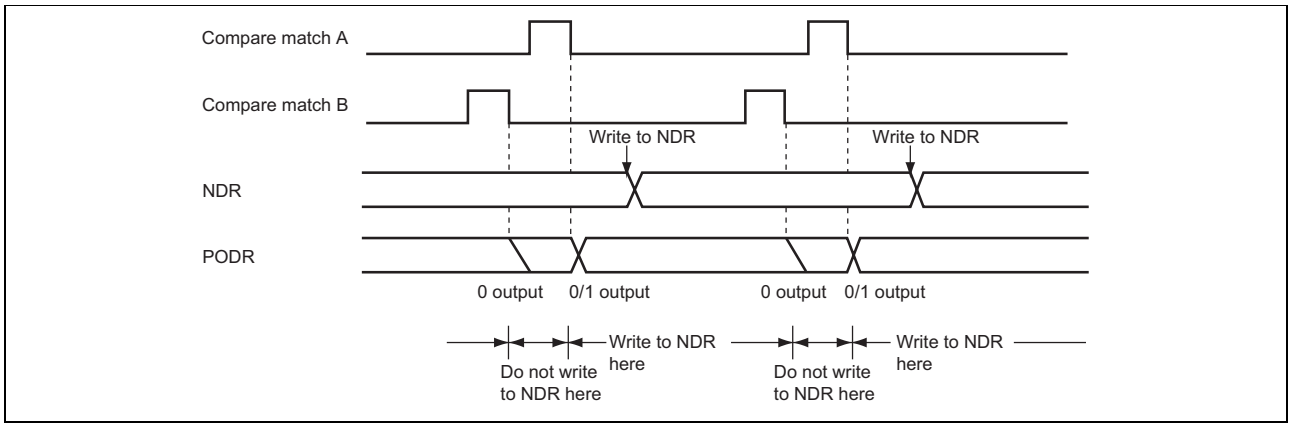


Figure 4 Non-Overlapping Operation and NDR Write Timing

3.3 PODR Output Values During Non-Overlapping Periods

Table 2 lists the PODR output values during the non-overlapping periods.

Table 2 PODR Output Truth Table During Non-Overlapping Periods (Direct Output Mode)

Conditions		Result
Bit transferred to NDR at preceding TPU compare match	**Bit transferred to NDR at TPU compare match**	**PODR bit output during non-overlapping period**
0	0	0
0	1	0
1	0	0
1	1	1

4. Operation

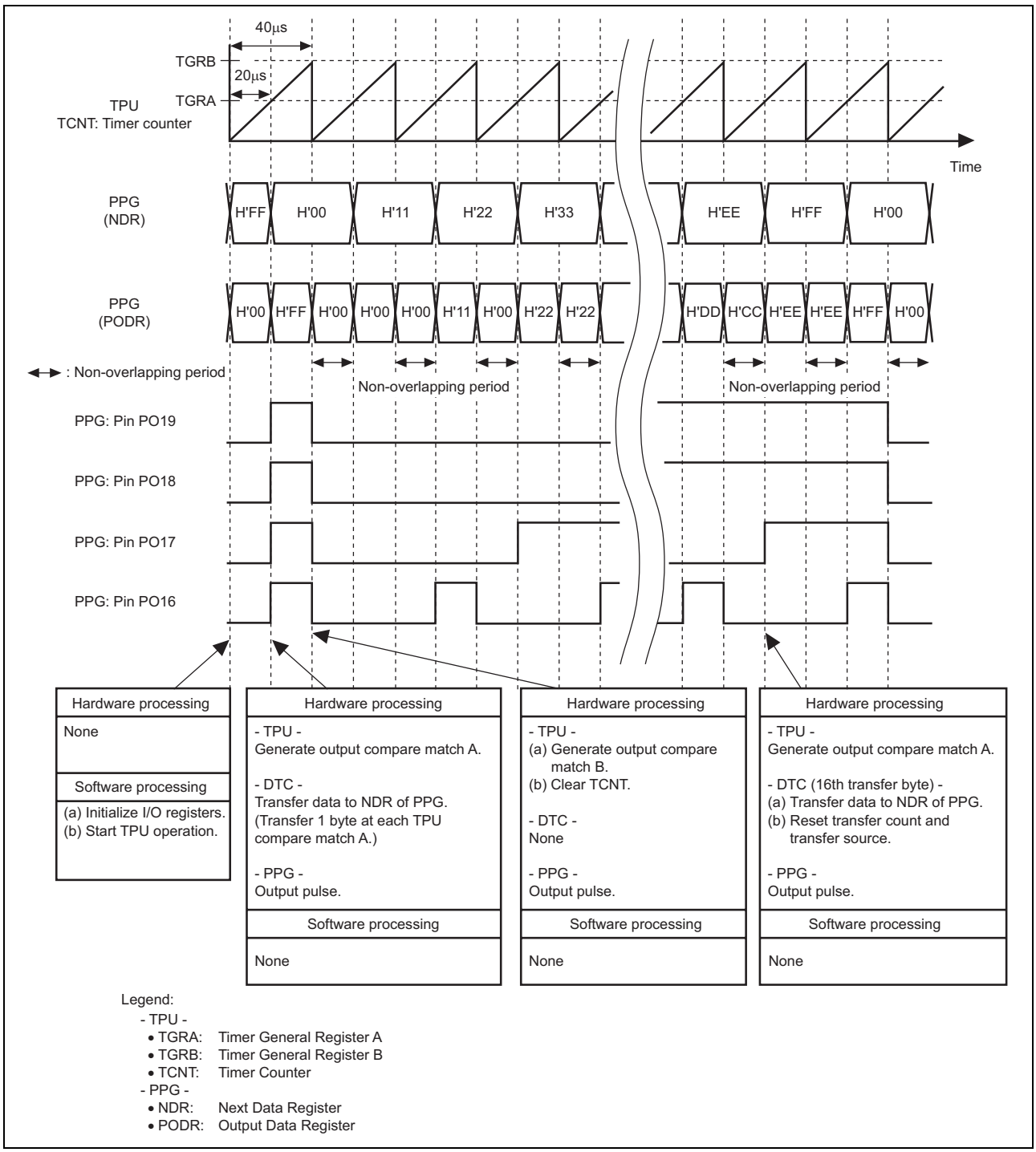


Figure 5 Operation

5. Software Description

5.1 Symbolic Constants

Table 3 List of Symbolic Constants

Constant Name	Setting Value	Description	Used by Functions
MAX_PPG_DATA_CNT	16	Max. PPG output data count	—

5.2 ROM Variables

Table 4 List of ROM Variables

Type	Variable Name	Setting Value	Description	Used by Functions
const unsigned char	c_ppg_data [MAX_PPG_DATA_CNT]	0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77, 0x88, 0x99, 0xAA, 0xBB, 0xCC, 0xDD, 0xEE, 0xFF	PPG output data	init

5.3 List of Functions

Table 5 List of Functions

Function Name	Description
PowerON_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	• Main function Calls init function and starts TPU operation.
init	• I/O register initialization function Initializes registers.

5.4 Functions

5.4.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Flowchart

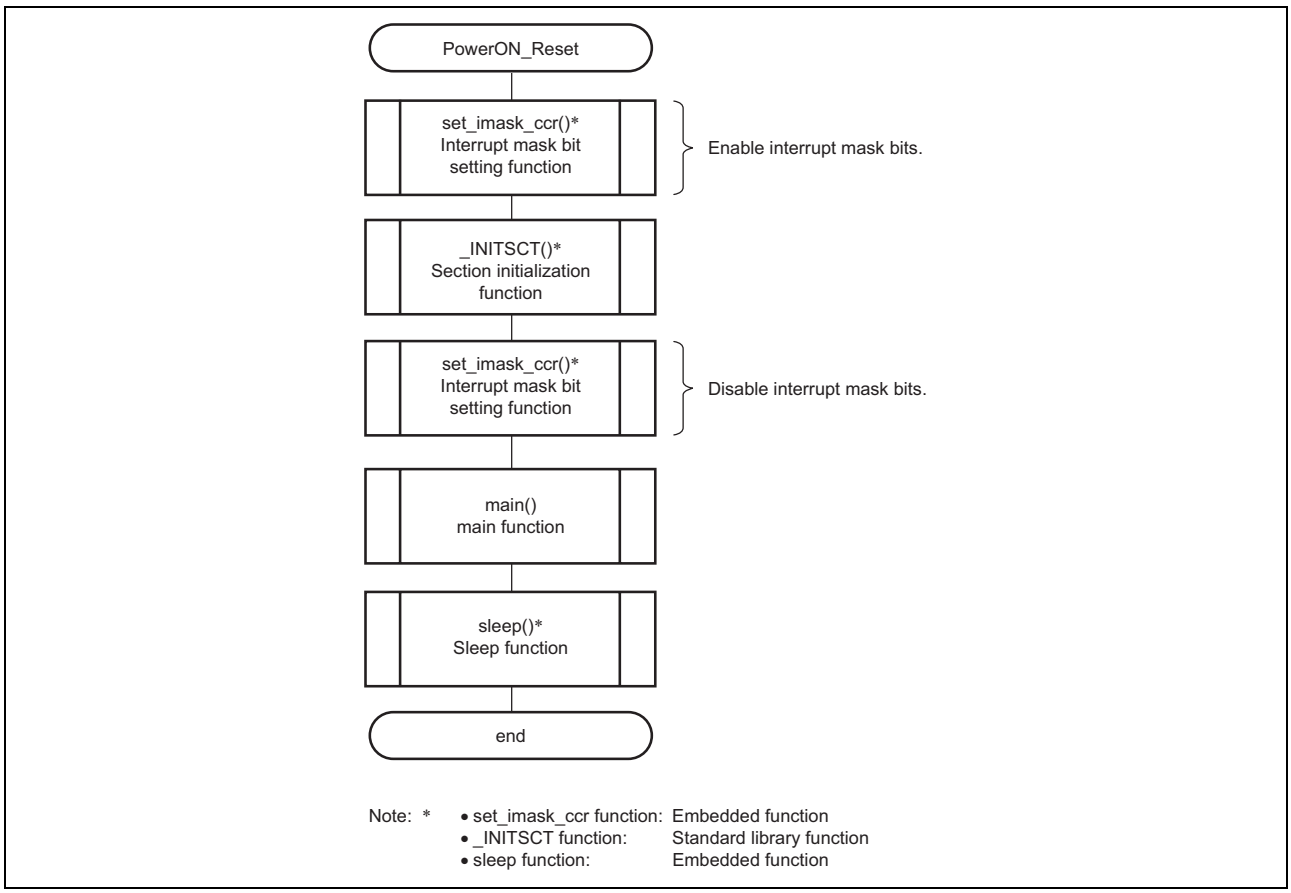


Figure 6 Flowchart (PowerON_Reset)

5.4.2 main Function

(1) Functional Overview

The main function calls the init function to initialize registers and starts the TPU.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this sample task and differ from the initial values.

- Timer Start Register (TSTRB) - Number of bits: 8, Address: H'FFFB00

Bit	Bit Name	Set Value	R/W	Descriptions
0	CST0	1	R/W	Counter Start 0 This bit selects operation or stoppage for TCNT. 1: TCNT6 performs count operation

(5) Flowchart

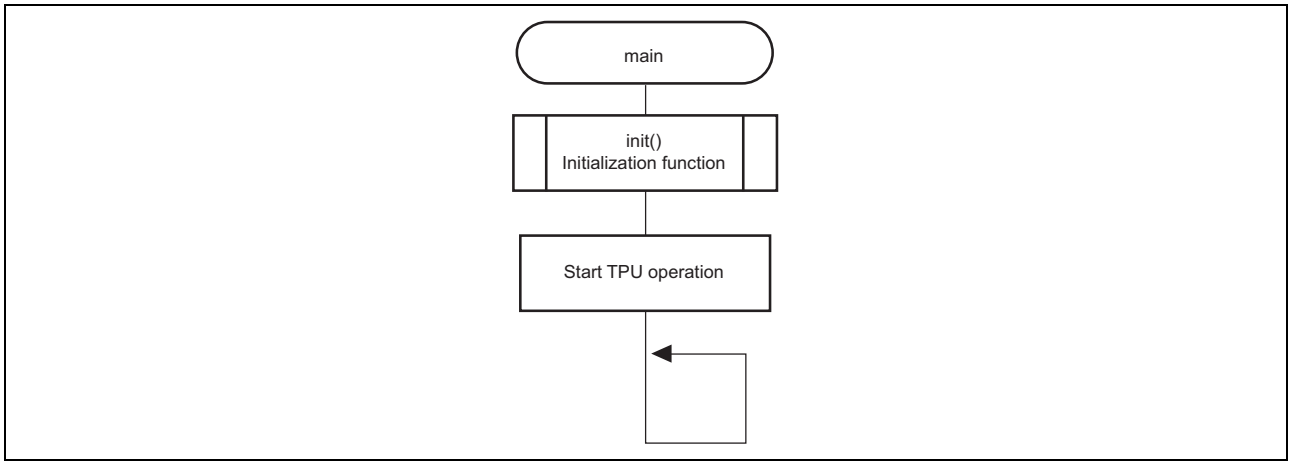


Figure 7 Flowchart (main)

5.4.3 init Function

(1) Functional Overview

The init function initializes various registers.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this sample task and differ from the initial values.

- System Clock Control Register (SCKCR) - Number of bits: 16, Address: H'FFFDC4

Bit	Bit Name	Set Value	R/W	Descriptions
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to the
8	ICK0	0	R/W	CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA controls the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, and clearing the bit to 0 clears the module stop state.

- Module Stop Control Register A (MSTPCRA) - Number of bits: 16, Address: H'FFFDC8

Bit	Bit Name	Set Value	R/W	Descriptions
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop state for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after module stop state has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled
1	MSTPA1	0	R/W	16-bit timer pulse unit (TPU channels 11 to 6)

- MSTPCRC controls the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, and clearing the bit to 0 clears the module stop state.

- Module Stop Control Register C (MSTPCRC) - Number of bits: 16, Address: H'FFFDCC

Bit	Bit Name	Set Value	R/W	Descriptions
8	MSTPC8	0	R/W	Programmable pulse generator (PPG_1: PO31 to PO16)

- Port Function Control Register D (PFCRD) - Number of bits: 8, Address: H'FFFBCD

Bit	Bit Name	Set Value	R/W	Descriptions
7	PCJKE	1	R/W	Ports J and K Enable Enables or disables the port J and K pin functions. 1: Port s J and K are enabled (ports D and E are disabled).

- Timer Start Register (TSTRB) - Number of bits: 8, Address: H'FFFB00

Bit	Bit Name	Set Value	R/W	Descriptions
0	CST0	0	R/W	Counter Start 0 This bit selects operation or stoppage for TCNT. 0: TCNT6 count operation is stopped.

- Timer Status Register (TSR) - Number of bits: 8, Address: H'FFFB15

Bit	Bit Name	Set Value	R/W	Descriptions
0	TGFA	0	R/(W)	Input Capture/Output Compare Match Flag A Status flag that indicates the occurrence of TGRA input capture or compare match. [Clearing condition] When 0 is written to TGFA after reading TGFA as 1

- Timer Control Register (TCR) - Number of bits: 8, Address: H'FFFB10

Bit	Bit Name	Set Value	R/W	Descriptions
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	1	R/W	These bits select the TCNT counter clearing source.
5	CCLR0	0	R/W	010: TCNT is cleared at TGRB compare match /input capture.
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. 00: Internal clock counts at falling edge.
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock.
0	TPSC0	0	R/W	000: Internal clock counts on Pϕ/1.

- Timer Mode Register (TMDR) - Number of bits: 8, Address: H'FFFB11

Bit	Bit Name	Set Value	R/W	Descriptions
5	BFB	0	R/W	Buffer Operation B Specifies whether TGRB is to normally operate, or TGRB and TGRD are to be used together for buffer operation. 0: TGRB operates normally
4	BFA	0	R/W	Buffer Operation A Specifies whether TGRA is to normally operate, or TGRA and TGRC are to be used together for buffer operation. 0: TGRA operates normally
3	MD3	0	R/W	Modes 3 to 0
2	MD2	0	R/W	Set the timer operating mode.
1	MD1	0	R/W	0000: Operates normally
0	MD0	0	R/W	

- Timer I/O Control Register H (TIORH) - Number of bits: 8, Address: H'FFFB12

Bit	Bit Name	Set Value	R/W	Descriptions
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	1	R/W	These bits specify the function of TGRB.
5	IOB1	1	R/W	0111: TIOCB pin initial output value is 1, toggle output at compare
4	IOB0	1	R/W	match.
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	1	R/W	These bits specify the function of TGRA.
1	IOA1	1	R/W	0111: TIOCA pin initial output value is 1, toggle output at compare
0	IOA0	1	R/W	match.

- Timer I/O Control Register L (TIORL) - Number of bits: 8, Address: H'FFFB13

Bit	Bit Name	Set Value	R/W	Descriptions
7	IOD3	0	R/W	I/O Control B3 to B0
6	IOD2	1	R/W	These bits specify the function of TGRD.
5	IOD1	1	R/W	0111: TIOCD pin initial output value is 1, toggle output at compare
4	IOD0	1	R/W	match.
3	IOC3	0	R/W	I/O Control A3 to A0
2	IOC2	1	R/W	These bits specify the function of TGRC.
1	IOC1	1	R/W	0111: TIOCC pin initial output value is 1, toggle output at compare
0	IOC0	1	R/W	match.

- Timer Interrupt Enable Register (TIER) - Number of bits: 8, Address: H'FFFB14

Bit	Bit Name	Set Value	R/W	Descriptions
0	TGIEA	1	R/W	TGR Interrupt Enable A Enables/disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 1: Interrupt requests (TGIA) by TGFA bit enabled

- Timer Counter (TCNT) - Number of bits: 16, Address: H'FFFB16
  Function: TCNT is a 16-bit readable/writable counter.
  Setting value: H'0000
- Timer General Register A (TGRA) - Number of bits: 8, Address: H'FFFB18
  Function: TGRA is a 16-bit readable/writable register that functions as both an output compare and an input capture register.
  Setting value: H'01F3 (period: 20 µs)
- Timer General Register B (TGRB) - Number of bits: 8, Address: H'FFFB1A
  Function: TGRB is a 16-bit readable/writable register that functions as both an output compare and an input capture register.
  Setting value: H'03E7 (period: 40 µs)
- Timer Synchronization Register (TSYRB) - Number of bits: 8, Address: H'FFFB01

Bit	Bit Name	Set Value	R/W	Descriptions
0	SYNC0	0	R/W	Timer Synchronization 6 This bit selects whether operation is independent of or synchronized with other channels. 0: TCNT6 operates independently.

- Output Data Register L (PODRL) - Number of bits: 8, Address: H'FFF63B
  Function: PODRL stores pulse output values.
  Setting value: H'00
- Next Data Enable Register H (NDERH) - Number of bits: 8, Address: H'FFF638
  Function: NDERH selects the PPG pulse output pin on a bit-by-bit basis. When a bit is set to 1, the value in the corresponding NDRH bit is transferred to PODRH by the selected output trigger. Values are not transferred from NDRH to PODRH for bits cleared to 0.
  Setting value: H'00
- Next Data Enable Register L (NDERL) - Number of bits: 8, Address: H'FFF639
  Function: NDERL selects the PPG pulse output pin on a bit-by-bit basis. When a bit is set to 1, the value in the corresponding NDRL bit is transferred to PODRL by the selected output trigger. Values are not transferred from NDRL to PODRL for bits cleared to 0.
  Setting value: H'0F

- PPG Output Control Register (PCR) - Number of bits: 8, Address: H'FFF636

Bit	Bit Name	Set Value	R/W	Descriptions
1	G0CMS1	0	R/W	Group 4 Compare Match Select 1 and 0
0	G0CMS0	0	R/W	These bits select the output trigger of pulse output group 0. 00: Compare match in TPU channel 6

- PPG Output Mode Register (PMR) - Number of bits: 8, Address: H'FFF637

Bit	Bit Name	Set Value	R/W	Descriptions
4	G0INV	1	R/W	Group 4 Inversion This bit selects direct output or inverted output for pulse output group 4. 1: Direct output
0	G0NOV	1	R/W	Group 4 Non-Overlap Selects normal or non-overlapping operation for pulse output group 4. 1: Non-overlapping operation (output values updated by compare match A or B on the selected TPU channel)

- Next Data Register L (NDRL) - Number of bits: 8, Address: H'FFF63D
  Function: NDRL stores the next data for pulse output. The NDR addresses differ depending on whether the pulse output groups have the same output trigger or different output triggers.
  Setting value: H'0F
- DTC Vector Base Register (DTCVBR) - Number of bits: 32, Address: H'FFFD80
  Function: DTCVBR is a 32-bit register that specifies the base address for vector table address calculation.
  Setting value: H'2000
- DTC Enable Register E (DTCERE) - Number of bits: 16, Address: H'FFFF28
  Function: DTCER is a register that specifies the DTC activation interrupt source.
  Setting value: H'0800 (interrupt source: TGI6A)
- DTC Source Address Register (SAR) - Number of bits: 32, Address: H'FFB000 (internal RAM area)
  Function: SAR is a 32-bit register that designates the source address of data to be transferred by the DTC.
  Setting value: c_ppg_data[0] address
- DTC Destination Address Register (DAR) - Number of bits: 32, Address: H'FFB004 (internal RAM area)
  Function: DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC.
  Setting value: H'00FFF63D (NDRL register address)

- DTC Mode Register A (MRA) - Number of bits: 8, Address: H'FFB000 (internal RAM area)

Bit	Bit Name	Set Value	R/W	Descriptions
7	MD1	0	R/W	DTC Mode 1 and 0
6	MD0	1	R/W	Specify DTC transfer mode. 01: Repeat mode
5	Sz1	0	R/W	DTC Data Transfer Size 1 and 0
4	Sz0	0	R/W	Specify the size of data to be transferred. 00: Byte-size transfer
3	SM1	1	R/W	Source Address Mode 1 and 0
2	SM0	0		Specify an SAR operation after a data transfer. 10: SAR is incremented after a transfer

- DTC Mode Register B (MRB) - Number of bits: 8, Address: H'FFB004 (internal RAM area)

Bit	Bit Name	Set Value	R/W	Descriptions
7	CHNE	0	R/W	DTC Chain Transfer Enable This bit enables or disables chain transfer. 0: Chain transfer disabled
5	DISEL	0	R/W	DTC Interrupt Select When this bit is cleared to 0, an interrupt request is sent to the CPU only when the specified data transfer ends.
4	DTS	1	R/W	DTC Transfer Mode Select This bit specifies either the source or destination as the repeat area in repeat transfer mode. 1: Source specified as repeat area
3	DM1	0	R/W	Destination Address Mode 1 and 0
2	DM0	0	R/W	These bits specify the DAR operation after a data transfer. 0X: DAR is fixed.

- DTC Transfer Counter Register A (CRA) - Number of bits: 16, Address: H'FFB008 (internal RAM area)
  Function: CRA specifies the number of data transfers to be performed by the DTC. In repeat transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL).
  Setting value: H'00FFF63D (NDRL register address)

(5) Flowchart

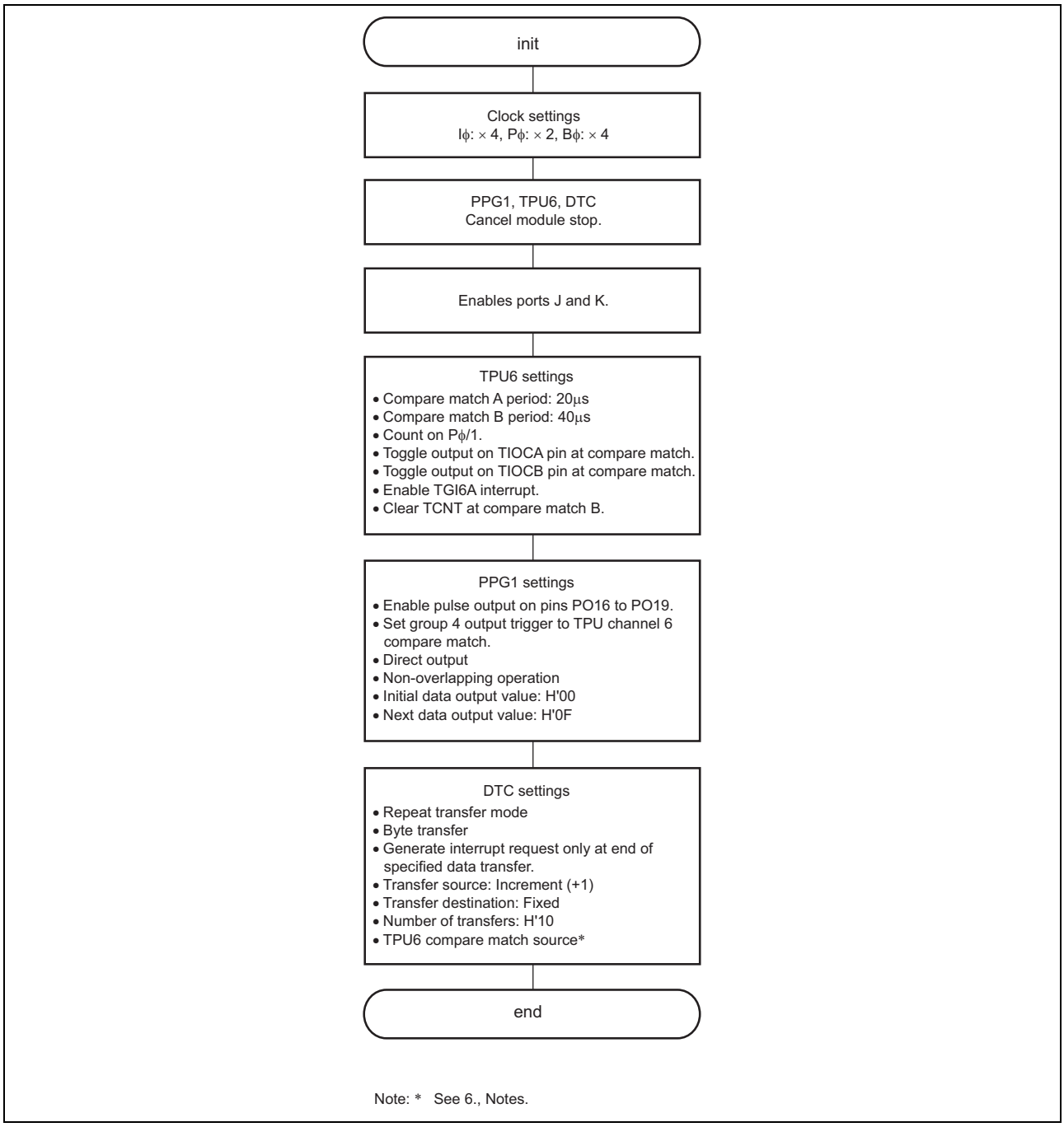


Figure 8 Flowchart (init)

6. Notes

(1) When using PPG1, always set TIOR in the TPU, which acts as the activation source, to toggle output at compare match and set PPG1 to output. For details, see the relevant hardware manual.
(2) The address of the next data register (NDR) differs depending on whether the pulse output groups have the same output trigger or different output triggers. For details, see the relevant hardware manual.
(3) When a conflict occurs between an overwrite (setting to 1 or 0) of the DTC enable register (DTCER) and the generation of a DTC activation source interrupt, activation of the DTC and interrupt exception processing by the CPU may both occur at the same time. In some cases, two interrupts may be generated at once. If there is a possibility of conflict between an overwrite of DTCER and generation of a DTC activation source interrupt, mask the interrupt when writing to DTCER. For details, see the relevant hardware manual or technical news/technical update.

7. Reference Documents

- Hardware Manual
  H8SX/1648, H8SX/1648A, H8SX/1648L, H8SX/1648G, H8SX/1648H Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Technical News/Technical Updates
  (The latest information can be downloaded from the Renesas Technology Web site.)

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Revision Record

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