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H8S Family

Long-Period Pulse Output by Cascading the TPU Channels

Introduction

The two channels of 16-bit timer counters of the 16-bit timer pulse unit (TPU) are cascaded to function as a 32-bit timer counter. The resulting 32-bit timer counter outputs long-period pulses with a 0 to 100% variable duty cycle.

Target Device

H8S/2339

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1. Specifications

- Two channels of 16-bit counters are cascaded to function as a 32-bit counter. The resulting counter outputs long-period pulses with a variable duty cycle, which is controlled by varying the high pulse width as shown in figure 1.
- The duty cycle can be set in the range from 0 to 100%, with a resolution of 1/65536.
- In 20 MHz (19.6608 MHz) operation, the pulse period can be set in the range from approximately 6.66 ms to 218.23 s in 3.33-ms units.

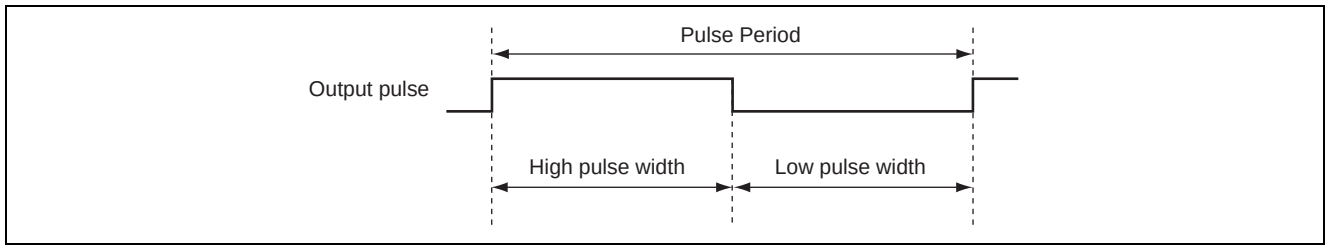


Figure 1 Example of Long-Period Pulse Output by Cascaded TPU Channels

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents	
Operating frequency	Input clock:	19.6608 MHz
	System clock:	19.6608 MHz
	Peripheral module clock:	19.6608 MHz
	Bus master clock:	19.6608 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	
Development tool	HEW Version 3.01 (release1)	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.0.00.005 (from Renesas Technology Corp.)	
Compile option	-cpu = 2000a:24, -code = machinecode, -optimize = 1	

3. Description of Functions

Figure 2 shows a block diagram of the 16-bit timer pulse unit (TPU), and the following describes the registers of the TPU.

- Timer Control Register (TCR0)
  TCR sets the clearing condition and clock source of the timer counter, TCNT, for each channel.
- Timer Mode Register (TMDR0)
  TMDR sets the operating mode, normal operation or buffer operation, for each channel.
- Timer I/O Control Registers (TIOR0H and TIOR0L)
  TIOR controls output signals by setting the initial output value and output value in compare-match/input-capture operation for each TGR.
- Timer Interrupt Enable Register (TIER0)
  TIER enables or disables interrupts for each channel.
- Timer Status Register (TSR0)
  TSR indicates the statuses for each channel.
- Timer Counter (TCNT0)
  TCNT is a 16-bit counter that can be read or written to. Access to this counter must be in 16-bit units.
- Timer General Registers (four registers from TGR0A to TGR0D)
  TGR0A to TGR0D are 16-bit readable/writable registers that are used for output compare or input capture. Access to these registers must be in 16-bit units.
- Timer Start Register (TSTR)
  TSTR selects to start or stop the operation of TCNTs for channels 0 to 5.

Note The register names with "0" in the above description are channel 0 registers. Each channel has a set of such registers.

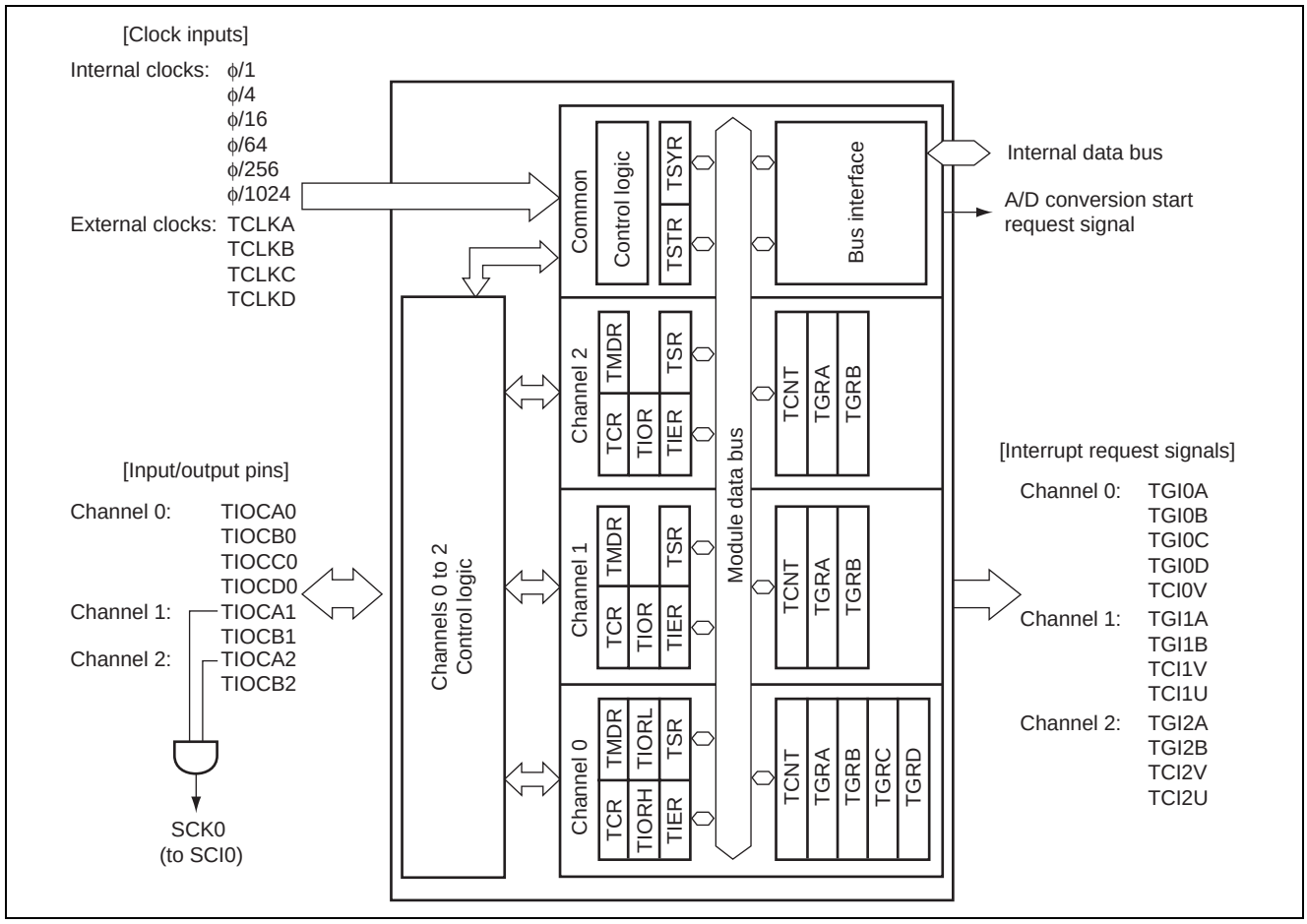


Figure 2 Block Diagram of TPU

4. Description of Operation

Figure 3 illustrates the operation of this sample task. Long-period pulses are output through the hardware and software processing shown in the figure.

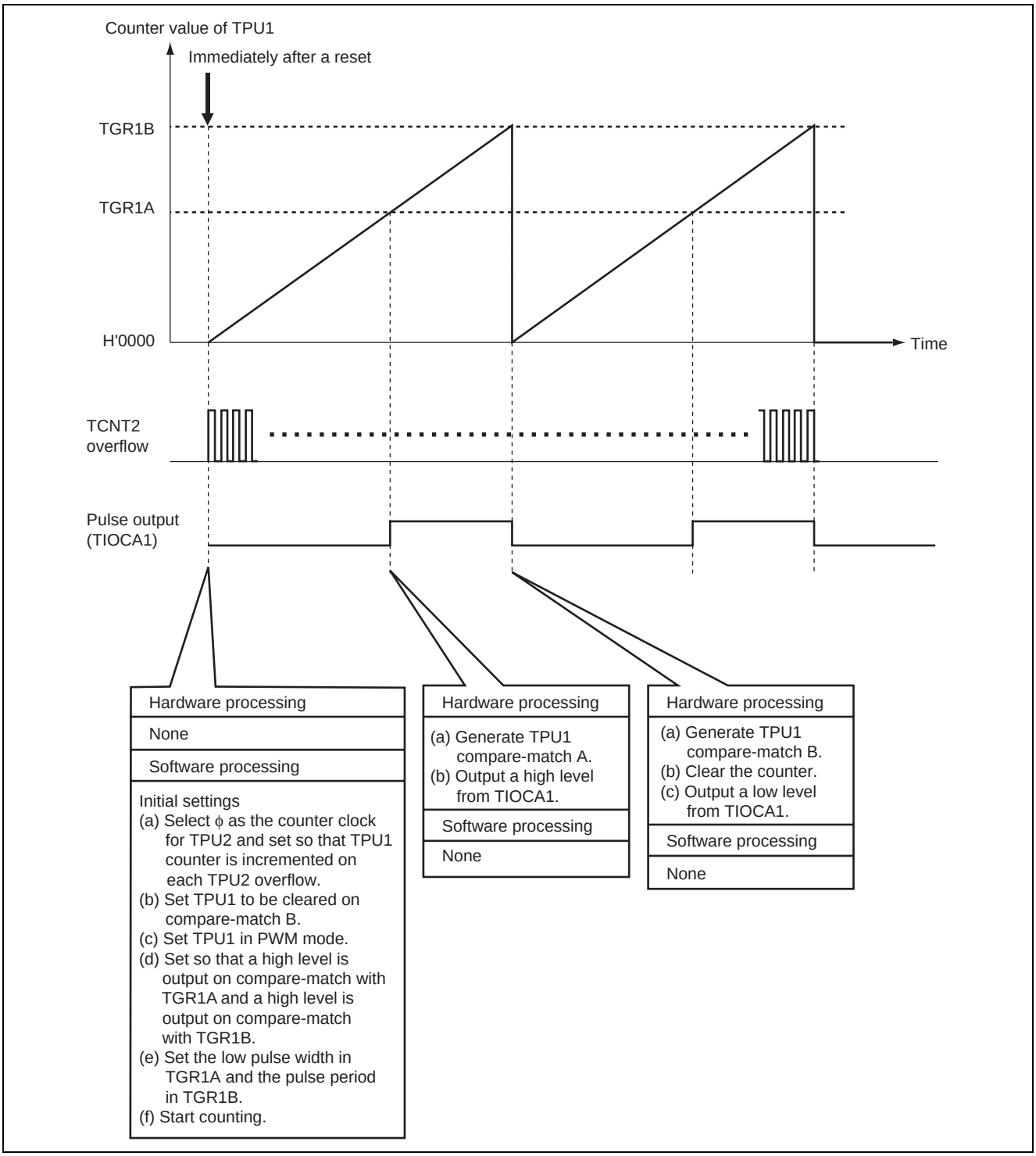


Figure 3 Operation of Long-Period Pulse Output

5. Description of Software

5.1 Module

Table 2 describes the module of this sample task.

Table 2 Description of Module

Module Name	Label Name	Functions
Main routine	tpucasm	Outputs long-period pulses by cascading the TPU1 and TPU2 counters to form a 32-bit counter.

5.2 Arguments

Table 3 describes the arguments used in this sample task.

Table 3 Description of Arguments

Label	Description	Data Length	Used in	I/O
lpul_wid	Sets the timer value that determines the low-level with of the output pulse. Low pulse width (ms) = (timer value + 1) × {(65535 +1) × clock ϕ period} (Clock ϕ period is 50.86 ns when the operating frequency is 19.6608 MHz)	1 word	Main routine	Input
lpul_cyc	Sets the timer value that determines the period of the output pulse. Pulse period (ms) = (timer value + 1) × {(65535 + 1) × clock ϕ period} (Clock ϕ period is 50.86 ns when the operating frequency is 19.6608 MHz)	1 word	Main routine	Input

5.3 Internal Registers

The internal registers used in this sample task are described in table 4.

Table 4 Description of Internal Registers

Register	Name	Function	Address	Setting
TSR1	TCFD	Timer Status Register (Count Direction Flag) TCFD = 0 indicates that TCNT is a down counter. TCFD = 1 indicates that TCNT is an up counter.	H'FFFFE5 Bit 7	0
	TCFU	Timer Status Register (Underflow Flag) TCFU = 0 indicates that TCNT has not underflowed. TCFU = 1 indicates that TCNT has underflowed. (TCNT value has changed from H'0000 to H'FFFF.)	H'FFFFE5 Bit 5	0
	TCFV	Timer Status Register (Overflow Flag) TCFV = 0 indicates that TCNT has not overflowed. TCFV = 1 indicates that TCNT has overflowed. (TCNT value has changed from H'FFFF to H'0000.)	H'FFFFE5 Bit 4	0
	TGFB	Timer Status Register (Input Capture/Output Compare Flag B) TGFB = 0 indicates TCNT ≠ TGFB. TGFB = 1 indicates TCNT = TGFB.	H'FFFFE5 Bit 1	0
	TGFA	Timer Status Register (Input Capture/Output Compare Flag A) TGFA = 0 indicates TCNT ≠ TGFA. TGFA = 1 indicates TCNT = TGFA.	H'FFFFE5 Bit 0	0
TMDR1	BFB	Timer Mode Register (Buffer Operation B) BFB = 0 selects normal operation of TGRB. BFB = 1 selects buffered operation of TGRB and TGRD.	H'FFFFE1 Bit 5	0
	BFA	Timer Mode Register (Buffer Operation A) BFA = 0 selects normal operation of TGRA. BFA = 1 selects buffered operation of TGRA and TGRC.	H'FFFFE1 Bit 4	0
	MD3 MD2 MD1 MD0	Timer Mode Register (Mode 3 to 0) When MD3 to MD0 = 0000, the TPU operates in normal mode. When MD3 to MD0 = 0010, the TPU operates in PWM mode 1.	H'FFFFE1 Bits 3 to 0	0,0,1,0

Register	Name	Function	Address	Setting
TCR1	CCLR1 CCLR0	Timer Control Register (Counter Clear 1, 0) When CCLR1 and CCLR0 = 00, clearing of TCNT is disabled. When CCLR1 and CCLR0 = 10, TCNT is cleared on compare-match or input capture of TGRB.	H'FFFFE0 Bit 6 Bit 5	1,0
	CKEG1 CKEG0	Timer Control Register (Clock Edge 1, 0) When CKEG1 and CKEG0 = 00, TCNT counts the rising edges. When CKEG1 and CKEG0 = 01, TCNT counts the falling edges.	H'FFFFE0 Bit 4 Bit 3	0,0
	TPSC2 TPSC1 TPSC0	Timer Control Register (Timer Prescaler 2, 1, 0) When TPSC2 to TPSC0 = 000, the clock source of TCNT is ϕ/1. When TPSC2 to TPSC0 = 111, TCNT counts the overflow or underflow of TCNT2.	H'FFFFE0 Bits 2 to 0	1,1,1
TCNT1		Timer Counter 16-bit timer counter	H'FFFFE6 Bits 15 to 0	H'0000
TGR1A		Timer General Register A 16-bit register that is used for output compare or input capture	H'FFFFE8 Bits 15 to 0	H'0002
TGR1B		Timer General Register B 16-bit register that is used for output compare or input capture	H'FFFFEA Bits 15 to 0	H'0004
TIOR1	IOB3 to IOB0	Timer I/O Control Register (I/O Control B3 to B0) These bits set the output level on compare-match with TGRB.	H'FFFFE2 Bits 7 to 4	0,1,0,1
	IOA3 to IOA0	Timer I/O Control Register (I/O Control A3 to A0) These bits set the output level on compare-match with TGRA.	H'FFFFE2 Bits 3 to 0	0,0,1,0
TCR2	CCLR1 CCLR0	Timer Control Register (Counter Clear 1, 0) When CCLR1 and CCLR0 = 00, clearing of TCNT is disabled. When CCLR1 and CCLR0 = 10, TCNT is cleared on compare-match or input capture of TGRB.	H'FFFFF0 Bit 6 Bit 5	0,0
	CKEG1 CKEG0	Timer Control Register (Clock Edge 1, 0) When CKEG1 and CKEG0 = 00, TCNT counts the rising edges. When CKEG1 and CKEG0 = 01, TCNT counts the falling edges.	H'FFFFF0 Bit 4 Bit 3	0,0
	TPSC2 TPSC1 TPSC0	Timer Control Register (Timer Prescaler 2, 1, 0) When TPSC2 to TPSC0 = 000, the clock source of TCNT is ϕ/1. When TPSC2 to TPSC0 = 111, the clock source of TCNT is ϕ/1024.	H'FFFFF0 Bits 2 to 0	0,0,0
TCNT2		Timer Counter 16-bit timer counter	H'FFFFF6 Bits 15 to 0	H'0000
TSTR		Timer Start Register A bit of this register starts/stops the operation of TCNT for the corresponding channel (channels 0 to 5).	H'FFFFC0 Bits 5 to 0	H'06

5.4 RAM Usage

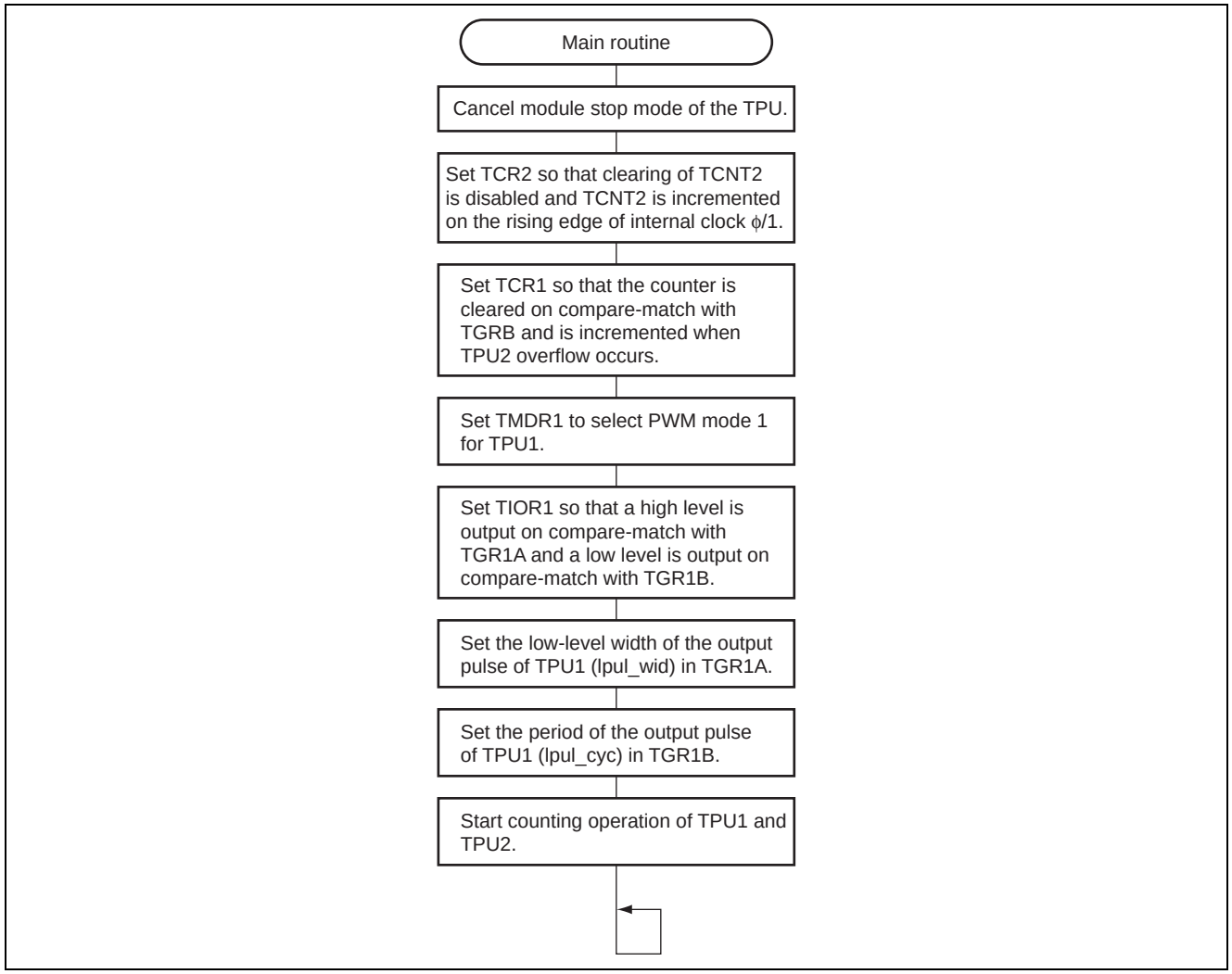
Table 5 describes the RAM usage in this sample task.

Table 5 Description of RAM

Label Name	Function (Setting Used in This Sample Task)	Data Length	Used In
lpul_wid	Stores the data to be set in TGR1A (H'0002)	1 word	Main routine
lpul_cyc	Stores the data to be set in TGR1B (H'0004)	1 word	Main routine

6. Flowchart

6.1 Main Routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.09.05	—	First edition issued

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