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H8S Family

8-Bit Timer in Cascade Connection

Introduction

This application note discusses the output compare operation when two channels of the 8-bit timer (TMR) are cascaded to function as a 16-bit timer.

Target Device

H8S/2339

Contents

1. Specifications

- The two channels of the 8-bit timer module are cascaded to function as a 16-bit timer, using channel 0 for the upper 8 bits and channel 1 for the lower 8 bits.
- Output pulse period is set in TCORA, and the count value for low-level output is set in TCORB.
- By the setting of TCR0, TCR1, TCSR0, and TCSR1, TCNT0 and TCNT1 are made to function as a 16-bit counter. A pulse signal with the duty cycle that is determined by TCORA and TCORB settings is output from TMO0 (pin 77).
- Period f and duty cycle are set according to the following formulae:

f = (TOCRA0 or TOCRA1 setting value + 1) × (1/(ϕ/8)) Note: ϕ = 19.6608 MHz
In this sample task:
f = (43690 + 1) × (1/(ϕ/8)) ≈ 17.777 ms Note: H'AAAA = 43690

Duty cycle = (High-level pulse width × (1/(ϕ/8)))/f
In this sample task:
Duty cycle = ((((43690 + 1) – (13107 + 1)) × (1/(ϕ/8)))/17.777 ms × 100% Note: H'3333 = 13107
= (12.444 ms/17.777 ms) × 100%
≈ 70.5%

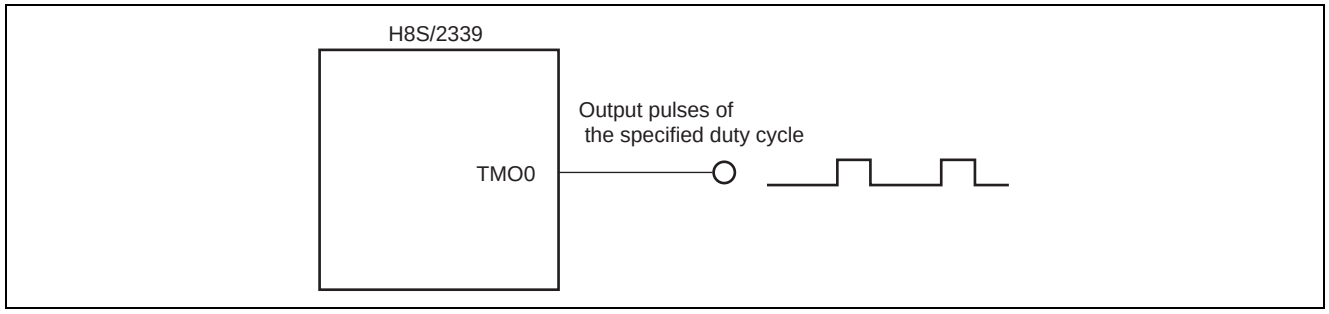


Figure 1 Example of TMR Pulse Output with Controllable Duty Cycle

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents	
Operating frequency	Input clock:	19.6608 MHz
	System clock:	19.6608 MHz
	Peripheral module clock:	19.6608 MHz
	Bus master clock:	19.6608 MHz
Operating mode	Mode 6 (MD2 = 1,MD1 = 1, MD0 = 0)	
Development tool	HEW Version 3.01 (release1)	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.0.0.00.005 (from Renesas Technology Corp.)	
Compile options	-cpu=2000a:24, -code = machinecode, -optimize=1	

3. Description of Functions

Figure 2 shows a block diagram of the 8-bit timer, and the following is the description of the registers of the 8-bit timer.

3.1 8-Bit Timer Registers

- Timer Counter (TCNT)
  The timer counter (TCNT) is an 8-bit up counter that can be read or written to. TCNT0 and TCNT1 can be used together and can be word-accessed as a 16-bit register. The operating clock is selected by the CKS2 to CKS0 bits in TCR. TCNT can be cleared by an external reset input signal or a compare-match signal, either of which is selected by the CCLR1 and CCLR0 bits in TCR. When TCNT overflows (H'FF → H'00), OVF in TCSR is set to 1. The initial value of TCNT is H'00.

- Time Constant Register A/B (TCORA/TCORB)
  The time constant register A/B (TCORA/TCORB) is an 8-bit register that can be read or written to. TCORx0 and TCORx1 can also be used together as a 16-bit register and can be word-accessed. The TCORx value is always compared with TCNT and if they match, CMFA or CMFB in TCSR is set to 1. However, this comparison is disabled in T2 state of a write cycle to TCORx. These match signals (compare-match x) can be used in combination with the settings of OS3 to OS0 bits in TCSR to control the timer output from the TMO0 pin. The initial value of TCORx is H'FF.

- Timer Control Register (TCR)
  The timer control register (TCR) selects TCNT input clock, specifies TCNT clearing condition, and controls interrupt requests.

- Timer Control/Status Register (TCSR)
  The timer control/status register (TCSR) contains status flags and controls output on compare-match.

- Operation in Cascade Connection
  When the CKS2 to CKS0 bits in TCR0 are set to B'100, the timer functions as a single 16-bit timer with channel 0 assigned to the upper 8 bits and channel 1 assigned to the lower 8 bits.
  — Setting of Compare-Match Flags
  — The CMF flag in TCSR0 is set to 1 when a 16-bit compare-match occurs.
  — The CMF flag in TCSR1 is set to 1 when a lower 8-bit compare-match occurs.

- Counter Clearing Specification
  — If the CCLR1 and CCLR0 bits in TCR0 have been set for counter clear on compare-match, the 16-bit counter (TCNT0 and TCNT1 together) is cleared when a 16-bit compare-match occurs. The 16-bit counter (TCNT0 and TCNT1 together) is also cleared when counter clearing by the TMRI0 pin has been set.
  — The settings of the CCLR1 and CCLR0 bits in TCR1 are ignored. The lower 8 bits of the counter alone cannot be cleared.

- Pin Output
  — Control of output from the TMO0 pin by the OS3 to OS0 bits in TCSR0 is in accordance with the 16-bit compare-match conditions.
  — Control of output from the TMO1 pin by the OS3 to OS0 bits in TCSR1 is in accordance with the lower 8-bit compare-match conditions.

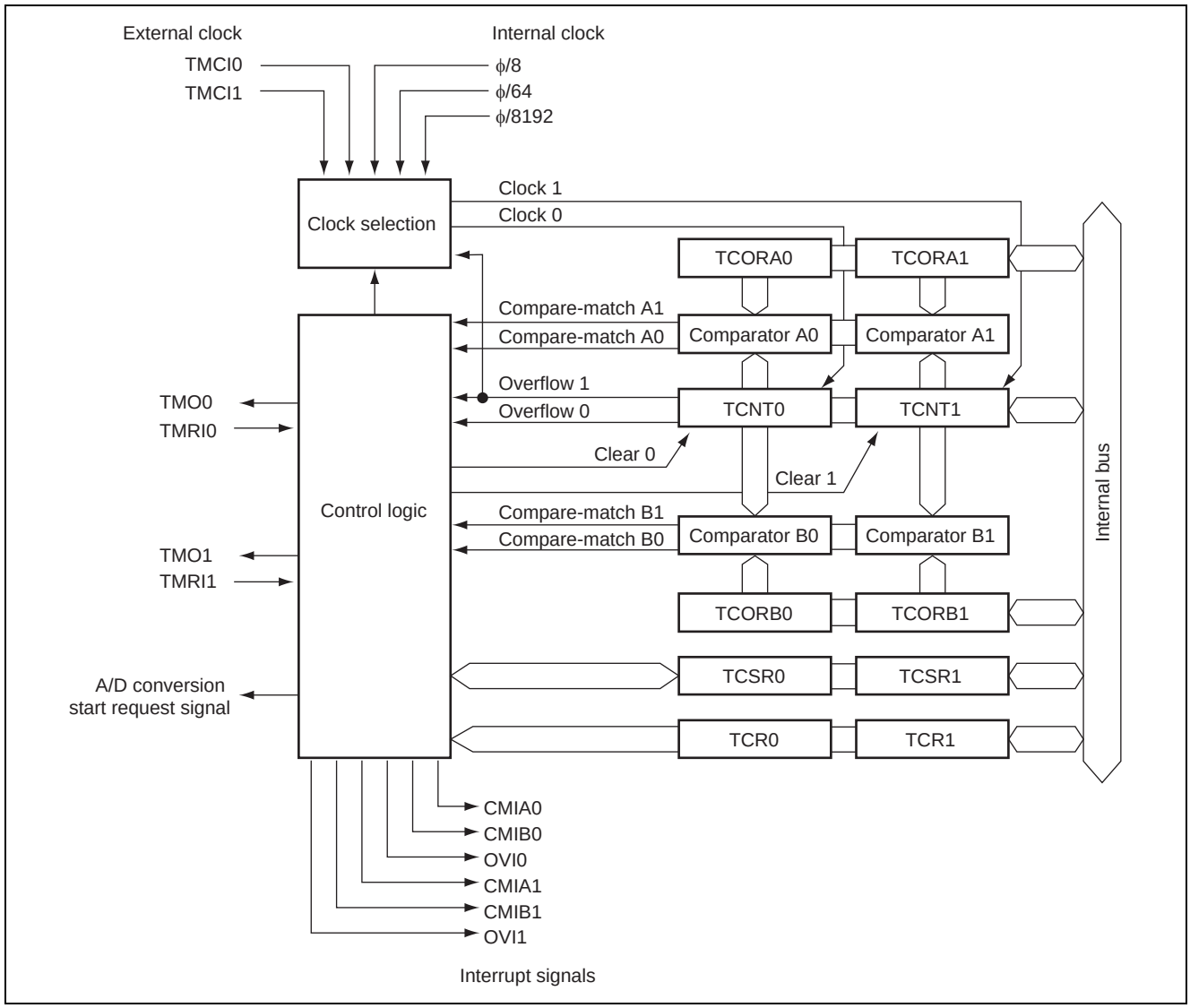


Figure 2 Block Diagram of 8-Bit Timer

4. Description of Operation

Figure 3 illustrates the operation of this sample task. A pulse signal of a specified duty cycle is output using the TMR's compare-match function through the hardware and software processing shown in the figure.

1. The period count value H'AAAA is set in TCORA, and low-level output count value H'3333 is set in TCORB. Pulses are output according to values in TCORA and TCORB, which are controlled by TCR and TCSR.
2. Any desired low-level output width (this determines the duty cycle) is obtained with the TCORB setting.

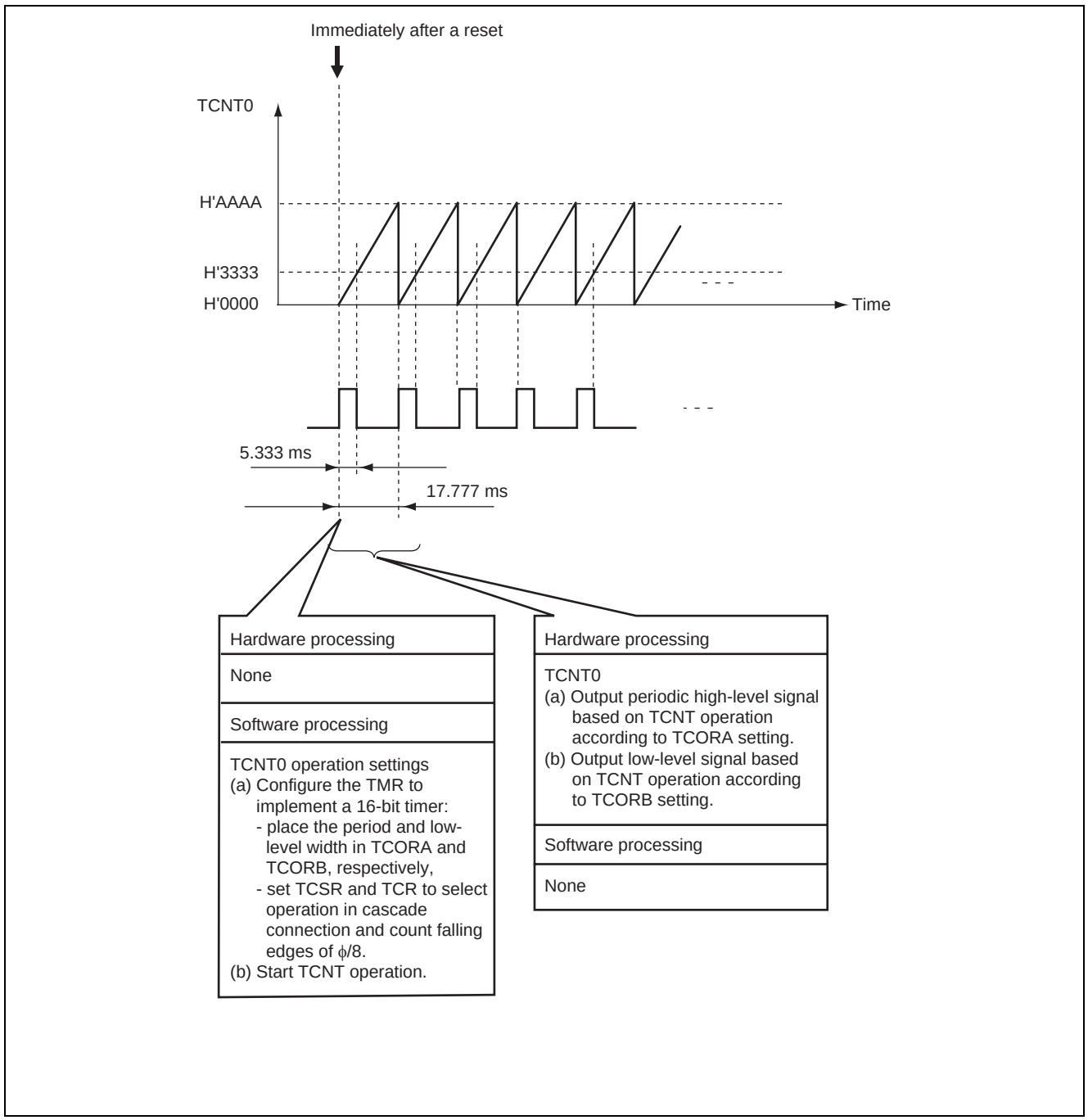


Figure 3 Output of Pulses with a Specified Duty Cycle Using 8-Bit Timer

5. Description of Software

5.1 Module

Table 2 Description of Module

Module Name	Label Name	Functions
Main routine	main	Outputs pulses with a specified duty cycle based on counting by TCNT.

5.2 Arguments

This sample program does not use arguments.

5.3 Internal Registers

The internal registers used in this sample task are described in table 3.

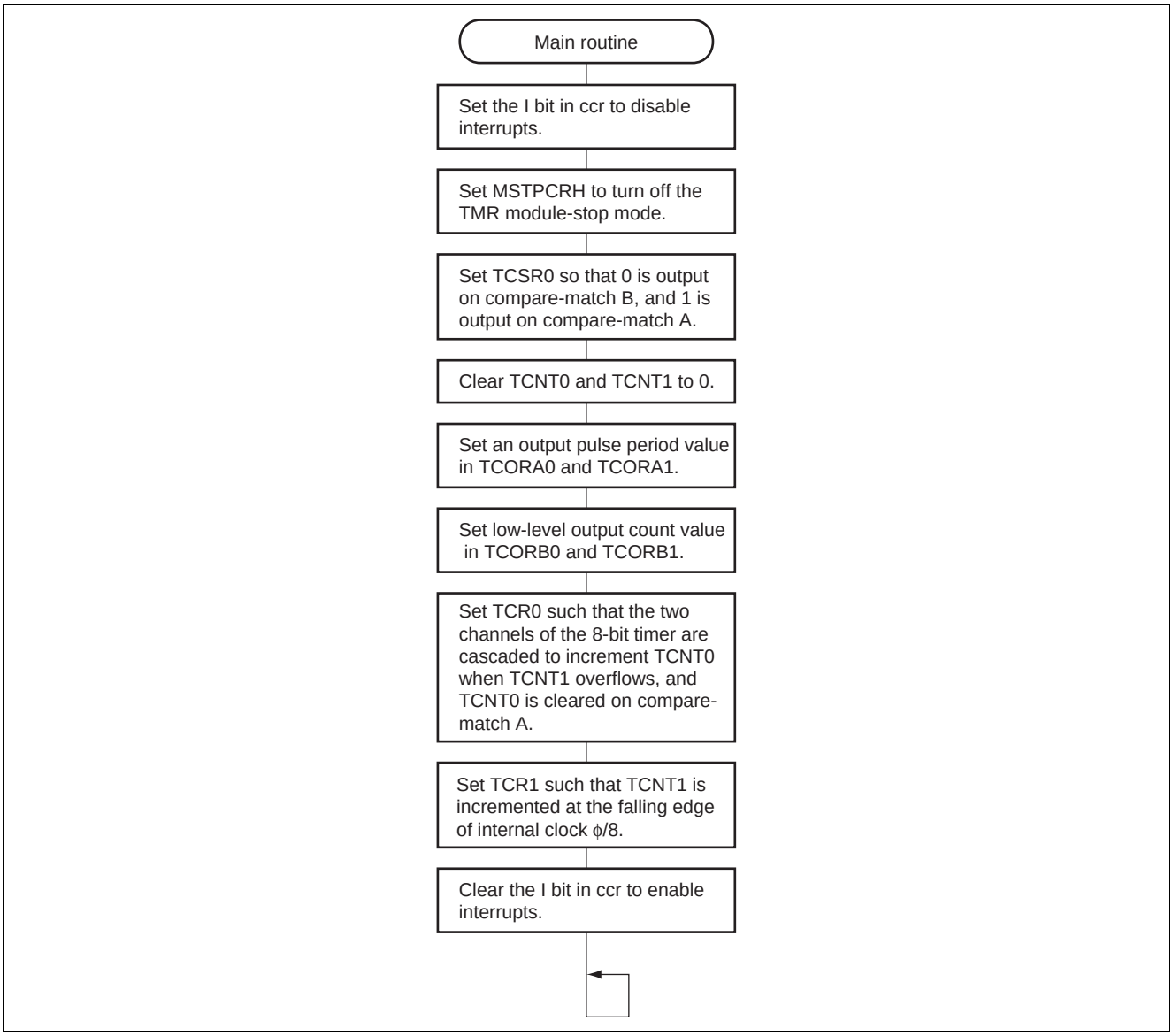
Table 3 Description of Internal Registers (1)

Register Name		Function	Address	Setting
TCNT0, TCNT1		Timer Counter 16-bit up counter that can be read or written to.	H'FFFFB8	H'0000
TCORA0, TCORA1		Time Constant Register A In this sample task, TCORA0 and TCORA1 are used as a 16-bit register that can be read or written to.	H'FFFFB4	H'AAAA
TCORB0, TCORB1		Time Constant Register B In this sample task, TCORB0 and TCORB1 are used as a 16-bit register that can be read or written to.	H'FFFFB6	H'3333
TCR0	CMIEB	Timer Control Register (Compare-Match Interrupt Enable B) When CMIEB = 0, CMFB interrupt request (CMIB) is disabled. When CMIEB = 1, CMFB interrupt request (CMIB) is enabled.	H'FFFFB0 Bit 7	0
	CMIEA	Timer Control Register (Compare-Match Interrupt Enable A) When CMIEA = 0, CMFA interrupt request (CMIA) is disabled. When CMIEA = 1, CMFA interrupt request (CMIA) is enabled.	H'FFFFB0 Bit 6	0
	OVIE	Timer Control Register (Timer Overflow Interrupt Enable) When OVIE = 0, OVF interrupt request (OVI) is disabled. When OVIE = 1, OVF interrupt request (OVI) is enabled.	H'FFFFB0 Bit 5	0
	CCLR1 CCLR0	Timer Control Register (Counter Clear 1, 0) When CCLR1 and CCLR0 = [0, 1], TCNT is cleared on compare-match A. When CCLR1 and CCLR0 = [1, 0], TCNT is cleared on compare-match B. Note: For other setting values, refer to the hardware manual.	H'FFFFB0 Bit 4 Bit 3	0, 1

Register	Name	Function	Address	Setting
TCR0	CKS2 CKS1 CKS0	Timer Control Register (Clock Select 2 to 0) When CKS2, CKS1, and CKS0 = [0, 0, 0], clock input is disabled. When CKS2, CKS1, and CKS0 = [1, 0, 0], TCNT0 is incremented at each overflow of TCNT1. Note: For other setting values, refer to the hardware manual.	H'FFFFB0 Bits 2 to 0	1, 0, 0
TCSR0	CMFB	Timer Control/Status Register (Compare-Match Flag B) CMFB = 0 indicates that TCNT does not match TCORB. CMFB = 1 indicates that TCNT matches TCORB.	H'FFFFB2 Bit 7	0
	CMFA	Timer Control/Status Register (Compare-Match Flag A) CMFA = 0 indicates that TCNT does not match TCORA. CMFA= 1 indicates that TCNT matches TCORA.	H'FFFFB2 Bit 6	0
	OVF	Timer Control/Status Register (Timer Overflow Flag) OVF = 0 indicates that a TCNT has not overflowed. OVF= 1 indicates that a TCNT has overflowed (H'FF → H'00).	H'FFFFB2 Bit 5	0
	ADTE	Timer Control/Status Register (A/D Trigger Enable) When ADTE = 0, A/D conversion start request on compare-match A is disabled. When ADTE = 1, A/D conversion start request on compare-match A is enabled.	H'FFFFB2 Bit 4	0
	OS3 OS2	Timer Control/Status Register (Output Select 3, 2) When OS3 and OS2 = [0, 0], no output change. When OS3 and OS2 = [0, 1], 0 is output on compare-match B. Note: For other setting values, refer to the hardware manual.	H'FFFFB2 Bit 3 Bit 2	0, 1
	OS1 OS0	Timer Control/Status Register (Output Select 1, 0) When OS1 and OS0 = [1, 0], 1 is output on compare-match A. When OS1 and OS0 = [1, 1], the output is toggled on compare-match A. Note: For other setting values, refer to the hardware manual.	H'FFFFB2 Bit 1 Bit 0	1, 0
TCR1	CKS2 CKS1 CKS0	Timer Control Register (Clock Select 2 to 0) When CKS2, CKS1, and CKS0 = [0, 0, 0], clock input is disabled. When CKS2, CKS1, and CKS0 = [0, 0, 1], TCNT1 is incremented at the falling edge of the internal clock ϕ/8. Note: For other setting values, refer to the hardware manual.	H'FFFFB1 Bits 2 to 0	0, 0, 1

6. Flowchart

6.1 Main Routine



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		Description	
Rev.	Date	Page	Summary
1.00	Mar.09.05	—	First edition issued

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