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Renesas Electronics Corporation

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H8/38076R

Counting Interrupts Using 16-Bit Timer Counter Function of Timer F

Introduction

The 16-bit timer counter function of timer F is used to count timer F interrupts. The sample task ends when the interrupt count reaches 50.

Target Device

H8/38076R

Contents

1. Specifications

In this sample task an interrupt request indicating a timer F overflow is generated each time timer counter F (TCF) overflows, and an 8-bit timer set in RAM is decremented as part of the timer F interrupt processing routine.

- An 8-bit timer set in RAM is decremented by the timer F interrupt processing routine. When the timer F interrupt count reaches 50, timer F interrupt requests are disabled and the sample task ends.
- Settings are made so that timer F interrupts are generated every 26.215 ms when timer counter F (TCF) overflows.
- This sample task uses the 16-bit timer counter function of timer F to count timer F interrupts.

2. Description of Functions

2.1 Functions

A block diagram of the 16-bit timer counter function of timer F is shown in figure 1. The 16-bit timer counter function of timer F is described below.

1. System Clock (ϕ)
   This 10-MHz clock is the reference clock for operation of the CPU and peripheral functions.

2. Prescaler S (PSS)
   PSS is a 13-bit counter that counts up once per period.

3. Timer F Functions
   This 16-bit timer has an output compare function. It can be used for external event counting or as a multifunction timer for a variety of applications, including counter resetting, interrupt request, and toggle output using compare match signals. It can also be used as two independent 8-bit timers (timer FH and timer FL).

- Timer counter F (TCF)
  TCF is a 16-bit readable/writeable up-counter that is incremented by input of an internal or an external clock. Five input clock options are available: the system clock divided by 4, 16, or 32; the subclock divided by 4; or an external clock.
  In this sample task the system clock divided by 4 is selected as the TCF input clock.
- Timer control register F (TCRF)
  TCRF switches between 16-bit mode and 8-bit mode, selects among the four internal clocks and an external event, and selects the output level of the TMOFH and TMOFL pins.
- Timer control/status register F (TCSRF)
  TCSRF performs counter clear selection, overflow flag and compare match flag settings, and controls enabling of overflow interrupt requests.

4. Interrupt Controller Functions
   The following registers are used to control interrupts.

- Interrupt enable register 2 (IENR2)
  IENR2 controls timer F interrupts.
- Interrupt request register 2 (IRR2)
  IRR2 is the interrupt request status register for timer F interrupts.

The method of calculating the timer counter F (TCF) overflow period for this sample task is shown below.

$$\text{TCF overflow cycle} = \frac{1}{\text{System clock} / 4} \times 65536$$

$$= \frac{1}{10\ \text{MHz} / 4} \times 65536$$

$$= 26.215\ \text{ms}$$

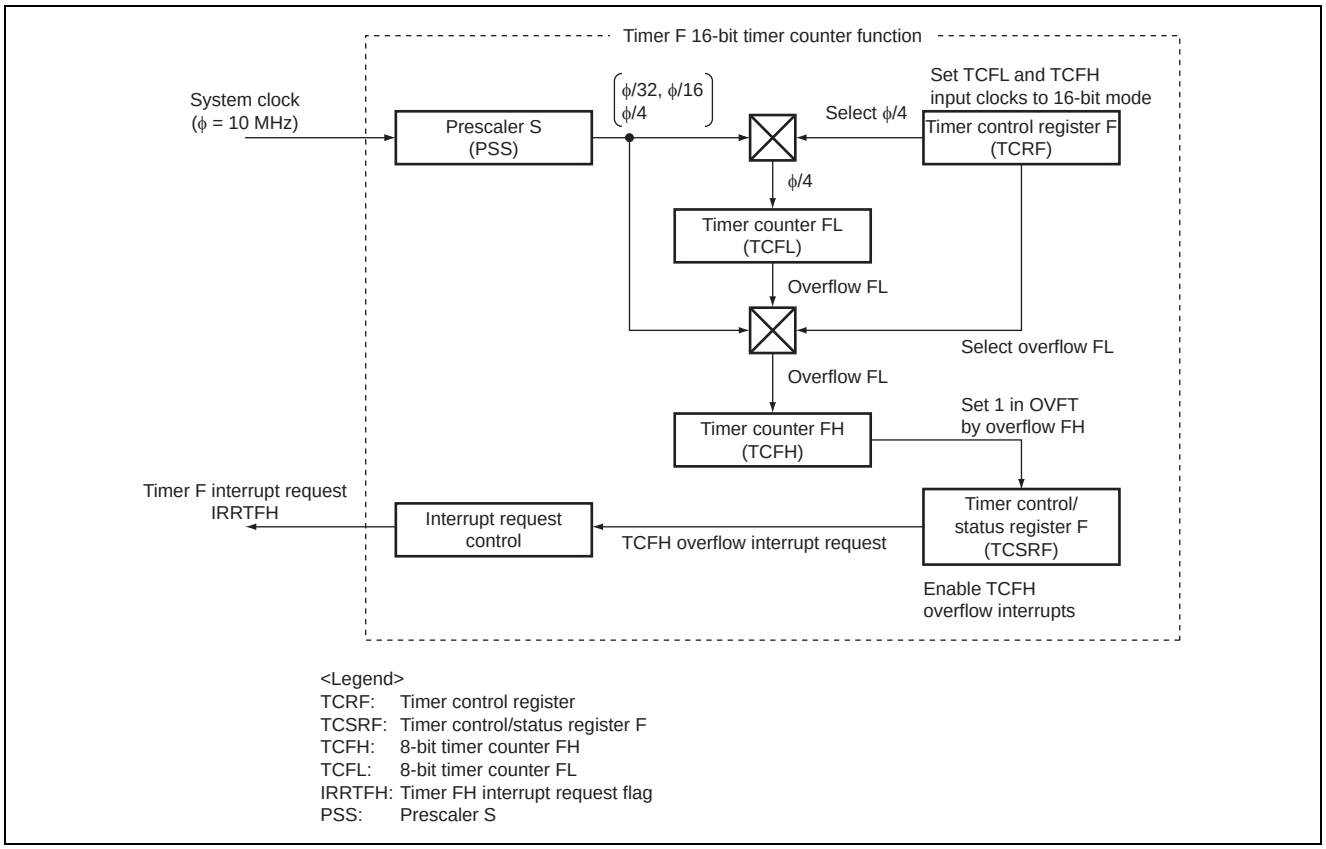


Figure 1 Block Diagram of 16-Bit Timer Counter Function of Timer F

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. The 16-bit timer counter function of timer F is used to count interrupts as shown in table 1.

Table 1 Assignment of Functions

Elements	Description
TCRF	Sets TCF as 16-bit counter, selects ϕ/4 as TCF input clock
TCSRF	Enables TCF overflow interrupts, disables clearing TCF by compare match, TCF status register
TCF	16-bit counter using system clock divided by 4 as input clock
IENTFH	Enables timer F interrupt requests
IRRTFH	Timer F interrupt request flag

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 2. Using the hardware and software processing shown in figure 2 the 16-bit timer counter function of timer F is used to count interrupts.

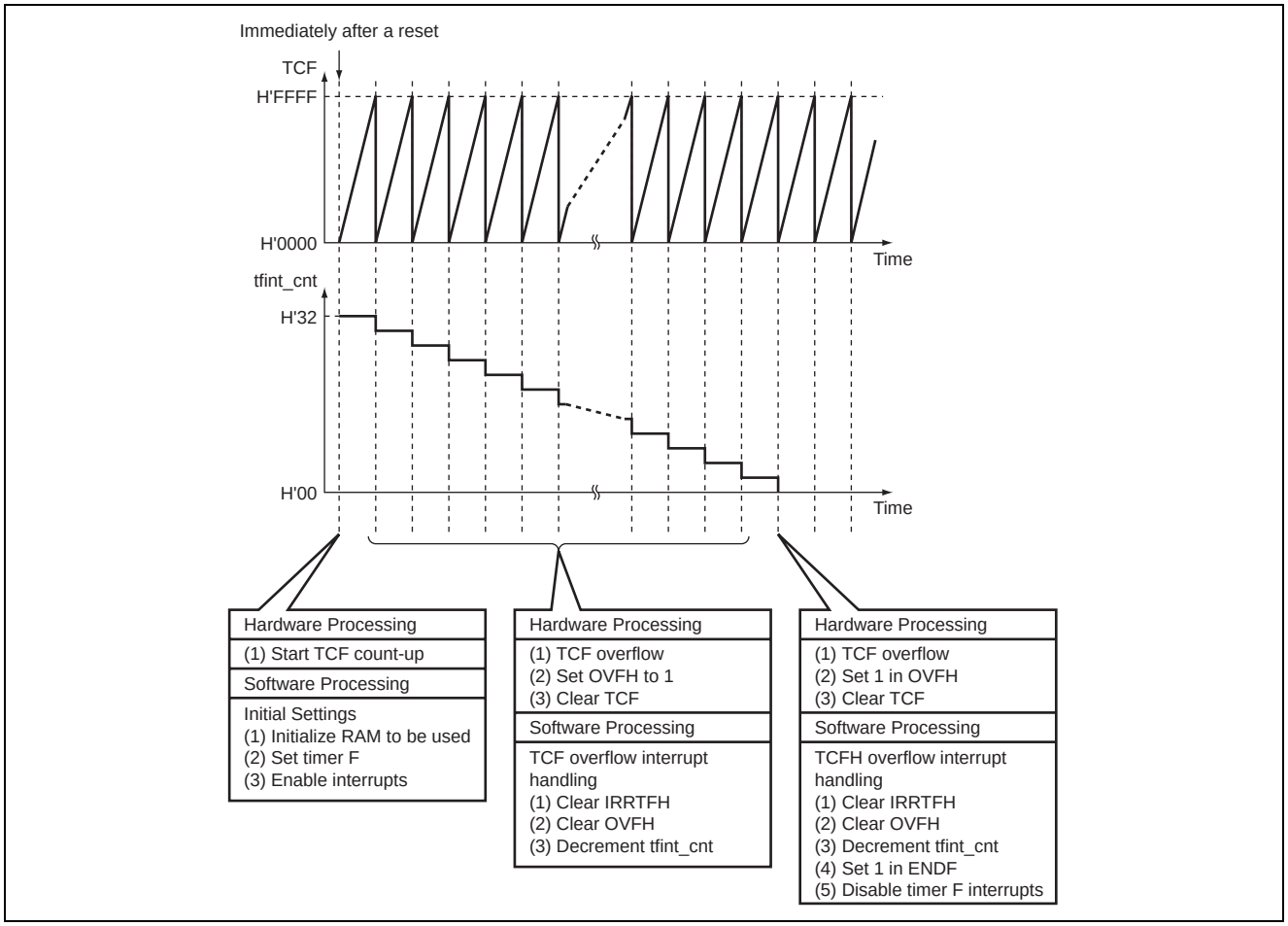


Figure 2 Principles of Operation

4. Description of Software

4.1 Description of Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	Settings for timer F 16-bit timer counter function Selects ϕ/4 as the TCF clock source, enables TCF overflow interrupts, and disables clearing the counter by compare match Initializes RAM area to be used, enables interrupts
tfint	Timer F overflow interrupt handling Clears IRRTFH and OVFH, decrements 8-bit counter, and disables timer F overflow interrupts after counting 50 timer F overflow interrupts

4.2 Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

The internal registers used in this sample task are shown below.

- TCRF Timer Control Register F Address: H'FFB6

Bit	Bit Name	Set Value	R/W	Description
6	CKSH2	0	W	Clock Select H
5	CKSH1	0	W	Selects the clock input to TCFH from among internal clock
4	CKSH0	0	W	sources or TCFL overflow. 000: 16-bit mode, counting on TCFL overflow signal 001: 16-bit mode, counting on TCFL overflow signal 010: 16-bit mode, counting on TCFL overflow signal
2	CKSL2	1	W	Clock Select L
1	CKSL1	1	W	Select the clock input to TCFL from among internal clock
0	CKSL0	0	W	sources or external event input. 110: Counting on internal clock ϕ/4

- TCSRF Timer Control/Status Register F Address: H'FFB7

Bit	Bit Name	Set Value	R/W	Description
7	OVFH	Undefined	R/W*	Timer Overflow Flag H [Setting condition] • When TCFH overflows from H'FF to H'00 [Clearing condition] • When 0 is written to this bit after reading it as 1
5	OVIEH	1	R/W	Timer Overflow Interrupt Enable H Enables or disables interrupt generation when TCFH overflows. 1: TCFH overflow interrupt requests enabled
4	CCLRH	0	R/W	Counter Clear H In 16-bit mode this bit selects whether TCF is cleared when TCF and OCRF match. In 16-bit mode: 0: TCF clearing by compare match disabled

Note: * Only 0 can be written to clear the flag.

- TCF Timer Counter F Address: H'FFB8

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	Undefined	R/W	Output Compare Register F When CKSH2 in TCRF is set to 0 TCF operates as a 16-bit counter. The TCF input clock is selected by bits CKSL2 to CKSL0 in TCF. TCF can be cleared in the event of a compare match by CCLRH in TCSRF. When TCF overflows from H'FFFF to H'0000, OVFH in TCSRF is set to 1. If the value of OVIEH in TCSRF is 1 at this time, IRRTFH in IRR2 is set to 1, and if in addition the value of IENTFH in IENR2 is 1, an interrupt request is sent to the CPU.
14	Bit 14	Undefined	R/W	
13	Bit 13	Undefined	R/W	
12	Bit 12	Undefined	R/W	
11	Bit 11	Undefined	R/W	
10	Bit 10	Undefined	R/W	
9	Bit 9	Undefined	R/W	
8	Bit 8	Undefined	R/W	
7	Bit 7	Undefined	R/W	
6	Bit 6	Undefined	R/W	
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

- IENR2 Interrupt Enable Register 2 Address: H'FFF4

Bit	Bit Name	Set Value	R/W	Description
3	IENTFH	1	R/W	Timer FH Interrupt Enable Timer FH interrupt requests are enabled when this bit is set to 1. 1: Timer FH interrupt requests enabled

- IRR2 Interrupt Request Register 2 Address: H'FFF7

Bit	Bit Name	Set Value	R/W	Description
3	IRRTFH	Undefined	R/W	Timer FH Interrupt Request Flag [Setting condition] • When timer FH compare match or overflow occurs [Clearing condition] • When 0 is written to this bit

4.4 RAM Usage

The RAM usage in this sample task is as follows.

- tfint_cnt

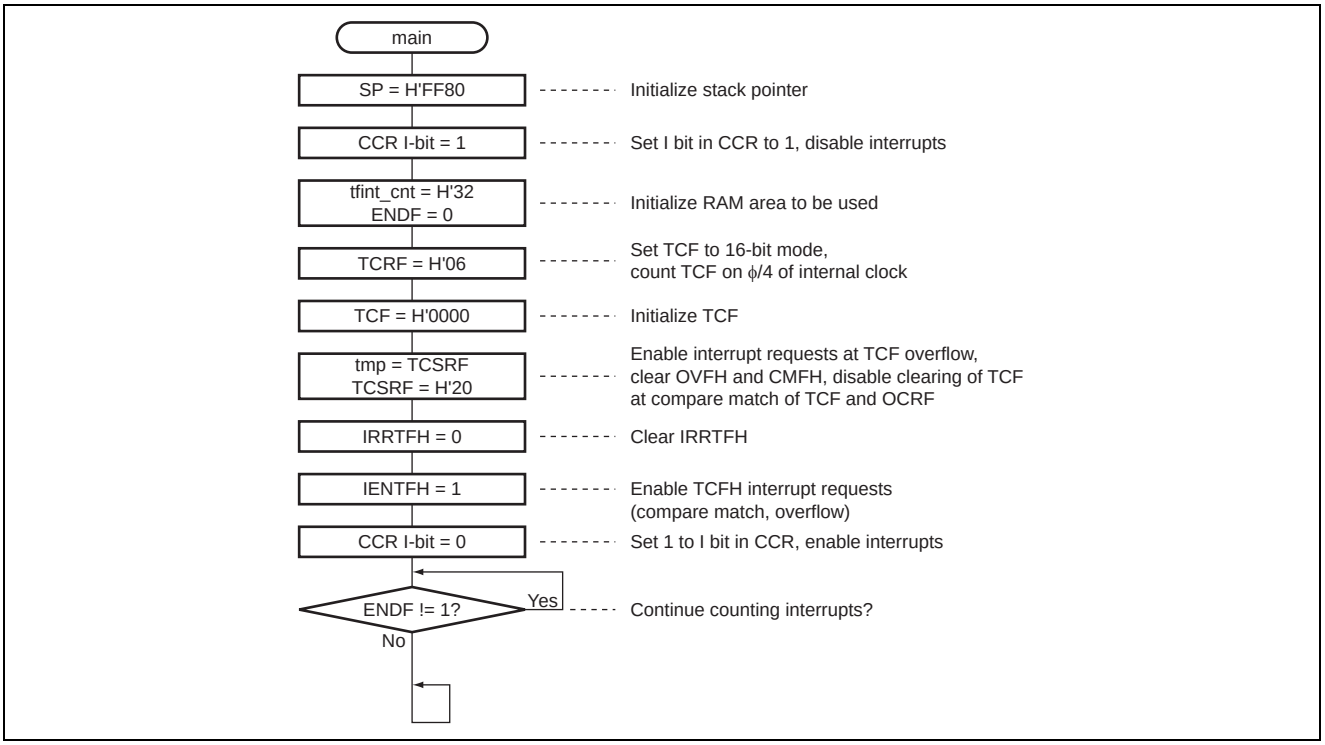
Bit	Bit Name	Description	Amount of Memory Used	Used in
0 to 7	—	8-bit counter	1 byte	main tfint

- usrf

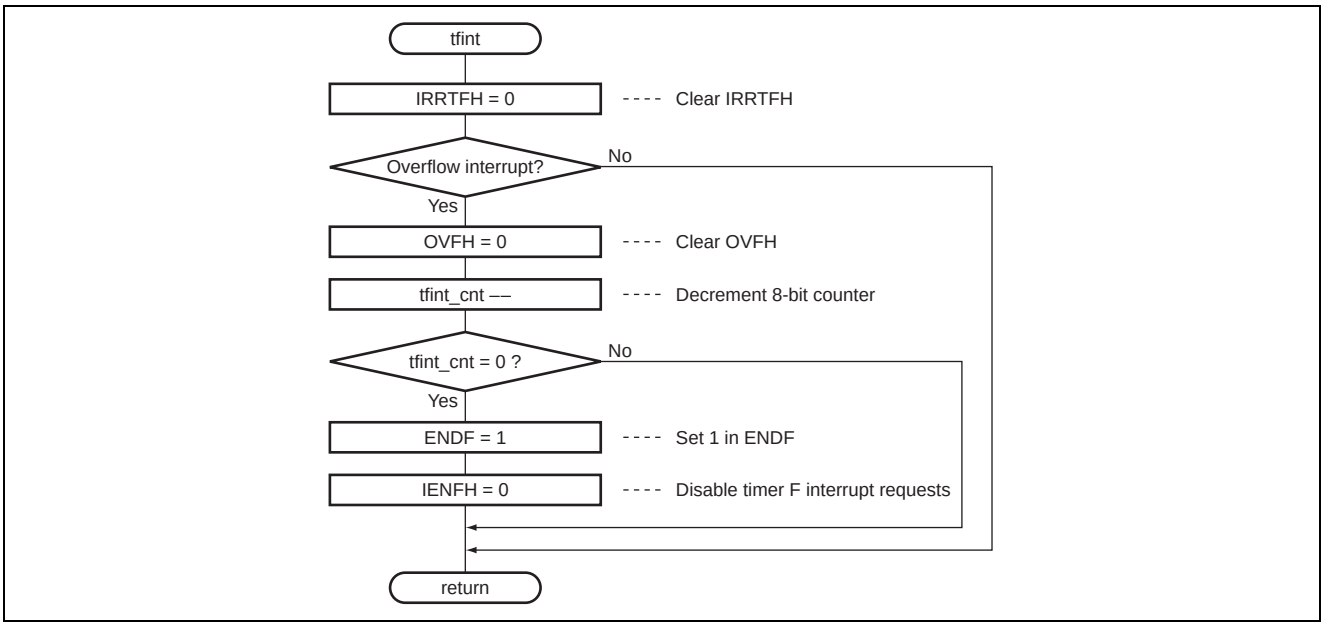
Bit	Bit Name	Description	Amount of Memory Used	Used in
0	ENDF	Flag to determine whether the counter value of 8-bit counter is H’00.	1 bit	main tfint

5. Flowchart

5.1 main



5.2 tfint



5.3 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.18.05	—	First edition issued

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