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H8/300H Tiny Series

Reset Operation upon Detecting Low Voltage

Introduction

An internal low-voltage detection circuit is used for setting/canceling internal reset operations at low voltages.

Target Device

H8/3687G

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1. Specifications

1. An internal low-voltage detection circuit is used, and when the voltage falls to 3.6 V or lower, an internal reset occurs.
2. While in low-voltage reset state, when the voltage rises to 3.6 V or higher, PSS starts counting upward, and the internal reset is cancelled after 131,072 states have passed.
3. In order to confirm the operating/reset state, connect an LED to pin P74. In the operating state, the LED is turned on (P74 = 0), and in the reset state the LED is turned off (P74 = 1).
4. If the IRQ switch is turned on, the low-voltage detection circuit is canceled.
5. A connection example for this task appears in figure 1.1.

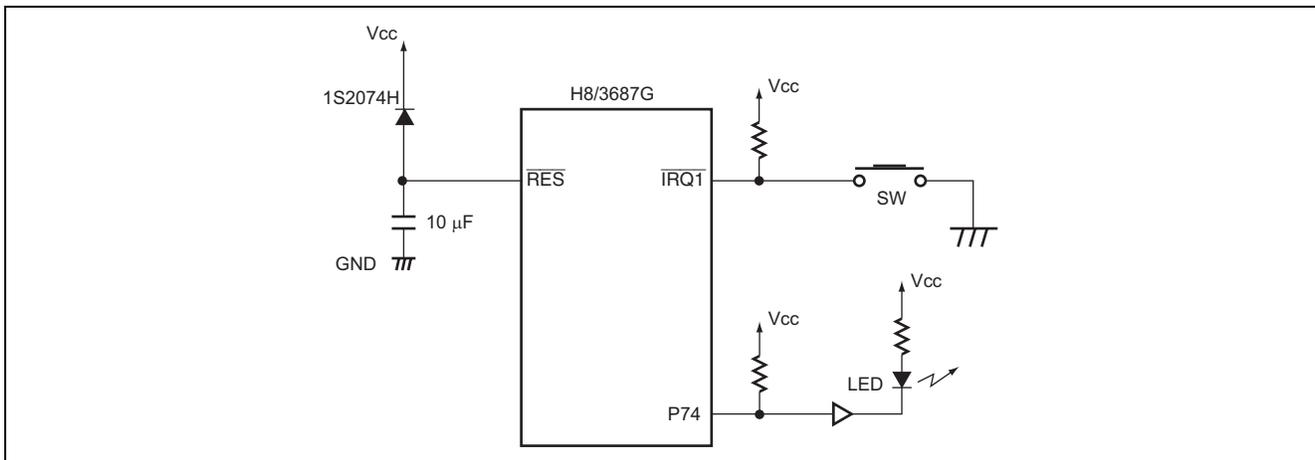


Figure 1.1 Connection example for this task

2. Description of Functions

In this sample task, the optional internal low-voltage detection circuit is used to control the reset operation at low voltages. A block diagram of the low-voltage detection circuit appears in figure 2.1. Below, the block diagram of the low-voltage detection circuit is described.

- System clock (ϕ) is a 16 MHz clock which serves as the reference clock for operation of the CPU and peripheral functions.
- Prescaler S (PSS) is functions as a 13-bit counter when ϕ is input, counting up one each cycle.
- Low-voltage detection control register (LVDCR) is controls the low-voltage detection circuit. In this sample task, the low-voltage detection circuit is used, and sets the reset detection voltage to 2.3 V.

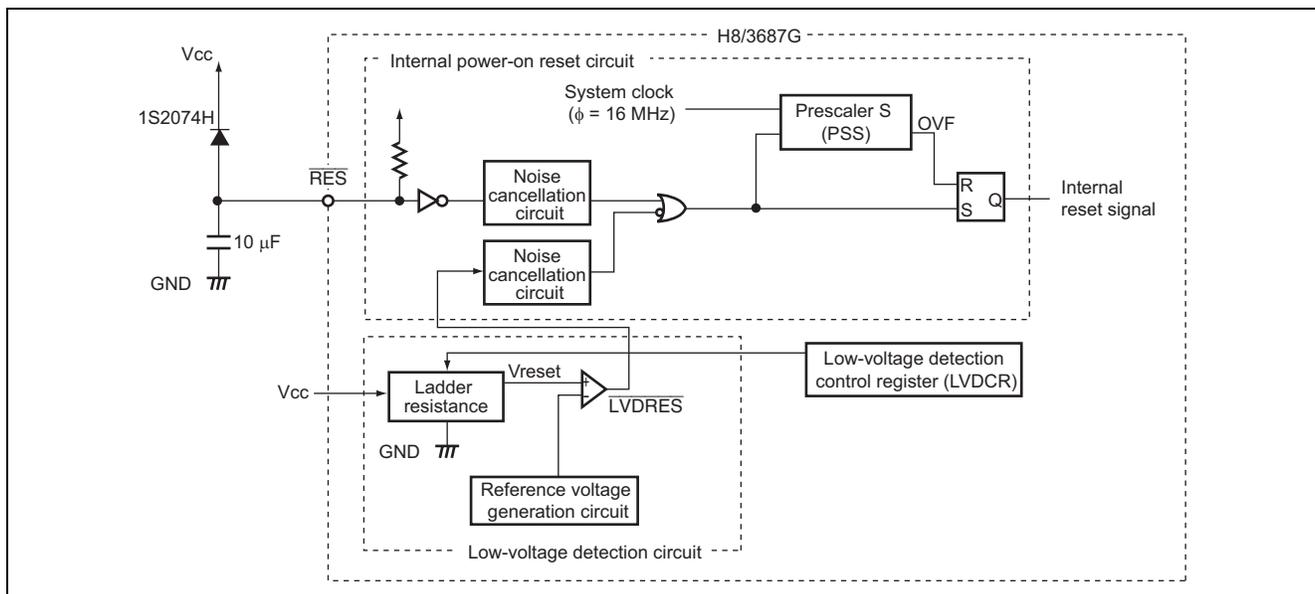


Figure 2.1 Block diagram of the low-voltage detection circuit

3. Description of Operation

Figure 3.1 shows the procedure for setting and canceling low-voltage detection reset circuit, and reset operation on low voltage detection.

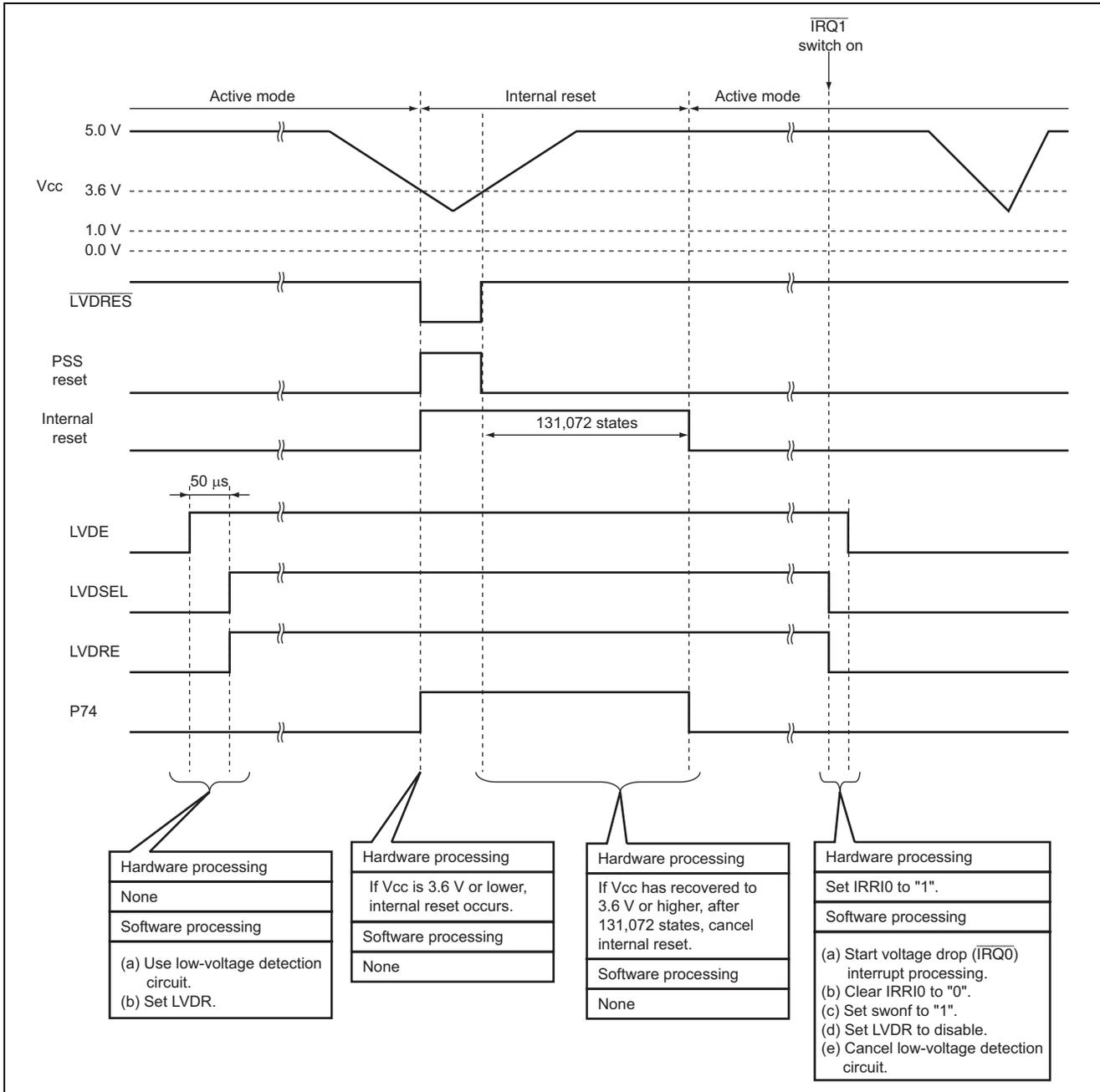


Figure 3.1 Description of operation

4. Description of Software

4.1 Description of modules

Modules in this sample task are listed in table 4.1.

Table 4.1 Description of modules

Module name	Label name	Function
Main routine	main	Set low-voltage detection circuit, enable interrupts, control LED (P74), and judge switch connected to IRQ0
Switch on	irq1int	IRQ1 interrupt processing Set swonf to 1

4.2 Description of arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers Used

Internal registers used in this sample task are indicated below.

- LVDCR Low-voltage detection control register Address: 0xF730

Bit	Bit name	Setting	Function
7	LVDE	1	LVD enable LVDE = 0: Low-voltage detection circuit is not used (standby state) LVDE = 1: Low-voltage detection circuit is used
3	LVDSSEL	1	LVDR detection level selection LVDSSEL = 0: Sets reset detection voltage to 2.3 V LVDSSEL = 1: Sets reset detection voltage to 3.6 V
2	LVDRRE	1	LVDR enable LVDRRE = 0: Disables reset by LVDR LVDRRE = 1: Enables reset by LVDR

- PDR7 Port data register 7 Address: 0xFFDA

Bit	Bit name	Setting	Function
4	P74	0	Port data register 74 P74 = 0: Pin P74 output level Low P74 = 1: Pin P74 output level High

- PMR1 Port mode register 1 Address: 0xFFE0

Bit	Bit name	Setting	Function
5	IRQ1	1	Selects function of pin P15/IRQ1/TMIB1 IRQ1 = 0: Sets pin P15/IRQ1/TMIB1 to P15 I/O pin function IRQ1 = 1: Sets pin P15/IRQ1/TMIB1 to /IRQ1/TMIB1 input pin

- PCR7 Port control register 7 Address: 0xFFEA

Bit	Bit name	Setting	Function
4	PCR74	0	Port control register 74 PCR74 = 0: Sets pin P74 to P74 input pin function PCR74 = 1: Sets pin P74 to P74 output pin function

- IEGR1 Interrupt edge select register 1 Address: 0xFFFF2

Bit	Bit name	Setting	Function
0	IEG1	1	IRQ1 edge select IEG1 = 0: Selects falling edge as IRQ1 pin input detection edge IEG1 = 1: Selects rising edge as IRQ1 pin input detection edge

- IENR1 Interrupt enable register 1 Address: 0xFFFF4

Bit	Bit name	Setting	Function
1	IEN1	1	IRQ1 interrupt request enable IEN1 = 0: Disables interrupt requests at pin IRQ1 IEN1 = 1: Enables interrupt requests at pin IRQ1

- IRR1 Interrupt flag register 1 Address: 0xFFFF6

Bit	Bit name	Setting	Function
1	IRRI1	0	IRQ1 interrupt request flag IRR1 = 0: IRQ1 pin interrupt not requested IRR1 = 1: IRQ1 pin interrupt requested

4.4 Description of RAM Used

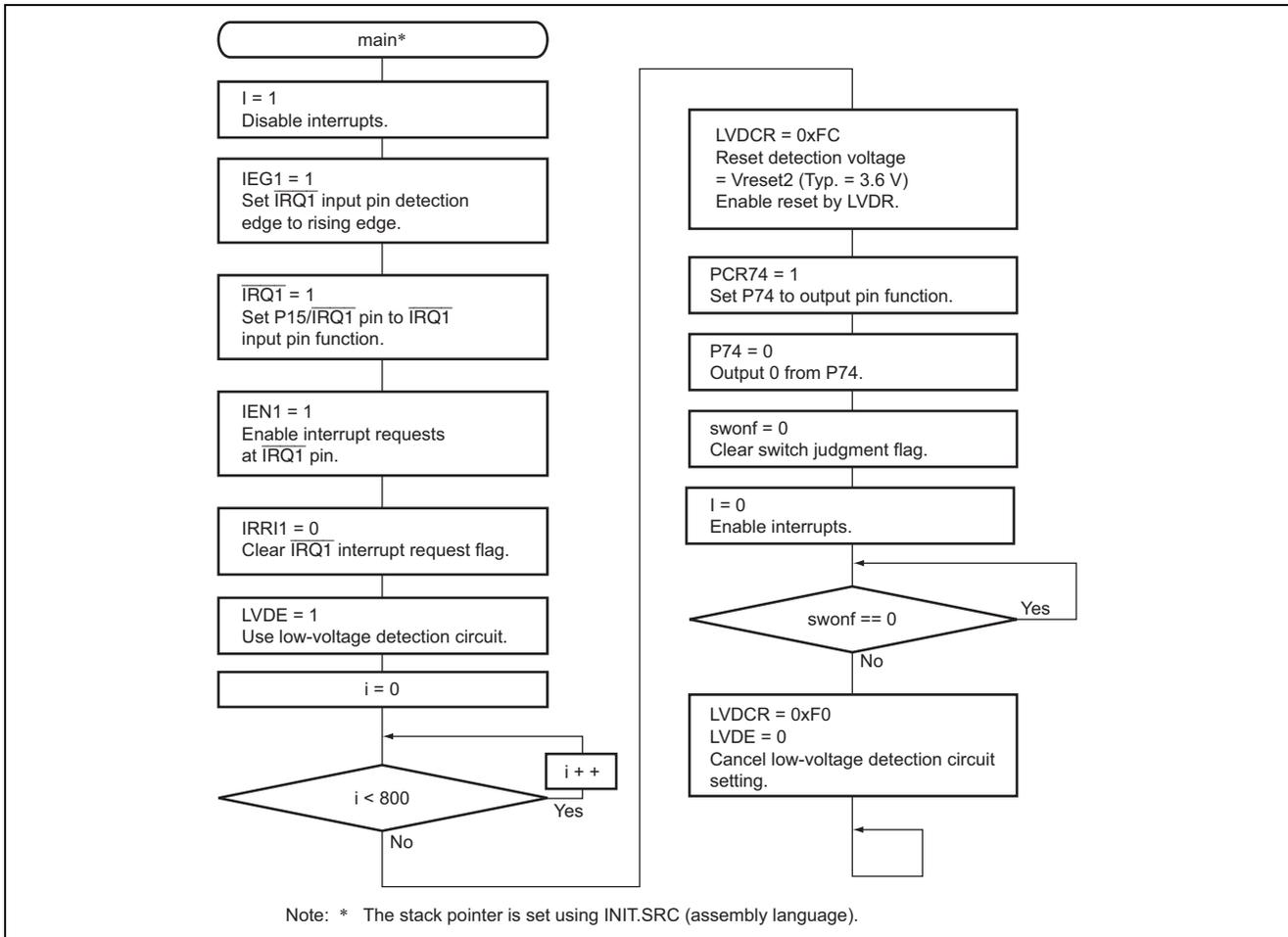
The RAM used in this sample task is described in table 4.2.

Table 4.2 Description of RAM used

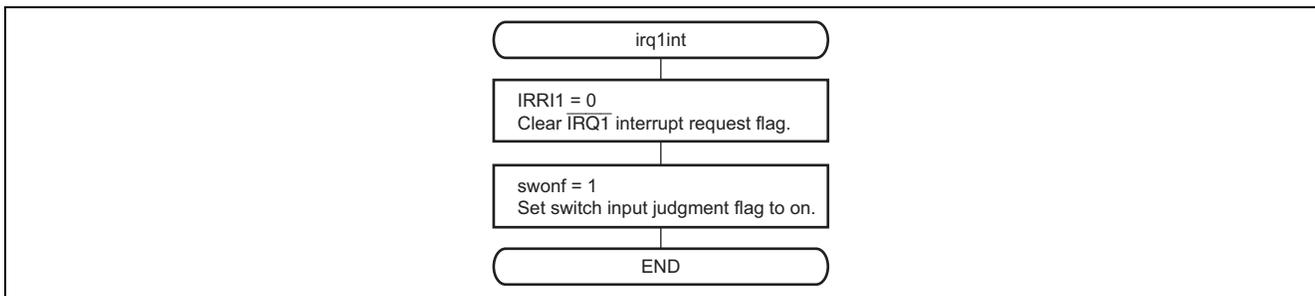
Label name	Function	Size	Used in
swonf	Flag determining switch input on/off status	1 byte	Main routine Switch on

5. Flowcharts

1. Main routine



2. Switch-on



6. Program Listing

```

/*****
/*
/* H8/300HN Series -H8/3687G-
/* Application Note
/*
/* 'Reset by lowvoltage'
/*
/* Function
/* : Low-voltage detection circuit
/*
/* External Clock : 16MHz
/* Internal Clock : 16MHz
/* Sub Clock      : 32.768kHz
/*
*****/

#include <machine.h>

/*****
/* Symbol Definition
*****/
struct BIT {
    unsigned char  b7:1;    /* bit7 */
    unsigned char  b6:1;    /* bit6 */
    unsigned char  b5:1;    /* bit5 */
    unsigned char  b4:1;    /* bit4 */
    unsigned char  b3:1;    /* bit3 */
    unsigned char  b2:1;    /* bit2 */
    unsigned char  b1:1;    /* bit1 */
    unsigned char  b0:1;    /* bit0 */
};

#define LVDCR      *(volatile unsigned char *)0xF730      /* Low-voltage-detection control register */
#define LVDCR_BIT  (*(struct BIT *)0xF730)               /* Low-voltage-detection control register */
#define LVDE       LVDCR_BIT.b7                          /* LVD Enable */
#define LVDSSEL    LVDCR_BIT.b3                          /* LVDI Detection Level Select */
#define LVDRE      LVDCR_BIT.b2                          /* LVDR Enable */
#define PDR7_BIT   (*(struct BIT *)0xFFDA)               /* Port Data Register 7 */
#define P74        PDR7_BIT.b4                          /* Port Data Register 7 bit4 */
#define PMR1_BIT   (*(struct BIT *)0xFFE0)               /* Port mode register 1 */
#define IRQ1       PMR1_BIT.b5                          /* P15/IRQ1 Pin Function Switch */
#define PCR7_BIT   (*(struct BIT *)0xFFEA)               /* Port Control Register 7 */
#define PCR74      PCR7_BIT.b4                          /* Port Control Register 7 bit4 */
#define IEGR1_BIT  (*(struct BIT *)0xFFF2)               /* Interrupt Edge Select Register 1 */
#define IEG1       IEGR1_BIT.b1                          /* IRQ1 Edge Select */
#define IENR1_BIT  (*(struct BIT *)0xFFFF4)              /* Interrupt Enable Register 1 */
#define IEN1       IENR1_BIT.b1                          /* IRQ1 Interrupt Enable */
#define IRR1_BIT   (*(struct BIT *)0xFFFF6)              /* Interrupt Request Register 1 */
#define IRR11      IRR1_BIT.b1                          /* IRQ1 Interrupt Request Flag */

#pragma interrupt (irqlint)

```

```

/*****
/*  Function define
/*****
extern void INIT ( void );          /* SP Set
void main ( void );
void irqlint ( void );

/*****
/*  RAM define
/*****
volatile unsigned char swonf;

/*****
/*  Vector Address
/*****
#pragma section V1          /* VECTOR SECTOIN SET
void (*const VEC_TBL1[])(void) = {
    INIT                    /* 00 Reset
};
#pragma section V2          /* VECTOR SECTOIN SET
void (*const VEC_TBL2[])(void) = {
    irqlint                 /* 1E IRQ1 Interrupt
};

#pragma section          /* P
/*****
/*  Main Program
/*****
void main ( void )
{
    unsigned short i;

    set_imask_ccr(1);        /* Interrupt Disable
                               /*
    IEG1 = 1;               /* IRQ1 pin input is Rising edge
    IRQ1 = 1;               /* Select IRQ1 pin
    IEN1 = 1;               /* IRQ1 Interrupt Enable
    IRR11 = 0;              /* IRQ1 Flag Clear

    LVDE = 1;               /* LVD Enable
    for(i=0; i<800; i++);   /* 50us Wait
    LVDCR = 0xFC;           /* LVD = 3.6V LVD Reset Enable

    PCR74 = 1;              /* P74 Output Pin
    P74 = 0;                /* P74 is Low
    swonf = 0;              /* Initialize swonf
    set_imask_ccr(0);       /* Interrupt Enable
    while(swonf == 0);

    LVDCR = 0xF0;           /* clearing LVDRE, LVDDE, LVDUE to 0
    LVDE = 0;               /* clear LVDE 0

    while(1);
}

```

```
/*-----*/
/*  IRQ1 Interrupt                                     */
/*-----*/
void irq1int ( void )
{
    IRR11 = 0;                                       /* Clear IRR11          */
    swonf = 1;                                       /* Set swonf            */
}

```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x001E
P	0x0100
B	0xFB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.29.03	—	First edition issued
2.00	May.07.04	—	Clerical error correction

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