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H8/300H SLP Series

Pulse Output Using TPU Output Compare Function

Introduction

The output compare function of the 16-bit timer pulse unit (TPU) is used to output pulses with a 4-ms cycle and 50% duty cycle from an output compare output pin (TIOCA1).

Target Device

H8/38076R

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1. Specifications

- The output compare function of the 16-bit timer pulse unit (TPU) is used to output pulses with a 4-ms cycle and 50% duty cycle from an output compare output pin (TIOCA1).
- An example of pulse output by means of the TPU output compare function is shown in figure 1.

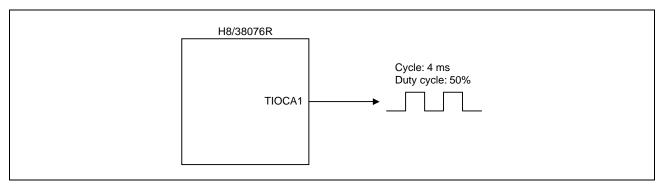


Figure 1 Example of Pulse Output Using TPU Output Compare Function

2. Functions Used

2.1 TPU Output Compare Function

In this sample task, the output compare function of the TPU is used to output pulses with a 4-ms cycle and 50% duty cycle from an output compare output pin (TIOCA1). A block diagram of the output compare function of the TPU is shown in figure 2. The block diagram of the output compare function of the TPU is explained below.

- Timer control register_1 (TCR_1)
 - Selects timer counter 1 (TCNT 1) counter clearing source, the input clock edge, and the clock source.
- Timer mode register_1 (TMDR_1)
 - Sets the operating mode of channel 1.
- Timer I/O control register_1 (TIOR_1)
 - Controls timer general register A 1 (TGRA 1).
- Timer counter_1 (TCNT_1)
 - A 16-bit readable/writable counter that counts using the rising edge of internal clock $\phi/4$
- Timer general register A_1 (TGRA_1)
 - A 16-bit readable/writable output compare register
- Timer start register (TSTR)
 - Controls operation/stopping of timer counter 1 (TCNT 1).
- An example of output compare output cycle calculation is shown below.

$$(\phi = 10 \text{ MHz}, \text{TCNT}_1 \text{ input clock} = \phi/4, \text{TGRA}_1 = \text{H}'1387 = 4999)$$

Pulse cycle =
$$\frac{\text{TGRA}_1 \text{ set value} + 1}{\text{TCNT 1 input clock}} \times 2 = \frac{4999 + 1}{10 \text{ MHz} / 4} \times 2 = 4 \text{ ms}$$



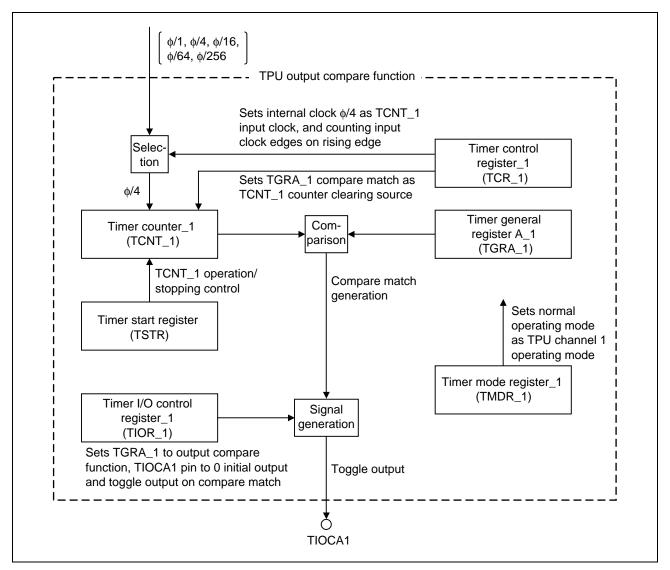


Figure 2 Block Diagram of TPU Output Compare Function



2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, pulses are output by means of the output compare function of the TPU.

Table 1 Assignment of Functions

Elements	Description
TCR_1	Sets TGRA_1 compare match as TCNT_1 counter clearing source, rising edge as input clock edge, and internal clock $\phi/4$ as clock source
TMDR_1	Sets normal operating mode as TPU channel 1 operating mode
TIOR_1	Sets output compare register as TGRA_1 function, initial output 0 and toggle output on compare match for TIOCA1 pin function
TCNT_1	16-bit counter using internal clock φ/4 as clock source
TGRA_1	16-bit output compare register, pulse cycle set to 4 ms
TSTR	Sets TCNT_1 count operation
TIOCA1	TGRA_1 output compare output pin



3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, pulses are output by means of the TPU output compare function.

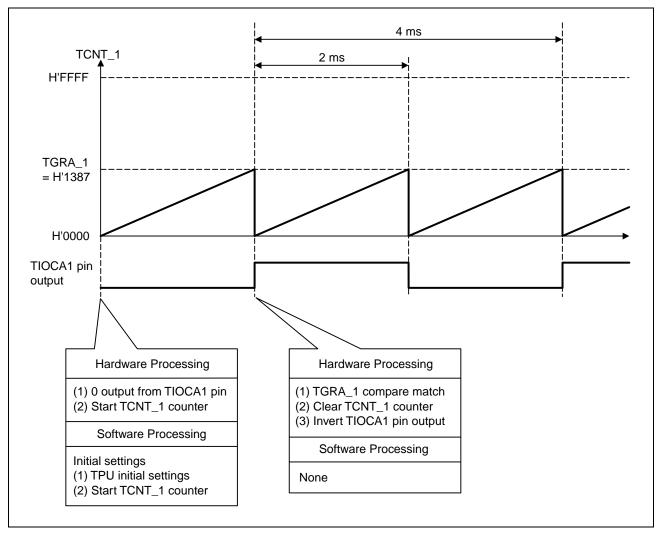


Figure 3 Principles of Operation



4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	TPU initial settings, TCNT_1 count operation start, interrupt enabling

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

•	TSTR Timer s	start register	Address	s: H'F030
Bit	Bit Name	Set Value	R/W	Description
1	CST1	1	R/W	Counter start 1
				Selects TCNT_1 operation or stopping.
				CST1 = 1: TCNT_1 performs count operation

•	• TCR_1 Timer control register_1		r_1	Address: H'F040
Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	0	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_1 counter clearing source.
				CCLR1 = 0, CCLR0 = 1: TCNT_1 cleared by TGRA_1 compare match
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_1 input clock edge.
				CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	0	R/W	Timer prescaler 2, 1, 0
1	TPSC1	0	R/W	Select the TCNT_1 clock source.
0	TPSC0	1	R/W	TPSC2 = 0, TPSC1 = 0, TPSC0 = 1: Counts on internal clock $\phi/4$

•	TMDR_1 Tim	er mode registe	er_1	Address: H'F041
Bit	Bit Name	Set Value	R/W	Description
1	MD1	0	R/W	Mode 1, 0
0	MD0	0	R/W	Select the TPU_1 operating mode.
				MD1 = 0, MD0 = 0: TPU_1 set to normal operation mode



H8/300H SLP Series Pulse Output Using TPU Output Compare Function

• TIOR_1 Timer I/O control register_1				Address: H'F042	
Bit	Bit Name	Set Value	R/W	Description	
3	IOA3	0	R/W	I/O control A3 to A0	
2	IOA2	0	R/W	Select the function of TGRA_1.	
1	IOA1	1	R/W	IOA3 = 0, IOA2 = 0, IOA1 = 1, IOA0 = 1: TGRA_1 function is output	
0	IOA0	1	R/W	compare register, TIOCA1 pin function is toggle output on compare match with initial output = 0	

• T	CNT_1 Time	er counter_1	Address	s: H'F046
Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_1
14	Bit 14	0	R/W	16-bit readable/writable counter. TCNT_1 is initialized to H'0000 at a
13	Bit 13	0	R/W	reset. TCNT_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
12	Bit 12	0	R/W	be accessed in 10-bit drifts.
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	



H8/300H SLP Series Pulse Output Using TPU Output Compare Function

•	TGRA_1 Tim	er general regis	ter A_1	Address: H'F048
Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer general register A_1
14	Bit 14	0	R/W	A 16-bit readable/writable register, functioning as either output
13	Bit 13	0	R/W	compare or input capture register. TGRA_1 is initialized to H'FFFF at a reset. TGRA_1 cannot be accessed in 8-bit units, and must always
12	Bit 12	1	R/W	be accessed in 16-bit units.
11	Bit 11	0	R/W	Note: Set value: H'1387
10	Bit 10	0	R/W	
9	Bit 9	1	R/W	
8	Bit 8	1	R/W	
7	Bit 7	1	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	1	R/W	
1	Bit 1	1	R/W	
0	Bit 0	1	R/W	

4.4 Constants Used

No constants are used in this sample task.

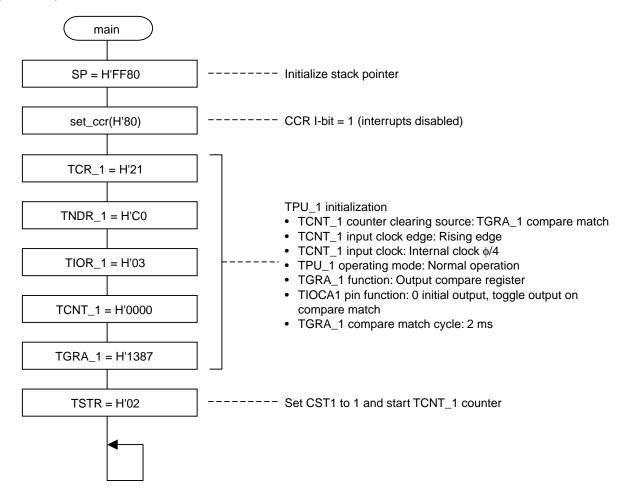
4.5 RAM Usage

No RAM is used in this sample task.



5. Flowcharts

5.1 main



• Link Address Specifications

Section Name	Address
CV1	H'0000
P	H'0100



Revision Record

LINGER	ın	tia	n
Descr	ıv	uv	

Rev.	Date	Page	Summary
1.00	Sep.16.04		First edition issued

H8/300H SLP Series Pulse Output Using TPU Output Compare Function

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