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# SH7263/SH7203 Group

## Example of Setting the CPG to Change the Operating Frequency

### Introduction

This application note describes an example of reconfiguration to change the operating frequency of the clock pulse generator (CPG) of the SH7263/SH7203.

### Target Device

SH7263/SH7203

### Contents

# 1. Preface

## 1.1 Specifications

The settings of the clock pulse generator (CPG) are modified to change the operating frequency.

A watchdog timer (WDT) is used to allow a time period for stabilization of the PLL circuit that is required to change the multiplication ratio of the PLL circuit.

## 1.2 Modules Used

- Clock pulse generator (CPG)
- Watchdog timer (WDT)

## 1.3 Applicable Conditions

- MCU: SH7263/SH7203
- Operating frequency: Internal clock: 200 MHz
  Bus clock: 6.66 MHz
  Peripheral clock: 33.33 MHz
- Compiler: SuperH RISC Engine Family C/C++ Compiler Package Ver.9.01
  (from Renesas Technology Corp.)
- Compiler options: -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc"
  -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath
  -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0
  -struct_alloc=1 -nologo

## 1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note "*SH7263/SH7203 Initialization Example*". Please refer to that note in combination with this one.

## 2. Description of the Sample Application

In this sample application, the watchdog timer (WDT) is used to count the clock oscillation stabilization time when the operating frequency is changed.

### 2.1 Operational Overview of Modules Used

After the multiplication ratio of the PLL circuit of the clock pulse generator (CPG) is changed, a certain amount of time must be provided for PLL operation to become stable. The built-in watchdog timer (WDT) is used to secure this PLL stabilization time.

When the TME (timer enable) bit is set to 0, overwriting the value in the frequency control register of the CPG (FRQCR) to change the multiplication ratio of the PLL circuit will cause the internal activity of the CPU to halt and the WDT to start counting. When the WDT overflows, clock supply by the CPG starts so operation of the CPU is resumed.

Tables 1 and 2 are the summaries of CPG and WDT features. Figures 1 and 2 show the block diagrams of CPG and WDT.

**Table 1 Overview of CPG**

| Item | Description |
|---|---|
| Clock operating mode | Four modes |
| Generated clock signals | Internal (Iϕ): Used by the CPU and cache<br>Peripheral (Pϕ): Used by on-tip peripheral modules<br>Bus (Bϕ): Used by the external bus interface |
| Frequency changing function | Frequencies of the internal and peripheral clocks can be changed independently by the PLL and divider circuits in the CPG. |
| Control of power-down modes | The clock can be stopped in sleep mode, software standby mode and deep standby mode, and the specific modules can be stopped using the module standby function. For details on clock control in the power-down modes, see section 32, Power-Down Modes. |

**Table 2 Overview of WDT**

| Item | Description |
|---|---|
| Number of channels | 1 |
| Counter | 8-bit counter (up-counter only) |
| Timer mode | Watchdog timer mode or interval timer mode |
| Pin function | The $\overline{\text{WDTOVF}}$ signal is output when the counter overflows in watchdog timer mode |
| Clock source | Pϕ, Pϕ/64, Pϕ/128, Pϕ/256, Pϕ/512, Pϕ/1024, Pϕ/4096, Pϕ/16384<br>Pϕ: Clock for on-chip peripheral modules |
| Method of activation | Watchdog timer/interval timer: Activated by software<br>Frequency adjustment: Activated by software<br>Exit from software standby mode: Interrupt detection |

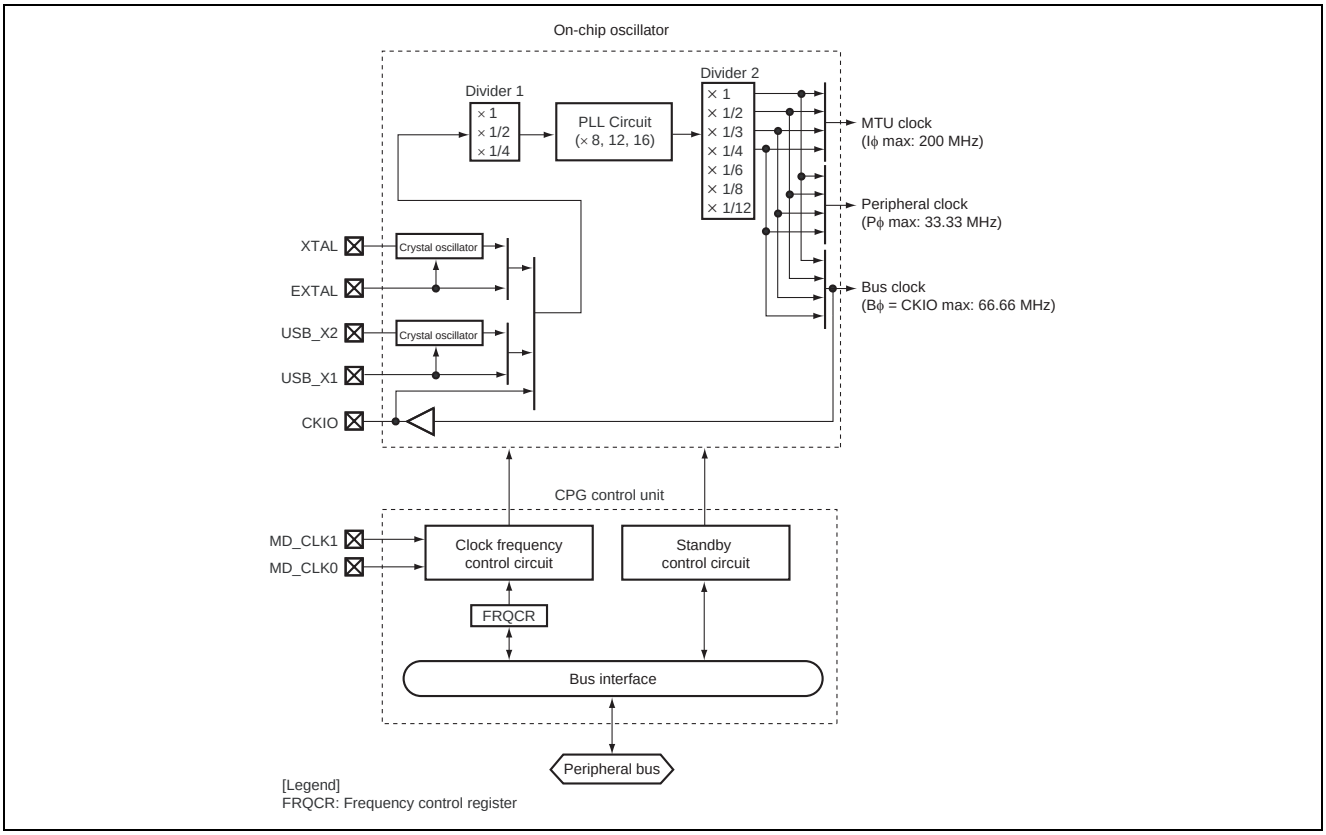



**Figure 1 Block Diagram of the CPG**

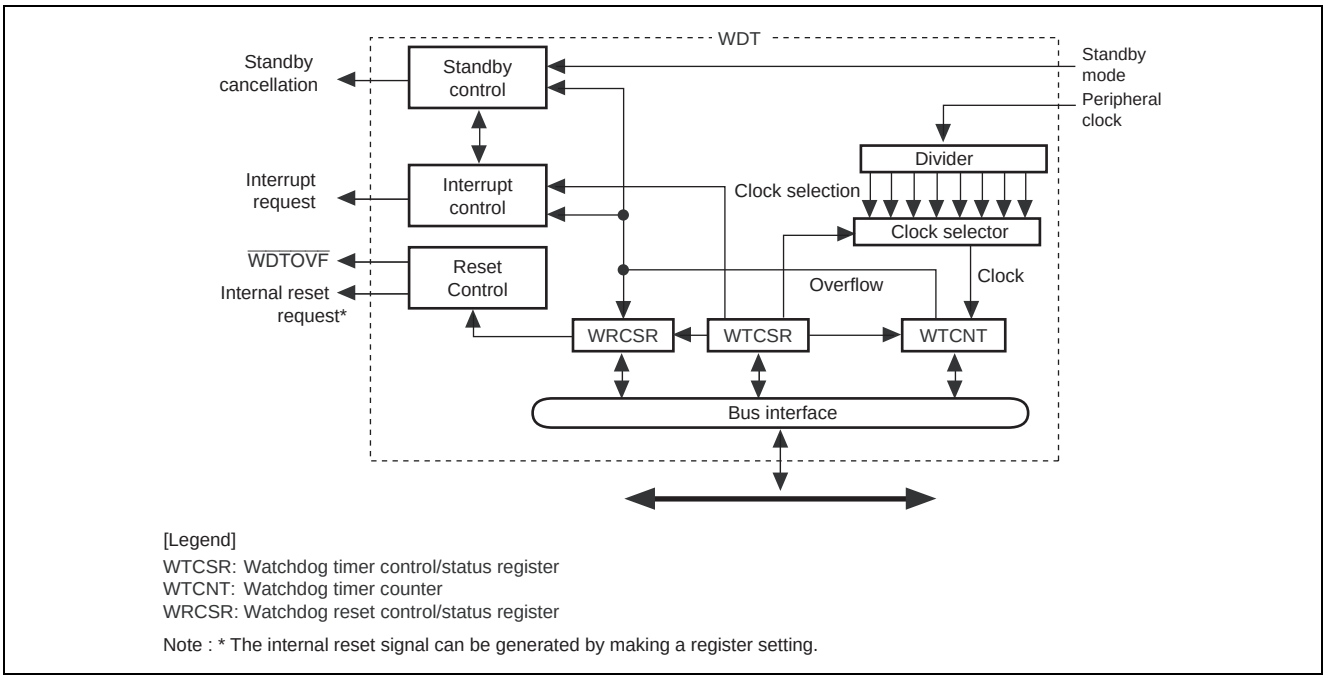
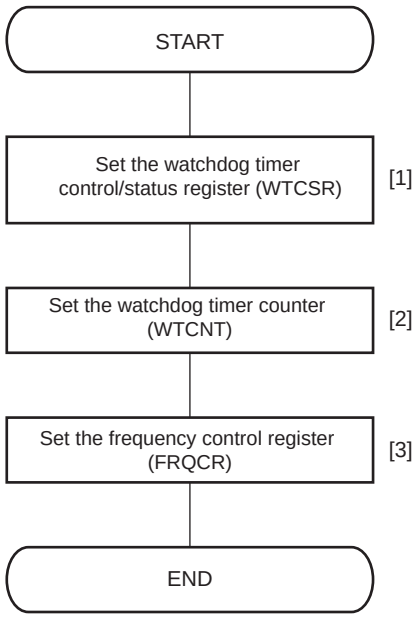



**Figure 2 Block Diagram of the WDT**

## 2.2 Procedure for Setting Modules Used

Figure 3 shows the procedure for settings to change the operating frequencies. For details on registers, refer to the *SH7263/SH7203 Group Hardware Manual*.




[1] Setting of the watchdog timer control/status register (WTCSR)
- Clear theTME (timer enable) bit to 0.
  [Function] Stops the timer.
  TME should be cleared to 0 if the WDT is to be used on exit from software standby mode or when the clock frequency is changed.
- Set the CKS (clock select) bit
  [Function] Selects from Pϕ to Pϕ/16384 as the counter clock signal

[2] Setting of the watchdog timer counter (WTCNT)
[Function] Up-counter

[3] Setting of the frequency control register (FRQCR)
- Set the STC (the frequency multiplication ratio of the PLL circuit) bits
  [Function] Selects a factor from ×8 to ×16 as the frequency multiplication ratio of the PLL circuit
- Set the IFC (internal clock frequency division ratio) bit
  [Function] Specifies a frequency division ratio of ×1 to ×1/2 for the internal clock with respect to the output frequency of the PLL circuit
- Set the PFC (peripheral clock frequency division ratio) bits
  [Function] Specifies a frequency division ratio from ×1/4 to ×1/12 for the peripheral clock with respect to the output frequency of the PLL circuit

**Figure 3 Example Flow for Settings to Change the Operating Frequency**

## 2.3 Description of the Sample Program

Table 3 gives the register settings to be used when the operating frequency is changed, and Table 4 shows the operating frequencies used in this sample program.

Figure 4 shows the operation timing of the sample program.

**Table 3 Register Settings for Changing the Operating Frequency**

| Register Name | Address | Setting | Description |
|---|---|---|---|
| Watchdog timer control/status register (WTCSR) | H'FFFE 0000 | H'A51E | TME = 0 Timer is disabled<br>CKS = [2:0] = B'110 : 1/4096 × Pϕ<br>Overflow cycle (31.5 ms) |
| Watchdog timer counter (WTCNT) | H'FFFE 0002 | H'5AAD | Set the count value so that the oscillation stabilization time becomes 10 ms or more.<br>(H'100 – H'AD) × (1/4096 × Pϕ) = 10.20 ms |
| Frequency control register (FRQCR) | H'FFFE 0010 | H'1104 | STC[1:0] = B'01 : ×12 (multiplication ratio for the PLL circuit)<br>IFC = 0 : ×1 (frequency division ratio for the internal clock)<br>PFC[2:0] = B'100 : × 1/6 (frequency division ratio for the peripheral clock) |

**Table 4 Operating Frequencies Set by the Sample Program**

| | Clock Operating Mode | FRQCR Setting | Clock Ratio (I:B:P) | Operating Frequencies (I:B:P) |
|---|---|---|---|---|
| Initial operating frequency | Mode 0 | H'0003 | 8:4:2 | 133 MHz : 66 MHz : 33 MHz |
| Operating frequency after change | Mode 0 | H'1104 | 12:4:2 | 200 MHz : 66 MHz : 33 MHz |

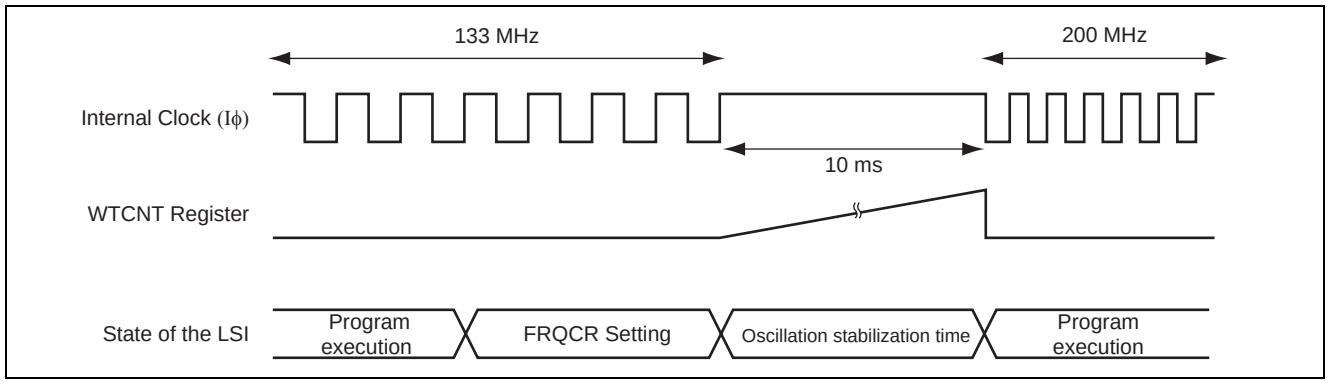



**Figure 4 Operation Timing of Sample Program**

## 3. Listing of the Sample Program

1. Sample Program Listing: cpg.c (1)

```
 1 /*""FILE COMMENT""*******************************************************************************
 2 *
 3 *   System Name: SH7203 Sample Program
 4 *   File Name  : cpg.c
 5 *   Version    : 1.00.00
 6 *   Contents   : CPG setting process
 7 *   Model      : M3A-HS30
 8 *   CPU        : SH7203
 9 *   Compiler   : SHC9.1.1.0
10 *   OS         : none
11 *
12 *   Note       :*
13 *                 <Caution>
14 *                 This sample program is for reference
15 *                 and its operation is not guaranteed.
16 *                 Customers should use this sample program for technical reference
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18 *
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24 *   Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
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26 *
27    history      :2007.11.13  ver.1.00.00
28 *""FILE COMMENT END""*******************************************************************************/
29 #include “iodefine.h”
30
31 /* ==== Prototype Declaration ==== */
32 void io_set_cpg(void);
33
```

2. Sample Program Listing: cpg.c (2)

```
/*""FUNC COMMENT""*****************************************************************************
* ID            :
* Outline       : CPG settings
*-----------------------------------------------------------------------------------------------
* Include       : #include “iodefine.h”
*-----------------------------------------------------------------------------------------------
* Declaration   : void io_set_cpg(void);
*-----------------------------------------------------------------------------------------------
* Function      : Clock pulse generator (CPG) is set to the internal clock
                : (I Clock), peripheral clock (P Clock), bus clock (B Clock), and
                : I Clock = 200MHz, B Clock = 66.66MHz, P Clock = 33.3MHz
*-----------------------------------------------------------------------------------------------
* Argument      : None
*-----------------------------------------------------------------------------------------------
* Return Value  : None
*-----------------------------------------------------------------------------------------------
* Notice         : This setting example is the case that the function’s input clock
                 : is 16.67MHz and clock mode is 0.
*""FUNC COMMENT END""*************************************************************************/
void io_set_cpg(void)
{
   /* ==== CPG Setting ==== */
   WDT.WTCSR.WORD = 0xa51e;              /* WDT Clock select  */
                                         /* 1/4096xP-phy (33.3MHz)  */
   WDT.WTCNT.WORD = 0x5aad;              /* Initial value of Counter: D’173 10mS  */
   CPG.FRQCR.WORD = 0x1104;
        /* PLL1 (x12), I:B:P=12:4:2
        * CKIO:Output at time usually, Output when bus right is opened, output at standby“L”
        * Clockin = 16.67MHz, CKIO = 66.6MHz
        * I Clock = 200MHz, B Clock = 66.66MHz,
        * P Clock = 33.3MHz
        */
   /* ---- The clock of all modules is permitted. ---- */
        CPG.STBCR3.BYTE = 0x00;
        CPG.STBCR4.BYTE = 0x08;
        CPG.STBCR5.BYTE = 0x00;
        CPG.STBCR6.BYTE = 0x02;

}

/* End of File */
```

## 4. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7203 Group Hardware Manual
  SH7263 Group Hardware Manual
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