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SH7206 Group

Example of Cache Memory Setting

Introduction

This application note describes an example of cache-function settings for the SH7206.

Target Device

SH7206

Contents

1. Overview

1.1 Specifications

The instruction cache and operand cache are enabled and placed in the write-back mode.

1.2 Modules Used

Instruction cache and operand cache

1.3 Applicable Conditions

- MCU: SH7206 (R5S72060)
- Operating frequencies: Internal clock at 200 MHz
  Bus clock at 66.67 MHz
  Peripheral clock at 33.33 MHz
- C compiler: Manufactured by Renesas Technology Corp.
  Version 9.00 C/C++ compiler package for the SuperH RISC engine Family
- Compiler options: Default settings of the High-performance Embedded Workshop (-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Operation of the sample program in this application note has been confirmed with the setting conditions given in the application note *Example of SH7206 Initial Configuration.* Please refer to that document when setting up this sample task.

2. Description of Application Example

The instruction cache and operand cache are used in this sample task.

2.1 Functions Used: Overview of Operation

If the instruction cache and operand cache are enabled (respectively, when the ICE and OCE bits in register CCR1 are set to 1), whenever an instruction or data in a cache-enabled area is accessed, the cache is searched to see if the desired instruction or data is in the cache. The cache is searched according to the following procedure.

1. A single entry is selected by using bits 10 to 4 of the address used to access memory and the tag addresses at the corresponding entry number in all four ways are read. At this time, the highest-order three bits of the tag address are always clear (0).
2. Bits 31 to 11 of the address used to access memory are compared with the read tag address. Address comparison is with the tag addresses read out from the entries in all four ways.
3. When the comparison shows a match and the selected entry is valid (V = 1), a cache hit is said to have occurred. When the comparison does not show a match or the selected entry is not valid (V = 0), a cache miss is said to have occurred.
4. When the cache is hit, the long-word (LW) of data at the position in the data array defined by bits 3 and 2 of the accessed address is read or written.

Table 1 Overview of the Caches

Item	Overview
Capacity	Instruction cache: 8 Kbytes Operand cache: 8 Kbytes
Structure	Instructions and data are separated; each cache is 4-way set associative
Cache lock function	Ways 2 and 3 can be locked (only in the operand cache)
Line size	16 bytes
Number of entries/ways	128
Write system	Write-back and write-through methods are selectable.
Replacement method	Least-recently-used (LRU) algorithm

Note: Please refer to the section ‘Cache’ in the *SH7206 Group Hardware Manual* for details on the caches.

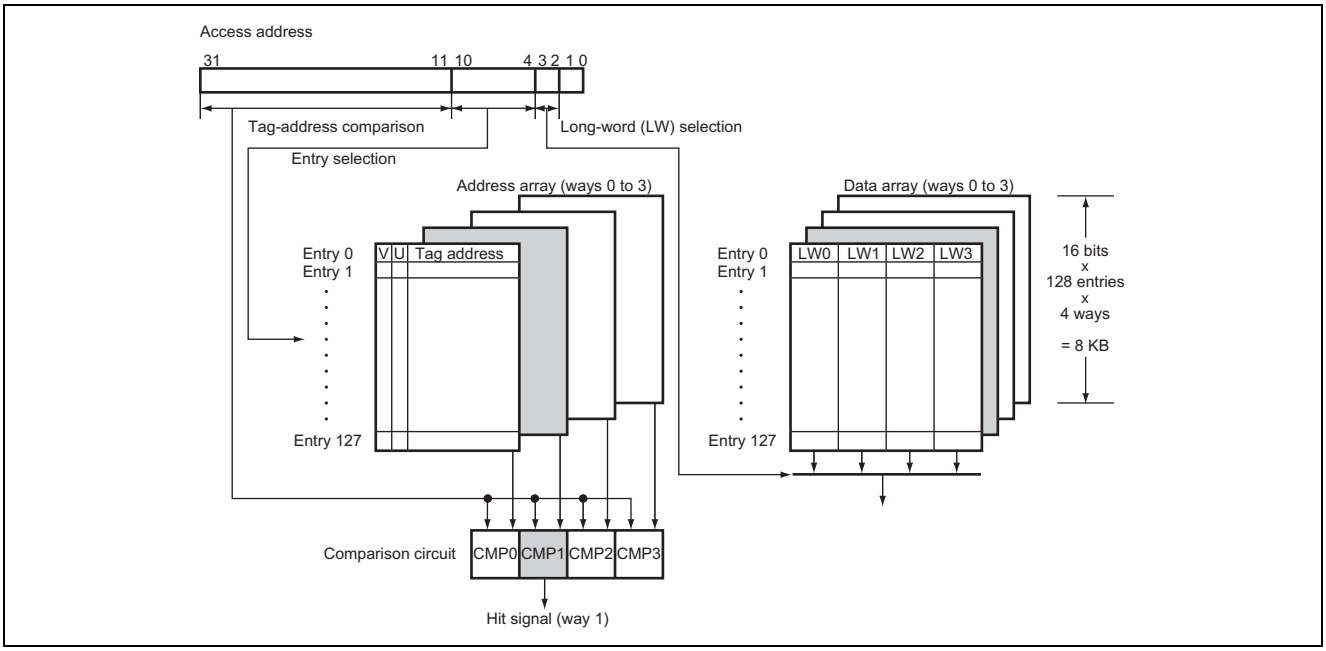


Figure 1 Overview of the Cache-Search Scheme

2.2 Procedure for Setting Up the Functions

The procedure for setting up the caches is described below.

Cache control register 1 (CCR1) is used to select the cache mode. Once CCR1 has been set, areas for which caching has been enabled must be accessed after the CCR1 register has been read so that such areas are not accessed while the cache mode is updated. Also, program code that manipulates the cache control registers must be executed from an area for which caching is disabled.

Figure 2 is a flow chart showing an example of the procedure used to enable both the instruction cache and operand cache.

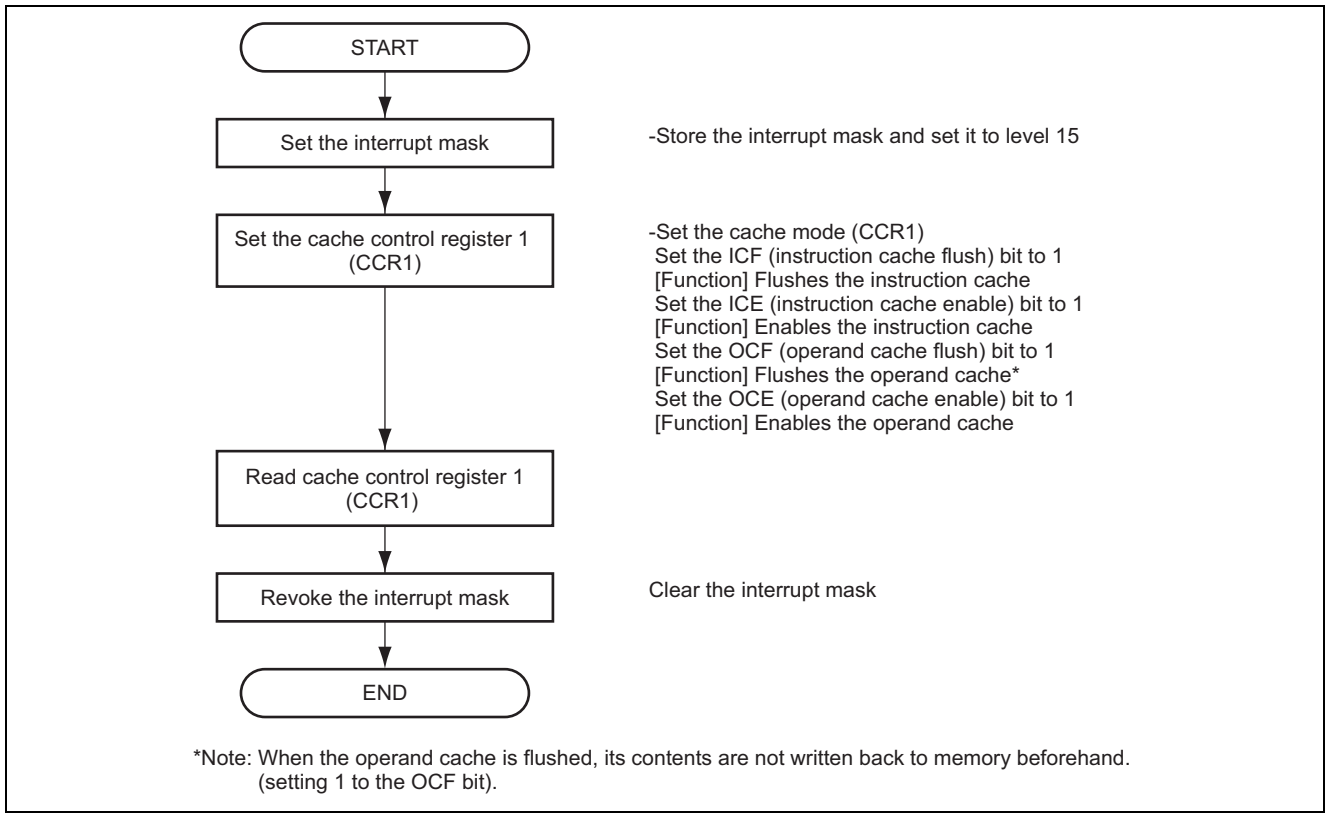


Figure 2 Example Flow for Setting Up the Cache

2.3 Operation of the Sample Program

In the sample program, the instruction cache and operand cache are enabled with operation in the write-back mode. At this time, a single line of cache memory is filled. Since the operand cache is enabled (the write-back mode) for the target region of memory, the data is actually written to the cache memory. That is, the data is not reflected in the external memory (SDRAM).

The section name of the cache manipulation function is changed so that this function is placed in a cache-disabled space.

2.4 Procedure for Processing by the Sample Program

Table 2 describes how the cache is set up by the sample program, and table 3 describes macro definitions used in the sample program. Figure 3 is a flow chart of processing by the sample program.

Table 2 Cache Settings

Name of Register	Address	Setting Value	Function
Cache control register 1 (CCR1)	H'FFFC 1000	H'0000 0909	-ICF = 1: Instruction cache flush -ICE = 1: Instruction cache enable -OCF = 1: Operand cache flush -OCE = 1: Operand cache enable Note: ICF and OCF are always read as 0.

Table 3 Cache-Related Macro Definitions in the Sample Program

Macro Definition	Value Represented	Function as Setting for CCR1
CACHE_OFF	H'0000	Turns the cache off
CACHE_I_FLUSH	H'0800	Instruction cache flush
CACHE_I_ON	H'0100	Instruction cache enable
CACHE_O_FLUSH	H'0001	Operand cache flush
CACHE_O_ON	H'0008	Operand cache enable
CACHE_O_WT	H'0002	Operand cache write-through mode

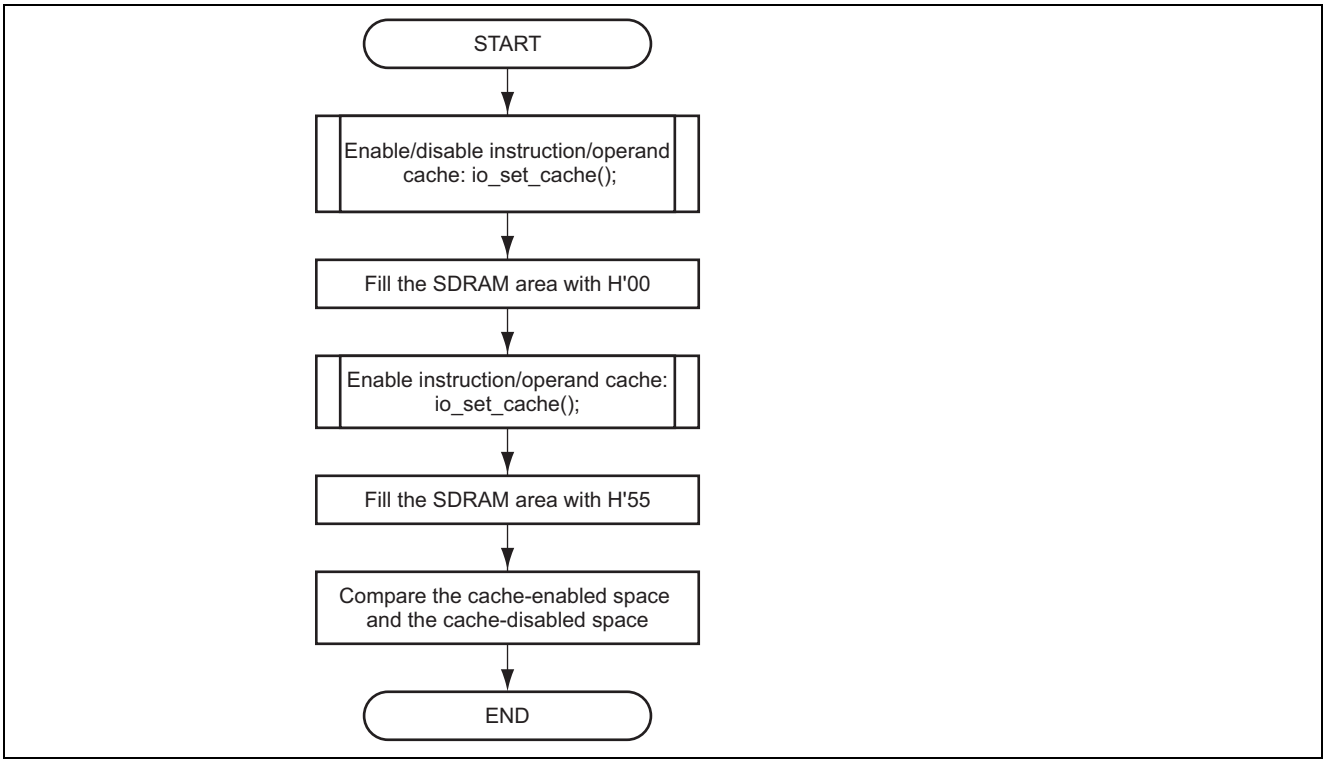


Figure 3 Flow of Processing by the Sample Program

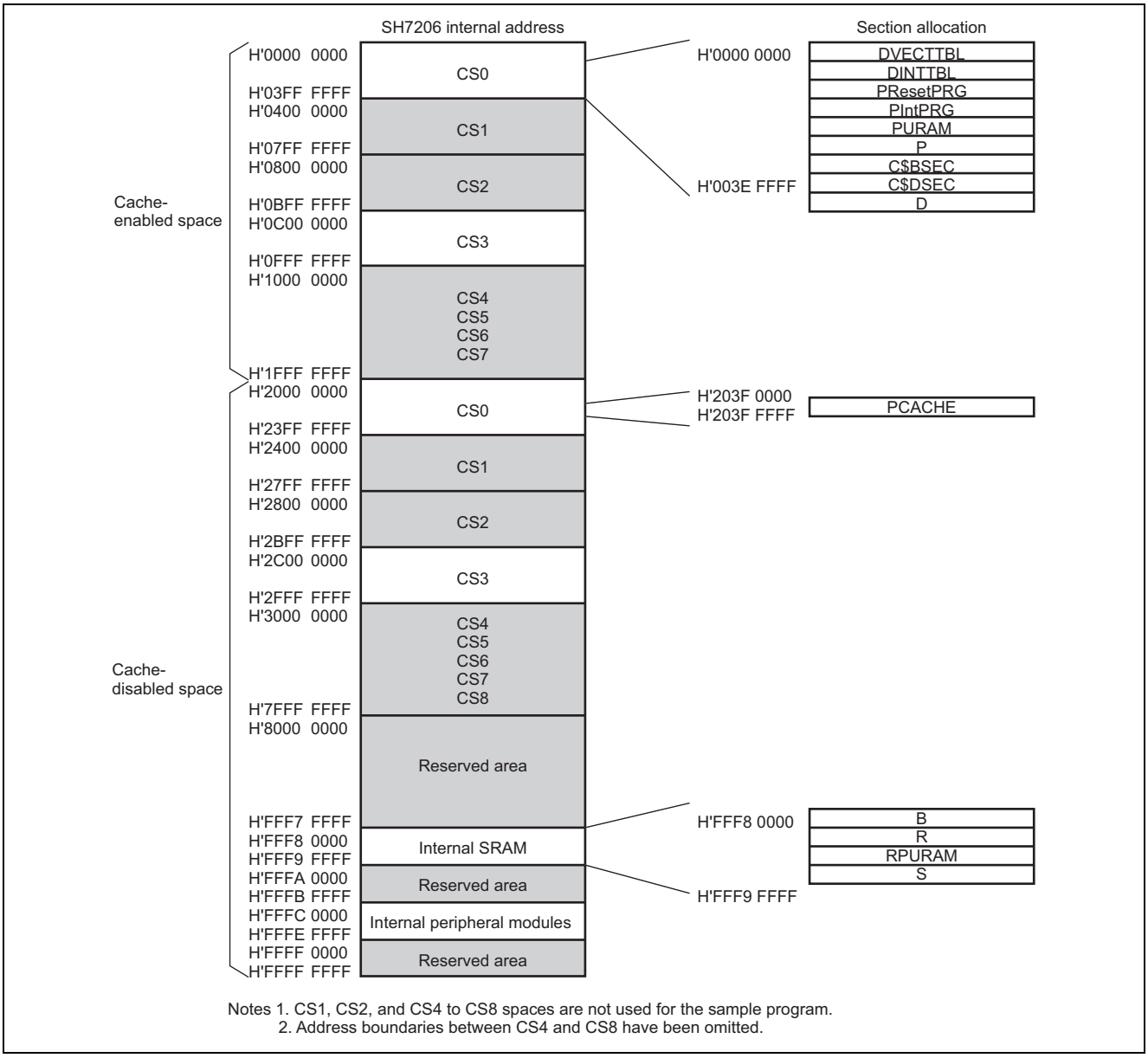
2.5 Allocation of Sections in the Sample Program

The #pragma section directive is used with the corresponding extended compiler function to set a section name for the function that actually manipulates the cache control registers.

In the sample program, the area for program code of the io_set_cache function is set to the PCACHE section. Only this part of the program is allocated to a cache-disabled space of the SH7206. That is, the rest of the program is allocated to a space where caching is performed if it is enabled (the P section).

Section allocation is specified by the linker editor options.

Figure 4 is a memory map for the sample program.



Notes 1. CS1, CS2, and CS4 to CS8 spaces are not used for the sample program.
2. Address boundaries between CS4 and CS8 have been omitted.

Figure 4 Memory Map for the Sample Program

3. Sample Program

- Sample Program: Listing of “main.c” (1)

```
1     /*""FILE COMMENT""*****************************************************/
2     *
3     *       System Name : SH7206 Sample Program
4     *       File Name   : cache.c
5     *       Version     : 1.00.00
6     *       Contents    : Example of setting the main cache register
7     *       Model       : M3A-HS60
8     *       CPU         : SH7206
9     *       Compiler    : SHC9.0.00
10    *       OS          : None
11    *
12    *       Note        : Sample program to confirm the cache operation.
13    *
14    *                     <Caution>
15    *                     This entire sample program is for reference only and
16    *                     its operation is not guaranteed.
17    *                     Please use this sample as a technical reference
18    *                     in software development.
19
20    *       Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
21    *       AND Renesas Solutions Corp. All Rights Reserved
22    *
23    *       History   : 2004.10.28 ver.0.01.00
24    *""FILE COMMENT END""*************************************************/
25    #include <machine.h>
26    #include "iodefine.h"    /* iodefine.h is automatically generated by the High-
27                                performance Embedded Workshop.                 */
28
29    /* ==== Macro definitions ==== */
30    /* ---- Cache settings ---- */
31    #define CACHE_OFF      0x0000u
32    #define CACHE_I_FLUSH    0x0800u
33    #define CACHE_I_ON     0x0100u
34    #define CACHE_O_FLUSH    0x0008u
35    #define CACHE_O_ON     0x0001u
36    #define CACHE_IO_ON    (CACHE_I_ON | CACHE_O_ON)
37    #define CACHE_O_WT     0x0002u
38
39    /* ---- SDRAM area addresses ---- */
40    #define SDRAM_ADDR1 (unsigned char *)(0x0c000000)   /* Cache-enabled area   */
41    #define SDRAM_ADDR2 (unsigned char *)(0x2c000000)   /* cache-disabled area  */
42
43
44    /* ==== Prototype declaration ==== */
45    void main(void);
46    int io_set_cache(unsigned int mode);
```

- Sample Program: Listing of “main.c” (2)

```
47    /*""FUNC COMMENT""*************************************************************
48    * ID                 :
49    * Overview of module : Sample program main (example of using cache memory)
50    *------------------------------------------------------------------------------
51    * Include            :
52    *------------------------------------------------------------------------------
53    * Declaration        : void main(void)
54    *------------------------------------------------------------------------------
55    * Functions          : Sample of enabling/disabling cache memory.
56    *                    : After the SDRAM area has been initialized with the
57    *                    : operand cache OFF, a fill operation is performed with
58    *                    : the operand cache ON and the cached area is compared
59    *                    : with its shadow in the cache-disabled space.
60    *------------------------------------------------------------------------------
61    * Argument           : None
62    *------------------------------------------------------------------------------
63    * Return value       : None
64    *------------------------------------------------------------------------------
65    * Caution      : In this sample program, the cache is flushed. Therefore,
66    *              : when the cache is enabled by a program for initialization,
67    *              : content of cache will be invalidated.
68    *""FUNC COMMENT END""*********************************************************/
69    void main(void)
70    {
71    int i;
72    unsigned char *ptr1,*ptr2;
73
74    /* ==== Disabling instruction and operand caches ==== */
75    io_set_cache(CACHE_OFF | CACHE_I_FLUSH | CACHE_O_FLUSH);
76
77    /* ==== Filling SDRAM area with 0x00 ==== */
78    ptr1 = SDRAM_ADDR1;
79    for(i=0; i < 16 ; i++){
80         *ptr1++ = 0;
81    }
82
```

- Sample Program: Listing of “main.c” (3)

```
83    /* ==== Enabling instruction/operand cache ==== */
84    io_set_cache(CACHE_I_ON | CACHE_O_ON | CACHE_I_FLUSH | CACHE_O_FLUSH);
85
86    /* ==== Filling SDRAM area with 0x55 ==== */
87    ptr1 = SDRAM_ADDR1;
88    for(i=0; i < 16 ; i++){
89         *ptr1++ = 0x55;
90    }
91
92    /* ==== Comparing cache-enabled and cache-disabled spaces   ==== */
93    ptr1 = SDRAM_ADDR1;      /* Cache-enabled space  */
94    ptr2 = SDRAM_ADDR2;      /* Cache-disabled space */
95
96    for(i=0; i < 16; i++){
97         if(*ptr1++ == *ptr2++){
98            while(1){
99               /* Error in operand-cache setting */
100           }
101        }
102   }
103
104   while(1){
105        /* Program end */
106   }
107
108   }
```

- Sample Program: Listing of “main.c” (4)

```
109  #pragma section CACHE    /* Allocated in the CS0 shadow area*/
110  /*""FUNC COMMENT""*******************************************************
111  *ID                :
112  * Overview of module: Cache setting
113  *------------------------------------------------------------------------
114  * Include           : #include "iodefine.h"
115  *------------------------------------------------------------------------
116  * Declaration       : int io_set_cache(unsigned int mode)
117  *------------------------------------------------------------------------
118  * Function          : Cache is set in the mode specified by argument mode
119  *                   :
120  *------------------------------------------------------------------------
121  * Argument   : unsigned int mode: Combos of the following modes are obtained
122  *          by logical OR: CACHE_I_FLUSH : Instruction cache flush
123  *            :          : CACHE_I_ON    : Instruction cache enable
124  *            :          : CACHE_O_FLUSH : Operand cache flush
125  *            :          : CACHE_O_ON    : Operand cache enable
126  *            :          : CACHE_IO_ON   : Instruction/operand cache ON
127  *            :          : CACHE_O_WT    : Write-through mode
128  *            :          : CACHE_OFF     : Instruction/operand cache disable
129  *------------------------------------------------------------------------
130  * Return value          : 0             : Normally finished
131  *------------------------------------------------------------------------
132  * Caution               :
133  *""FUNC COMMENT END""*****************************************************/
134  int io_set_cache(unsigned int mode)
135  {
136  volatile unsigned long reg;
137  int mask;
138
139  /* ==== Setting interrupt mask ==== */
140  mask = get_imask();
141  set_imask(15);            /* Set to level 15 */
142
143  /* ==== Setting cache register ==== */
144  CCNT.CCR1.LONG = mode;
145
146  /* ==== Reading cache register ==== */
147  reg = CCNT.CCR1.LONG ;
148
149  /* ==== Canceling interrupt mask ==== */
150  set_imask(mask);          /* Set to the original level */
151
152  return 0;
153  }
154
155  /* End of file */
```

4. Documents for Reference

- Software manual
  SH-2A SH2A-FPU Software Manual Rev.3.00
  If you don't already have it, please download the latest version from the homepage of Renesas Technology Corp.

- Hardware manual
  SH7206 Group Hardware Manual Rev.1.00
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