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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

Eight-Digit BCD Division (DIVD)

Introduction

Divides one eight-digit BCD (binary coded decimal) number by another, and places the result of division (eight-digit BCD) in general registers.

Target Device

H8/300H Tiny Series

Contents

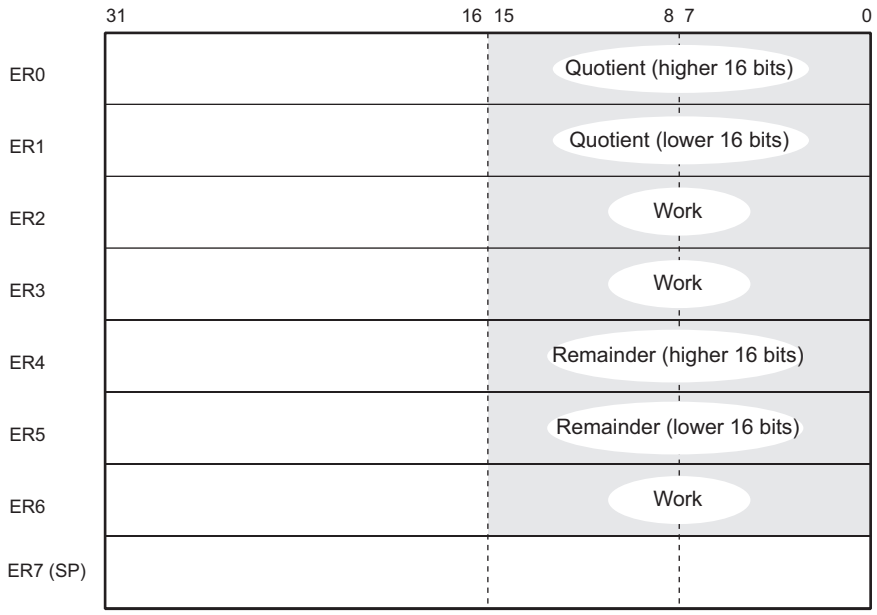
1. Function

1. Divides one eight-digit BCD (binary coded decimal) number by another, and sets the result (eight BCD digits) in general registers.
2. The arguments are all unsigned integers.
3. Data operations are entirely within the general registers.

2. Arguments

Contents		Storage Location	Data Length (Bytes)
Input	Dividend	R0, R1	4
	Divisor	R2, R3	4
Output	Result (quotient)	R0, R1	4
	Result (remainder)	R4, R5	4
	Occurrence of divide-by-zero error	Z flag (CCR)	—

3. Changes to Internal Registers and Flags



I	UI	H	U	N	Z	V	C
–	–	↕	–	↕	↕	↕	↕

–: No change
↕: Varies
0: Fixed to 0
1: Fixed to 1

4. Programming Specifications

Program memory (bytes)
84
Data memory (bytes)
0
Stack (bytes)
0
Number of cycles
1162
Re-entrant
Yes
Relocatable
Yes
Interrupts during execution
Yes

5. Note

The number of cycles in the programming specifications is that required to calculate 99999999/9999.

6. Description

6.1 Description of Functions

1. The arguments are as follows.
   R0: Set the higher-order four digits (32 bits) of the eight-digit BCD dividend here. The higher-order four digits of the eight-digit BCD result (quotient) are placed here by the execution of the DIVD subroutine.
   R1: Set the lower-order four digits of the dividend here. The lower-order four digits of the quotient are placed here by the subroutine.
   R2: Set the higher-order four digits of the eight-digit BCD divisor here.
   R3: Set the lower-order four digits of the divisor here.
   R4: The higher-order four digits of the eight-digit BCD remainder are placed here as an output argument.
   R5: The lower-order four digits of the remainder are placed here.
   Z flag (CCR): Indicates the occurrence of an error (division by 0).
   Z flag = 1: Indicates that the divisor is zero.
   Z flag = 0: Indicates that the divisor is non-zero.

2. The following figure illustrates the execution of the DIVD subroutine. With the input arguments set as shown, a DIVD call places the results of division in R0, R1, R4, and R5.

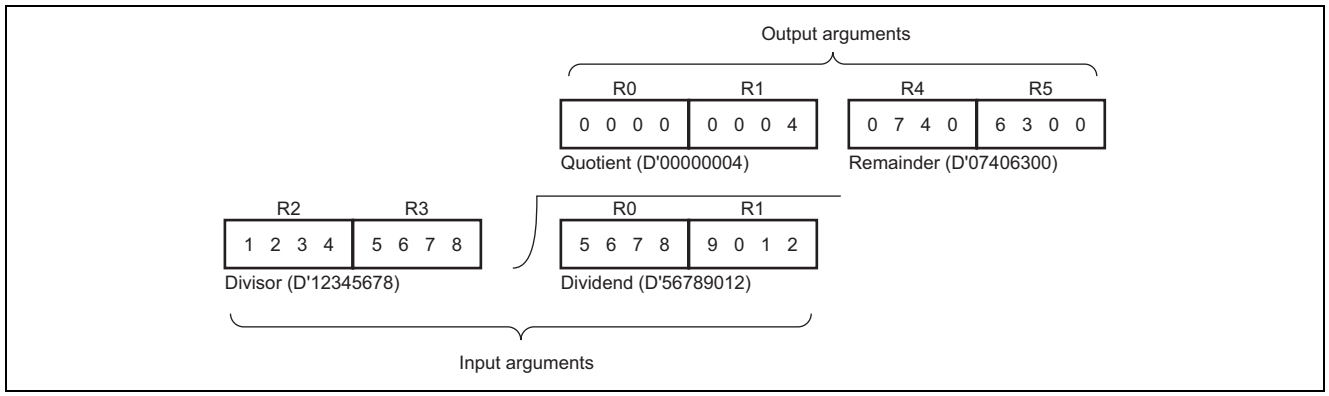


Figure 1 Example of DIVD Execution

3. Table 1 shows the results when "0" is set as an input argument.

Table 1 Results When "0" Is Set As an Input Argument

Input Arguments		Output Arguments		
Dividend (R0, R1)	**Divisor (R2, R3)**	**Quotient (R0, R1)**	**Remainder (R4, R5)**	**Error (Z)**
H'********	H'00000000	H'********	H'00000000	1
H'00000000	H'********	H'00000000	H'00000000	0
H'00000000	H'00000000	H'00000000	H'00000000	1

Note: H'**** indicates a hexadecimal number.

6.2 Usage Notes

1. Any higher-order digit of an input argument that is not to be used must be explicitly set to “0”. Otherwise, the result may not be correct because of the undefined data in the higher-order digits.
   Example: To divide 567890 (dividend) by 23410 (divisor), the higher-order two digits of the dividend should be set to 0 and the higher-order three digits of the divisor should be set to 0, as is shown in the figure below.

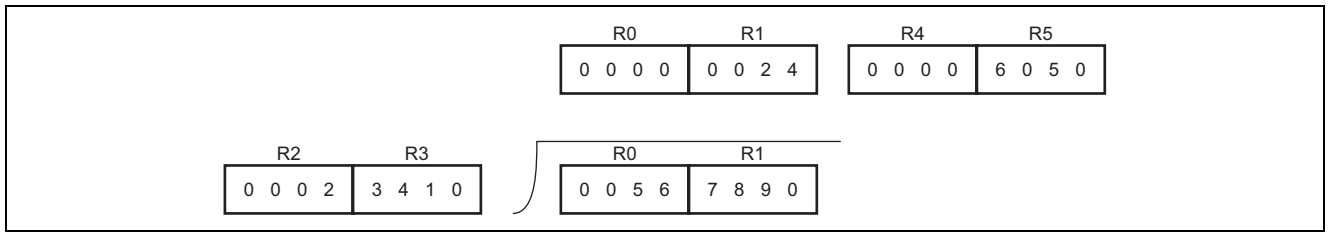


Figure 2 Division When Higher-order Digits are not Used

2. Since the quotient is set in R0 and R1, the dividend is lost in the execution of DIVD. When you will still require the dividend, save it elsewhere in memory beforehand.

6.3 Description of Data Memory

No data memory is used by DIVD.

6.4 Example of Usage

```
WORK1   . RES. W 2          ..... Reservation of the data memory area for setting of the 8-digit BCD dividend by the user program.
WORK2   . RES. W 2          ..... Reservation of the data memory area for setting of the 8-digit BCD divisor by the user program.
WORK3   . RES. W 2          ..... Reservation of the data memory area that will hold the 8-digit BCD quotient for the user program.
WORK4   . RES. W 2          ..... Reservation of the data memory area that will hold the 8-digit BCD remainder for the user program.
            .
            .
            .
        MOV. W @WORK1, R0   ..... Sets the 8-digit BCD dividend specified by the user program.
        MOV. W @WORK1+2, R1
        MOV. W @WORK2, R2   ..... Sets the 8-digit BCD divisor specified by the user program.
        MOV. W @WORK2+2, R3
        JSR    @DIVD        ..... Subroutine call of DIVD.
        BEQ.   ERROR        ..... When an error occurs after the result of division, branches to processing routine.
        MOV. W R0, @WORK3   ..... Transfers the result from the output argument to the data memory of the user program.
        MOV. W R1, @WORK3+2
        MOV. W R4, @WORK4
        MOV. W R5, @WORK4+2
            .
            .
            .
ERROR   Divide-by-0 process routine
```

6.5 Principles of Operation

1. Decimal division is done by repeated subtraction. The following figure shows an example of division (64733088/5).

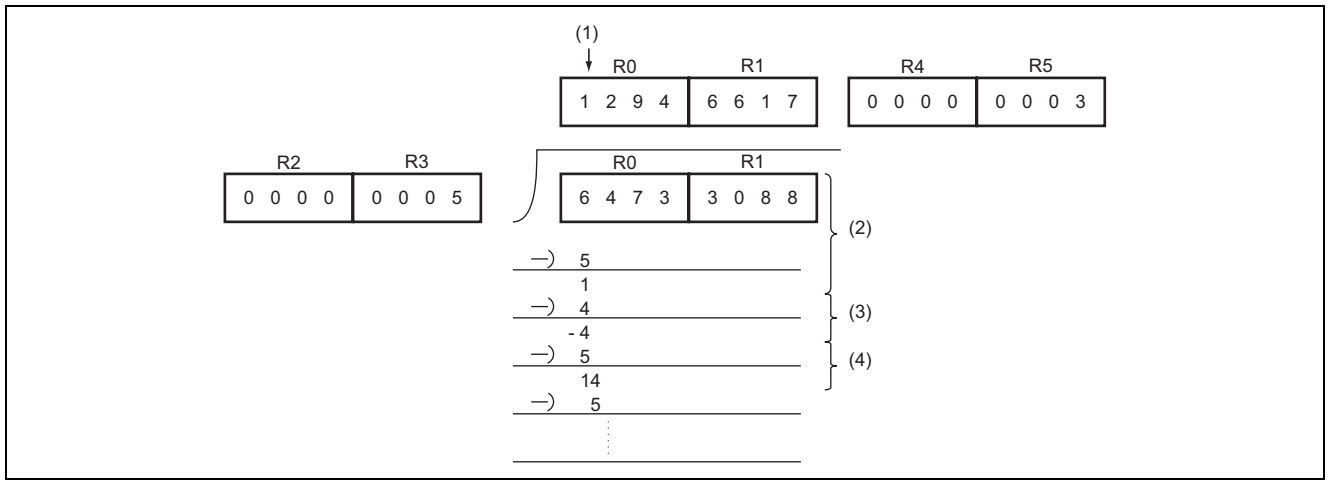
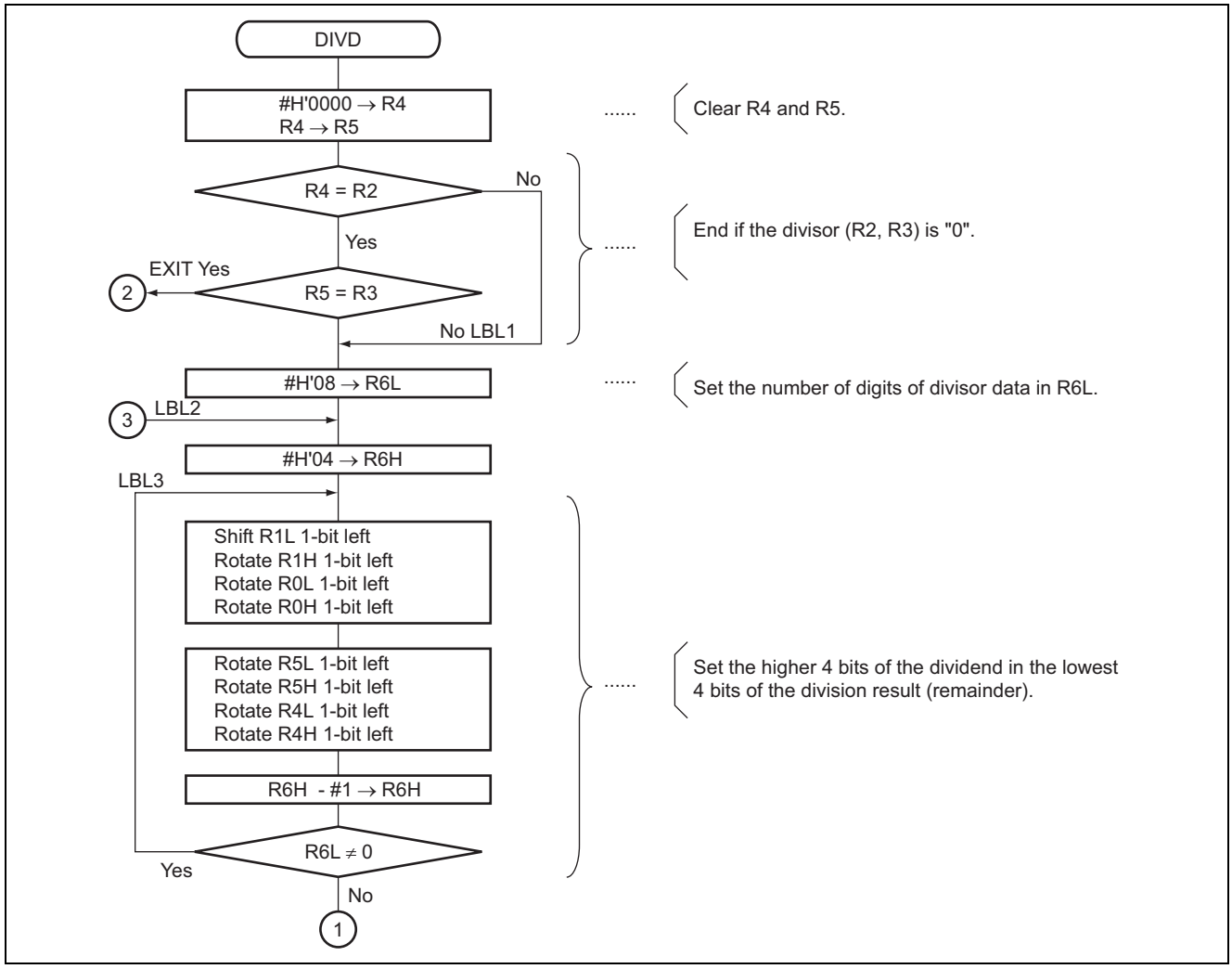
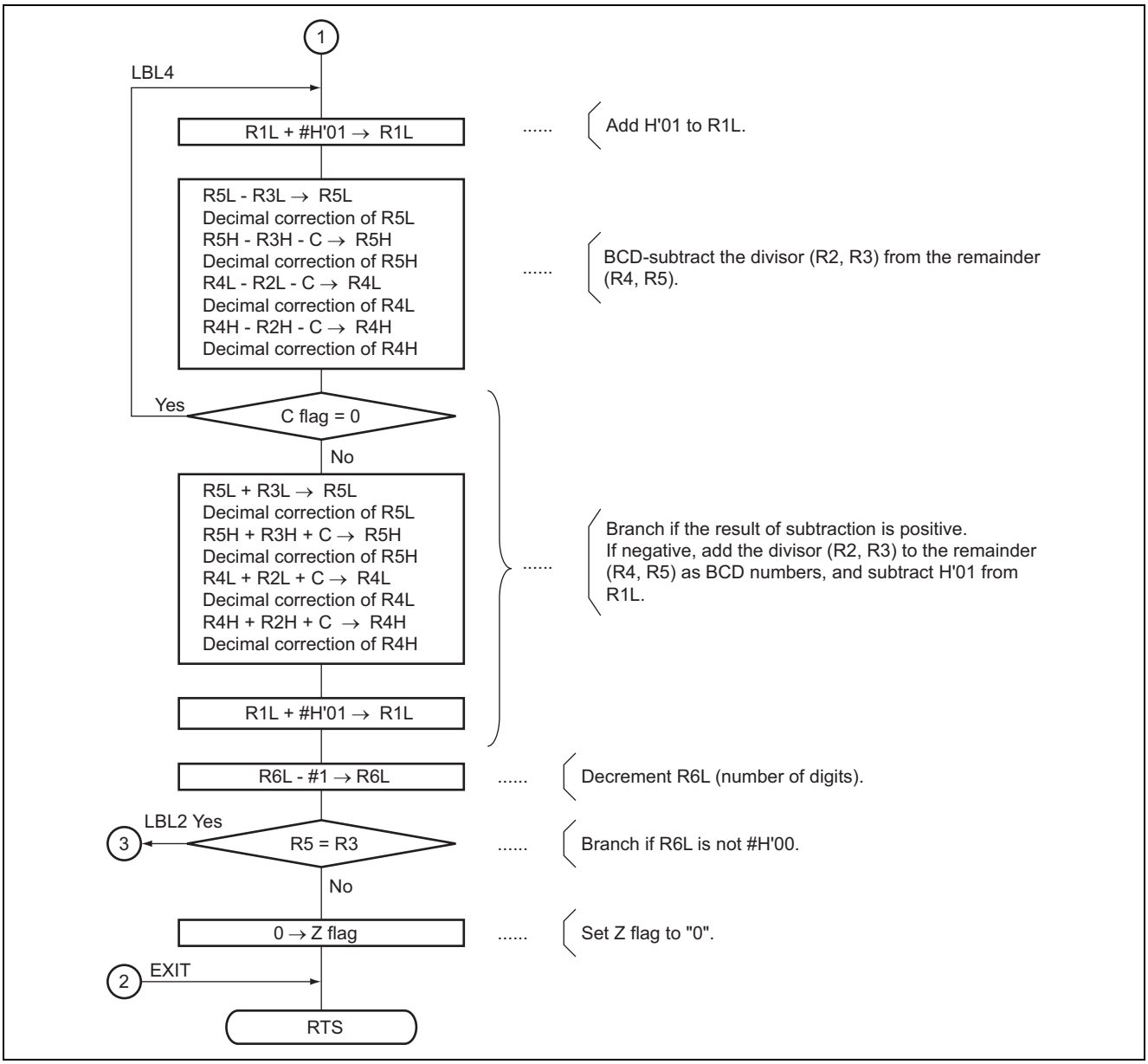


Figure 3 Division (64733088/5)

2. Details of the program are given below.
   1) The divisor is shifted four bits (one BCD digit) leftward, and the higher-order four bits of the dividend are placed in the lower-order BCD digit of the registers used to store the remainder.
   2) The divisor is subtracted from the dividend digit in the remainder registers and this is repeated until subtraction yields a negative result; the number of successful subtractions is then set in the lower-order four bits (least significant digit) of the register for storage of the dividend ((2) → (3) → (1) in the figure above). When the result of subtraction is negative, the divisor is added to the remainder digit to restore it to its value before the last subtraction (i.e., the actual remainder) ((4) in figure 3).
   3) Steps 1) and 2) are repeated eight times (the number of digits).

7. Flowchart


DIVD
#H'0000 → R4
R4 → R5
.....
Clear R4 and R5.
R4 = R2
No
Yes
EXIT Yes
2
R5 = R3
No LBL1
.....
End if the divisor (R2, R3) is "0".
#H'08 → R6L
.....
Set the number of digits of divisor data in R6L.
3
LBL2
#H'04 → R6H
LBL3
Shift R1L 1-bit left
Rotate R1H 1-bit left
Rotate R0L 1-bit left
Rotate R0H 1-bit left
Rotate R5L 1-bit left
Rotate R5H 1-bit left
Rotate R4L 1-bit left
Rotate R4H 1-bit left
.....
Set the higher 4 bits of the dividend in the lowest 4 bits of the division result (remainder).
R6H - #1 → R6H
R6L ≠ 0
Yes
No
1


1
LBL4
R1L + #H'01 → R1L
R5L - R3L → R5L
Decimal correction of R5L
R5H - R3H - C → R5H
Decimal correction of R5H
R4L - R2L - C → R4L
Decimal correction of R4L
R4H - R2H - C → R4H
Decimal correction of R4H
Yes
C flag = 0
No
R5L + R3L → R5L
Decimal correction of R5L
R5H + R3H + C → R5H
Decimal correction of R5H
R4L + R2L + C → R4L
Decimal correction of R4L
R4H + R2H + C → R4H
Decimal correction of R4H
R1L + #H'01 → R1L
R6L - #1 → R6L
LBL2 Yes
3
R5 = R3
No
0 → Z flag
2
EXIT
RTS
.....
Add H'01 to R1L.
.....
BCD-subtract the divisor (R2, R3) from the remainder (R4, R5).
.....
Branch if the result of subtraction is positive.
If negative, add the divisor (R2, R3) to the remainder (R4, R5) as BCD numbers, and subtract H'01 from R1L.
.....
Decrement R6L (number of digits).
.....
Branch if R6L is not #H'00.
.....
Set Z flag to "0".

8. Program Listing

```
 1                          1  ;*************************************************************
 2                          2  ;*                                                           *
 3                          3  ;*          NAME : MULTIPLE-PRECISION DECIMAL DIVISION       *
 4                          4  ;*                 (DIVD)                                    *
 5                          5  ;*                                                           *
 6                          6  ;*************************************************************
 7                          7  ;*                                                           *
 8                          8  ;*         ENTRY : R2,R3        (DIVISOR)                  *
 9                          9  ;*               : R0,R1        (DIVIDEND)                 *
10                         10  ;*                                                           *
11                         11  ;*        RETURN : R0,R1        (QUOTIENT)                 *
12                         12  ;*                 R4,R5        (REMAINDER)                *
13                         13  ;*                 Z flag of CCR (Z=1: FALSE,  Z=0: TRUE)  *
14                         14  ;*                                                           *
15                         15  ;*************************************************************
16                         16  ;
17                         17          .CPU        300HN
18  0000                   18          .SECTION    DIVD_code,CODE,ALIGN=2
19                         19          .EXPORT     DIVD
20                         20  ;
21        00000000         21  DIVD    .EQU        $           ;Entry point
22  0000 79040000          22          MOV.W       #H'0000,R4  ;Clear R4
23  0004 0D45              23          MOV.W       R4,R5       ;Clear R5
24  0006 1D42              24          CMP.W       R4,R2
25  0008 4604              25          BNE         LBL1        ;Branch if Z=0
26  000A 1D53              26          CMP.W       R5,R3
27  000C 4744              27          BEQ         EXIT        ;Branch to the exit if Z=1
28                         28  ;
29  000E                   29  LBL1
30  000E FE08              30          MOV.B       #H'08,R6L   ;Set bit counter
31  0010                   31  LBL2
32  0010 F604              32          MOV.B       #H'04,R6H   ;Set bit counter
33  0012                   33  LBL3
34  0012 1009              34          SHLL.B      R1L         ;Shift dividend
35  0014 1201              35          ROTXL.B     R1H
36  0016 1208              36          ROTXL.B     R0L
37  0018 1200              37          ROTXL.B     R0H
38  001A 120D              38          ROTXL.B     R5L
39  001C 1205              39          ROTXL.B     R5H
40  001E 120C              40          ROTXL.B     R4L
41  0020 1204              41          ROTXL.B     R4H
42  0022 1A06              42          DEC.B       R6H         ;Decrement bit counter2
43  0024 46EC              43          BNE         LBL3        ;Branch if Z=0
44  0026                   44  LBL4
45  0026 0A09              45          INC.B       R1L         ;Increment R1L
46  0028 18BD              46          SUB.B       R3L,R5L     ;R5L - R3L     -->R5L
47  002A 1F0D              47          DAS.B       R5L         ;Decimal adjust R5H
48  002C 1E35              48          SUBX.B      R3H,R5H     ;R5H - R3H - C -->R5H
49  002E 1F05              49          DAS.B       R5H         ;Decimal adjust R5H
50  0030 1EAC              50          SUBX.B      R2L,R4L     ;R4L - R2L - C -->R4L
51  0032 1F0C              51          DAS.B       R4L         ;Decimal adjust R4L
52  0034 1E24              52          SUBX.B      R2H,R4H     ;R4H - R2H - C -->R4H
```

```
 53   0036 1F04              53            DAS.B       R4H         ;Decimal adjust R4H
 54   0038 44EC              54            BCC         LBL4        ;Branch if C=0
 55                          55     ;
 56   003A 08BD              56            ADD.B       R3L,R5L     ;R3L + R5L     -->R5L
 57   003C 0F0D              57            DAA.B       R5L         ;Decimal adjust R5L
 58   003E 0E35              58            ADDX.B      R3H,R5H     ;R3H + R5H + C -->R5H
 59   0040 0F05              59            DAA.B       R5H         ;Decimal adjust R5H
 60   0042 0EAC              60            ADDX.B      R2L,R4L     ;R2L + R4L + C -->R4L
 61   0044 0F0C              61            DAA.B       R4L         ;Decimal adjust R4L
 62   0046 0E24              62            ADDX.B      R2H,R4H     ;R2H + R4H + C -->R4H
 63   0048 0F04              63            DAA.B       R4H         ;Decimal adjust R4H
 64   004A 1A09              64            DEC.B       R1L         ;Decrement R1L
 65   004C 1A0E              65            DEC.B       R6L         ;Decrement R6L
 66   004E 46C0              66            BNE         LBL2
 67   0050 06FB              67            ANDC.B      #B'11111011,CCR     ;Clear Z
 68                          68     ;
 69   0052                   69     EXIT
 70   0052 5470              70            RTS
 71                          71     ;
 72                          72            .END
*****TOTAL ERRORS       0
*****TOTAL WARNINGS     0
```

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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