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Renesas Electronics Corporation

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APPLICATION NOTE

Eight-Bit-Parallel and A/D Input through Port B

Introduction

Reads data from port B as an I/O port, while also using it as the analog input port for the A/D converter.

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. Reads data from port B as an I/O port, while also using it as the analog input port for the A/D converter.
2. Each pin of Port B is pulled up and set to a high input state.
3. The data read from port B is output on port 8.

2. Description of Functions

1. In this sample task, port B is used for the input of 8-bit-parallel data while also providing the analog input pin for one A/D-converter channel.
   1) Figure 2.1 is a block diagram of the I/O port. The block diagram is described below.
      - The port data register (PDRB) is an 8-bit register which stores the data from PB7 to PB0, the bits of port B. In a read access to port B, the PDRB value is directly read.
      - Since port B also provides the analog input pin for the A/D converter, "0" is read out from the bit which is selected for this role by the channel select bits (CH2 to CH0) in the A/D control status register (ADCSR).
      - To correctly read out the 8-bit data of port B, the program takes the logical OR of the data initially read out from PDRB and the data read out from PDRB after switching of the specified A/D conversion channel to another channel.
      - The result of this logical OR is taken as the data for output on port 8.
      - The port control register 8 (PCR8) controls whether each pin of P87 to P80 of port 8 is an input or output. For example, when the PCR87 bit is set, the P87 pin functions as an output pin; and when PCR87 is cleared, the P87 pin functions as an input pin.
      - The port data register 8 (PDR8) is an 8-bit register which stores data of P87 to P80 of port 8.

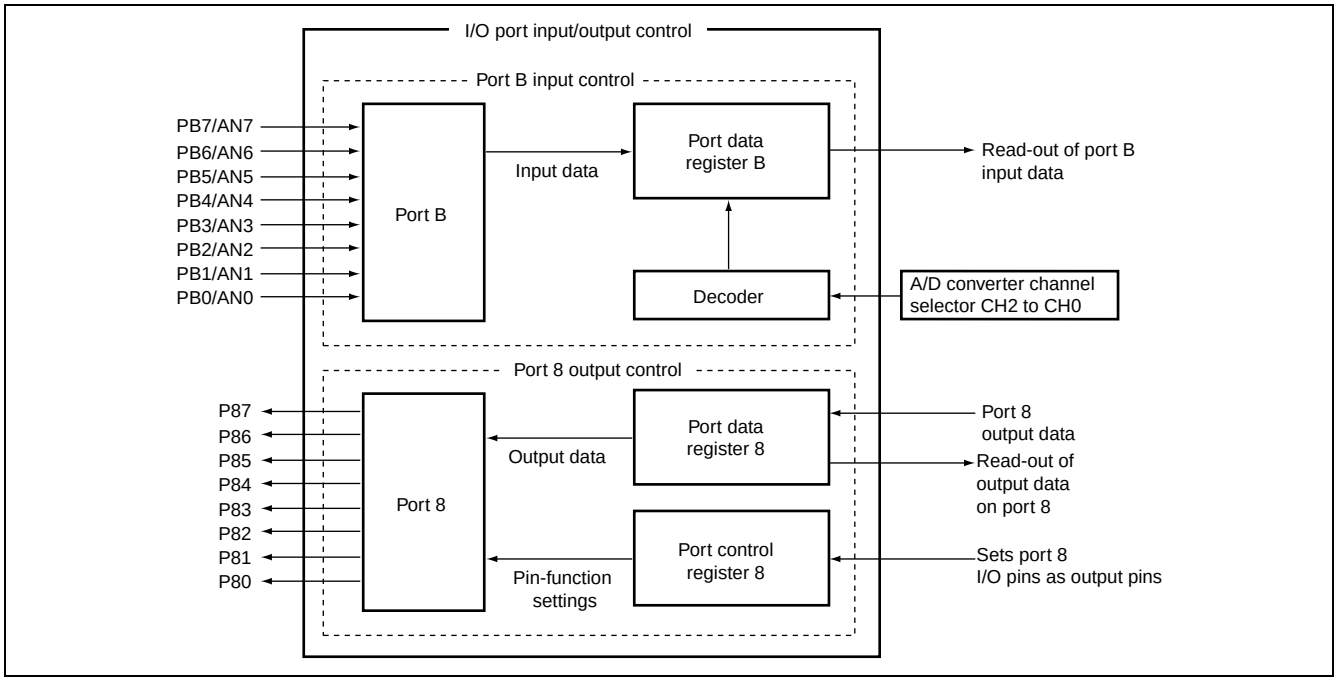


Figure 2.1 Port B Input Function and Port 8 I/O Function

2. Table 2.1 lists the assignment of functions for this sample task. Eight-bit parallel input to port B is performed by assigning functions as shown in table 2.1.

Table 2.1 Function Assignments

Item	Function Assigned
PDRB	Stores data of the port B pins, PB7 to PB0.
PCR8	Sets the port 8 I/O pin functions.
PDR8	Stores data of the port 8 pins, P87 to P80.
ADCSR	Sets speed of and starts A/D conversion, indicates completion of conversion, and specifies analog input pin or pins to be used.

3. Description of Operation

1. Figure 3.1 gives a description of the task's operation. Port B parallel input is performed through software processing as shown in the figure. Operation of this task is in the sequence from left to right of figure 3.1.

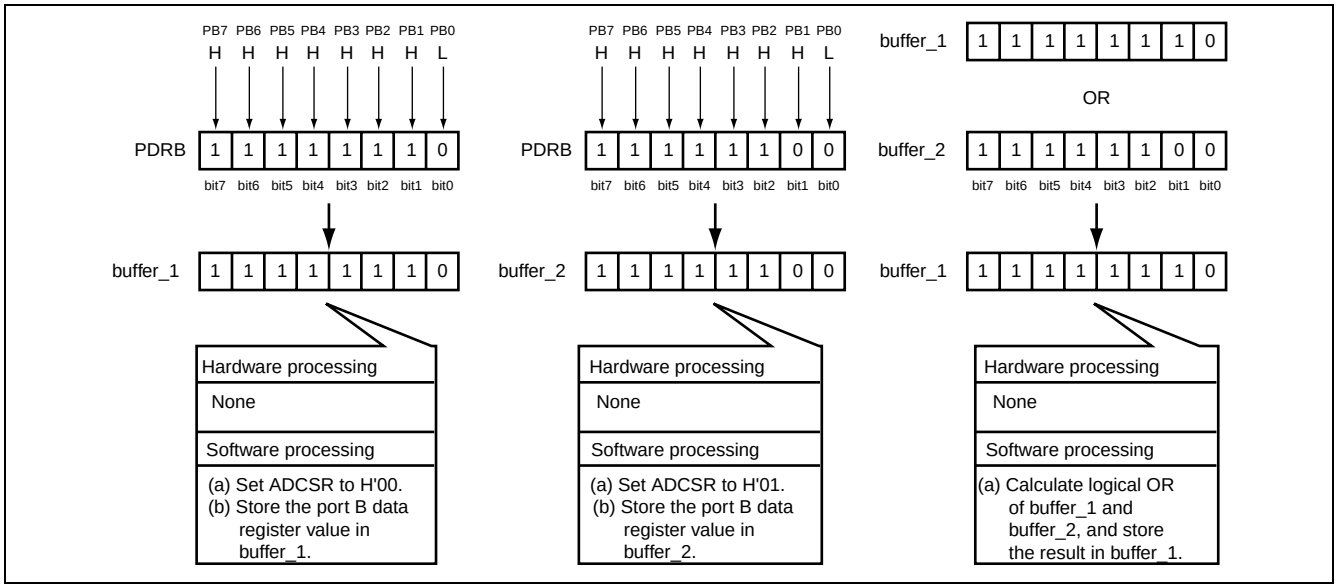


Figure 3.1 Description of Port B 8-Bit Parallel Input Operation

4. Description of Software

4.1 Module

Table 4.1 lists the single module of this sample task.

Table 4.1 Description of Module

Module Name	Label Name	Function
Main routine	main	Uses port B as an input port and outputs the data input via port B from port 8.

4.2 Arguments

No arguments are used by this task.

4.3 Internal Registers Used

Table 4.2 lists the internal registers used in this sample task.

Table 4.2 Internal Registers Used

Register Name	Function	Address	Setting
PDRB	Port data register B: The input value of each pin is read by reading this register. However, if port B pin is designated as an analog input channel by ADCSR in A/D converter, 0 is read.	H'FFDD	—
PCR8	Port control register 8: When PCR87–PCR80 = H'00, I/O pins P87–P80 function as inputs. When PCR87–PCR80 = H'FF, I/O pins P87–P80 function as outputs.	H'FFEB	H'FF
PDR8	Port data register 8: When P87–P80 = H'00, output level on pins P87–P80 is "Low". When P87–P80 = H'FF, output level on pins P87–P80 is "High".	H'FFDB	—
ADCSR	A/D control/status register When SCAN = "0", single mode is selected: When CH2 = "0", CH1 = "0", CH0 = "0", AN0 is selected. When CH2 = "0", CH1 = "0", CH0 = "1", AN1 is selected. When CH2 = "0", CH1 = "1", CH0 = "0", AN2 is selected. When CH2 = "0", CH1 = "1", CH0 = "1", AN3 is selected. When CH2 = "1", CH1 = "0", CH0 = "0", AN4 is selected. When CH2 = "1", CH1 = "0", CH0 = "1", AN5 is selected. When CH2 = "1", CH1 = "1", CH0 = "0", AN6 is selected. When CH2 = "1", CH1 = "1", CH0 = "1", AN7 is selected. When SCAN = "1", scan mode is selected: When CH2 = "0", CH1 = "0", CH0 = "0", AN0 is selected. When CH2 = "0", CH1 = "0", CH0 = "1", AN0–AN1 are selected. When CH2 = "0", CH1 = "1", CH0 = "0", AN0–AN2 are selected. When CH2 = "0", CH1 = "1", CH0 = "1", AN0–AN3 are selected. When CH2 = "1", CH1 = "0", CH0 = "0", AN4 is selected. When CH2 = "1", CH1 = "0", CH0 = "1", AN4–AN5 are selected. When CH2 = "1", CH1 = "1", CH0 = "0", AN4–AN6 are selected. When CH2 = "1", CH1 = "1", CH0 = "1", AN4–AN7 are selected. Note: AN4 to AN7 are not present in the 42-pin version.	H'FFB8	H'00

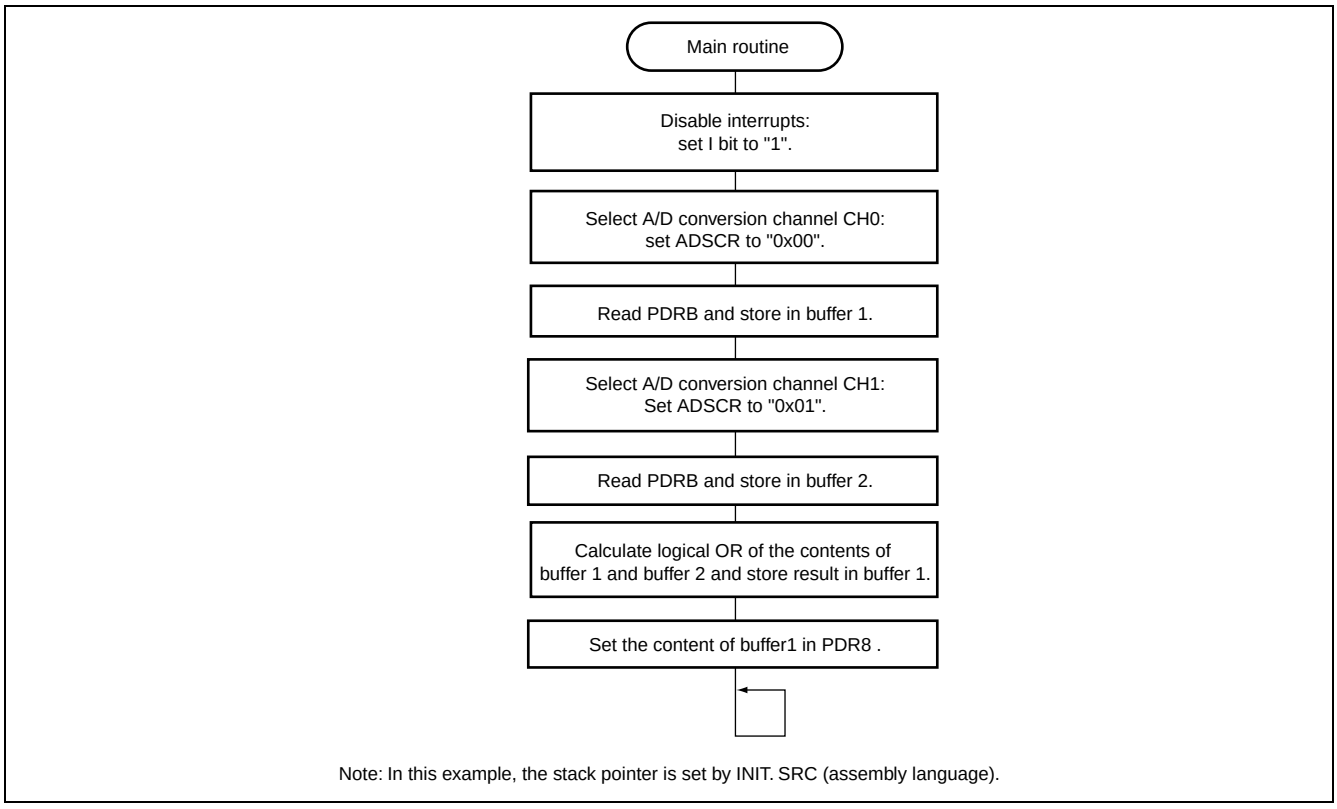
4.4 Description of RAM Usage

RAM usage by this sample task is listed in table 4.3.

Table 4.3 RAM Usage

Label Name	Function	Address	Used in
buffer 1	Port B input-data storage buffer 1	H'FB80	Main routine
buffer 2	Port B input-data storage buffer 2	H'FB81	Main routine

5. Flowchart



Note: In this example, the stack pointer is set by INIT. SRC (assembly language).

6. Program Listing

INIT. SRC (program listing)

```
      .EXPORT   _INIT
      .IMPORT   _main
 ;
      .SECTION  P,CODE
 _INIT:
      MOV.W     #H'FF80,R7
      LDC.B     #B'10000000,CCR
      JMP       @_main
 ;
      .END
```

```
/************************************************************/
/*                                                          */
/*  H8/300H Tiny Series -H8/3664-                           */
/*  Application Note                                        */
/*                                                          */
/*  Port B 8-bit Parallel Input and A/D Read                */
/*                                                          */
/*  Function                                                */
/*  : Port B Read                                           */
/*                                                          */
/*  External Clock: 16MHz                                   */
/*  Internal Clock: 16MHz                                   */
/*  Sub-clock:  32.768kHz                                   */
/*                                                          */
/************************************************************/

#include    <C:\ch38\include\machine.h>
```

```
/************************************************************/
/*  Symbol Definitions                                      */
/************************************************************/
struct BIT {
    unsigned char   b7:1;     /* bit7 */
    unsigned char   b6:1;     /* bit6 */
    unsigned char   b5:1;     /* bit5 */
    unsigned char   b4:1;     /* bit4 */
    unsigned char   b3:1;     /* bit3 */
    unsigned char   b2:1;     /* bit2 */
    unsigned char   b1:1;     /* bit1 */
    unsigned char   b0:1;     /* bit0 */
};
#define   ADDRA      *(volatile unsigned int *)0xFFB0  /* A/D Data Register A           */
#define   ADDRB      *(volatile unsigned int *)0xFFB2  /* A/D Data Register B           */
#define   ADDRC      *(volatile unsigned int *)0xFFB4  /* A/D Data Register C           */
#define   ADDRD      *(volatile unsigned int *)0xFFB6  /* A/D Data Register D           */
#define   ADCSR      *(volatile unsigned char *)0xFFB8 /* A/D Control/Status Register   */
#define   ADCSR_BIT  (*(struct BIT *)0xFFB8)           /* A/D Control/Status Register   */
#define   ADF        ADCSR_BIT.b7                      /* A/D END Flag                  */
#define   ADIE       ADCSR_BIT.b6                      /* A/D Interrupt Enable          */
#define   ADST       ADCSR_BIT.b5                      /* A/D Start                     */
#define   SCAN       ADCSR_BIT.b4                      /* A/D Scan Mode                 */
#define   CKS        ADCSR_BIT.b3                      /* A/D Clock Select              */
#define   CH2        ADCSR_BIT.b2                      /* Channel Select 2              */
#define   CH1        ADCSR_BIT.b1                      /* Channel Select 1              */
#define   CH0        ADCSR_BIT.b0                      /* Channel Select 0              */
#define   PDRB       *(volatile unsigned char *)0xFFDD /* Port Data Register B          */
#define   PCR8       *(volatile unsigned char *)0xFFEB /* Port Control Register 8       */
#define   PDR8       *(volatile unsigned char *)0xFFDB /* Port Data Register 8          */
#define   buffer1    *(volatile unsigned char *)0xFB80 /* buffer RAM 1                  */
#define   buffer2    *(volatile unsigned char *)0xFB81 /* buffer RAM 2                  */

/************************************************************/
/* Function Definition                                      */
/************************************************************/
extern  void    INIT( void );                          /* SP Set                        */
void    main    ( void );
```

```
/************************************************************/
/*  Vector Address                                          */
/************************************************************/

#pragma section     V1                              /* VECTOR-SETTING SECTION        */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f                                            */
    INIT                                            /* 00 Reset                      */
};
#pragma section                                     /* P                             */

/************************************************************/
/*  Main Program                                            */
/************************************************************/
void main ( void )
{
    ADCSR = 0x00;                                   /* A/D Enable Channel Initialize */

    buffer1 = PDRB;                                 /* Read Port B                   */

    ADCSR = 0x01;                                   /* A/D Enable Channel change     */

    buffer2 = PDRB;                                 /* Read Port B                   */

    buffer1 = buffer2;                              /* PB_Data <- Port B Status      */

    PDR8 = buffer1;

    while(1){
       ;
    }
}
```

Link-address specification:

Section Name	Address
CV1	H'0000
P	H'0100
B	H'FB80