Driving Differential, Single-Ended, and/or Frequency Generator Crystal Inputs

Abstract

This application note describes various ways to drive the crystal input pin or a differential receiver. The input pin may be named X1 or Xin. If the input is AC coupled, the crystal oscillator circuit will bias the crystal input in its linear analog region. Directly driving Xin with a LVCMOS clock without a capacitor is allowed and is the most common way to connect a clock oscillator to Xin. The clock oscillator output buffer needs to match the impedance of the trace to the Xin pin. The common way to do this is with a series resistor. If this is not done there may be overshoot and undershoot on the input pin. If the clock is DC coupled it should not exceed Vdd of the input or undershoot below ground. If the clock is AC coupled the amplitude should be between 500mV and Vdd*2/3.

Contents

# 1. Common LVCMOS Clock Oscillator to Crystal Input

On some devices the maximum V_{High} voltage is 1.2 volts for Xin. Verify maximum V_{High}. A resistor voltage divider can be used to reduce V_{High}. If it is not needed RX should be 33 ohms and RY not used.
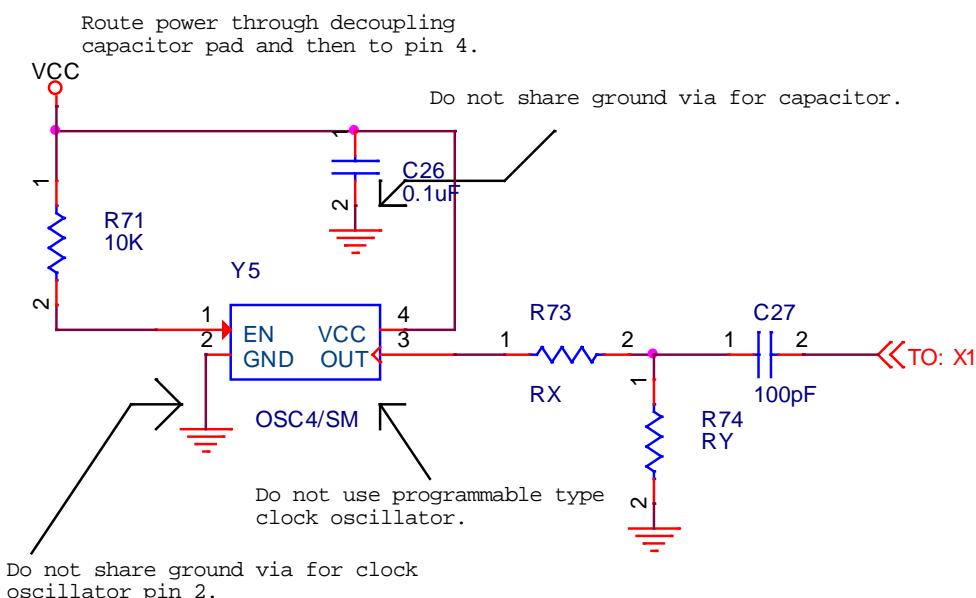
Vcc	RX	RY
1.8	56	150
2.5	91	100
3.3	120	75

Route power through decoupling capacitor pad and then to pin 4.

Do not share ground via for capacitor.

VCC

C26
0.1uF

R71
10K

Y5

EN   VCC
GND   OUT

OSC4/SM

Do not use programmable type clock oscillator.

R73
RX

C27
100pF

TO: X1

R74
RY

Do not share ground via for clock oscillator pin 2.

2. Clock Oscillator to Single-Ended HCSL Input

Route power through decoupling capacitor pad and then to pin 4.

VCC

Do not share ground via for capacitor.

V3.3

C2
0.1uF

R2
10K

Y2

EN   VCC
GND   OUT

OSC4/SM

Do not use programmable type clock oscillator.

R5
200

R6
68

R3
8.2K

U1A

HCSL Input

R7
1K

C4
0.1uF

Do not share ground via for clock oscillator pin 2.

3. LVPECL Driving Crystal Input

LVPECL driving Crystal input

C5

1 2
100 pF

U2A

1 2
50 R8

1 2
50 R10

1 2
50 R11

XIN

XOUT

Crystal Input

4. SMA or BNC Input

CONNECTOR COAX-50_OHM
J1

1

C9

1 2
100pF

R14
49.9

TO: X1

2

5. LVDS Driving Crystal

LVDS driving Crystal input C6

1 2
100 pF

U2B

1 2
100 R9

3
XIN

XOUT
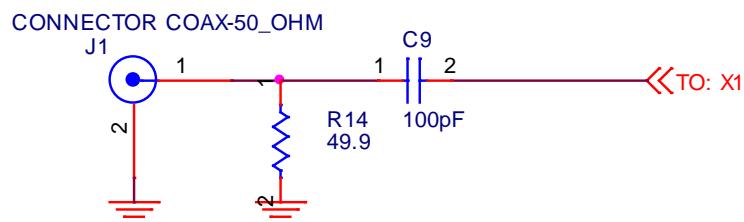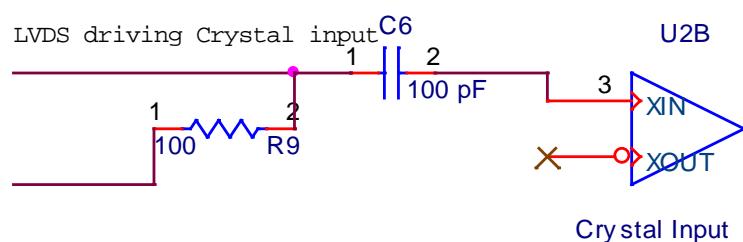
Crystal Input

6. Stuff Option for Coax Input or Crystal Input

Crystal CL and load capacitors may be different.

Over Lap Pads
of C5.2 and C6.1

TO: X1

TO: X2

Y3
CRYSTAL_8pF

CONNECTOR COAX-50_OHM
J2

C14
100pF

R23
49.9

C15
6.8 pF

C16
6.8 pF

Populate Y3, C6, and C7
or
J2, R9, C5.
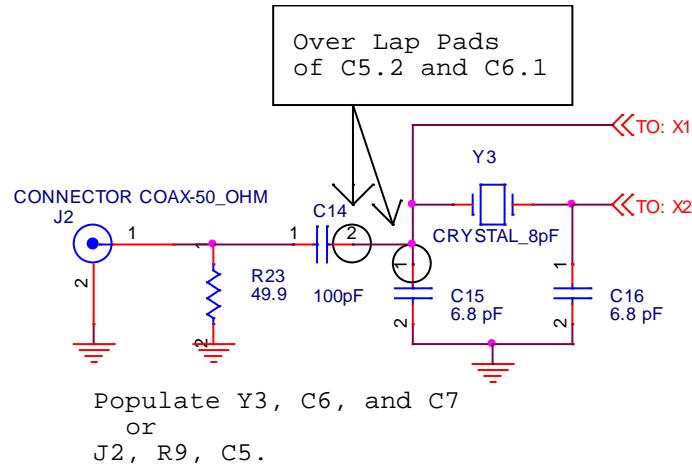
7. HSCL Driving LVDS Input

HCSL driving LVDS receiver input

Vdd

R1A   R1B

C23
470 pF

U4B

1
100   R68
2

C24
470 pF

R2A   R2B

LVDS Input
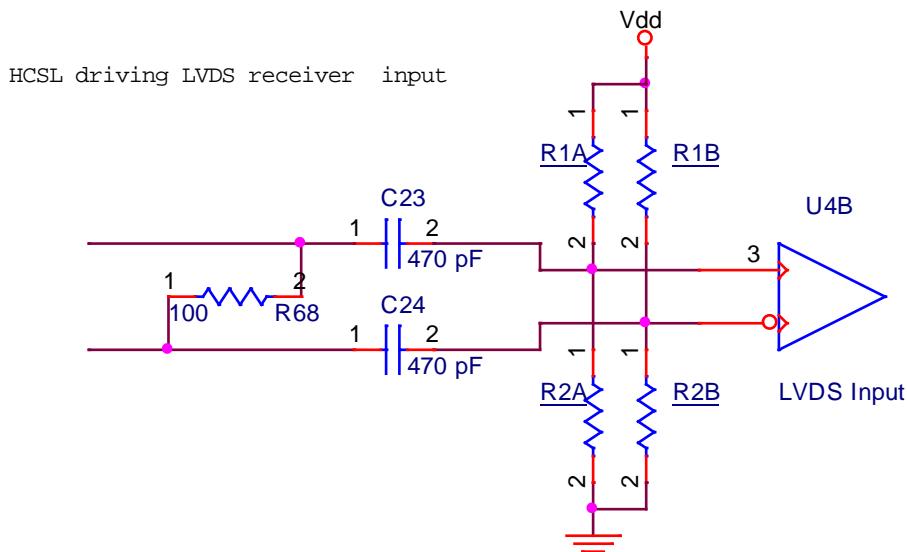
100Ω		
Vdd	R1	R2
1.8 V	3000	6800
2.5 V	4300	4300
3.3 V	5600	3300

8. LVDS Driving HCSL Input

LVDS driving HCSL receiver input

100Ω		
Vdd	R1	R2
1.8 V	10K	2.4K
2.5 V	15K	2.4K
3.3 V	18K	2.2K
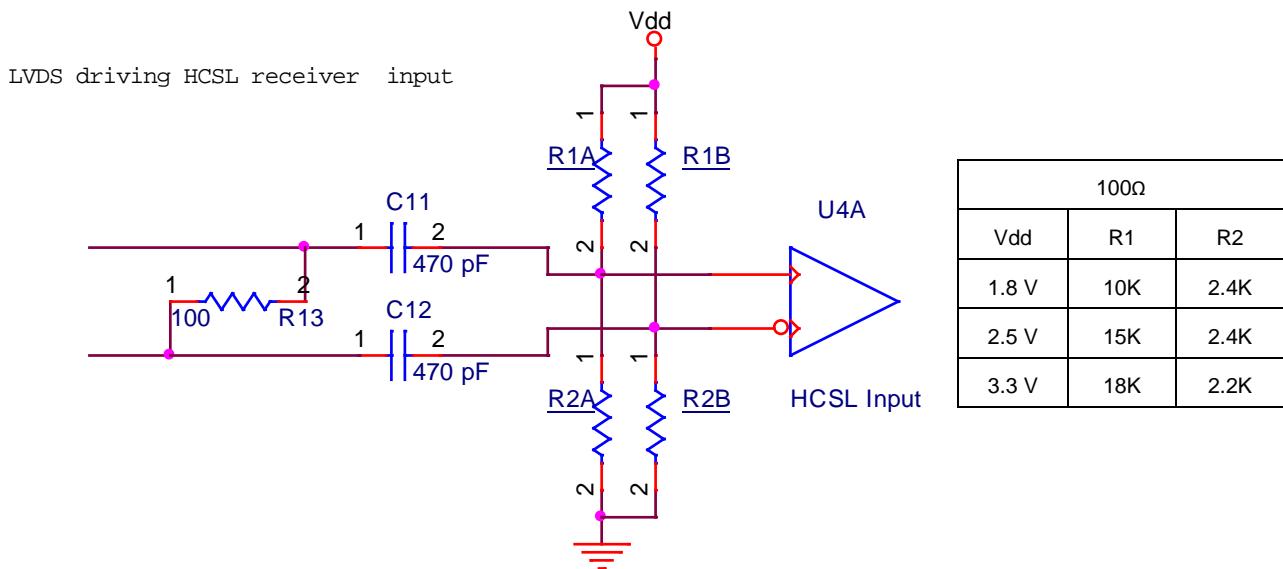
9. Dual Layout for Crystal or Clock Oscillator

Many clock generators have built-in crystal load capacitors. C2 and C3 are No Stuff in that application. TCXO or XO has square wave output. If TCXO sine wave output R1 = 100pF.

```
If Xtal              If XO or TCXO
R1,R5 = 0 Ohm        R1 =33 Ohm
                     R4 = 10K
POP: C2,C3           POP: C1
NO POP: C1,R2,R4     NO POP: C2,C3,R5
```

Layout note:
Overlap R4.2 & C3.1
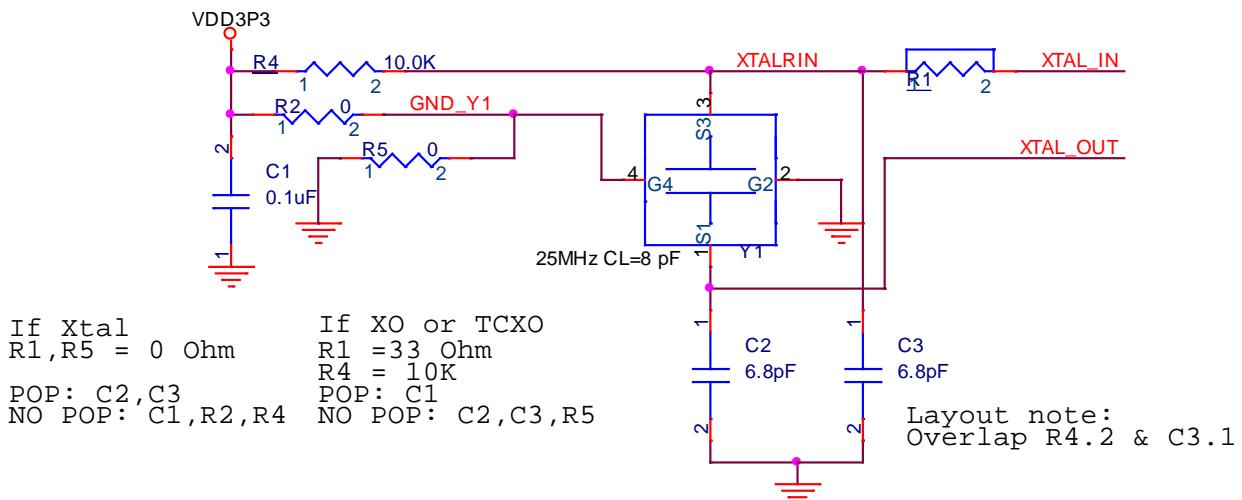
10. Cable-Connected HCSL Clock Termination

For more information, see the PCI Express External Cabling Specification.

85 Ω			100 Ω		
Vdd	R1a,b	R2a,b	Vdd	R1a,b	R2a,b
1.8 V	220	51	1.8 V	240	62
2.5 V	300	50	2.5 V	360	56
3.3 V	390	47	3.3 V	470	56
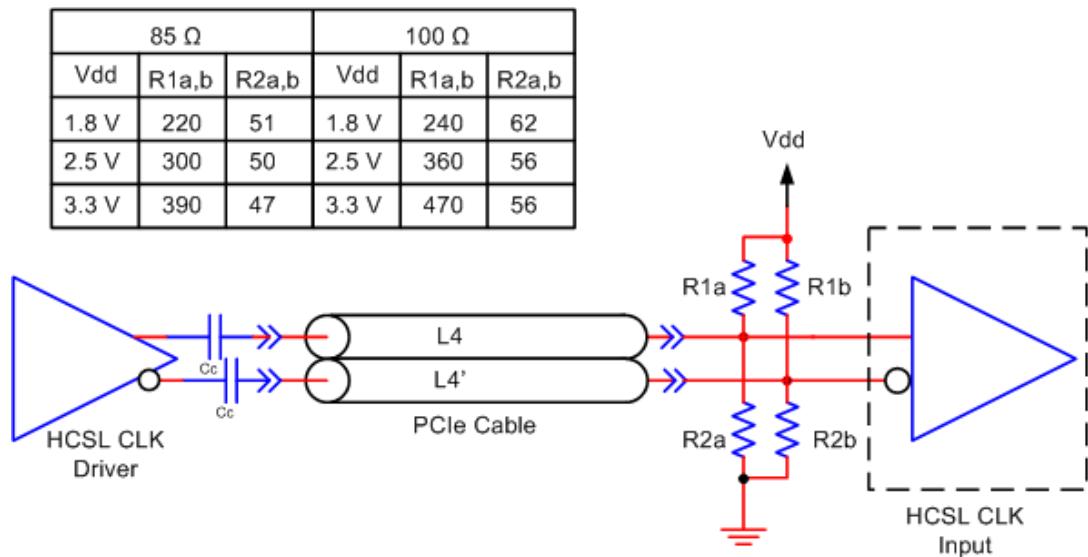
11. Level Shifting Single-Ended LVCMOS Input
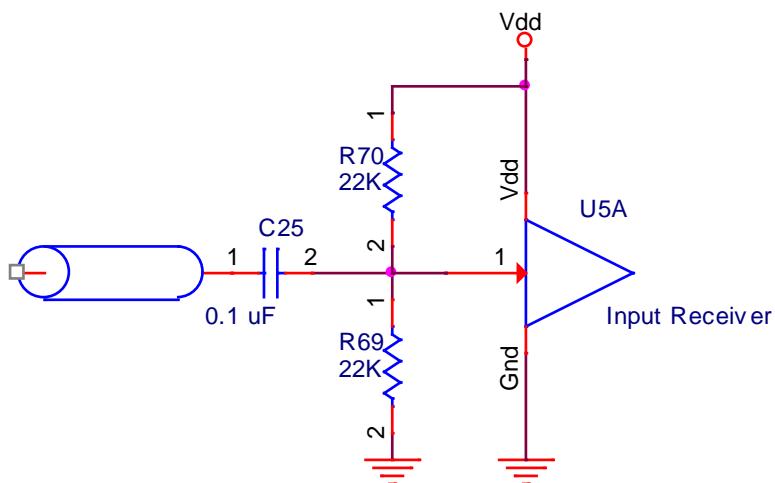
12. Revision History

Revision	Date	Description
1.0	Jun.18.20	Initial release.

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