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# SH7280 Group

## DMAC Dual Address Mode

### Introduction

This application note provides an example of DMA transfer by means of the dual address mode of the direct memory access controller (DMAC) of the SH7285.

### Target Device

SH7285

### Contents

# 1. Preface

## 1.1 Specifications

- DMA transfer from the on-chip RAM to external SDRAM is performed on DMAC channel 0 in dual address mode.
- Auto-request mode is used to request the DMAC to transfer five sets of 32-bit data (total 20 bytes).

## 1.2 Module Used

- Direct memory access controller (DMAC channel 0)

## 1.3 Applicable Conditions

- MCU: SH7285/SH7286/SH7243
- Operating frequency: Internal clock 100 MHz
  Bus clock 50 MHz
  Peripheral clock 50 MHz
- C compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01 Release01 from Renesas Technology Corp.
- Compiler options: -cpu=sh2a -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath-errorpath -global_volatile=0 -opt_range=all -infinite_loop=0-del_vacant_loop=0 -struct_alloc=1 -nologo

## 2. Description of the Sample Application

This sample program employs the direct memory access controller (DMAC) to perform DMA transfer from the on-chip RAM to external SDRAM in dual address mode.

### 2.1 Summary of MCU Module Used

In dual address mode, both the transfer source and destination are accessed (selected) by an address. The transfer source and destination can be located externally or internally. DMA transfer requires two bus cycles because data are read from the transfer source in a data read cycle and written to the transfer destination in a data write cycle. After the read cycle, the data for transfer are temporarily stored in the DMAC. For example in transfer between external memories, data are read to the DMAC from one region of external memory in a data read cycle, after which data are written to the other region of external memory in a data write cycle.

The flow of data in dual address mode is illustrated in figure 1. A block diagram of the DMAC is shown in figure 2. The settings of the DMAC are listed in table 1.

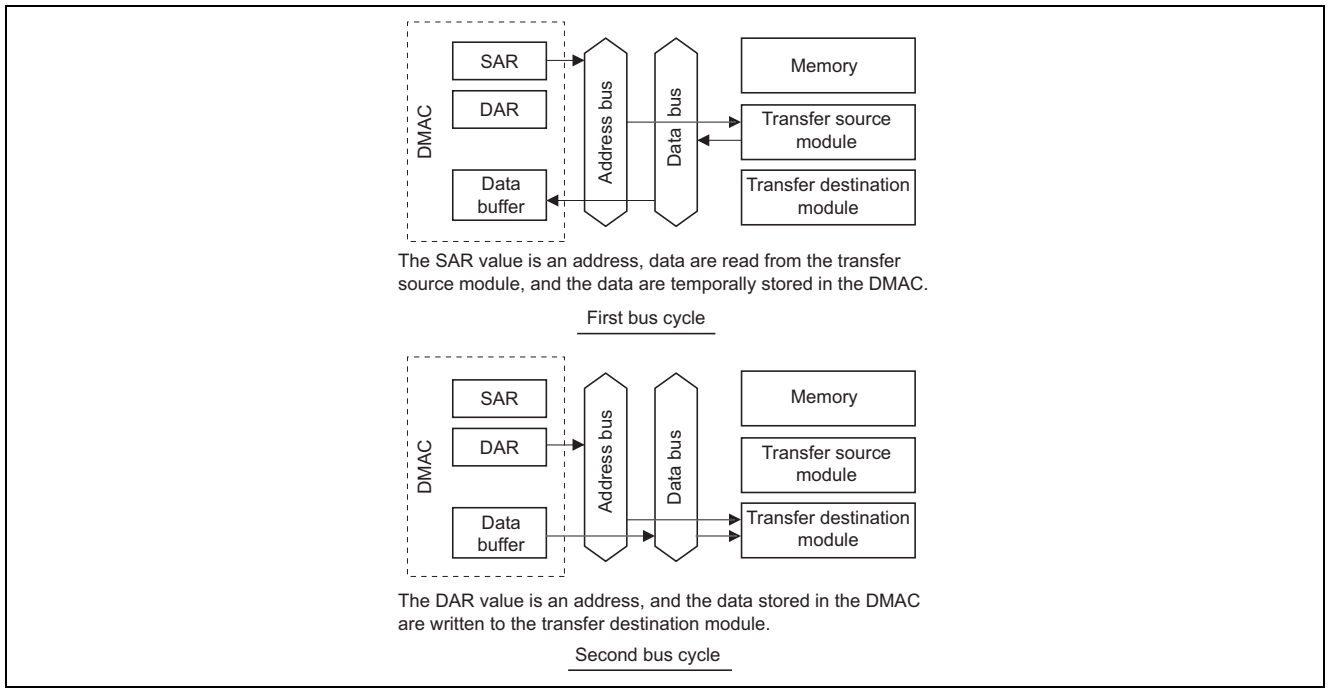
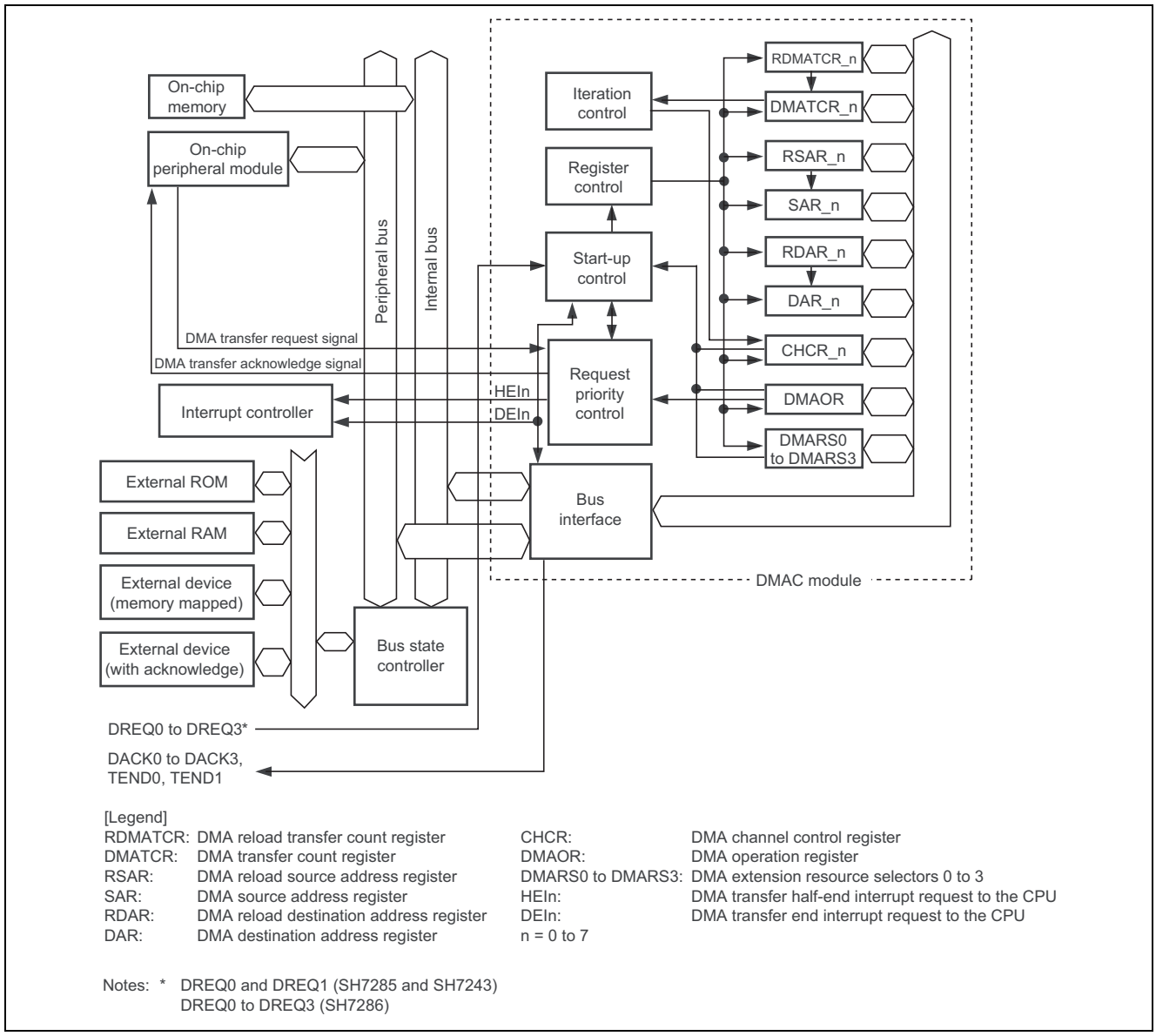



**Figure 1 Flow of Data in Dual Address Mode**

**Table 1 Settings of DMAC**

| Item | Setting |
|---|---|
| Address mode | Dual address |
| Transfer request | Auto request (transfer requests are made by software) |
| Transfer count | 5 transfers (20 bytes of data in total are transferred) |
| Bus mode | Burst mode |
| Transfer source address | On-chip RAM<br>(automatic incrementation according to the data size after each transfer) |
| Transfer destination address | SDRAM (H'0C00 0000) in the CS3 space<br>(automatic incrementation according to the data size after each transfer) |
| Transfer data size | Longword (32 bits) |
| Interrupt | Transfer end interrupt enabled |

Note: For details on the DMAC, refer to the section on the direct memory access controller (DMAC) in the *SH7280 Group Hardware Manual*.




[Legend]

| | | | |
|---|---|---|---|
| RDMATCR: | DMA reload transfer count register | CHCR: | DMA channel control register |
| DMATCR: | DMA transfer count register | DMAOR: | DMA operation register |
| RSAR: | DMA reload source address register | DMARS0 to DMARS3: | DMA extension resource selectors 0 to 3 |
| SAR: | DMA source address register | HEIn: | DMA transfer half-end interrupt request to the CPU |
| RDAR: | DMA reload destination address register | DEIn: | DMA transfer end interrupt request to the CPU |
| DAR: | DMA destination address register | n = 0 to 7 | |

Notes: * DREQ0 and DREQ1 (SH7285 and SH7243)
DREQ0 to DREQ3 (SH7286)

**Figure 2 Block Diagram of the DMAC**

## 2.2 Procedure for Setting the Module Used

This section describes the procedure for specifying initial settings for operating the DMAC in dual address mode. Auto-request mode is used for requesting transfer. A flowchart of the DMAC initialization is shown in figure 3. For details on registers, refer to the *SH7280 Group Hardware Manual*.

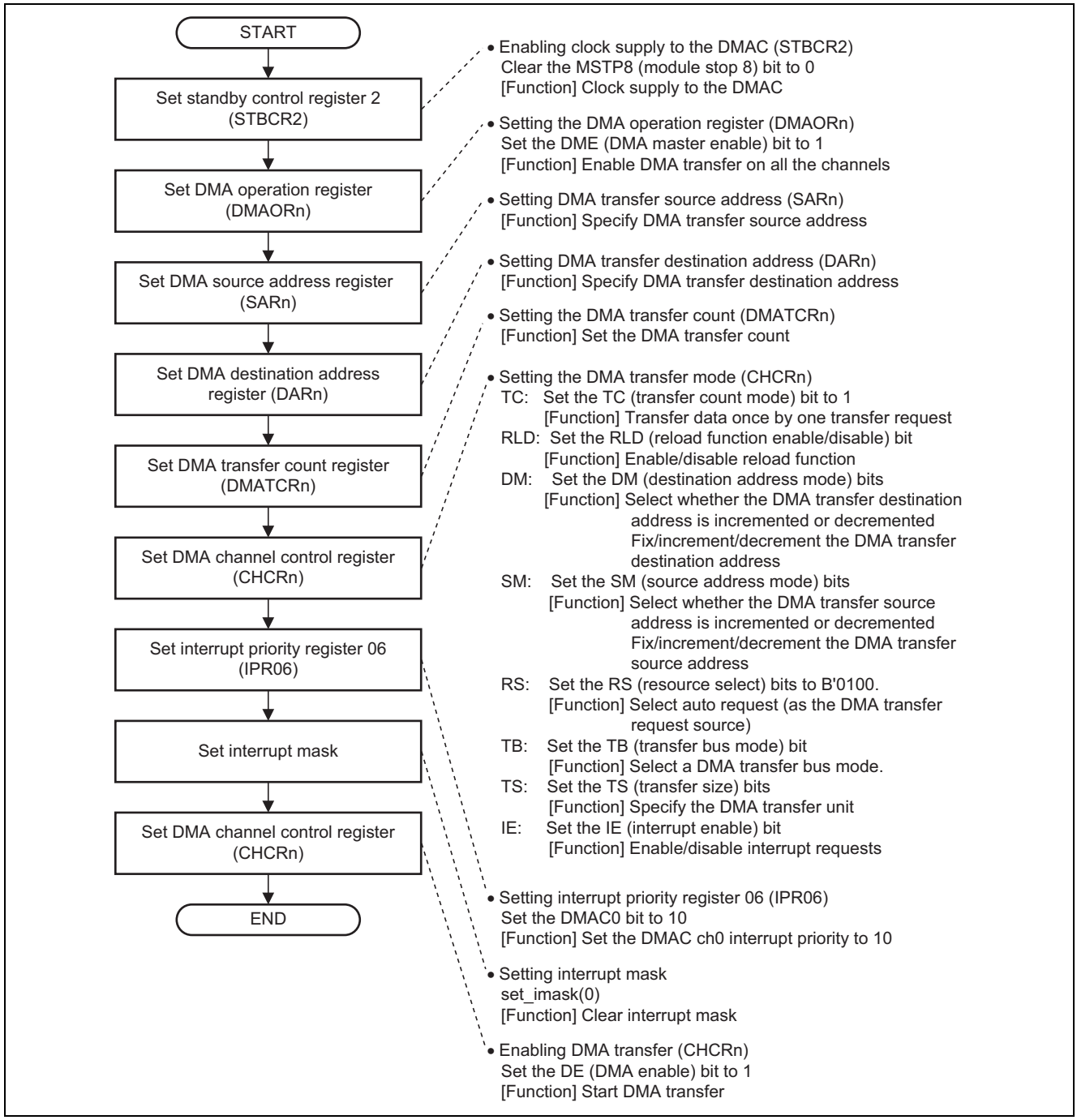



**Figure 3 Flowchart of DMAC Initialization**

## 2.3 Description of the Sample Program

The operation of the sample program is described in figure 4 and table 2.

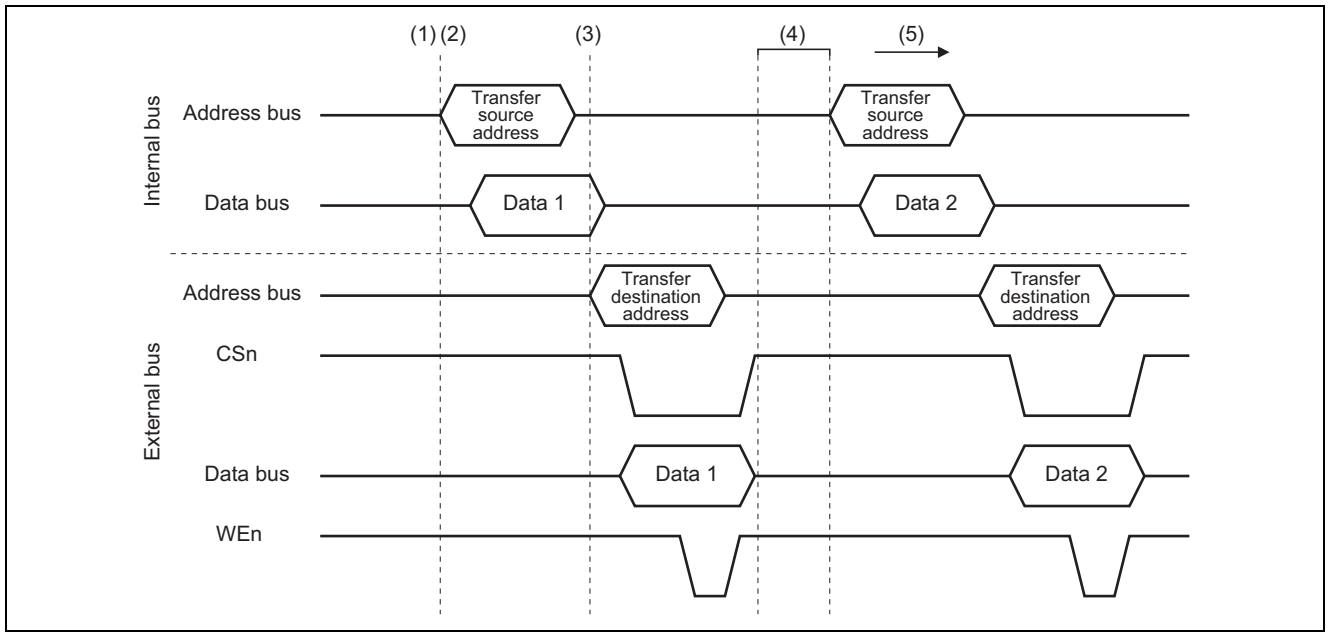



**Figure 4 Operation in Dual Address Mode**

**Table 2 Processing**

| | Software Processing | Hardware Processing |
|---|---|---|
| (1) | Setting the DE bit in CHCR0 to 1 after all the other settings have been specified. (DMAC0 starts operation) | Output of the transfer source address to the internal address bus |
| (2) | — | Output of data from the on-chip RAM to the internal data bus |
| (3) | — | Output of CSn and WEn signals, address, and data to the external bus |
| (4) | — | Incrementing of SAR0 and DAR0 |
| (5) | — | Repeating until DMATCR0 becomes 0 |

## 2.4 Usage Notes on Sample Program

In this sample program, addresses where the source and destination areas for transfer start are specified as absolute addresses for clarity. Ensure that sections used by the user program do not overlap with the source and destination regions that start from the absolute addresses.

## 2.5 Procedure for Processing by the Sample Program

In the sample program, DMA transfer of 20-byte data from the on-chip RAM to external SDRAM is performed, after which transfer end interrupt processing is performed to disable DMA transfer.

The register settings for the sample program are listed in table 3. Also, a flowchart of the sample program is shown in figure 5.

**Table 3 Register Settings for Sample Program**

| Register Name | Address | Setting | Description |
|---|---|---|---|
| Standby control register 2 (STBCR2) | H'FFFE 0018 | H'00 | MSTP8 = "0": DMAC operates |
| DMA channel control register_0 (CHCR0) | H'FFFE 100C | H'0000 5474 | TC = "0": Transfer data once per DMA request<br>RLD = "0": Disable reload function<br>DM = "B'01": Increment the destination address<br>SM = "B'01": Increment the source address<br>RS = "B'0100": Auto request<br>TB = "1": Burst mode<br>TS = "B'10": Longword transfer<br>IE = "1": Enable interrupt requests |
| | | H'0000 5475 | DE = "1": Enable DMA transfer |
| | | H'0000 5470 | IE = "0": Disable interrupt requests<br>TE = "0": Clear the transfer end flag<br>DE = "0": Disable DMA transfer |
| DMA source address register_0 (SAR0) | H'FFFE 1000 | Address of transfer source data | Start address of the transfer source: set to an address in the on-chip RAM area |
| DMA destination address register_0 (DAR0) | H'FFFE 1004 | H'0C00 0000 | Start address of the transfer destination: set to an address in the external memory area* |
| DMA transfer count register_0 (DMATCR0) | H'FFFE 1008 | H'05 | Transfer count: 5 transfers |
| DMA operation register (DMAOR) | H'FFFE 1200 | H'0001 | DME = "1": Enable DMA transfer on all channels |
| DMA extension resource selector_0 (DMARS0) | H'FFFE 1300 | H'0000 | Not used for auto request |

Note: * Addresses in external memory areas vary with the target board.

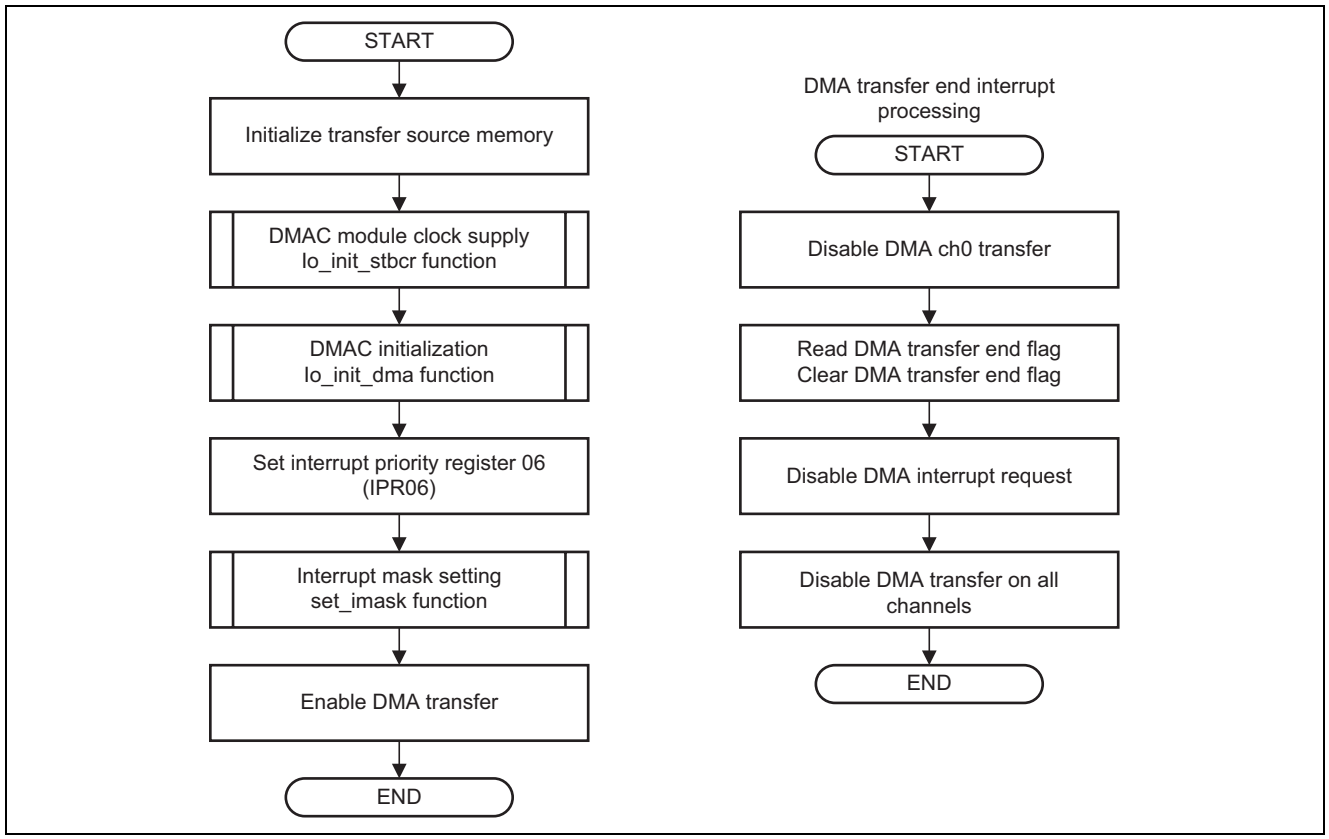



**Figure 5 Flowchart of Processing by the Sample Program**

## 3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*****************************************************************
*
*       System Name : SH7285 Sample Program
*       File Name   : main.c
*       Contents    : DMA dual address mode sample program
*       Version     : 1.00.00
*       Model       : M3A-HS85
*       CPU         : SH7285
*       Compiler    : SHC9.1.1.0
*       note        : DMA transfer from the on-chip RAM to externally connected
*                     SDRAM is performed using the DMAC in dual address mode.
*                     Auto request mode is used for requesting the DMAC
*                     to transfer 5 sets of 32-bit data (total 20 bytes).
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*
*       history   : 2008.02.26 ver.1.00.00
*""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include "iodefine.h"       /* SH7285 iodefine  */


/* ==== prototype declaration ==== */
void main(void);
void io_init_stbcr(void);
void io_init_dma(unsigned long sar, unsigned long dar, unsigned long num);

/* ==== symbol definition ==== */
#define NUM 5
#define SDRAM_ADDR 0x0c000000ul     /* DMA source address(SDRAM) */

/* ==== RAM allocation variable declaration ==== */
unsigned long Data[NUM];

/*""FUNC COMMENT""*****************************************************
 * Outline     : Sample program main
 *---------------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *             : #include <machine.h>
 *---------------------------------------------------------------------
 * Declaration : void main(void);
 *---------------------------------------------------------------------
 * Function    : Sample program main
 *---------------------------------------------------------------------
 * Argument    : void
 *---------------------------------------------------------------------
 * Return Value: void
 *---------------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""************************************************/

```

2. Sample Program Listing: main.c (2)

```
 58    void main(void)
 59    {
 60        /* ==== Transfer data set ==== */
 61        Data[0] = 0x11111111ul;
 62        Data[1] = 0x22222222ul;
 63        Data[2] = 0x33333333ul;
 64        Data[3] = 0x44444444ul;
 65        Data[4] = 0x55555555ul;
 66
 67        /* ==== Setting of power down mode ==== */
 68        io_init_stbcr();
 69
 70        /* ==== Setting of DMAC ==== */
 71        io_init_dma((unsigned long)&Data[0], SDRAM_ADDR, NUM);
 72
 73        /* ==== interrupt priority register ==== */
 74        INTC.IPR06.BIT._DMAC0 = 10u;
 75
 76        /* ==== clear the interrupt mask ==== */
 77        set_imask(0);
 78
 79        /* ==== DMA transfer start ==== */
 80        DMAC0.CHCR.BIT.DE = 1ul;
 81
 82        while(1){
 83            /* loop */
 84      }
 85    }
 86
 87    /*""FUNC COMMENT""*****************************************************
 88     * Outline     : Exiting module standby mode
 89     *-----------------------------------------------------------------------
 90     * Include     : #include "iodefine.h"
 91     *-----------------------------------------------------------------------
 92     * Declaration : void io_init_stbcr(void);
 93     *-----------------------------------------------------------------------
 94     * Function    : Exiting module standby mode
 95     *-----------------------------------------------------------------------
 96     * Argument    : void
 97     *-----------------------------------------------------------------------
 98     * Return Value: void
 99     *-----------------------------------------------------------------------
100     * Notice      :
101     *""FUNC COMMENT END""*************************************************/
102    void io_init_stbcr(void)
103    {
104        /* ==== Setting of power down mode ==== */
105        STB.CR2.BIT._DMAC = 0u;            /* Clear the DMAC module standby mode */
106    }
```

3. Sample Program Listing: main.c (3)

```
107    /*""FUNC COMMENT""*************************************************************
108     * Outline     : DMAC setting
109     *-------------------------------------------------------------------------
110     * Include     : #include "iodefine.h"
111     *-------------------------------------------------------------------------
112     * Declaration : void io_init_dma(unsigned long sar, unsigned long dar,
113     *             :                  unsigned long num);
114     *-------------------------------------------------------------------------
115     * Function    : Setting the DMAC
116     *-------------------------------------------------------------------------
117     * Argument    : unsigned long sar : transfer source address
118     *             : unsigned long dar : transfer destination address
119     *             : unsigned long num : transfer count
120     *-------------------------------------------------------------------------
121     * Return Value: void
122     *-------------------------------------------------------------------------
123     * Notice      :
124     *""FUNC COMMENT END""*************************************************/
125    void io_init_dma(unsigned long sar, unsigned long dar, unsigned long num)
126    {
127
128        /* ==== Setting of DMAC ==== */
129        /* ---- DMA operation register(DMAOR) ---- */
130        DMAC.DMAOR.BIT.DME = 1u;            /* DMA master enable */
131
132        /* ---- DMA source address registers(SAR) ---- */
133        DMAC0.SAR = (void *)sar;            /* DMA source address */
134        /* ---- DMA Destination Address Registers(DAR) ---- */
135        DMAC0.DAR = (void *)dar;            /* DMA destination address */
136        /* ---- DMA transfer count registers(DMATCR) ---- */
137        DMAC0.DMATCR = num;                 /* DMA transfer count */
138
139        /* ---- DMA channel control registers(CHCR) ---- */
140        DMAC0.CHCR.LONG = 0x00005474ul;
141                /* 15-14 = b'01  - Destination address is incremented       */
142                /* 13-12 = b'01  - Source address is incremented            */
143                /* 11-8  = b'0100- Auto request                             */
144                /* 7-6   = b'01  - DREQ detected at falling edge            */
145                /* 5     = b'1   - Burst mode                               */
146                /* 4-3   = b'10  - Longword unit(four bytes)                */
147                /* 2     = b'1   - Enables an interrupt request             */
148                /* 1     = b'0   - Transfer End Flag                        */
149                /* 0     = b'0   - DMA transfer disabled                    */
150    }
```

4. Sample Program Listing: main.c (4)

```
/*""FUNC COMMENT""*****************************************************
 * Outline     : DMA transfer end interrupt
 *---------------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *---------------------------------------------------------------------
 * Declaration : void io_int_dma(void);
 *---------------------------------------------------------------------
 * Function    : 1. Disabling DMA transfer
 *             : 2. Clearing the transfer end flag
 *             : 3. Disabling interrupt requests
 *             : 4. Disabling DMA transfer on all the channels
 *             : 5. Dummy read
 *---------------------------------------------------------------------
 * Argument    : void
 *---------------------------------------------------------------------
 * Return Value: void
 *---------------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*************************************************/
void io_int_dma(void)
{
  volatile unsigned long dummy;

    DMAC0.CHCR.BIT.DE = 0x00ul;       /* Clear the DE bit */

    DMAC0.CHCR.BIT.TE = 0x00ul;       /* Clear the TE bit */

    DMAC0.CHCR.BIT.IE = 0x00ul;       /* Clear the IE bit */

    DMAC.DMAOR.BIT.DME = 0x00u;       /* DMA master disable */

  dummy = DMAC0.CHCR.BIT.TE;
}
/* End of File */
```

## 4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7280 Group Hardware Manual
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