R32C/100 Series

DMA II Setting Example (Multiple Transfer)

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1. Abstract

This application note describes the setting procedure to perform a multiple transfer when using DMAC II.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):
MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the user's manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Operation Overview

Multiple memory-to-memory transfers (max. seven times) are performed from different source addresses to different destination addresses by one transfer request.
When the multiple transfer is selected, the following transfer functions are not available: the calculation transfer, burst transfer, chained transfer, and DMA II transfer complete interrupt.
Table 3.1 lists Specifications of DMAC II and Settings. Table 3.2 lists DMAC II Specifications.

Table 3.1 Specifications of DMAC II and Settings

Item	Selectable Function	Setting
Transfer sizes	8 bits or 16 bits	8 bits
Transfer types	Memory → Memory	Memory → Memory
Source addressing	Fixed Increment	Increment
Destination addressing	Fixed Increment	Increment
Calculation transfer	Not used	Not used
Burst transfer	Not used	Not used
Transfer complete interrupt	Not used	Not used
Chained transfer	Not used	Not used

Table 3.2 DMAC II Specifications

Item	Setting
Number of transfers	2
Number of multiple transfers	2
Transfer data 1	01h, 03h
Transfer data 2	7Fh, FFh
Trigger for DMAC II	INT0 interrupt

3.1 Operation Example

This operation example explains DMA II transfer based on the settings in this application note.
When an INT0 interrupt request is generated, multiple memory-to-memory transfers are performed in 8-bit data from different source addresses to different destination addresses with one transfer request.
Figure 3.1 shows the DMAC II Multiple Transfer.
Numbers (1) and (2) in the parenthesis in the figure explain:

(1) When an INT0 interrupt request is generated, data from different source addresses are transferred to their respective destination addresses. After the transfer is completed, the addresses in different source addresses and destination addresses are incremented by 1 and the counter value of the transfer counter is decremented by 1.

(2) When the next INT0 interrupt is generated, the same process as described above in (1) is carried out. Then, the counter value of the transfer counter becomes 0, indicating the multiple transfer is completed.

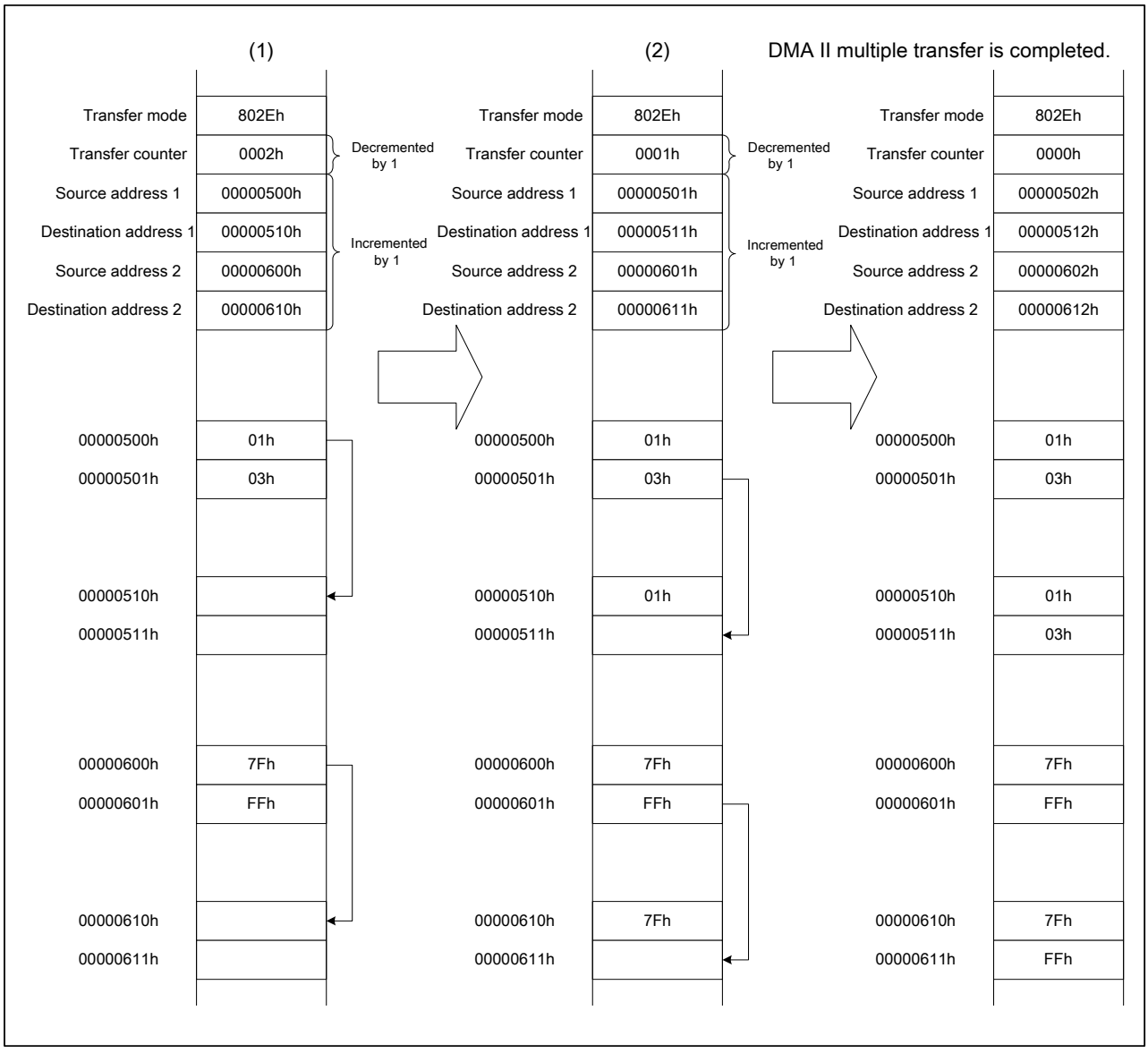


Figure 3.1 DMAC II Multiple Transfer

4. Application Example

This application note explains settings for multiple memory-to-memory transfers using DMAC II.

4.1 Setting for DMAC II

When using DMAC II, set the following:

- Registers RIPL1 and RIPL2
- DMAC II index
- The interrupt control register of the peripheral function triggering DMAC II
- The relocatable vector of the peripheral function triggering DMAC II
- IRLT bit in the IIOiIE register if the intelligent I/O interrupt is used.
  Refer to the user's manual for details on the IIOilE register (i = 0 to 11).

4.1.1 Registers RIPL1 and RIPL2

When the DMAII bits in registers RIPL1 and RIPL2 are set to 1 (DMA II transfer selected) and the FSIT bits are set to 0 (normal interrupt selected), DMAC II is triggered by an interrupt of any peripheral function with bits ILVL2 to ILVL0 in the corresponding interrupt control register set to 111b (level 7).
Set the same value to registers RIPL1 and RIPL2.
Table 4.1 lists Setting Values in Registers RIPL1 and RIPL2.

Table 4.1 Setting Values in Registers RIPL1 and RIPL2

Register Name	Setting Value	Remarks
RIPL1 and RIPL2	20h	Bits RLVL2 to RLVL0 are 000b (level 0)
		FSIT bit is 0 (use interrupt request level 7 for normal interrupt)
		b4 is 0
		DMAII bit is 1 (use interrupt request level 7 for fast interrupt)
		b7, b6 are 0

4.1.2 DMAC II Index

The DMAC II index is a data table of 12 to 60 bytes. It stores parameters for transfer mode, transfer counter, source address, and destination address.
The DMAC II index should be allocated on the RAM.
Figure 4.1 shows the Configuration of the DMAC II Index when the multiple transfer is selected.

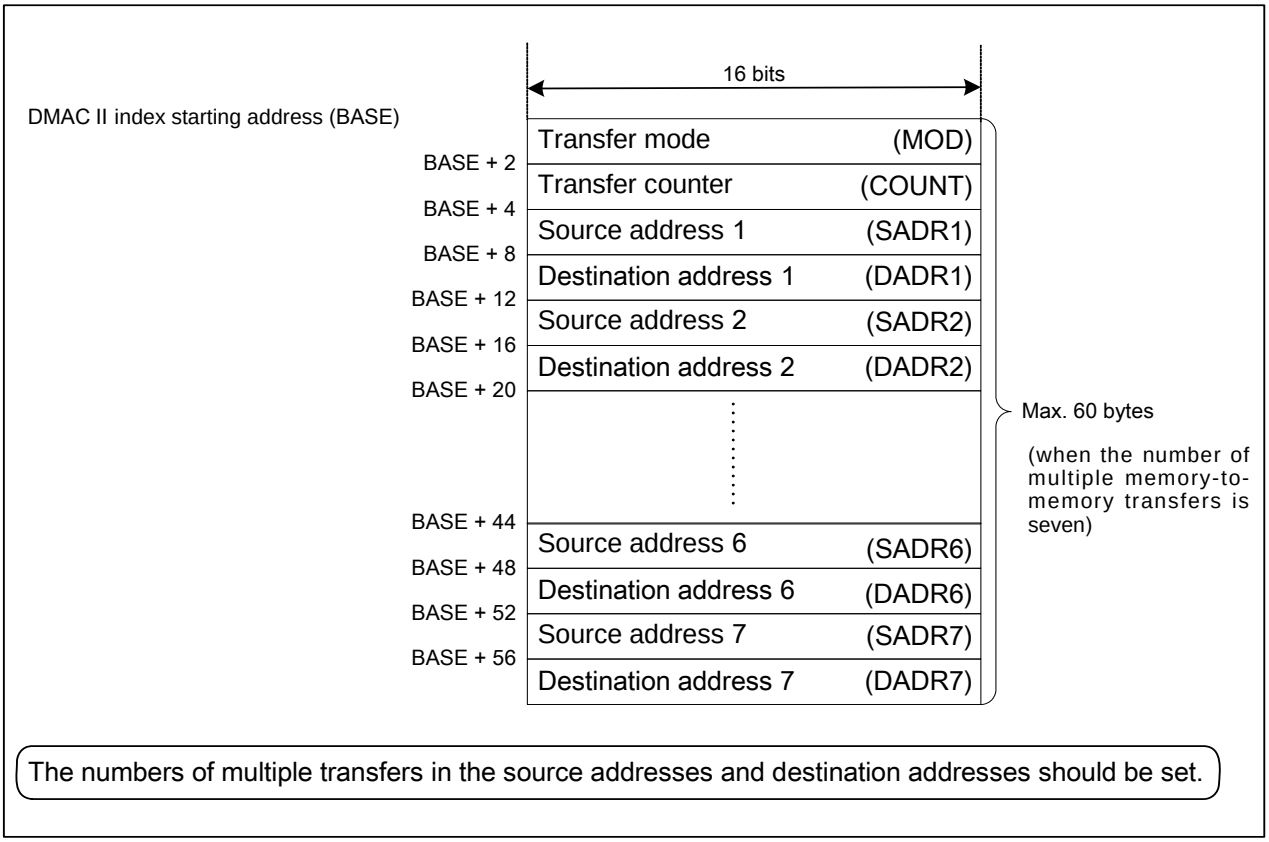


Figure 4.1 Configuration of the DMAC II Index

The following are the details on the DMAC II index.

- Transfer mode (MOD)
  2-byte data is required to set transfer mode.
- Transfer counter (COUNT)
  2-byte data is required to set the transfers to be performed.
- Source address (SADR) (i = 1 to 7)
  4-byte data is required to set a source address in a memory or an immediate data.
- Destination address (DADRi)
  4-byte data is required to set a destination address in a memory

4.1.3 Interrupt Control Register of the Peripheral Function

Set bits ILVL2 to ILVL0 in the interrupt control register for the peripheral interrupt triggering DMAC II to 111b (level 7).

4.1.4 Relocatable Vector Table of the Peripheral Function

Set the starting address of the DMAC II index to the interrupt vector for the peripheral interrupt triggering DMAC II.

In this application note, the INT0 interrupt is used for the interrupt triggering DMAC II. Figure 4.2 shows the setting by asm function in the C language program. In this setting example, the DMAC II index (dm_index) is set as the relocatable vector table.

```
asm(“      .rvector    31,_dm_index”);      //Definite DMACII Index (Software Interrupt Number 31)
```

Figure 4.2 Setting Example for the Starting Address of the DMAC II Index to the Interrupt Vector

4.2 Setting Overview

Figure 4.3 shows the Setting Procedure for DMAC II Multiple Transfer. Refer to section 4.3 "Register Settings" for detailed settings of the items below.

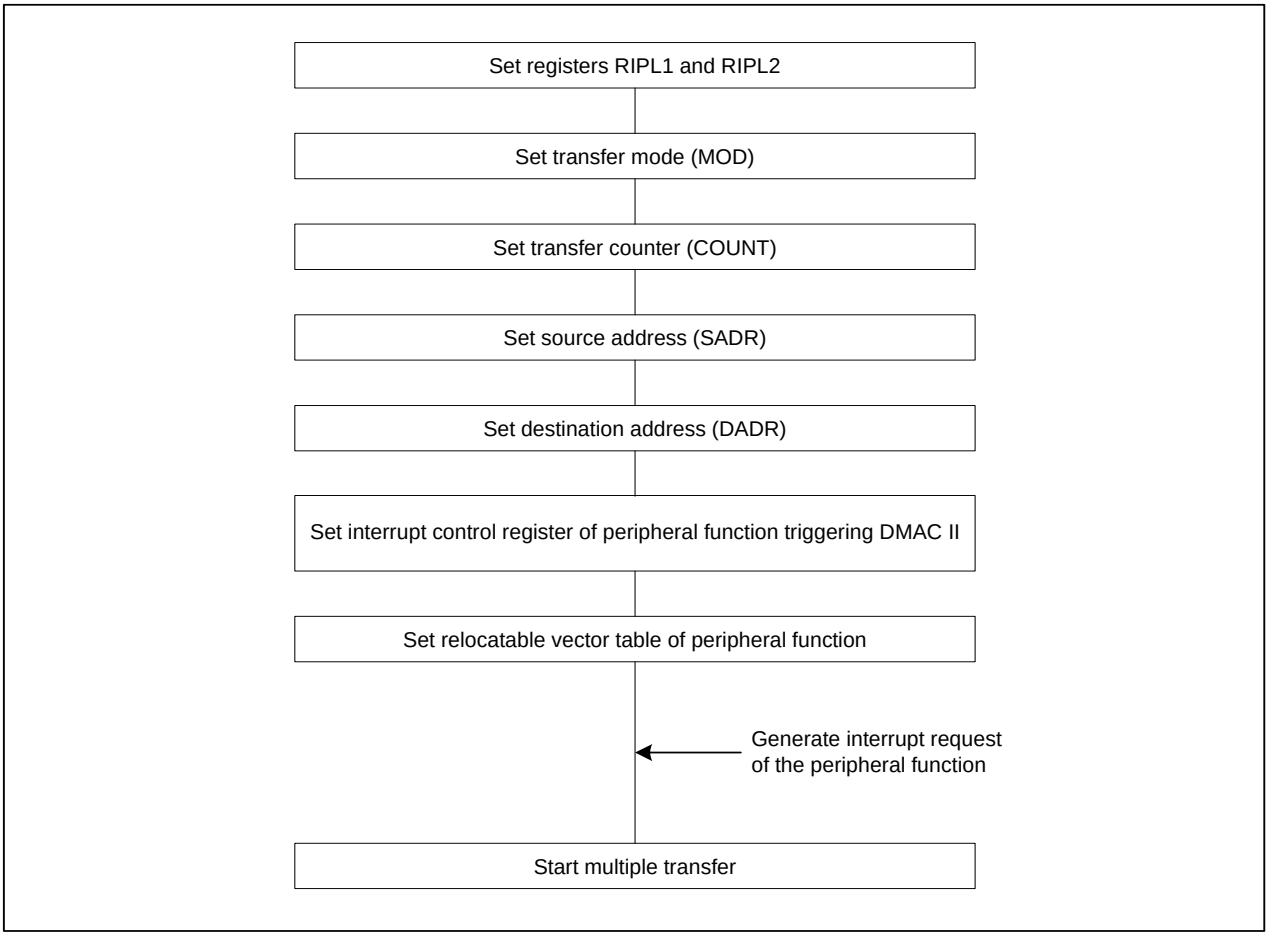
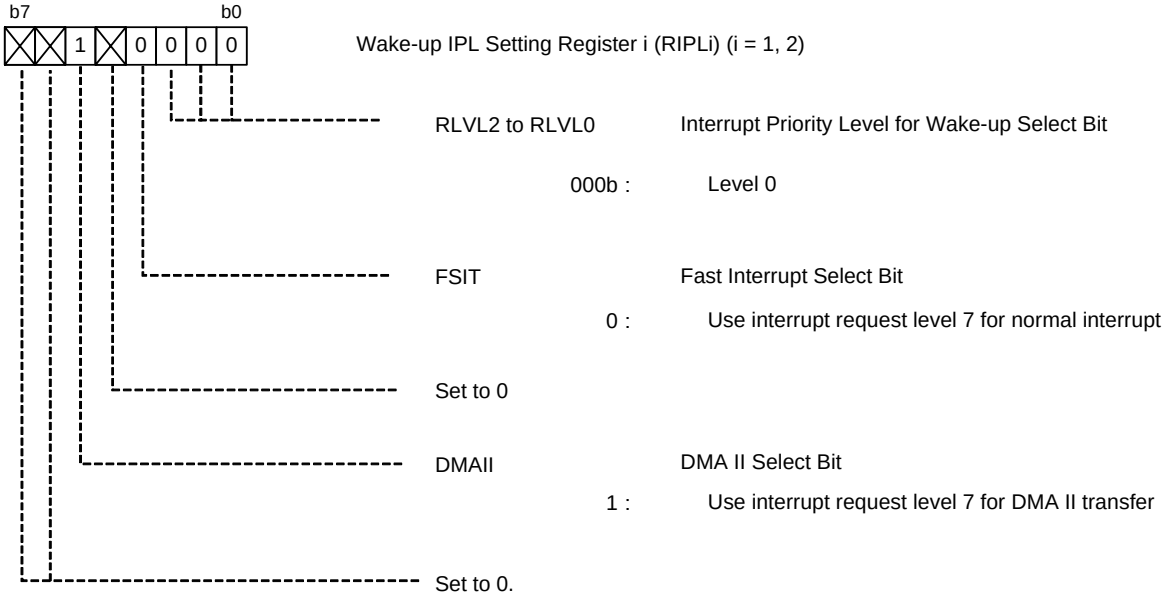


Figure 4.3 Setting Procedure for DMAC II Multiple Transfer

4.3 Register Settings

Set registers RIPL1 and RIPL2.



Registers RIPL1 and RIPL2 should be identically set

Bits ILVL2 to ILVL0 in the interrupt control register should be set after the DMAII bit is set
The DMA II transfer is not affected by the I flag or the IPL

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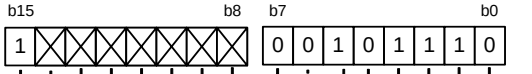
Set the transfer mode (MOD).



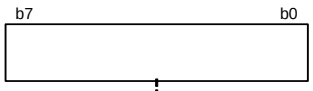
Transfer Mode (MOD) — The MOD should be allocated on the RAM

- SIZE — Transfer Size Select Bit
  - 0: 8 bits
- IMM — Reserved
  - Set to 1
- UPDS — Source Addressing Select Bit
  - 1: Incrementing addressing
- UPDD — Destination Addressing Select Bit
  - 1: Incrementing addressing
- CNT2 to CNT0 — Transfer Number Set Bit
  - 001b: Once
  - 010b: Twice
  - ⋮ Do not set bits CNT2 to CNT0 to 000b.
  - 110b: Six times
  - 111b: Seven times
- CHAIN — Reserved
  - Set to 0
- Set to 0
- MULT — Multiple Transfer Select Bit
  - 1: Used

As shown above, when the MULT bit is 0, bits b4 to b6 are OPER, BRST, and INTE, respectively. When the MULT bit is 1, bits b4 to b6 become CNT0, CNT1, and CNT2, respectively

Set bits CNT2 to CNT0 to select the number of multiple transfers

Set the transfer counter (COUNT).



Transfer Counter (COUNT)

When transfer counter is set to 0000h, data transfer is not performed.

Set the number of transfers to be performed.

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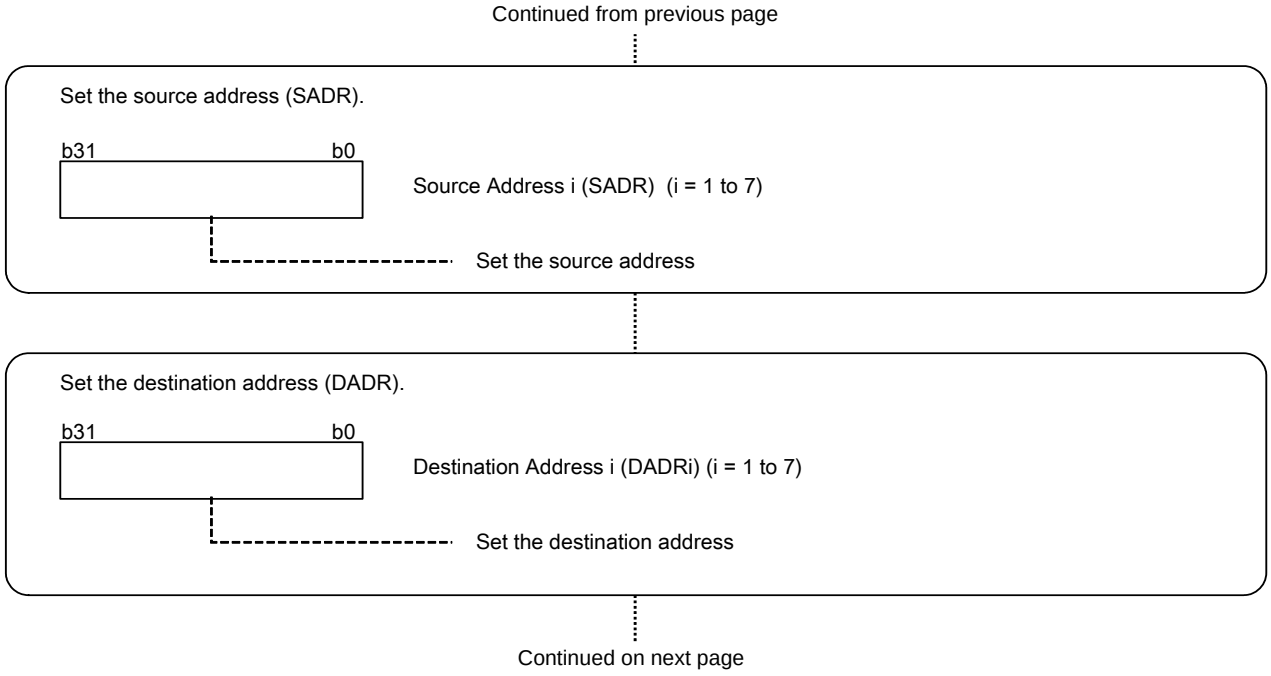
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Set the source address (SADR).
b31
b0
Source Address i (SADR) (i = 1 to 7)
Set the source address
Set the destination address (DADR).
b31
b0
Destination Address i (DADRi) (i = 1 to 7)
Set the destination address
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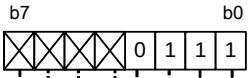
Set the control registers for the peripheral interrupt triggering DMAC II.
In registers used for the peripheral interrupt triggering DMAC II, bits ILVL2 to ILVL0 should be set to 111b (level 7)



Interrupt Control Register

TA0IC to TA4IC, TB0IC to TB5IC, S0TIC to S8TIC, S0RIC to S8RIC, BCN0IC to BCN6IC, DM0IC to DM3IC, AD0IC, KUPIC, IIO0IC to IIO11IC, I2CIC, I2CLIC, C0FTIC to C1FTIC, C0FRIC to C1FRIC, C0TIC to C1TIC, C0RIC to C1RIC, C0EIC to C1EIC, C0WIC to C1WIC

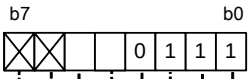
ILV2 to ILV0 Interrupt Request Level Select Bit

111b : Level 7

IR Interrupt Request Flag (1)

0 : No interrupt requested

Set to 0.



Interrupt Control Register (INT0IC to INT8IC)

ILV2 to ILV0 Interrupt Request Level Select Bit

111b : Level 7

IR Interrupt Request Flag (1)

0 : No interrupt requested

POL Polarity Select Bit (2)

0 : Select the falling edge or a low

1 : Select the rising edge or a high

LVS Level/Edge Sensitive Select Bit (3)

0 : Edge sensitive

1 : Level sensitive

Set to 0.

Notes:
1. Set the IR bit to 0.
2. This bit should be set to 0 (the falling edge or low level) to set the corresponding bit in registers IFSR0 and IFSR1 to 1 (both edges).
3. To select the level sensitive, the corresponding bit in registers IFSR0 and IFSR1 should be set to 0 (one edge)

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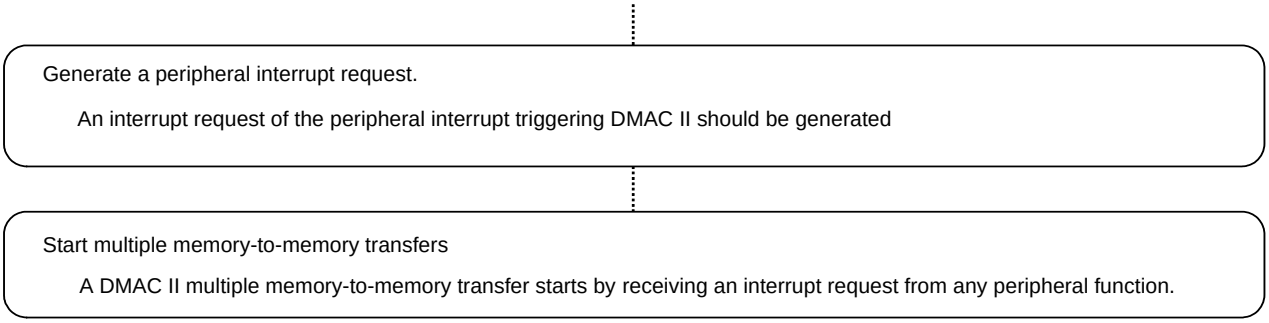

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5.1 Program Flowchart

The sample program is comprised of the main function.
Figure 5.1 shows the Main Function Flowchart.

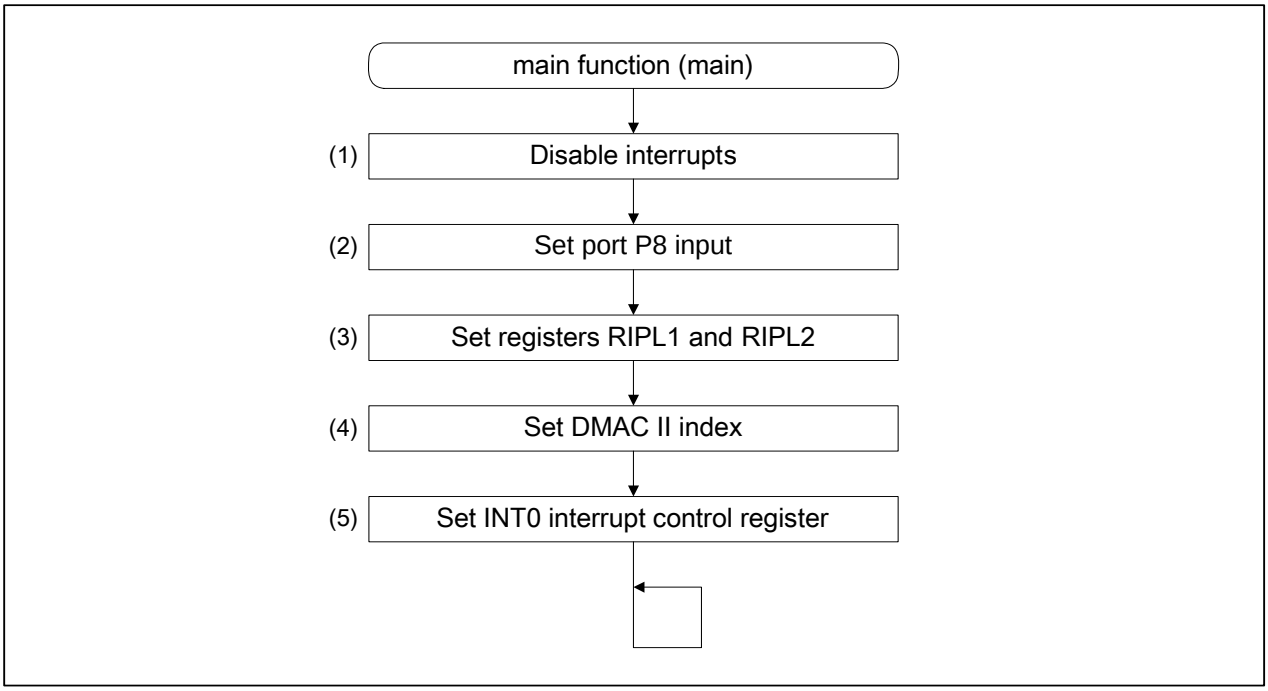

Figure 5.1 Main Function Flowchart

6. Reference Documents

User's Manual
R32C/118 Group User's Manual Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C compiler manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R32C/100 Series DMA II Setting Example (Multiple Transfer)

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		Page	Summary
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1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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