RX671 Group, RX66N Group

Differences Between the RX671 Group and the RX66N Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX671 Group and RX66N Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 145-pin package version of the RX671 Group and the 224-pin package version of the RX66N Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX671 Group and RX66N Group

Contents

1. Comparison of Built-In Functions of RX671 Group and RX66N Group

A comparison of the built-in functions of the RX671 Group and RX66N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX671 Group and RX66N Group.

Table 1.1 Comparison of Built-In Functions of RX671 Group and RX66N Group

Function	RX66N	RX671
CPU	○	
Operating mode	■	
Address space	●/■	
Resets	○	
Option-setting memory (OFSM)	▲	
Voltage detection circuit (LVDA)	○	
Clock generation circuit	●/■	
Clock frequency accuracy measurement circuit (CAC)	■	
Low power consumption function	●/■	
Battery backup function (VBATTB)	●	
Register write protection function	▲/●	
Exception handling	○	
Interrupt controller (ICUD): RX66N, (ICUE): RX671	●/■	
Buses	●/■	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa): RX66N, (DMACAb): RX671	●	
EXDMA controller (EXDMACa)	○	
Data transfer controller (DTCb)	○	
Event link controller (ELC)	■	
I/O ports	●	
Multi-function pin controller (MPC)	●/■	
Multi-function timer pulse unit 3 (MTU3a)	○	
Port output enable 3 (POE3a)	■	
General PWM timer (GPTW)	○	×
GPTW port output enable (POEG)	○	×
16-bit timer pulse unit (TPUa)	○	
Programmable pulse generator (PPG)	○	
8-bit timer (TMR): RX66N, (TMRb): RX671	●	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	○	
Realtime clock (RTCd)	○	
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	○	
Ethernet controller (ETHERC)	○	×
DMA controller for the ethernet controller (EDMACa)	○	×
PHY management interface (PMGI)	○	×
USB 2.0 FS Host/Function module (USBb)	●	
Serial communications interface (SCIj, SCIi, SCIh): RX66N, (SCIk, SCIm, SCIh): RX671	●	
Serial communications interface (RSCI)	×	○
I²C bus interface (RIICa)	○	

Function	RX66N	RX671
High-speed I²C bus interface (RIICHS)	×	○
CAN module (CAN)	●	
Serial peripheral interface (RSPIc): RX66N, (RSPId): RX671	●	
Serial peripheral interface (RSPIA)	×	○
Quad serial peripheral interface (QSPI): RX66N, quad SPI memory interface (QSPIX): RX671	●	
CRC calculator (CRCA)	○	
Serial sound interface (SSIE)	■	
SD host interface (SDHI)	○	
Multimedia card interface (MMCIF)	○	×
Parallel data capture unit (PDC)	○	×
Graphic LCD controller (GLCDC)	○	×
2D drawing engine (DRW2D)	○	×
Remote control signal receiver (REMCa)	×	○
Capacitive touch sensing unit (CTSUa)	×	○
Boundary scan	▲	
Trusted Secure IP (TSIP)	○	
12-bit A/D converter (S12ADFa)	■	
12-bit D/A converter (R12DAa)	○	×
Temperature sensor (TEMPS)	○	
Data operation circuit (DOC): RX66N, (DOCA): RX671	●	
RAM	■	
Standby RAM	■	
Flash memory (FLASH)	▲/■	
Packages	●/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 Operating Modes

Table 2.1 is a comparison of operating mode registers.

Table 2.1 Comparison of Operating Mode Registers

Register	Bit	RX66N	RX671
SYSCR1	ECCRAME	ECCRAM enable bit	—

2.2 Address Space

Figure 2.1 is a comparative memory map of single-chip mode, Figure 2.2 is a comparative memory map of on-chip ROM enabled extended mode, and Figure 2.3 is a comparative memory map of on-chip ROM disabled extended mode.

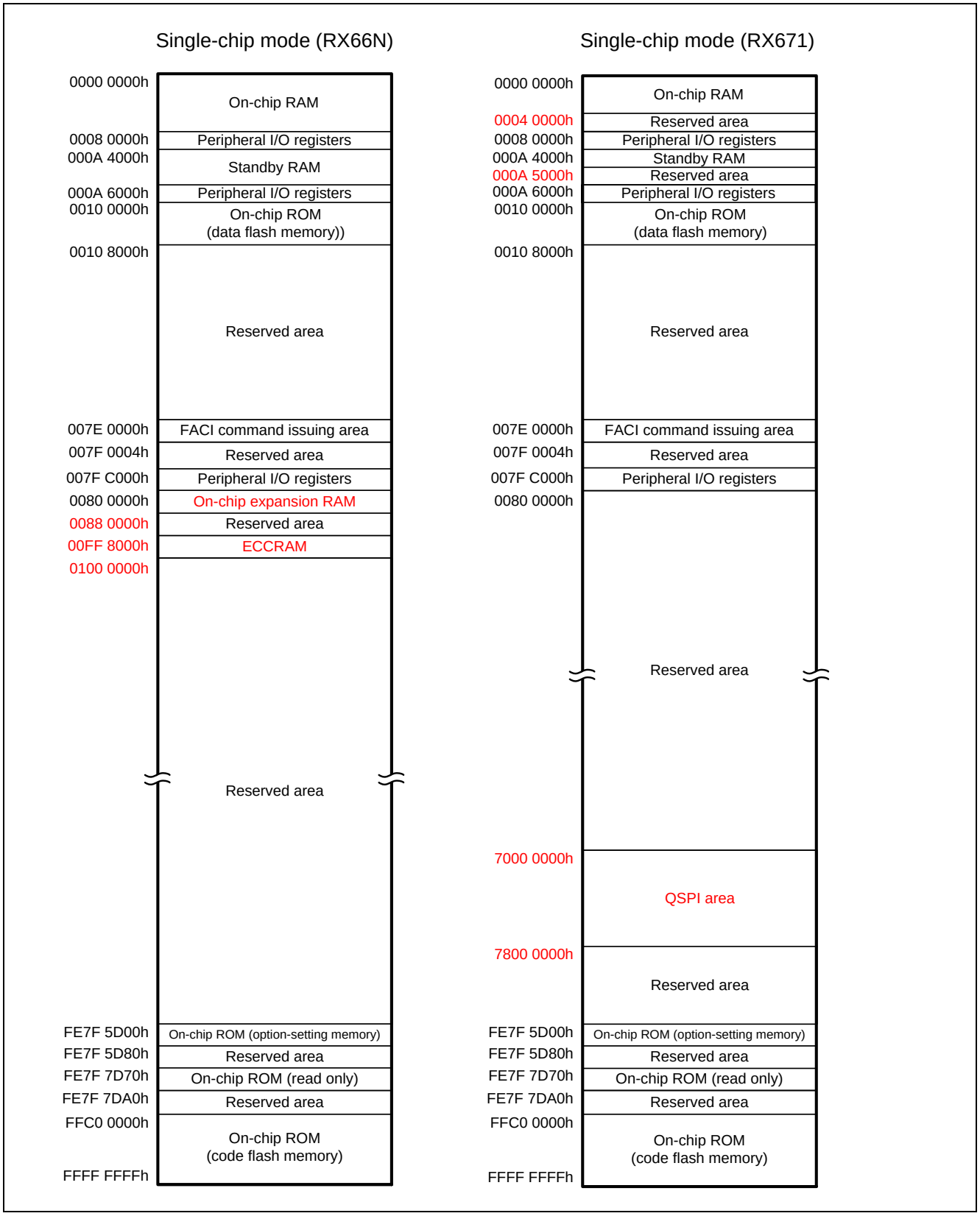

Figure 2.1 Comparative Memory Map of Single-Chip Mode

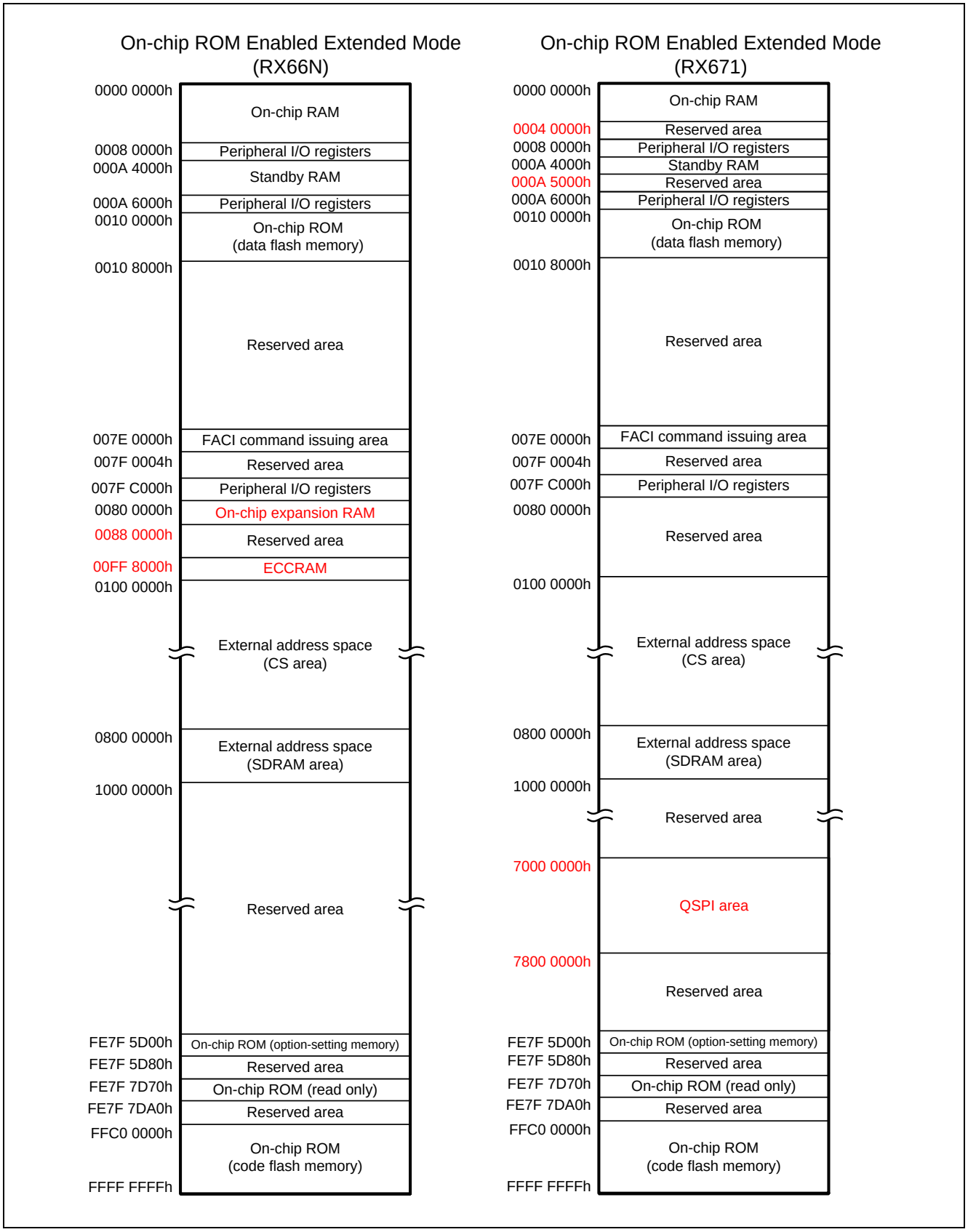

Figure 2.2 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

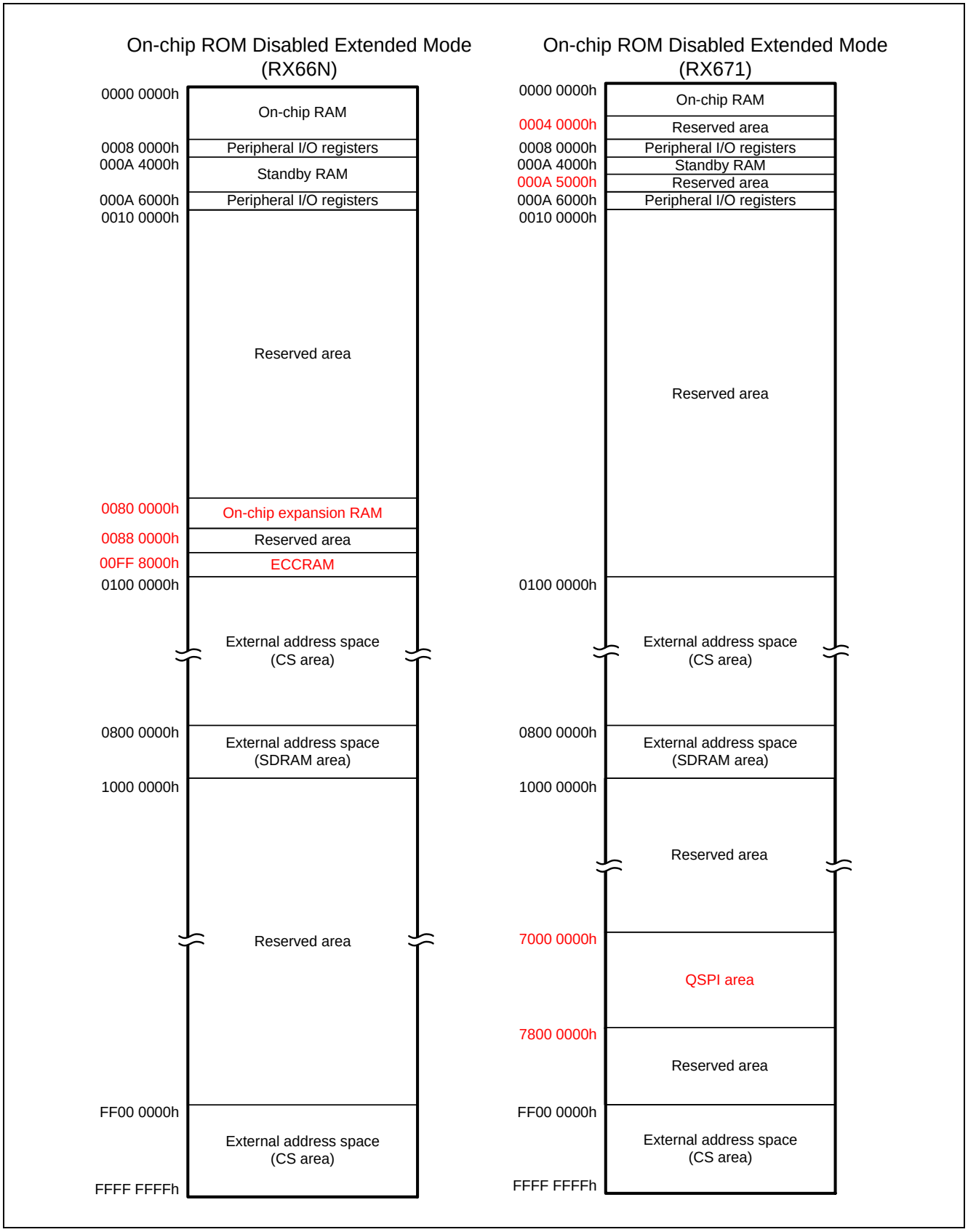

Figure 2.3 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

2.3 Option-Setting Memory

Table 2.2 is a comparison of option-setting memory registers.

Table 2.2 Comparison of Option-Setting Memory Registers

Register	Bit	RX66N (OFSM)	RX671 (OFSM)
SPCC	OCDE	—	On-chip debugger connection enable bit
TMEF	TMEFDB[2:0]	Dual-bank TM enable bits b30 b28 0 0 0: The TM function for blocks 78 and 79 in the code flash memory is enabled in dual mode. 1 1 1: The TM function for blocks 78 and 79 in the code flash memory is disabled in dual mode. Settings other than the above are prohibited.	Dual-bank TM enable bits b30 b28 0 0 0: The TM function for blocks 46 and 47 in the code flash memory is enabled in dual mode. 1 1 1: The TM function for blocks 46 and 47 in the code flash memory is disabled in dual mode. Settings other than the above are prohibited.
BANKSEL	BANKSWP[2:0]	Startup bank switch bits b2 b0 0 0 0: These bits specify the address range of bank 1 from FFE0 0000h to FFFF FFFFh and bank 0 from FFC0 0000h to FFDF FFFFh. 1 1 1: These bits specify the address range of bank 1 from FFC0 0000h to FFDF FFFFh and bank 0 from FFE0 0000h to FFFF FFFFh. Settings other than the above are prohibited.	Startup bank switch bits b2 b0 0 0 0: These bits specify the address range of bank 1 from FFF0 0000h to FFFF FFFFh and bank 0 from FFE0 0000h to FFEF FFFFh. 1 1 1: These bits specify the address range of bank 1 from FFE0 0000h to FFEF FFFFh and bank 0 from FFF0 0000h to FFFF FFFFh. Settings other than the above are prohibited.

2.4 Clock Generation Circuit

Table 2.3 is a comparative overview of the clock generation circuits, and Table 2.4 is a comparison of clock generation circuit registers.

Table 2.3 Comparative Overview of Clock Generation Circuits

Item	RX66N	RX671
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU, GLCDC, DRW2D, PMGI, and GPTW. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the external bus clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, QSPIX, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, SCIm, RSCI, MTU, and RIICHS. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (ADCLK = PCLKC (unit 0), PCLKD (unit 1)) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the external bus clock (SDCLK) to be supplied to the SDRAM. Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the REMC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC. • Generates the VBATT clock (VBATCLK) to be supplied to the VBATT. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX66N	RX671
Operating frequency	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 80 MHz (max.) • SDCLK pin output: 80 MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT25M pin output: 25 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 1 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.)*1 • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 1 kHz to 16 MHz • REMSCLK: 32.768 kHz • VBATCLK: 32.768 kHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 30 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU and GPTW pins can be forcedly driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU pin can be forcedly driven high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT

Item	RX66N	RX671
PLL frequency synthesizer	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
PLL frequency synthesizer for specific purposes (PPLL)	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	—
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function • Support for user trimming
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2
Control of output on SDCLK pin	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Note: 1. The contents of the ROMWT register must be changed when the ICLK frequency is greater than 60 MHz.

Table 2.4 Comparison of Clock Generation Circuit Registers

Register	Bit	RX66N	RX671
SCKCR	BCK[3:0]	External bus clock (BCLK) select bits b19 b16 0 0 0 0: ×1/1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 1 0 0 1: ×1/3 Settings other than the above are prohibited.	External bus clock (BCLK) select bits b19 b16 0 0 0 0: ×1/1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than the above are prohibited.
PLLCR	PLLSRCSEL	PLL Clock Source Select*1 0: Main clock oscillator 1: HOCO	PLL Clock Source Select 0: Main clock oscillator 1: HOCO*2
ROMWT	—	—	ROM wait cycle setting register
OSCOVFSR	PPLOVF	PPLL clock oscillation stabilization flag	—
CKOCR	CKOSEL[2:0]	CLKOUT output source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit 1 1 0: PPLL circuit Settings other than the above are prohibited.	CLKOUT output source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.
PACKCR	—	Specific-use clock control register	—
PPLLCR	—	PPLL control register	—
PPLLCR2	—	PPLL control register 2	—
PPLLCR3	—	PPLL control register 3	—
SOSCCR2	—	—	Sub-clock oscillator control register 2
BKSCCR	—	—	Backup area sub-clock control register
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0 to 2)

Note: 1. Set this bit to 0 when using the USB.
Note: 2. When using USB, be sure to enable the FLL function.

2.5 Clock Frequency Accuracy Measurement Circuit

Table 2.5 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.6 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.5 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX66N (CAC)	RX671 (CAC)
Measurement target clocks	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.6 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX66N (CAC)	RX671 (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M)	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M)	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.6 Low Power Consumption

Table 2.7 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.8 is a comparison of low power consumption registers.

Table 2.7 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX66N	RX671
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PPLL	Operation possible	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM, expansion RAM, and ECCRAM: RX66N RAM: RX671	Operation possible (retained)	Operation possible (retained)
	Standby RAM	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USBFS Host/Function module (USB)	Operation possible	Operation possible
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX66N	RX671
All-module clock stop mode	PPLL	Operation possible	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM, expansion RAM, and ECCRAM: RX66N RAM: RX671	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS Host/Function module (USB)	Stopped	Stopped
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible*1	Operation possible*1
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	PPLL	Stopped	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM, expansion RAM, and ECCRAM: RX66N RAM: RX671	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS Host/Function module (USB)	Stopped	Stopped
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX66N	RX671
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)
	PLL	Stopped	Stopped
	PPLL	Stopped	—
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM, expansion RAM, and ECCRAM: RX66N RAM: RX671	Stopped (undefined)	Stopped (undefined)
	Standby RAM	Stopped (retained/undefined)	Stopped (retained/undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS Host/Function module (USB)	Stopped (retained/undefined)	Stopped (retained/undefined)
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE)	Stopped (undefined)	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

Table 2.8 Comparison of Low Power Consumption Registers

Register	Bit	RX66N	RX671
MSTPCRA	MSTPA7	General PWM timer/GPTW dedicated port output enable module stop bit	—
	MSTPA19	12-bit D/A converter module stop bit	—
MSTPCRB	MSTPB2	CAN module 2 module stop bit	—
	MSTPB15	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 0) modules stop bit	—
	MSTPB18	—	USB 2.0 FS interface 1 module stop bit*1
	MSTPB22	Parallel data capture unit module stop bit	—
MSTPCRC	MSTPC2	Expansion RAM module stop bit	—
	MSTPC6	ECCRAM module stop bit	—
	MSTPC23	Quad serial peripheral interface module stop bit	—
	MSTPC28	2D drawing engine module stop bit	—
	MSTPC29	Graphic-LCD controller module stop bit	—
MSTPCRD	—	Module stop control register D	Module stop control register D
		Initial values after a reset are different.	
	MSTPD0	Module stop D0 bit	—
	MSTPD1	Module stop D1 bit	Quad SPI memory interface module stop bit
	MSTPD2	Module stop D2 bit	Serial communication interface 11 module stop bit
	MSTPD3	Module stop D3 bit	Serial communication interface 10 module stop setting bit
	MSTPD4	Module stop D4 bit	—
	MSTPD5	Module stop D5 bit	High-speed I^2C bus interface module stop bit
	MSTPD6	Module stop D6 bit	—
	MSTPD7	Module stop D7 bit	Remote control signal receiver module stop bit
	MSTPD12	—	Capacitive touch sensing unit module stop bit
	MSTPD14	Extended serial sound interface 1 module stop bit	—
MSTPCRD	MSTPD21	MMC host interface module stop bit	—
	MSTPD26	—	Serial peripheral interface module stop setting bit
DPSIER3	DRMCIE	—	REMC interrupt deep standby cancel signal enable bit
	DTADIE	—	VBATT tamper detection deep standby cancel signal enable bit
DPSIFR3	DRMCIF	—	Deep standby cancel by REMC interrupt flag
	DTADIF	—	VBATT tamper detection deep standby cancel flag
DPSBKRy	—	Deep standby backup register y (y = 0 to 31)	—

Note: 1. When transitioning to software standby mode after writing a new value to the STPB18 bit, execute a WAIT instruction after two cycles of the USB clock (UCLK) have elapsed since the write.

2.7 Battery Backup Function

Table 2.9 is a comparative overview of the battery backup functions, and Table 2.10 is a comparison of battery backup function registers.

Table 2.9 Comparative Overview of Battery Backup Functions

Item	RX66N	RX671 (VBATTB)
Backup target	• Sub-clock oscillator • Realtime clock (RTC)	All modules in the backup area • Backup register • Sub-clock oscillator • Power-down detection circuit • Tamper detection circuit • Realtime clock (RTC)
Backup register	—	128 bytes Can be erased immediately when tamper detection occurs.
Backup area power-down detection	—	Generates a backup area reset signal when the power supply voltage to the backup area drops.
Tamper event detection	—	Detects unauthorized access to the system, and provides notification by setting a flag or generating an interrupt. • A timestamp can be obtained when tamper detection occurs. • Tamper input pins: 3 (TAMPI0 to TAMPI2) • Built-in noise filter (sampling rate: 32.768 kHz, three-match detection) • Can be used as a source for triggering return from deep software standby mode.

Table 2.10 Comparison of Battery Backup Function Registers

Register	Bit	RX66N	RX671 (VBATTB)
BKPSR	—	—	Backup area power supply status register
TAMPSR	—	—	Tamper status register
TAMPCR	—	—	Tamper control register
TCECR	—	—	Time capture event control register
TAMPICR1	—	—	Tamper/RTCIC input control register 1
TAMPICR2	—	—	Tamper/RTCIC input control register 2
TAMPIMR	—	—	Tamper/RTCIC input monitor register
BKRn	—	—	Backup register n (n = 0 to 127)

2.8 Register Write Protection Function

Table 2.11 is a comparative overview of the register write protection functions.

Table 2.11 Comparative Overview of Register Write Protection Functions

Item	RX66N	RX671
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PACKCR PLLCR, PLLCR2, PPLLCR, PPLLCR2, PPLLCR3, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, CKOCR	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, CKOCR, FLLCR1, FLLCR2, HOCOTRR0, HOCOTRR1, HOCOTRR2, CTSUTRMR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR • Registers related to battery backup: BKSCCR, BKPSR, SOSCCR2, TAMPSR, TAMPCR, TCECR, TAMPICR1, TAMPICR2, TAMPIMR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Interrupt Controller

Table 2.12 is a comparative overview of the interrupt controllers, and Table 2.13 is a comparison of interrupt controller registers.

Table 2.12 Comparative Overview of Interrupt Controllers

Item		RX66N (ICUD)	RX671 (ICUE)
Interrupts	Peripheral function interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX66N (ICUD)	RX671 (ICUE)
Interrupts	External pin interrupts	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of sources: 2	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt occurs at detection of main clock oscillation having stopped.	Interrupt occurs at detection of main clock oscillation having stopped.
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.

Item		RX66N (ICUD)	RX671 (ICUE)
Non-maskable interrupts	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in the RAM (including the expansion RAM) or an ECC error is detected in the ECCRAM.	Interrupt occurs when a parity check error is detected in the RAM.
	Double-precision floating-point exceptions	Exceptions from double-precision floating-point coprocessor	Exceptions from double-precision floating-point coprocessor
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB0 resume, RTC alarm, RTC period, IWDT, VBATT tamper detection, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB0 resume, RTC alarm, RTC period, IWDT, VBATT tamper detection, REMC interrupt).
	Deep software standby mode	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB0 resume, RTC alarm, RTC period, VBATT tamper detection, REMC interrupt).

Table 2.13 Comparison of Interrupt Controller Registers

Register	Bit	RX66N (ICUD)	RX671 (ICUE)
GRPBL2	—	Group BL2 interrupt request register	—
GENBL2	—	Group BL2 interrupt request enable register	—
PIBRk	—	Software configurable interrupt B request register k (k = 0h to Bh)	Software configurable interrupt B request register k (k = 0h to Ch)
PIARk	—	Software configurable interrupt A request register k (k = 0h to Ah, Ch)	Software configurable interrupt A request register k (k = 0h to 5h, Bh)

2.10 Buses

Table 2.14 is a comparative overview of the buses, Table 2.15 is a comparative overview of the external buses, and Table 2.16 is a comparison of bus registers.

Table 2.14 Comparative Overview of Buses

Item		RX66N	RX671
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Connected to expansion RAM, ECCRAM	—
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC, DMAC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)

Item		RX66N	RX671
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USB, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USB, DOC, CTSU, REMC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC, PMGI, GPTW, MTU, SCIi, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (MTU, SCIm, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	• Connected to peripheral modules (GLCDC and DRW2D) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (RSCI, RSPIA, and RIICHS) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)
Internal expansion bus	QSPI area	—	• Connected to external SPI devices • Operates in synchronization with the system clock (ICLK)

Table 2.15 Comparative Overview of External Buses

Item	RX66N	RX671
External address space	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be selected independently for each area. — Separate bus: An 8, 16, or 32-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be selected independently for each area.	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be selected independently for each area. — Separate bus: An 8 or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be selected independently for each area.
CS area controller	• Recovery cycles can be inserted. — Up to 15 cycles for read recovery — Up to 15 cycles for write recovery • Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access). • Wait control — Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#) — Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR# to WR3#) — Ability to specify data output start and end timing • Write access mode: Single write strobe mode or byte strobe mode • Separate bus or address/data multiplexed bus can be specified for each area.	• Recovery cycles can be inserted. — Up to 15 cycles for read recovery — Up to 15 cycles for write recovery • Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access). • Wait control — Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#) — Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1#) — Ability to specify data output start and end timing • Write access mode: Single write strobe mode or byte strobe mode • Separate bus or address/data multiplexed bus can be specified for each area.
SDRAM area controller	• Multiplexed output of row address/ column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh • CAS latency can be specified from one to three cycles.	• Multiplexed output of row address/ column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh • CAS latency can be specified from one to three cycles.
Write buffer function	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.
Frequencies	• The CS area controller (CSC) operates in synchronization with BCLK. • The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.	• The CS area controller (CSC) operates in synchronization with BCLK. • The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.

Table 2.16 Comparison of Bus Registers

Register	Bit	RX66N	RX671
CSnCR (n = 0 to 7)	BSIZE[1:0]	External bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited.	External bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: Setting prohibited. 1 0: 8-bit bus space selected 1 1: Setting prohibited.
SDCCR	BSIZE[1:0]	SDRAM bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited.	SDRAM bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: Setting prohibited. 1 0: 8-bit bus space selected 1 1: Setting prohibited.
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Extended bus master 1 1 1: EXDMAC	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: EXDMAC
BUSPRI	BPRA[1:0]	Memory bus 1 and 3 (RAM/expansion RAM) priority control bits	Memory bus 1 (RAM) priority control bits
	BPXB[1:0]	—	Internal expansion bus priority control bits
EBMAPCR	—	Extended bus master priority control register	—

2.11 DMA Controller

Table 2.17 is a comparative overview of the DMA controllers, and Table 2.18 is a comparison of DMA controller registers.

Table 2.17 Comparative Overview of DMA Controllers

Item		RX66N (DMACAa)	RX671 (DMACAb)
Number of channels		8 channels (DMACm (m = 0 to 7))	8 channels (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	4 GB (00000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		64 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)	64 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	Single data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,024 data units	Number of data units: 1 to 1,024 data units
Transfer modes	Normal transfer mode	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units
	Block transfer mode	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended

Item		RX66N (DMACAa)	RX671 (DMACAb)
		repeat area for transfer source or destination	repeat area for transfer source or destination
Interrupt request	Transfer end interrupt	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link function		Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.18 Comparison of DMA Controller Registers

Register	Bit	RX66N (DMACAa)	RX671 (DMACAb)
DMSAR	—	DMA source address register Specifies the start address of the transfer source. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA source address register Specifies the start address of the transfer source. 00000000h to FFFFFFFFh (4 GB)
DMDAR	—	DMA destination address register Specifies the start address of the transfer destination. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA destination address register Specifies the start address of the transfer destination. 00000000h to FFFFFFFFh (4 GB)

2.12 Event Link Controller

Table 2.19 is a comparative overview of the event link controllers, Table 2.20 is a comparison of event link controller registers, Table 2.21 lists correspondences between ELSRn registers and peripheral modules, and Table 2.22 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.19 Comparative Overview of Event Link Controllers

Item	RX66N (ELC)	RX671 (ELC)
Event link function	• 123 event signals can be directly connected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be enabled on a single port corresponding to the specified bit. — Port group*1: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.	• 99 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be specified on a single port. — Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Note: 1. An event is generated when the corresponding input signal on a single port or port group set to input changes.

Table 2.20 Comparison of Event Link Controller Registers

Register	Bit	RX66N (ELC)	RX671 (ELC)
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45, and 48 to 57)	Event link setting register n (n = 0, 3, 4, 7, 10 to 15, 18 to 28, 33, 35 to 38, and 45)
	ELS[7:0]	Event link select bits 00h: Event output to the corresponding peripheral module is disabled. 01h to CDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to DFh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.

Table 2.21 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX66N (ELC)	RX671 (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR14	—	CTSU
ELSR15	S12AD (ELCTRG00N)	S12AD
ELSR16	DA0	—
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR33	CMTW0	CMTW0
ELSR35	TPU0	TPU0
ELSR36	TPU1	TPU1
ELSR37	TPU2	TPU2
ELSR38	TPU3	TPU3
ELSR45	S12AD1 (ELCTRG1N)	S12AD1
ELSR48	GPTW event source A (common to all channels)	—
ELSR49	GPTW event source B (common to all channels)	—
ELSR50	GPTW event source C (common to all channels)	—
ELSR51	GPTW event source D (common to all channels)	—
ELSR52	GPTW event source E (common to all channels)	—
ELSR53	GPTW event source F (common to all channels)	—
ELSR54	GPTW event source G (common to all channels)	—
ELSR55	GPTW event source H (common to all channels)	—
ELSR56	S12AD (ELCTRG01N)	—
ELSR57	S12AD1 (ELCTRG11N)	—

Table 2.22 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX66N (ELC)	RX671 (ELC)
01h	Multifunction timer pulse unit 3	MTU0 compare match 0A	MTU0 compare match 0A
02h		MTU0 compare match 0B	MTU0 compare match 0B
03h		MTU0 compare match 0C	MTU0 compare match 0C
04h		MTU0 compare match 0D	MTU0 compare match 0D
05h		MTU0 compare match 0E	MTU0 compare match 0E
06h		MTU0 compare match 0F	MTU0 compare match 0F
07h		MTU0 overflow	MTU0 overflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
25h		TMR1 compare match A1	TMR1 compare match A1
26h		TMR1 compare match B1	TMR1 compare match B1
27h		TMR1 overflow	TMR1 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Bh		TMR3 compare match A3	TMR3 compare match A3
2Ch		TMR3 compare match B3	TMR3 compare match B3
2Dh		TMR3 overflow	TMR3 overflow
2Eh	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	Peripheral Module	RX66N (ELC)	RX671 (ELC)
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h		RSPI0 idle	RSPI0 idle
54h		RSPI0 receive data full	RSPI0 receive buffer full
55h		RSPI0 transmit data empty	RSPI0 transmit buffer empty
56h		RSPI0 transmit end	RSPI0 communication end
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit
63h	I/O ports	Input edge detection of input port group 1	Input edge detection of input port group 1
64h		Input edge detection of input port group 2	Input edge detection of input port group 2
65h		Input edge detection of single input port 0	Input edge detection of single input port 0
66h		Input edge detection of single input port 1	Input edge detection of single input port 1
67h		Input edge detection of single input port 2	Input edge detection of single input port 2
68h		Input edge detection of single input port 3	Input edge detection of single input port 3
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met
6Ch	12-bit A/D converter	S12AD1 A/D conversion end	S12AD1 A/D conversion end
7Eh	Compare match timer W	CMTW channel 0 compare match	CMTW channel 0 compare match
80h	General PWM timer	GPTW0 compare match A	—
81h		GPTW0 compare match B	—
82h		GPTW0 compare match C	—
83h		GPTW0 compare match D	—
84h		GPTW0 compare match E	—
85h		GPTW0 compare match F	—
86h		GPTW0 overflow	—
87h		GPTW0 underflow	—
88h		GPTW1 compare match A	—
89h		GPTW1 compare match B	—
8Ah		GPTW1 compare match C	—
8Bh		GPTW1 compare match D	—
8Ch		GPTW1 compare match E	—

Value of ELS[7:0] Bits	Peripheral Module	RX66N (ELC)	RX671 (ELC)
8Dh	General PWM timer	GPTW1 compare match F	—
8Eh		GPTW1 overflow	—
8Fh		GPTW1 underflow	—
90h		GPTW2 compare match A	—
91h		GPTW2 compare match B	—
92h		GPTW2 compare match C	—
93h		GPTW2 compare match D	—
94h		GPTW2 compare match E	—
95h		GPTW2 compare match F	—
96h		GPTW2 overflow	—
97h		GPTW2 underflow	—
98h		GPTW3 compare match A	—
99h		GPTW3 compare match B	—
9Ah		GPTW3 compare match C	—
9Bh		GPTW3 compare match D	—
9Ch		GPTW3 compare match E	—
9Dh		GPTW3 compare match F	—
9Eh		GPTW3 overflow	—
9Fh		GPTW3 underflow	—
ACh	16-bit timer pulse unit	TPU0 compare match A	TPU0 compare match A
ADh		TPU0 compare match B	TPU0 compare match B
AEh		TPU0 compare match C	TPU0 compare match C
AFh		TPU0 compare match D	TPU0 compare match D
B0h		TPU0 overflow	TPU0 overflow
B1h		TPU1 compare match A	TPU1 compare match A
B2h		TPU1 compare match B	TPU1 compare match B
B3h		TPU1 overflow	TPU1 overflow
B4h		TPU1 underflow	TPU1 underflow
B5h		TPU2 compare match A	TPU2 compare match A
B6h		TPU2 compare match B	TPU2 compare match B
B7h		TPU2 overflow	TPU2 overflow
B8h		TPU2 underflow	TPU2 underflow
B9h		TPU3 compare match A	TPU3 compare match A
BAh		TPU3 compare match B	TPU3 compare match B
BBh		TPU3 compare match C	TPU3 compare match C
BCh		TPU3 compare match D	TPU3 compare match D
BDh		TPU3 overflow	TPU3 overflow
C6h	General PWM timer	GPTW0 A/D converter start request A	—
C7h		GPTW0 A/D converter start request B	—
C8h		GPTW1 A/D converter start request A	—
C9h		GPTW1 A/D converter start request B	—
CAh		GPTW2 A/D converter start request A	—
CBh		GPTW2 A/D converter start request B	—

Value of ELS[7:0] Bits	Peripheral Module	RX66N (ELC)	RX671 (ELC)
CCh	General PWM timer	GPTW3 A/D converter start request A	—
CDh		GPTW3 A/D converter start request B	—
D0h	Serial communications interface	—	RSCI10 error
D1h		—	RSCI10 receive data full
D2h		—	RSCI10 receive data match
D3h		—	RSCI10 transmit data empty
D4h		—	RSCI10 transmit end
D5h		—	RSCI10 receive data mismatch
D6h		—	RSCI10 valid edge detection
D7h	High-speed I^2C bus interface	—	RIICHS0 communication error, event occurrence
D8h		—	RIICHS0 receive data full
D9h		—	RIICHS0 transmit data empty
DAh		—	RIICHS0 transmit end
DBh	Serial peripheral interface	—	RSPIA0 error
DCh		—	RSPIA0 idle
DDh		—	RSPIA0 receive buffer full
DEh		—	RSPIA0 transmit buffer empty
DFh		—	RSPIA0 communication end
Settings other than the above are prohibited.			

2.13 I/O Ports

Table 2.23 is a comparative overview of the I/O ports of 145- and 144-pin products, Table 2.24 is a comparative overview of the I/O ports of 100-pin products, Table 2.25 is a comparison of I/O port functions, and Table 2.26 is a comparison of I/O port registers.

Table 2.23 Comparative Overview of I/O Ports on 145- and 144-Pin Packages

Port Symbol	RX66N (145-, 144-Pin)	RX671 (145-, 144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77*1
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5
PORTH	—	PH1, PH2
PORTJ	PJ3, PJ5	PJ3, PJ5

Note: 1. The 145-pin TFLGA (0.65 mm pitch) product does not have pins P71 and P72.

Table 2.24 Comparative Overview of I/O Ports on 100-Pin Packages

Port Symbol	RX66N (100-Pin)	RX671 (100-Pin)
PORT0	P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH1, PH2
PORTJ	PJ3	PJ3

Table 2.25 Comparison of I/O Port Functions

Item	Port Symbol	RX66N	RX671
Input pull-up	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5
	PORTG	PG0 to PG7	—
	PORTH	PH0 to PH7	PH1, PH2
	PORTJ	PJ0 to PJ3, PJ5	PJ3, PJ5
	PORTK	PK0 to PK7	—
	PORTL	PL0 to PL7	—
	PORTM	PM0 to PM7	—
	PORTN	PN0 to PN5	—
	PORTQ	PQ0 to PQ7	—
Open-drain output function	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5
	PORTG	PG0 to PG7	—
	PORTH	PH0 to PH7	PH1, PH2
	PORTJ	PJ0 to PJ3, PJ5	PJ3, PJ5
	PORTK	PK0 to PK7	—
	PORTL	PL0 to PL7	—
	PORTM	PM0 to PM7	—

Item	Port Symbol	RX66N	RX671
Open-drain output function	PORTN	PN0 to PN5	—
	PORTQ	PQ0 to PQ7	—
Drive capacity switching function	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5
	PORTG	PG0 to PG7	—
	PORTH	PH0 to PH7	PH1, PH2
	PORTJ	PJ0 to PJ3, PJ5	PJ3, PJ5
	PORTK	PK0 to PK7	—
	PORTL	PL0 to PL7	—
	PORTM	PM0 to PM7	—
	PORTN	PN0 to PN5	—
	PORTQ	PQ0 to PQ7	—
5 V tolerant	PORT0	P07	P07
	PORT1	P11 to P17	P12 to P17
	PORT2	P20, P21	P20, P21
	PORT3	P30 to P33	P30 to P33
	PORT6	P67	P67
	PORT7	—	P73
	PORTC	PC0 to PC3	PC0 to PC3
	PORTJ	—	PJ3

Table 2.26 Comparison of I/O Port Registers

Register	Bit	RX66N	RX671
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, J to N, and Q)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, and J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, J to N, and Q)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, and J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to H, J to N, and Q)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, and J)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, J to N, and Q)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, and J)
ODR0	B0	Pm0 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm0 output type select bit (m = 0 to 9, A to E, H, and J)
	B2	Pm1 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm1 output type select bit (m = 0 to 9, A to E, H, and J)
	B3	PE1 output type select bit (m = 0 to 9, A to H, J to N, and Q)	PE1 output type select bit (m = 0 to 9, A to E, H, and J)
	B4	Pm2 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm2 output type select bit (m = 0 to 9, A to E, H, and J)
	B6	Pm3 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm3 output type select bit (m = 0 to 9, A to E, H, and J)
ODR1	B0	Pm4 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm4 output type select bit (m = 0 to 8, A to F, and J)
	B2	Pm5 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm5 output type select bit (m = 0 to 8, A to F, and J)
	B4	Pm6 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm6 output type select bit (m = 0 to 8, A to F, and J)
	B6	Pm7 output type select bit (m = 0 to 9, A to H, J to N, and Q)	Pm7 output type select bit (m = 0 to 8, A to F, and J)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, J to N, and Q)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, and J)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, G, H, J to N, and Q)	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, and H)
DSCR2	B0 to B7	Pm0 to Pm7 drive capacity control bits 2 (m = 0 to 3, 5, 7 to 9, A to E, G, H, J to N, and Q)	Pm0 to Pm7 drive capacity control bits 2 (m = 0 to 3, 5, 7 to 9, A to E, and H)

2.14 Multi-Function Pin Controller

Table 2.27 is a comparison of the assignments of multiplexed pins, and Table 2.28 to Table 2.50 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **blue text** designates pins that exist on the RX671 Group only and **orange text** pins that exist on the RX66N Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented. A filled circle (●) indicates cases where all pins are present among pin functions where there is a difference in the pins present on the RX671 Group and RX66N Group.

Table 2.27 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Interrupt	NMI (input)	P35	○	○	○	○
EXDMA controller	EDREQ0 (input)	P22	○	○	○	○
		P55	○	○	○	○
		P80	○	×	○	×
	EDACK0 (output)	P54	○	○	○	○
		P23	○	○	○	○
		P81	○	×	○	×
	EDREQ1 (input)	P24	○	○	○	○
		P33	○	○	○	○
		P82	○	×	○	×
	EDACK1 (output)	P25	○	○	○	○
		P56	○	×	○	×
		P83	○	×	○	×
		PJ3	○	○	○	○
Interrupt	IRQ0-DS (input)	P30	○	○	○	○
	IRQ0 (input)	PD0	○	○	○	○
		P50	×	×	○	○
		P60	×	×	○	×
		P70	×	×	○	×
		P90	×	×	○	×
		PA0	×	×	○	○
		PH1	×	×	○	○
	IRQ1-DS (input)	P31	○	○	○	○
	IRQ1 (input)	PD1	○	○	○	○
		P51	×	×	○	○
		P61	×	×	○	×
		P71	×	×	○*2	×
		PH2	×	×	○	○
	IRQ2-DS (input)	P32	○	○	○	○
	IRQ2 (input)	P12	○	○	○	○
		PD2	○	○	○	○
		P52	×	×	○	○
		P62	×	×	○	×
		P82	×	×	○	×
		PB2	×	×	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Interrupt	IRQ3-DS (input)	P33	○	○	○	○
	IRQ3 (input)	P13	○	○	○	○
		PD3	○	○	○	○
		P23	×	×	○	○
		P53	×	×	○	○
		P63	×	×	○	×
		P83	×	×	○	×
		PB3	×	×	○	○
	IRQ4-DS (input)	PB1	○	○	○	○
	IRQ4 (input)	P14	○	○	○	○
		P34	○	○	○	○
		PD4	○	○	○	○
		PF5	○	×	○	×
		P54	×	×	○	○
		P64	×	×	○	×
		PB4	×	×	○	○
	IRQ5-DS (input)	PA4	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○
		PD5	○	○	○	○
		PE5	○	○	○	○
		P25	×	×	○	○
		PA5	×	×	○	○
		PC5	×	×	○	○
	IRQ6-DS (input)	PA3	○	○	○	○
	IRQ6 (input)	P16	○	○	○	○
		PD6	○	○	○	○
		PE6	○	○	○	○
		P26	×	×	○	○
		P56	×	×	○	×
		PB6	×	×	○	○
	IRQ7-DS (input)	PE2	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○
		PD7	○	○	○	○
		PE7	○	○	○	○
		P27	×	×	○	○
		P77	×	×	○	×
		PA7	×	×	○	○
	IRQ8-DS (input)	P40	○	○	○	○
	IRQ8 (input)	P00	○	×	○	×
		P20	○	○	○	○
		P73	×	×	○	×
		P80	×	×	○	×
		PE0	×	×	○	○
	IRQ9-DS (input)	P41	○	○	○	○
	IRQ9 (input)	P01	○	×	○	×
		P21	○	○	○	○
		P81	×	×	○	×
		P91	×	×	○	×
		PE1	×	×	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Interrupt	IRQ10-DS (input)	P42	○	○	○	○
	IRQ10 (input)	P02	○	×	○	×
		P55	○	○	○	○
		P72	×	×	○*2	×
		P92	×	×	○	×
		PA2	×	×	○	○
		PC2	×	×	○	○
	IRQ11-DS (input)	P43	○	○	○	○
	IRQ11 (input)	P03	○	×	○	×
		PA1	○	○	○	○
		P93	×	×	○	×
		PC3	×	×	○	○
		PE3	×	×	○	○
		PJ3	×	×	○	○
	IRQ12-DS (input)	P44	○	○	○	○
	IRQ12 (input)	PB0	○	○	○	○
		PC1	○	○	○	○
		P24	×	×	○	○
		P74	×	×	○	×
		PC4	×	×	○	○
		PE4	×	×	○	○
	IRQ13-DS (input)	P45	○	○	○	○
	IRQ13 (input)	P05	○	○	○	○
		PC6	○	○	○	○
		P65	×	×	○	×
		P75	×	×	○	×
		PB5	×	×	○	○
		PJ5	×	×	○	×
	IRQ14-DS (input)	P46	○	○	○	○
	IRQ14 (input)	PC0	○	○	○	○
		PC7	○	○	○	○
		P66	×	×	○	×
		P76	×	×	○	×
		P86	×	×	○	×
		PA6	×	×	○	○
	IRQ15-DS (input)	P47	○	○	○	○
	IRQ15 (input)	P07	○	○	○	○
		P67	○	×	○	×
		P22	×	×	○	○
		P87	×	×	○	×
		PB7	×	×	○	○
Multi-function timer pulse unit 3	MTIOC0A (input/output)	P34	○	○	○	○
		PB3	○	○	○	○
	MTIOC0B (input/output)	P13	○	○	○	○
		P15	○	○	○	○
		PA1	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	○	○
		PB1	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Multi-function timer pulse unit 3	MTIOC0D (input/output)	P33	○	○	○	○
		PA3	○	○	○	○
	MTIOC1A (input/output)	P20	○	○	○	○
		PE4	○	○	○	○
	MTIOC1B (input/output)	P21	○	○	○	○
		PB5	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○
		PB5	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○
		PE5	○	○	○	○
	MTIOC3A (input/output)	P14	○	○	○	○
		P17	○	○	○	○
		PC1	○	○	○	○
		PC7	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○
		P22	○	○	○	○
		P80	○	×	○	×
		PB7	○	○	○	○
		PC5	○	○	○	○
		PE1	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○
		P56	○	×	○	×
		PC0	○	○	○	○
		PC6	○	○	○	○
		PJ3	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○
		P23	○	○	○	○
		P81	○	×	○	×
		PB6	○	○	○	○
		PC4	○	○	○	○
		PE0	○	○	○	○
	MTIOC4A (input/output)	P21	○	○	○	○
		P24	○	○	○	○
		P82	○	×	○	×
		PA0	○	○	○	○
		PB3	○	○	○	○
		PE2	○	○	○	○
	MTIOC4B (input/output)	P17	○	○	○	○
		P30	○	○	○	○
		P54	○	○	○	○
		PC2	○	○	○	○
		PD1	○	○	○	○
		PE3	○	○	○	○
	MTIOC4C (input/output)	P25	○	○	○	○
		P83	○	×	○	×
		P87	○	×	○	×
		PB1	○	○	○	○
		PE1	○	○	○	○
		PE5	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Multi-function timer pulse unit 3	MTIOC4D (input/output)	P31	○	○	○	○
		P55	○	○	○	○
		P86	○	×	○	×
		PC3	○	○	○	○
		PD2	○	○	○	○
		PE4	○	○	○	○
	MTIC5U (input)	P12	×	×	○	○
		PA4	○	○	○	○
		PD7	○	○	○	○
	MTIC5V (input)	PA6	○	○	○	○
		PD6	○	○	○	○
	MTIC5W (input)	PB0	○	○	○	○
		PD5	○	○	○	○
	MTIOC6A (input/output)	PE7	○	○	○	○
	MTIOC6B (input/output)	PA5	○	○	○	○
	MTIOC6C (input/output)	PE6	○	○	○	○
	MTIOC6D (input/output)	PA0	○	○	○	○
	MTIOC7A (input/output)	PA2	○	○	○	○
	MTIOC7B (input/output)	PA1	○	○	○	○
	MTIOC7C (input/output)	P67	○	×	○	×
	MTIOC7D (input/output)	P66	○	×	○	×
	MTIOC8A (input/output)	PD6	○	○	○	○
	MTIOC8B (input/output)	PD4	○	○	○	○
	MTIOC8C (input/output)	PD5	○	○	○	○
	MTIOC8D (input/output)	PD3	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○
		P24	○	○	○	○
		PA4	○	○	○	○
		PC6	○	○	○	○
		PD5	○	○	×	×
	MTCLKB (input)	P15	○	○	○	○
		P25	○	○	○	○
		PA6	○	○	○	○
		PC7	○	○	○	○
	MTCLKC (input)	P22	○	○	○	○
		PA1	○	○	○	○
		PC4	○	○	○	○
	MTCLKD (input)	P23	○	○	○	○
		PA3	○	○	○	○
		PC5	○	○	○	○
Port output enable 3	POE0# (input)	P32	○	○	○	○
		P93	○	×	○	×
		PC4	○	○	○	○
		PD1	○	○	○	○
		PD7	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Port output enable 3	POE4# (input)	P33	○	○	○	○
		P92	○	×	○	×
		PB5	○	○	○	○
		PD0	○	○	○	○
		PD6	○	○	○	○
	POE8# (input)	P17	○	○	○	○
		P30	○	○	○	○
		PD3	○	○	○	○
		PE3	○	○	○	○
		PJ5	○	×	○	×
	POE10# (input)	P32	○	○	○	○
		P34	○	○	○	○
		PA6	○	○	○	○
		PD5	○	○	○	○
	POE11# (input)	P33	○	○	○	○
		PB3	○	○	○	○
		PD4	○	○	○	○
General PWM timer W	GTADSM0 (output)	P12	○	○		
	GTADSM1 (output)	P13	○	○		
	GTETRGA (input)	P15	○	○		
	GTETRGB (input)	PA6	○	○		
	GTETRGC (input)	PC4	○	○		
	GTETRGD (input)	P14	○	○		
	GTIOC0A (input/output)	P23	○	○		
		P83	○	×		
		PA5	○	○		
		PD3	○	○		
		PE5	○	○		
	GTIOC0B (input/output)	P17	○	○		
		P81	○	×		
		PA0	○	○		
		PD2	○	○		
		PE2	○	○		
	GTIOC1A (input/output)	P22	○	○		
		PA2	○	○		
		PC5	○	○		
		PD1	○	○		
		PE4	○	○		
	GTIOC1B (input/output)	P67	○	×		
		P87	○	×		
		PC3	○	○		
		PD0	○	○		
		PE1	○	○		
	GTIOC2A (input/output)	P21	○	○		
		P82	○	×		
		PA1	○	○		
		PE3	○	○		

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
General PWM timer W	GTIOC2B (input/output)	P66	○	×		
		P86	○	×		
		PC2	○	○		
		PE0	○	○		
	GTIOC3A (input/output)	PC7	○	○		
		PE7	○	○		
	GTIOC3B (input/output)	PC6	○	○		
		PE6	○	○		
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	×	○	×
		PA0	○	○	○	○
	TIOCB0 (input/output)	P17	○	○	○	○
		PA1	○	○	○	○
	TIOCC0 (input/output)	P32	○	○	○	○
	TIOCD0 (input/output)	P33	○	○	○	○
		PA3	○	○	○	○
	TIOCA1 (input/output)	P56	○	×	○	×
		PA4	○	○	○	○
	TIOCB1 (input/output)	P16	○	○	○	○
		PA5	○	○	○	○
	TIOCA2 (input/output)	P87	○	×	○	×
		PA6	○	○	○	○
	TIOCB2 (input/output)	P15	○	○	○	○
		PA7	○	○	○	○
	TIOCA3 (input/output)	P21	○	○	○	○
		PB0	○	○	○	○
	TIOCB3 (input/output)	P20	○	○	○	○
		PB1	○	○	○	○
	TIOCC3 (input/output)	P22	○	○	○	○
		PB2	○	○	○	○
	TIOCD3 (input/output)	P23	○	○	○	○
		PB3	○	○	○	○
	TIOCA4 (input/output)	P25	○	○	○	○
		PB4	○	○	○	○
	TIOCB4 (input/output)	P24	○	○	○	○
		PB5	○	○	○	○
	TIOCA5 (input/output)	P13	○	○	○	○
		PB6	○	○	○	○
	TIOCB5 (input/output)	P14	○	○	○	○
		PB7	○	○	○	○
	TCLKA (input)	P14	○	○	○	○
		PC2	○	○	○	○
	TCLKB (input)	P15	○	○	○	○
		PA3	○	○	○	○
		PC3	○	○	○	○
	TCLKC (input)	P16	○	○	○	○
		PB2	○	○	○	○
		PC0	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
16-bit timer pulse unit	TCLKD (input)	P17	○	○	○	○
		PB3	○	○	○	○
		PC1	○	○	○	○
Programmable pulse generator	PO0 (output)	P20	○	○	○	○
	PO1 (output)	P21	○	○	○	○
	PO2 (output)	P22	○	○	○	○
	PO3 (output)	P23	○	○	○	○
	PO4 (output)	P24	○	○	○	○
	PO5 (output)	P25	○	○	○	○
	PO6 (output)	P26	○	○	○	○
	PO7 (output)	P27	○	○	○	○
	PO8 (output)	P30	○	○	○	○
	PO9 (output)	P31	○	○	○	○
	PO10 (output)	P32	○	○	○	○
	PO11 (output)	P33	○	○	○	○
	PO12 (output)	P34	○	○	○	○
	PO13 (output)	P13	○	○	○	○
		P15	○	○	○	○
	PO14 (output)	P16	○	○	○	○
	PO15 (output)	P14	○	○	○	○
		P17	○	○	○	○
	PO16 (output)	P73	○	×	○	×
		PA0	○	○	○	○
	PO17 (output)	PA1	○	○	○	○
		PC0	○	○	○	○
	PO18 (output)	PA2	○	○	○	○
		PC1	○	○	○	○
		PE1	○	○	○	○
	PO19 (output)	P74	○	×	○	×
		PA3	○	○	○	○
	PO20 (output)	P75	○	×	○	×
		PA4	○	○	○	○
	PO21 (output)	PA5	○	○	○	○
		PC2	○	○	○	○
	PO22 (output)	P76	○	×	○	×
		PA6	○	○	○	○
	PO23 (output)	P77	○	×	○	×
		PA7	○	○	○	○
		PE2	○	○	○	○
	PO24 (output)	PB0	○	○	○	○
		PC3	○	○	○	○
	PO25 (output)	PB1	○	○	○	○
		PC4	○	○	○	○
	PO26 (output)	P80	○	×	○	×
		PB2	○	○	○	○
		PE3	○	○	○	○
	PO27 (output)	P81	○	×	○	×
		PB3	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Programmable pulse generator	PO28 (output)	P82	○	×	○	×
		PB4	○	○	○	○
		PE4	○	○	○	○
	PO29 (output)	PB5	○	○	○	○
		PC5	○	○	○	○
	PO30 (output)	PB6	○	○	○	○
		PC6	○	○	○	○
	PO31 (output)	PB7	○	○	○	○
		PC7	○	○	○	○
8-bit timer	TMO0 (output)	P22	○	○	○	○
		PB3	○	○	○	○
		PH1	×	×	○	○
	TMCI0 (input)	P01	○	×	○	×
		P21	○	○	○	○
		PB1	○	○	○	○
	TMRI0 (input)	P00	○	×	○	×
		P20	○	○	○	○
		PA4	○	○	○	○
		PH2	×	×	○	○
	TMO1 (output)	P17	○	○	○	○
		P26	○	○	○	○
	TMCI1 (input)	P02	○	×	○	×
		P12	○	○	○	○
		P54	○	○	○	○
		PC4	○	○	○	○
	TMRI1 (input)	P24	○	○	○	○
		PB5	○	○	○	○
	TMO2 (output)	P16	○	○	○	○
		PC7	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○
		P31	○	○	○	○
		PC6	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○
		PC5	○	○	○	○
	TMO3 (output)	P13	○	○	○	○
		P32	○	○	○	○
		P55	○	○	○	○
	TMCI3 (input)	P27	○	○	○	○
		P34	○	○	○	○
		PA6	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○
		P33	○	○	○	○
Compare match timer W	TOC0 (output)	PC7	○	○	○	○
	TIC0 (input)	PC6	○	○	○	○
	TOC1 (output)	PE7	○	○	○	○
	TIC1 (input)	PE6	○	○	○	○
	TOC2 (output)	PD3	○	○	○	○
	TIC2 (input)	PD2	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Compare match timer W	TOC3 (output)	PE3	○	○	○	○
	TIC3 (input)	PE2	○	○	○	○
Realtime clock	RTCOUT (output)	P16	○	○	○	○
		P32	○	○	○	○
	RTCIC0 (input)*1	P30	○	○	○	○
	RTCIC1 (input)*1	P31	○	○	○	○
	RTCIC2 (input)*1	P32	○	○	○	○
Ethernet controller	REF50CK0 (input)	P76	○	×		
		PB2	○	○		
		PE5	○	○		
	RMII0_CRS_DV (input)	P83	○	×		
		PB7	○	○		
	RMII0_TXD0 (output)	P81	○	×		
		PB5	○	○		
	RMII0_TXD1 (output)	P82	○	×		
		PB6	○	○		
	RMII0_RXD0 (input)	P75	○	×		
		PB1	○	○		
	RMII0_RXD1 (input)	P74	○	×		
		PB0	○	○		
	RMII0_TXD_EN (output)	P80	○	×		
		PA0	○	○		
		PB4	○	○		
	RMII0_RX_ER (input)	P77	○	×		
		PB3	○	○		
	ET0_CRS (input)	P83	○	×		
		PB7	○	○		
	ET0_RX_DV (input)	PC2	○	○		
	ET0_EXOUT (output)	P55	○	○		
		PA6	○	○		
		PJ3	○	○		
	ET0_LINKSTA (input)	P34	○	○		
		P54	○	○		
		PA5	○	○		
	ET0_ETXD0 (output)	P81	○	×		
		PB5	○	○		
	ET0_ETXD1 (output)	P82	○	×		
		PB6	○	○		
	ET0_ETXD2 (output)	PC5	○	○		
	ET0_ETXD3 (output)	PC6	○	○		
	ET0_ERXD0 (input)	P75	○	×		
		PB1	○	○		
	ET0_ERXD1 (input)	P74	○	×		
		PB0	○	○		
	ET0_ERXD2 (input)	PC1	○	○		
		PE4	○	○		
	ET0_ERXD3 (input)	PC0	○	○		
		PE3	○	○		

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Ethernet controller	ET0_TX_EN (output)	P80	○	×		
		PA0	○	○		
		PB4	○	○		
	ET0_TX_ER (output)	PC3	○	○		
	ET0_RX_ER (input)	P77	○	×		
		PB3	○	○		
	ET0_TX_CLK (input)	PC4	○	○		
	ET0_RX_CLK (input)	P76	○	×		
		PB2	○	○		
		PE5	○	○		
	ET0_COL (input)	PC7	○	○		
	ET0_WOL (output)	P73	○	×		
		PA1	○	○		
		PA7	○	○		
	ET0_MDC (output)	P72	○	×		
		PA4	○	○		
	ET0_MDIO (input/output)	P71	○	×		
		PA3	○	○		
Ethernet PHY management interface	PMGI0_MDC (output)	P72	○	×		
		PA4	○	○		
	PMGI0_MDIO (input/output)	P71	○	×		
		PA3	○	○		
Serial communications interface	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○	○	○
		PJ3	○	○	○	○
	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	○	○
		P33	○	○	○	○
	SCK0 (input/output)	P22	○	○	○	○
		P34	○	○	○	○
	SMOSI0 (input/output)/ SSDA0 (input/output)/ TXD0 (output)	P20	○	○	○	○
		P32	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○
		P31	○	○	○	○
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○
		P30	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○
		P27	○	○	○	○
	SMOSI1 (input/output)/ SSDA1 (input/output)/ TXD1 (output)	P16	○	○	○	○
		P26	○	○	○	○
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	○	○	○
		PJ5	○	×	○	×
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	○	○	○
		P52	○	○	○	○
		P51	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial communications interface	SMOSI2 (input/output)/ SSDA2 (input/output)/ TXD2 (output)	P13	○	○	○	○
		P50	○	○	○	○
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	○	○
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	○	○
		P25	○	○	○	○
	SCK3 (input/output)	P15	○	○	○	○
		P24	○	○	○	○
	SMOSI3 (input/output)/ SSDA3 (input/output)/ TXD3 (output)	P17	○	○	○	○
		P23	○	○	○	○
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	×	○	×
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	×	○	×
	SCK4 (input/output)	PB3	○	×	○	×
	SMOSI4 (input/output)/ SSDA4 (input/output)/ TXD4 (output)	PB1	○	×	○	×
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○
		PC0	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	○	○
		PA3	○	○	○	○
		PC2	○	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○
		PC1	○	○	○	○
		PC4	○	○	○	○
	SMOSI5 (input/output)/ SSDA5 (input/output)/ TXD5 (output)	PA4	○	○	○	○
		PC3	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	○	○
		PJ3	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	○	×	○	×
		P33	○	○	○	○
		PB0	○	○	○	○
	SCK6 (input/output)	P02	○	×	○	×
		P34	○	○	○	○
		PB3	○	○	○	○
	SMOSI6 (input/output)/ SSDA6 (input/output)/ TXD6 (output)	P00	○	×	○	×
		P32	○	○	○	○
		PB1	○	○	○	○
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	○	×	○	×

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial communications interface	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P92	○	×	○	×
	SCK7 (input/output)	P56	○	×	○	×
		P91	○	×	○	×
	SMOSI7 (input/output)/ SSDA7 (input/output)/ TXD7 (output)	P55	○	×	○	×
		P90	○	×	○	×
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	●	●
	RTS8# (output)/ SCK8 (input/output)	PC5	○	○		
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○
	SCK8 (input/output)	PC5	×	×	○	○
	SMOSI8 (input/output)/ SSDA8 (input/output)/ TXD8 (output)	PC7	○	○	○	○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	○	●	●
	RTS9# (output)/ SCK9 (input/output)	PB5	○	○		
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	○
	SCK9 (input/output)	PB5	×	×	○	○
	SMOSI9 (input/output)/ SSDA9 (input/output)/ TXD9 (output)	PB7	○	○	○	○
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	○	○	○	○
	CTS10# (input)/ SCK10 (input/output)/ SS10# (input)	P83	●	×	○	×
	RTS10# (output)/ SCK10 (input/output)	P80	●	×	○	×
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	○	×	○	×
		P86	○	×	○	×
		PC6	○	○	○	○
	SCK10 (input/output)	PC5	○	○	○	○
		P80	×	×	○	×
		P83	×	×	○	×
	SMOSI10 (input/output)/ SSDA10 (input/output)/ TXD10 (output)	P82	○	×	○	×
		P87	○	×	○	×
		PC7	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial communications interface	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4	○	○	○	○
	CTS11# (input)/ SS11# (input)	P74	○	×	○	×
	RTS11# (output)/ SCK11 (input/output)	P75	●	×	○	×
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	○	×	○	×
		PB6	○	○	○	○
	SCK11 (input/output)	PB5	○	○	○	○
		P75	×	×	○	×
	SMOSI11 (input/output)/ SSDA11 (input/output)/ TXD11 (output)	P77	○	×	○	×
		PB7	○	○	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○
		PA6	×	×	○	○
	RXD12 (input)/ RXDX12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)	PE2	○	○	○	○
		PA2	×	×	○	○
	SCK12 (input/output)	PE0	○	○	○	○
		PA1	×	×	○	○
	SMOSI12 (input/output)/ SSDA12 (input/output)/ TXD12 (output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○
		PA4	×	×	○	○
I²C bus interface	SCL0[FM+] (input/output)	P12	○	○	○	○
	SDA0[FM+] (input/output)	P13	○	○	○	○
	SCL1 (input/output)	P21	○	○	○	○
	SDA1 (input/output)	P20	○	○	○	○
	SCL2-DS (input/output)	P16	○	○	○	○
	SDA2-DS (input/output)	P17	○	○	○	○
USB 2.0 FS Host/Function module	USB0_VBUS (input)	P16	○	○	○	○
	USB0_EXICEN (output)	P21	○	○	○	○
	USB0_VBUSEN (output)	P16	○	○	○	○
		P24	○	○	○	○
		P32	○	○	○	○
	USB0_OVRCURA-DS (input)/ USB0_OVRCURA (input)	P14	○	○	○	○
	USB0_OVRCURB (input)	P16	○	○	○	○
		P22	○	○	○	○
	USB0_ID (input)	P20	○	○	○	○
	USB0_DP (input/output)*1	PH1			○	○
	USB0_DM (input/output)*1	PH2			○	○
	USB1_VBUS (input)	P73			○*3	×
	USB1_EXICEN (output)	P80			○*3	×

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
USB 2.0 FS Host/Function module	USB1_VBUSEN (output)	P73			○*3	×
		P74			○*3	×
		P82			○*3	×
	USB1_OVRCURA (input)	P75			○*3	×
	USB1_OVRCURB (input)	P73			○*3	×
		P81			○*3	×
	USB1_ID (input)	P77			○*3	×
CAN module	CRX0 (input)	P33	○	○	○	○
		PD2	○	○	○	○
	CTX0 (output)	P32	○	○	○	○
		PD1	○	○	○	○
	CRX1-DS (input)	P15	○	○	○	○
	CRX1 (input)	P55	○	○	○	○
	CTX1 (output)	P14	○	○	○	○
		P23	○	○	×	×
		P54	○	○	○	○
	CRX2 (input)	P67	○	×		
	CTX2 (output)	P66	○	×		
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	○	○
		PC5	○	○	○	○
	MOSIA (input/output)	PA6	○	○	○	○
		PC6	○	○	○	○
	MISOA (input/output)	PA7	○	○	○	○
		PC7	○	○	○	○
	SSLA0 (output)	PA4	○	○	○	○
		PC4	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	○
		PC0	○	○	○	○
	SSLA2 (output)	PA1	○	○	○	○
		PC1	○	○	○	○
	SSLA3 (output)	PA2	○	○	○	○
		PC2	○	○	○	○
	RSPCKB (input/output)	P27	○	○	○	○
		PE5	○	○	○	○
	MOSIB (input/output)	P26	○	○	○	○
		PE6	○	○	○	○
	MISOB (input/output)	P30	○	○	○	○
		PE7	○	○	○	○
	SSLB0 (output)	P31	○	○	○	○
		PE4	○	○	○	○
	SSLB1 (output)	P50	○	○	○	○
		PE0	○	○	○	○
	SSLB2 (output)	P51	○	○	○	○
		PE1	○	○	○	○
	SSLB3 (output)	P52	○	○	○	○
		PE2	○	○	○	○
	RSPCKC (input/output)	P56	×	×	○	×
		PD3	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial peripheral interface	MOSIC (input/output)	P54	×	×	○	○
		PD1	○	○	○	○
	MISOC (input/output)	P55	×	×	○	○
		PD2	○	○	○	○
	SSLC0 (output)	PD4	○	○	○	○
	SSLC1 (output)	PD5	○	○	○	○
	SSLC2 (output)	PD6	○	○	○	○
	SSLC3 (output)	PD7	○	○	○	○
Quad serial peripheral interface (RX66N)/ quad SPI memory interface (RX671)	QSPCLK (output)	P77	○	×	○	×
		PD5	○	○	○	○
	QSSL (output)	P76	○	×	○	×
		PD4	○	○	○	○
	QMO/QIO0 (input/output)	PC3	●	×	○	○
		PD6	●	○	○	○
		PE6	×	×	○	○
	QMI/QIO1 (input/output)	PC4	●	×	○	○
		PD7	●	○	○	○
		PE7	×	×	○	○
	QIO2 (input/output)	P80	○	×	○	×
		PD2	○	○	○	○
	QIO3 (input/output)	P81	○	×	○	×
		PD3	○	○	○	○
Serial sound interface	AUDIO_CLK (input)	P00	○	×	×	×
		P22	○	○	○	○
		PC4	×	×	○	○
	SSIBCK0 (input/output)	P01	○	×	×	×
		P23	○	○	○	○
		PC5	×	×	○	○
	SSILRCK0 (input/output)	P21	○	○	○	○
		PF5	○	×	×	×
		PC6	×	×	○	○
	SSIRXD0 (input)	P20	○	○	○	○
		PJ5	○	×	×	×
		P53	×	×	○	○
	SSITXD0 (output)	P17	○	○	○	○
		PJ3	○	○	×	×
		PC7	×	×	○	○
	SSIBCK1 (input/output)	P02	○	×		
		P24	○	○		
	SSILRCK1 (input/output)	P05	○	○		
		P15	○	○		
	SSIDATA1 (input/output)	P03	○	×		
		P25	○	○		
SD host interface	SDHI_CLK (output)	P21	○	×	○	○
		P77	○	×	○	×
		PD5	○	○	○	○
	SDHI_CMD (input/output)	P20	○	×	○	○
		P76	○	×	○	×
		PD4	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
SD host interface	SDHI_CD (input)	P25	○	×	○	○
		P81	○	×	○	×
		PE6	○	○	○	○
		PA1	×	×	○	○
	SDHI_WP (input)	P24	○	×	○	○
		P80	○	×	○	×
		PE7	○	○	○	○
		PA2	×	×	○	○
	SDHI_D0 (input/output)	P22	○	×	○	○
		PC3	○	×	○	○
		PD6	○	○	○	○
		PE6	×	×	○	○
	SDHI_D1 (input/output)	P23	○	×	○	○
		PC4	○	×	○	○
		PD7	○	○	○	○
		PE7	×	×	○	○
	SDHI_D2 (input/output)	P75	○	×	○	×
		P87	○	×	○	×
		PD2	○	○	○	○
	SDHI_D3 (input/output)	P17	○	×	○	○
		PC2	○	×	○	○
		PD3	○	○	○	○
MMC host interface	MMC_RES# (output)	P75	○	×		
		PE7	○	○		
	MMC_CLK (output)	P77	○	×		
		PD5	○	○		
	MMC_CD (input)	PC2	○	×		
		PE6	○	○		
	MMC_CMD (input/output)	P76	○	×		
		PD4	○	○		
	MMC_D0 (input/output)	PC3	○	×		
		PD6	○	○		
	MMC_D1 (input/output)	PC4	○	×		
		PD7	○	○		
	MMC_D2 (input/output)	P80	○	×		
		PD2	○	○		
	MMC_D3 (input/output)	P81	○	×		
		PD3	○	○		
	MMC_D4 (input/output)	P82	○	×		
		PE0	○	○		
	MMC_D5 (input/output)	PC5	○	×		
		PE1	○	○		
	MMC_D6 (input/output)	PC6	○	×		
		PE2	○	○		
	MMC_D7 (input/output)	PC7	○	×		
		PE3	○	○		

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○
	AN003 (input)*1	P43	○	○	○	○
	AN004 (input)*1	P44	○	○	○	○
	AN005 (input)*1	P45	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○
	AN007 (input)*1	P47	○	○	○	○
	ADTRG0# (input)	P07	○	○	○	○
		P16	○	○	○	○
		P25	○	○	○	○
	AN100 (input)*1	PE2	○	○	×	×
		PD7	×	×	○	○
	AN101 (input)*1	PE3	○	○	×	×
		PD6	×	×	○	○
	AN102 (input)*1	PE4	○	○	×	×
		PD5	×	×	○	○
	AN103 (input)*1	PE5	○	○	×	×
		PD4	×	×	○	○
	AN104 (input)*1	PE6	○	○	×	×
		PD3	×	×	○	○
	AN105 (input)*1	PE7	○	○	×	×
		PD2	×	×	○	○
	AN106 (input)*1	PD6	○	○	×	×
		PD1	×	×	○	○
	AN107 (input)*1	PD7	○	○	×	×
		PD0	×	×	○	○
	AN108 (input)*1	PD0	○	○	×	×
		P90	×	×	○	×
	AN109 (input)*1	PD1	○	○	×	×
		P02	×	×	○	×
	AN110 (input)*1	PD2	○	○	×	×
		P01	×	×	○	×
	AN111 (input)*1	PD3	○	○	×	×
		P00	×	×	○	×
	AN112 (input)*1	PD4	○	○		
	AN113 (input)*1	PD5	○	○		
	AN114 (input)*1	P90	○	×		
	AN115 (input)*1	P91	○	×		
	AN116 (input)*1	P92	○	×		
	AN117 (input)*1	P93	○	×		
	AN118 (input)*1	P00	○	×		
	AN119 (input)*1	P01	○	×		
	AN120 (input)*1	P02	○	×		
	ANEX0 (output)*1	PE0	○	○	○	○
	ANEX1 (input)*1	PE1	○	○	○	○
	ADTRG1# (input)	P13	○	○	○	○
		P17	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
12-bit D/A converter	DA0 (output)*1	P03	○	×		
	DA1 (output)*1	P05	○	○		
Parallel data capture unit	PIXCLK (input)	P24	○	×		
	VSYNC (input)	P32	○	×		
	HSYNC (input)	P25	○	×		
	PIXD0 (input)	P15	○	×		
	PIXD1 (input)	P86	○	×		
	PIXD2 (input)	P87	○	×		
	PIXD3 (input)	P17	○	×		
	PIXD4 (input)	P20	○	×		
	PIXD5 (input)	P21	○	×		
	PIXD6 (input)	P22	○	×		
	PIXD7 (input)	P23	○	×		
	PCKO (output)	P33	○	×		
Clock generation circuit	CLKOUT (output)	P25	○	○	○	○
	CLKOUT25M (output)	P56	○	×		
	EXCIN (input)*1	PJ3			○	○
	EXTAL (input)*1	P36			○	○
	XTAL (output)*1	P37			○	○
Clock frequency measurement circuit	CACREF (input)	PA0	○	○	○	○
		PC7	○	○	○	○
Graphic-LCD controller	LCD_EXTCLK (input)	PD0	○	○		
	LCD_CLK (output)	PB5	○	○		
	LCD_TCON0 (output)	PB4	○	○		
	LCD_TCON1 (output)	PB3	○	○		
	LCD_TCON2 (output)	PB2	○	○		
	LCD_TCON3 (output)	PB1	○	○		
	LCD_DATA0 (output)	PB0	○	○		
	LCD_DATA1 (output)	PA7	○	○		
	LCD_DATA2 (output)	PA6	○	○		
	LCD_DATA3 (output)	PA5	○	○		
	LCD_DATA4 (output)	PA4	○	○		
	LCD_DATA5 (output)	PA3	○	○		
	LCD_DATA6 (output)	PA2	○	○		
	LCD_DATA7 (output)	PA1	○	○		
	LCD_DATA8 (output)	PA0	○	○		
	LCD_DATA9 (output)	PE7	○	○		
	LCD_DATA10 (output)	PE6	○	○		
	LCD_DATA11 (output)	PE5	○	○		
	LCD_DATA12 (output)	PE4	○	○		
	LCD_DATA13 (output)	PE3	○	○		
	LCD_DATA14 (output)	PE2	○	○		
	LCD_DATA15 (output)	PE1	○	○		
	LCD_DATA16 (output)	PE0	○	○		
	LCD_DATA17 (output)	PD7	○	○		
	LCD_DATA18 (output)	PD6	○	○		
	LCD_DATA19 (output)	PD5	○	○		
	LCD_DATA20 (output)	PD4	○	○		

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Graphic-LCD controller	LCD_DATA21 (output)	PD3	○	○		
	LCD_DATA22 (output)	PD2	○	○		
	LCD_DATA23 (output)	PD1	○	○		
Battery backup	TAMPI0 (input)*1	P30			○	○
	TAMPI1 (input)*1	P31			○	○
	TAMPI2 (input)*1	P32			○	○
Serial communications interface	RXD010 (input)/ SMISO010 (input/output)/ SSCL010 (input/output)	P81			○	×
		P86			○	×
		PC6			○	○
	TXD010 (output)/ SMOSI010 (input/output)/ SSDA010 (input/output)	P82			○	×
		P87			○	×
		PC7			○	○
	SCK010 (input/output)	P80			○	×
		P83			○	×
		PC5			○	○
	RTS010# (output)	P80			○	×
	CTS010# (input)/ SS010# (input)/ CTS010# (input)/ RTS010# (output)/ SS010# (input)	P83			○	×
		PC4			○	○
	DE010 (output)	P80			○	×
		PC4			○	○
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P76			○	×
		PB6			○	○
		PC0			○	○
	TXD011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P77			○	×
		PB7			○	○
		PC1			○	○
	SCK011 (input/output)	P75			○	×
		PB5			○	○
	TXDA011 (output)	PC1			○	○
	TXDB011 (output)	PC2			○	○
	RTS011# (output)	P75			○	×
	CTS011# (input)/ SS011# (input)	P74			○	×
	CTS011# (input)/ RTS011# (output)/ SS011# (input)	PB4			○	○
	DE011 (output)	P75			○	×
		PB4			○	○
High-speed I²C bus interface	SCLHS0[FM+/HS] (input/output)	P12			○	○
	SDAHS0[FM+/HS] (input/output)	P13			○	○

Module/ Function	Pin Function	Port Allocation	RX66N		RX671	
			145-/ 144-Pin	100-Pin	145-/ 144-Pin	100-Pin
Serial peripheral interface	RSPCK0 (input/output)	PA5			○	○
		PC5			○	○
	MOSI0 (input/output)	PA6			○	○
		PC6			○	○
	MISO0 (input/output)	PA7			○	○
		PC7			○	○
	SSL00 (input/output)	PA4			○	○
		PC4			○	○
	SSL01 (output)	PA0			○	○
		PC0			○	○
	SSL02 (output)	PA1			○	○
		PC1			○	○
	SSL03 (output)	PA2			○	○
		PC2			○	○
	SSL03 (output)	PA2			○	○
		PC2			○	○
Capacitive touch sensing unit	TSCAP (—)	PC4			○	○
	TS0 (output)	P34			○	○
	TS1 (output)	P33			○	○
	TS2 (output)	P27			○	○
	TS3 (output)	P26			○	○
	TS4 (output)	P25			○	○
	TS5 (output)	P24			○	○
	TS6 (output)	P23			○	○
	TS7 (output)	P22			○	○
	TS8 (output)	P21			○	○
	TS9 (output)	P20			○	○
	TS10 (output)	P15			○	○
	TS11 (output)	P14			○	○
	TS12 (output)	P53			○	○
	TS13 (output)	PC6			○	○
	TS14 (output)	PC5			○	○
	TS15 (output)	PC1			○	○
	TS16 (output)	PC0			○	○
Remote control signal receiver	PMC0-DS (input) *1	P53			○	○
		PB3			○	○
		PC3			○	○

Notes: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).
2. Not present on the 145-pin TFLGA product.
3. Supported on the 145-pin TFLGA product only.

Table 2.28 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX66N (n = 0 to 3, 5, 7)	RX671 (n = 0 to 3, 5, 7)
P00PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/SSDA6 010111b: AUDIO_CLK 011011b: QIO2-C	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/SSDA6
P01PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/SSCL6 010111b: SSIBCK0 011011b: QIO3-C	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/SSCL6
P02PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6 010111b: SSIBCK1	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6
P03PFS	PSEL[5:0]	Pin function select bits	—
P07PFS	PSEL[5:0]	Pin function select bits	—
P0nPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P00: AN118 (224/176/145/144-pin) P01: AN119 (224/176/145/144-pin) P02: AN120 (224/176/145/144-pin) P03: DA0 (224/176/145/144-pin) P05: DA1 (224/176/145/144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P00: AN111 (145/144-pin) P01: AN110 (145/144-pin) P02: AN109 (145/144-pin)

Table 2.29 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 2 to 7)
P10PFS	—	P10 pin function control register	—
P11PFS	—	P11 pin function control register	—
P12PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 011110b: GTADSM0 100101b: LCD_TCON1-A	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 101111b: SCLHS0[FM+/HS]
P13PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 011110b: GTADSM1 100101b: LCD_TCON0-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 101111b: SDAHS0[FM+/HS]
P14PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 011110b: GTETRGD 100101b: LCD_CLK-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 101011b: TS11

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 2 to 7)
P15PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 010111b: SSILRCK1 011100b: PIXD0 011110b: GTETRGA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 101011b: TS10
P17PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS 010111b: SSITXD0 011010b: SDHI_D3-C 011100b: PIXD3 011110b: GTIOC0B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS 010111b: SSITXD0 011010b: SDHI_D3-C
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (224/176-pin) P11: IRQ1 (224/176-pin) P12: IRQ2 (224/176/145/144/100-pin) P13: IRQ3 (224/176/145/144/100-pin) P14: IRQ4 (224/176/145/144/100-pin) P15: IRQ5 (224/176/145/144/100-pin) P16: IRQ6 (224/176/145/144/100-pin) P17: IRQ7 (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (145/144/100/64/48-pin) P13: IRQ3 (145/144/100/64/48-pin) P14: IRQ4 (145/144/100-pin) P15: IRQ5 (145/144/100-pin) P16: IRQ6 (145/144/100/64/48-pin) P17: IRQ7 (145/144/100/64/48-pin)

Table 2.30 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
P20PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRI0 000110b: PO0 001010b: TXD0/SMOSI0/SSDA0 001111b: SDA1 010011b: USB0_ID 010111b: SSIRXD0 011010b: SDHI_CMD-C 011100b: PIXD4	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRI0 000110b: PO0 001010b: TXD0/SMOSI0/SSDA0 001111b: SDA1 010011b: USB0_ID 010111b: SSIRXD0 011010b: SDHI_CMD-C 101011b: TS9
P21PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCI0 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1 010011b: USB0_EXICEN 010111b: SSILRCK0 011010b: SDHI_CLK-C 011100b: PIXD5 011110b: GTIOC2A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCI0 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1 010011b: USB0_EXICEN 010111b: SSILRCK0 011010b: SDHI_CLK-C 101011b: TS8
P22PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB 010111b: AUDIO_CLK 011000b: EDREQ0 011010b: SDHI_D0-C 011100b: PIXD6 011110b: GTIOC1A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB 010111b: AUDIO_CLK 011000b: EDREQ0 011010b: SDHI_D0-C 101011b: TS7

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
P23PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 010000b: CTX1 010111b: SSIBCK0 011000b: EDACK0 011010b: SDHI_D1-C 011100b: PIXD7 011110b: GTIOC0A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 010111b: SSIBCK0 011000b: EDACK0 011010b: SDHI_D1-C 101011b: TS6
P24PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 010111b: SSIBCK1 011000b: EDREQ1 011010b: SDHI_WP 011100b: PIXCLK	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 011000b: EDREQ1 011010b: SDHI_WP 101011b: TS5
P25PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 010111b: SSIDATA1 011000b: EDACK1 011010b: SDHI_CD 011100b: HSYNC 101010b: CLKOUT	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 011000b: EDACK1 011010b: SDHI_CD 101010b: CLKOUT 101011b: TS4

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
P26PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3# 001101b: MOSIB-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3# 001101b: MOSIB-A 101011b: TS3
P27PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A 101011b: TS2
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (224/176/145/144/100-pin) P21: IRQ9 (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (145/144/100-pin) P21: IRQ9 (145/144/100-pin) P22: IRQ15 (145/144/100-pin) P23: IRQ3 (145/144/100-pin) P24: IRQ12 (145/144/100-pin) P25: IRQ5 (145/144/100-pin) P26: IRQ6 (145/144/100/64/48-pin) P27: IRQ7 (145/144/100/64/48-pin)

Table 2.31 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX66N (n = 0 to 4)	RX671 (n = 0 to 4)
P32PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000011b: TIOCC0 000101b: TMO3 000110b: PO10 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 010011b: USB0_VBUSEN 011100b: VSYNC 100001b: POE10#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000011b: TIOCC0 000101b: TMO3 000110b: PO10 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 010011b: USB0_VBUSEN 100001b: POE10#
P33PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 011100b: PCKO 100001b: POE11#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 100001b: POE11# 101011b: TS1
P34PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 010001b: ET0_LINKSTA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 101011b: TS0

Table 2.32 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX66N (n = 0 to 2, 4 to 7)	RX671 (n = 0 to 6)
P53PFS	—	—	P53 pin function control register
P54PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 010001b: ET0_LINKSTA 011000b: EDACK0 100101b: LCD_DATA6-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 011000b: EDACK0
P55PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 001101b: MISOC-B 010000b: CRX1 010001b: ET0_EXOUT 011000b: EDREQ0 100101b: LCD_DATA5-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 001101b: MISOC-B 010000b: CRX1 011000b: EDREQ0
P56PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A 101010b: CLKOUT25M	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1
P57PFS	—	P57 pin function control register	—
P5nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P55: IRQ10 (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P50: IRQ0 (145/144/100-pin) P51: IRQ1 (145/144/100-pin) P52: IRQ2 (145/144/100-pin) P53: IRQ3 (145/144/100/64/48-pin) P54: IRQ4 (145/144/100-pin) P55: IRQ10 (145/144/100-pin) P56: IRQ6 (145/144-pin)

Table 2.33 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX66N (n = 6, 7)	RX671 (n = 0 to 7)
P60PFS	—	—	P60 pin function control register
P61PFS	—	—	P61 pin function control register
P62PFS	—	—	P62 pin function control register
P63PFS	—	—	P63 pin function control register
P64PFS	—	—	P64 pin function control register
P65PFS	—	—	P65 pin function control register
P66PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7D 010000b: CTX2 011110b: GTIOC2B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7D
P67PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C 010000b: CRX2 011110b: GTIOC1B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C
P6nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P67: IRQ15 (224/176/145/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ0 (145/144-pin) P61: IRQ1 (145/144-pin) P62: IRQ2 (145/144-pin) P63: IRQ3 (145/144-pin) P64: IRQ4 (145/144-pin) P65: IRQ13 (145/144-pin) P66: IRQ14 (145/144-pin) P67: IRQ15 (145/144-pin)

Table 2.34 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX66N (n = 1 to 7)	RX671 (n = 0 to 7)
P70PFS	—	—	P70 pin function control register
P71PFS	PSEL[5:0]	Pin function select bits	—
P72PFS	PSEL[5:0]	Pin function select bits	—
P73PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO16 010001b: ET0_WOL 100101b: LCD_EXTCLK-A	Pin function select bits 000000b: Hi-Z 000110b: PO16 010001b: USB1_VBUS 010010b: USB1_VBUSEN 010011b: USB1_OVRCURB

Register	Bit	RX66N (n = 1 to 7)	RX671 (n = 0 to 7)
P74PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO19 001011b: SS11#/CTS11# 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA21-A	Pin function select bits 000000b: Hi-Z 000110b: PO19 001011b: CTS11#/SS11# 010011b: USB1_VBUSEN 101101b: CTS011#/SS011#
P75PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100101b: LCD_DATA20-A	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010010b: USB1_OVRCURA 011010b: SDHI_D2-A 101100b: SCK011 101101b: RTS011# 101110b: DE011
P76PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: SMISO11/SSCL11/RXD11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100101b: LCD_DATA18-A	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: RXD11/SMISO11/SSCL11 011010b: SDHI_CMD-A 011011b: QSSL-A 101100b: RXD011/SMISO011/ SSCL011
P77PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: SMOSI11/SSDA11/TXD11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100101b: LCD_DATA17-A	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: TXD11/SMOSI11/SSDA11 010011b: USB1_ID 011010b: SDHI_CLK-A 011011b: QSPCLK-A 101100b: TXD011/SMOSI011/ SSDA011
P7nPFS	ISEL	—	Interrupt input function select bit

Table 2.35 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 3, 6, 7)
P80PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011000b: EDREQ0 011001b: MMC_D2-A 011010b: SDHI_WP 011011b: QIO2-A 100101b: LCD_DATA14-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010011b: USB1_EXICEN 011000b: EDREQ0 011010b: SDHI_WP 011011b: QIO2-A 101100b: SCK010 101101b: RTS010# 101110b: DE010
P81PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: SMISO10/SSCL10/RXD10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD 011011b: QIO3-A 011110b: GTIOC0B 100101b: LCD_DATA13-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: RXD10/SMISO10/SSCL10 010011b: USB1_OVRCURB 011000b: EDACK0 011010b: SDHI_CD 011011b: QIO3-A 101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: SMOSI10/SSDA10/TXD10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 011110b: GTIOC2A 100101b: LCD_DATA12-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: TXD10/SMOSI10/SSDA10 010011b: USB1_VBUSEN 011000b: EDREQ1 101100b: TXD010/SMOSI010/ SSDA010

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 3, 6, 7)
P83PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: SS10#/CTS10# 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011000b: EDACK1 011110b: GTIOC0A 100101b: LCD_DATA8-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 011000b: EDACK1 101100b: SCK010 101101b: CTS010#/SS010#
P84PFS	—	P84 pin function control register	—
P85PFS	—	P85 pin function control register	—
P86PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: SMISO10/SSCL10/RXD10 011100b: PIXD1 011110b: GTIOC2B	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P87PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: SMOSI10/SSDA10/TXD10 011010b: SDHI_D2-C 011100b: PIXD2 011110b: GTIOC1B	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 011010b: SDHI_D2-C 101100b: TXD010/SMOSI010/ SSDA010
P8nPFS	ISEL	—	Interrupt input function select bit

Table 2.36 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX66N (n = 0 to 3)	RX671 (n = 0 to 3)
P9nPFS	ISEL	—	Interrupt input function select bit
	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P90: AN114 (224/176/145/144-pin) P91: AN115 (224/176/145/144-pin) P92: AN116 (224/176/145/144-pin) P93: AN117 (224/176/145/144-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P90: AN108 (145/144-pin)

Table 2.37 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PA0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC0B 100101b: LCD_DATA8-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 001110b: SSL01-B
PA1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001101b: SSLA2-B 010001b: ET0_WOL 011110b: GTIOC2A 100101b: LCD_DATA7-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001100b: SCK12 001101b: SSLA2-B 001110b: SSL02-B 110001b: SDHI_CD
PA2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 011110b: GTIOC1A 100101b: LCD_DATA6-B	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3-B 001110b: SSL03-B 110001b: SDHI_WP

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PA3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B 101000b: PMGI0_MDIO	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5
PA4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B 101000b: PMGI0_MDC	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: SSLA0-B 001110b: SSL00-B
PA5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 011110b: GTIOC0A 100101b: LCD_DATA3-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 001110b: RSPCK0-B

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PA6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 011110b: GTETRGB 100101b: LCD_DATA2-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA-B 001110b: MOSI0-B
PA7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCB2 000110b: PO23 001101b: MISOA-B 010001b: ET0_WOL 100101b: LCD_DATA1-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCB2 000110b: PO23 001101b: MISOA-B 001110b: MISO0-B
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ11 (224/176/145/144/100-pin) PA3: IRQ6-DS (224/176/145/144/100-pin) PA4: IRQ5-DS (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (145/144/100-pin) PA1: IRQ11 (145/144/100/64/48-pin) PA2: IRQ10 (145/144/100/64/48-pin) PA3: IRQ6-DS (145/144/100-pin) PA4: IRQ5-DS (145/144/100/64/48-pin) PA5: IRQ5 (145/144/100-pin) PA6: IRQ14 (145/144/100/64/48-pin) PA7: IRQ7 (145/144/100/64-pin)

Table 2.38 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PB0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA0-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6
PB1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 010001b: ET0_ERXD0 010010b: RMII0_RXD0 100101b: LCD_TCON3-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6
PB2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_TCON2-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100101b: LCD_TCON1-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PB4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: SS9#/CTS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100100b: SS11#/CTS11#/RTS11# 100101b: LCD_TCON0-B	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#*1/RTS011#*1/ SS011# 101110b: DE011
PB5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 001011b: RTS9# 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100100b: SCK11 100101b: LCD_CLK-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100100b: SMISO11/SSCL11/RXD11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/SSCL11 101100b: RXD011/SMISO011/ SSCL011
PB7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_DV 100100b: SMOSI11/SSDA11/TXD11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/ SSDA011

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (224/176/145/144/100-pin) PB1: IRQ4-DS (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (145/144/100-pin) PB1: IRQ4-DS (145/144/100-pin) PB2: IRQ2 (145/144/100-pin) PB3: IRQ3 (145/144/100-pin) PB4: IRQ4 (145/144/100-pin) PB5: IRQ13 (145/144/100/64/48-pin) PB6: IRQ6 (145/144/100/64/48-pin) PB7: IRQ15 (145/144/100/64/48-pin)

Note: 1. Not usable as CTS011# when SCR1.CRSEP = 1. Can be used as RTS011#.

Table 2.39 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PC0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1-A 010001b: ET0_ERXD3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1-A 001110b: SSL01-A 101011b: TS16 101100b: RXD011/SMISO011/ SSCL011
PC1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 010001b: ET0_ERXD2 100101b: LCD_DATA22-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 001110b: SSL02-A 101011b: TS15 101100b: TXD011/SMOSI011/ SSDA011/TXDA011

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PC2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 011110b: GTIOC2B 100101b: LCD_DATA19-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 001110b: SSL03-A 011010b: SDHI_D3-A 101100b: TXDB011
PC3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QMO-A/QIO0-A 011110b: GTIOC1B 100101b: LCD_DATA16-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 011010b: SDHI_D0-A 011011b: QIO0-A
PC4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: SS8#/CTS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QMI-A/QIO1-A 011110b: GTETRGC 100100b: SS10#/CTS10#/RTS10# 100101b: LCD_DATA15-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0-A 001110b: SSL00-A 010111b: AUDIO_CLK 011010b: SDHI_D1-A 011011b: QIO1-A 100100b: CTS10#/RTS10#/SS10# 101011b: TSCAP 101100b: CTS010#*1/RTS010#*1/ SS010# 101110b: DE010

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PC5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001011b: RTS8# 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A 011110b: GTIOC1A 100100b: SCK10 100101b: LCD_DATA11-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001101b: RSPCKA-A 001110b: RSPCK0-A 010111b: SSIBCK0 100100b: SCK10 101011b: TS14 101100b: SCK010
PC6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A 011101b: TIC0 011110b: GTIOC3B 100100b: SMISO10/SSCL10/RXD10 100101b: LCD_DATA10-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 001110b: MOSI0-A 010111b: SSILRCK0 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 101011b: TS13 101100b: RXD010/SMISO010/ SSCL010

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PC7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000110b: PO31 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA-A 010001b: ET0_COL 011001b: MMC_D7-A 011101b: TOC0 011110b: GTIOC3A 100100b: SMOSI10/SSDA10/TXD10 100101b: LCD_DATA9-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000110b: PO31 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA-A 001110b: MISO0-A 010111b: SSITXD0 011101b: TOC0 100100b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010
PCnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (224/176/145/144/100-pin) PC1: IRQ12 (224/176/145/144/100-pin) PC6: IRQ13 (224/176/145/144/100-pin) PC7: IRQ14 (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (145/144/100/64-pin) PC1: IRQ12 (145/144/100/64-pin) PC2: IRQ10 (145/144/100-pin) PC3: IRQ11 (145/144/100-pin) PC4: IRQ12 (145/144/100/64/48-pin) PC5: IRQ5 (145/144/100/64/48-pin) PC6: IRQ13 (145/144/100/64/48-pin) PC7: IRQ14 (145/144/100/64/48-pin)

Note: 1. Not usable as CTS011# when SCR1.CRSEP = 1. Can be used as RTS011#.

Table 2.40 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PD0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: POE4# 011110b: GTIOC1B 100101b: LCD_EXTCLK-B	Pin function select bits 000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0 011110b: GTIOC1A 100101b: LCD_DATA23-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0
PD2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 011110b: GTIOC0B 100101b: LCD_DATA22-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2
PD3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 011110b: GTIOC0A 100101b: LCD_DATA21-B	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2
PD4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 011001b: MMC_CMD-B 011010b: SDHI_CMD-B 011011b: QSSL-B 100101b: LCD_DATA20-B	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 011010b: SDHI_CMD-B 011011b: QSSL-B

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PD5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKA 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011010b: SDHI_CLK-B 011011b: QSPCLK-B
PD6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QMO-B/QIO0-B 100101b: LCD_DATA18-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011010b: SDHI_D0-B 011011b: QIO0-B
PD7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QMI-B/QIO1-B 100101b: LCD_DATA17-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011010b: SDHI_D1-B 011011b: QIO1-B
PDnPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN108 (224/176/145/144/100-pin) PD1: AN109 (224/176/145/144/100-pin) PD2: AN110 (224/176/145/144/100-pin) PD3: AN111 (224/176/145/144/100-pin) PD4: AN112 (224/176/145/144/100-pin) PD5: AN113 (224/176/145/144/100-pin) PD6: AN106 (224/176/145/144/100-pin) PD7: AN107 (224/176/145/144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN107 (145/144/100-pin) PD1: AN106 (145/144/100-pin) PD2: AN105 (145/144/100/64/48-pin) PD3: AN104 (145/144/100/64/48-pin) PD4: AN103 (145/144/100/64/48-pin) PD5: AN102 (145/144/100/64/48-pin) PD6: AN101 (145/144/100/64-pin) PD7: AN100 (145/144/100/64-pin)

Table 2.41 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PE0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B 011001b: MMC_D4-B 011110b: GTIOC2B 100101b: LCD_DATA16-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B
PE1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLB2-B 011001b: MMC_D5-B 011110b: GTIOC1B 100101b: LCD_DATA15-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLB2-B
PE2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLB3-B 011001b: MMC_D6-B 011101b: TIC3 011110b: GTIOC0B 100101b: LCD_DATA14-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLB3-B 011101b: TIC3
PE3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 011110b: GTIOC2A 100101b: LCD_DATA13-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PE4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 011110b: GTIOC1A 100101b: LCD_DATA12-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B
PE5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTIOC0A 100101b: LCD_DATA11-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B
PE6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD 011101b: TIC1 011110b: GTIOC3B 100101b: LCD_DATA10-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011010b: SDHI_CD 011011b: QIO0-B 011101b: TIC1 110001b: SDHI_D0-B
PE7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP 011101b: TOC1 011110b: GTIOC3A 100101b: LCD_DATA9-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011010b: SDHI_WP 011011b: QIO1-B 011101b: TOC1 110001b: SDHI_D1-B

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 0 to 7)
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (224/176/145/144/100-pin) PE5: IRQ5 (224/176/145/144/100-pin) PE6: IRQ6 (224/176/145/144/100-pin) PE7: IRQ7 (224/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (145/144/100/64-pin) PE1: IRQ9 (145/144/100/64-pin) PE2: IRQ7-DS (145/144/100/64-pin) PE3: IRQ11 (145/144/100-pin) PE4: IRQ12 (145/144/100-pin) PE5: IRQ5 (145/144/100-pin) PE6: IRQ6 (145/144/100/64/48-pin) PE7: IRQ7 (145/144/100/64/48-pin)
PEnPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: ANEX0 (224/176/145/144/100-pin) PE1: ANEX1 (224/176/145/144/100-pin) PE2: AN100 (224/176/145/144/100-pin) PE3: AN101 (224/176/145/144/100-pin) PE4: AN102 (224/176/145/144/100-pin) PE5: AN103 (224/176/145/144/100-pin) PE6: AN104 (224/176/145/144/100-pin) PE7: AN105 (224/176/145/144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: ANEX0 (145/144/100/64-pin) PE1: ANEX1 (145/144/100/64-pin)

Table 2.42 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX66N (n = 0 to 2, 5)	RX671 (n = 5)
PF0PFS	—	PF0 pin function control register	—
PF1PFS	—	PF1 pin function control register	—
PF2PFS	—	PF2 pin function control register	—
PF5PFS	PSEL[5:0]	—	Pin function select bits

Table 2.43 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX66N (n = 0 to 7)	RX671 (n = 1, 2)
PH0PFS	—	PH0 pin function control register	—
PH1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMISO7/SSCL7/RXD7 001101b: MOSIA 011101b: TOC0 011110b: GTETRGB	Pin function select bits 000000b: Hi-Z 000101b: TMO0
PH2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SMOSI7/SSDA7/TXD7 001101b: MISOA 011110b: GTETRGC	Pin function select bits 000000b: Hi-Z 000101b: TMRI0
PH2PFS	—	PH2 pin function control register	—
PH3PFS	—	PH3 pin function control register	—
PH4PFS	—	PH4 pin function control register	—
PH5PFS	—	PH5 pin function control register	—
PH6PFS	—	PH6 pin function control register	—
PH7PFS	—	PH7 pin function control register	—

Table 2.44 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX66N (n = 0 to 3, 5)	RX671 (n = 3, 5)
PJ0PFS	—	PJ0 pin function control register	—
PJ1PFS	—	PJ1 pin function control register	—
PJ2PFS	—	PJ2 pin function control register	—
PJ3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 010111b: SSITXD0 011000b: EDACK1 011011b: QMO-C/QIO0-C	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 011000b: EDACK1
PJ5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 010111b: SSIRXD0 011011b: QMI-C/QIO1-C 100001b: POE8#	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 100001b: POE8#
PJnPFS	ISEL	—	Interrupt input function select bit

Table 2.45 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX66N	RX671
PKnPFS	—	PKn pin function control register (n = 0 to 7)	—

Table 2.46 Comparison of PLn Pin Function Control Register (PLnPFS)

Register	Bit	RX66N	RX671
PLnPFS	—	PLn pin function control register (n = 0 to 7)	—

Table 2.47 Comparison of PMn Pin Function Control Register (PMnPFS)

Register	Bit	RX66N	RX671
PMnPFS	—	PMn pin function control register (n = 0 to 7)	—

Table 2.48 Comparison of PNn Pin Function Control Register (PNnPFS)

Register	Bit	RX66N	RX671
PNnPFS	—	PNn pin function control register (n = 4, 5)	—

Table 2.49 Comparison of PQn Pin Function Control Register (PQnPFS)

Register	Bit	RX66N	RX671
PQnPFS	—	PQn pin function control register (n = 0 to 3)	—

Table 2.50 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX66N (MPC)	RX671 (MPC)
PFBCR0	ADRHMS ADRHMS2	A16 to A23 output enable bit A16 to A23 output enable 2 bit ADRHMS / ADRHMS2 0 / 0: Set PC0 to PC7. 0 / 1: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 0 / 0: 224- and 176-pin products: Set P90 to P97. 145- and 144-pin products: Set P90 to P93 (A20 to A23 not assigned). 1 / 1: Setting prohibited.	A16 to A23 output enable bit A16 to A23 output enable 2 bit ADRHMS / ADRHMS2 0 / 0: Set PC0 to PC7. 0 / 1: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 / 0: Set P90 to P93 (A20 to A23 not assigned). 1 / 1: Setting prohibited. Pins P71 and P72 are not present on the 145-pin TFLGA (0.65 mm pin pitch) product, so the ADRHMS and ADRHMS2 bits should be set to 00b or 10b when using external address buses A16 to A23.
	DH32E	D16 to D31 output enable bit	—
	WR32BC32E	WR3#/BC3# and WR2#/BC2# output enable bit	—
PFBCR1	WAITS[1:0]	WAIT select bits WAITS2 / WAITS[1:0] 0 / 0 0: Setting prohibited. 0 / 0 1: Set P55 as WAIT# input pin. 0 / 1 0: Set P5C as WAIT# input pin. 0 / 1 1: Set P51 as WAIT# input pin. 0 / 0 0: Set PF5 as WAIT# input pin. 1 / 0 1: Setting prohibited. 1 / 1 x: Setting prohibited.	WAIT select bits b1 b0 0 0: Setting invalid 0 1: Set P55 as WAIT# input pin. 1 0: Set P5C as WAIT# input pin. 1 1: Set P51 as WAIT# input pin. On 145-pin, 144-pin, and 100-pin products, P55 is set as the WAIT# input pin even when the value of these bits is 00b.
	ALES	ALE select bit	—
PFBCR3	SDCLKDRV	SDCLK pin driving ability select bit	—
	WAITS2	WAIT select bit 2	—
PFENET	—	Ethernet control register	—

2.15 Port Output Enable 3

Table 2.51 is a comparison of port output enable 3 registers.

Table 2.51 Comparative Overview of Port Output Enable 3

Register	Bit	RX66N (POE3a)	RX671 (POE3a)
M6SELR	—	MTU6 pin select register	—

2.16 8-Bit Timer

Table 2.52 is a comparative overview of 8-bit timer.

Table 2.52 Comparative Overview of 8-Bit Timer

Item	RX66N (TMR)	RX671 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 to TMR3)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.17 USB 2.0 FS Host/Function Module

Table 2.53 is a comparative overview of the USB 2.0 FS Host/Function module.

Table 2.53 Comparative Overview of USB 2.0 FS Host/Function Module

Item	RX66N (USBb)	RX671 (USBb)
Number of channels	1 channel	2 channels
Features	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — Support for Host controller, Function controller, and on-the-go (OTG) functionality (1 channels) • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected.	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — Support for Host controller, Function controller, and on-the-go (OTG) functionality (2 channels) • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected.
	When Host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub	When Host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub
	When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function	When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.

Item	RX66N (USBb)	RX671 (USBb)
Pipe configuration	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer, 64-byte single buffer • PIPE1 and PIPE2: — 64-byte double buffer can be specified for bulk transfer. — 256-byte double buffer can be specified for isochronous transfer. • PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer • PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer, 64-byte single buffer • PIPE1 and PIPE2: — 64-byte double buffer can be specified for bulk transfer. — 256-byte double buffer can be specified for isochronous transfer. • PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer • PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer
Other functions	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO port (n = 0 or 1) has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip D+/D– pull-up and pull-down resistors	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO port (n = 0 or 1) has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip D+/D– pull-up and pull-down resistors
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Note: 1. Low-speed transfer (1.5 Mbps) is not supported when Function controller operation is selected.

2.18 Serial Communications Interface

Table 2.54 is a comparative overview of the serial communications interfaces, Table 2.55 is a comparative listing of serial communications interface channels, Table 2.56 is a comparison of serial communications interface registers, and Table 2.57 is a comparison of TXDn pin control settings.

Table 2.54 Comparative Overview of Serial Communications Interfaces

Item		RX66N (SCIj, SCIi, SCIh)	RX671 (SCIk, SCIm, SCIh)
Number of channels		• SCIj: 7 channels • SCIi: 5 channels • SCIh: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.
Full-duplex communication		• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering	• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering
Data transfer		Selectable between LSB-first and MSB-first	Selectable between LSB-first and MSB-first
I/O signal level inversion		—	Ability to invert levels of input and output signals independently (SCI0 to SCI11)
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error (SCI0 to SCI12) • Data match (SCI0 to SCI11) • Receive data ready (SCI7 to SCI11) • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode) (SCI0 to SCI12)	• Transmit end, transmit data empty, receive data full, receive error (SCI0 to SCI12) • Data match (SCI0 to SCI11) • Receive data ready (SCI10 and SCI11) • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode) (SCI0 to SCI12)
Low power consumption function		Ability to transition each channel to module stop state	Ability to transition each channel to module stop state
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control

Item		RX66N (SCIj, SCIi, SCIh)	RX671 (SCIk, SCIm, SCIh)
Asynchronous mode	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
	Data match detection	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI0 to SCI11)	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI0 to SCI11)
	Start-bit detection	Selectable between low level and falling edge	Selectable between low level and falling edge
	Receive data sampling timing adjustment	—	Ability to change the sampling point for receive data forward or backward relative to a reference point at the center of the data (SCI0 to SCI11)
	Transmit signal change timing adjustment	—	Ability to delay the falling or rising edge of the transmit data (SCI0 to SCI11)
	Break detection	• Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly (SCI0 to SCI12) • Ability to detect a break by reading the SPTR.RXDMON flag (SCI10 and SCI11)	• Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly (SCI0 to SCI12) • Ability to detect a break by reading the SPTR.RXDMON flag (SCI0 to SCI11)
	Clock source	• Selectable between internal or external clock (SCI0 to SCI12) • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)	• Selectable between internal or external clock (SCI0 to SCI12) • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)
	Double-speed mode	Ability to select baud rate generator double-speed mode	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	The input signal paths from the RXDn pins incorporate digital noise filters.	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
Smart card interface mode	Error processing	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention

Item		RX66N (SCIj, SCIi, SCIh)	RX671 (SCIk, SCIm, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Support for fast mode	Support for fast mode
	Noise cancellation	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.
	Clock settings	Ability to select among four clock phase and clock polarity settings	Ability to select among four clock phase and clock polarity settings
Extended serial mode (supported by SCI12 only)	Start Frame transmission	• Ability to output Break Field low width/output completion interrupt function • Bus collision detection function/detection interrupt function	• Ability to output Break Field low width/output completion interrupt function • Bus collision detection function/detection interrupt function
	Start Frame reception	• Ability to detect Break Field low width/detection completion interrupt function • Control Field 0 and Control Field 1 data comparison/ match interrupt function • Ability to select between two data types for comparison (primary and secondary) in Control Field 1 • Ability to set priority interrupt bit in Control Field 1 • Support for Start Frames that do not include a Break Field • Support for Start Frames that do not include Control Field 0 • Bit rate measurement function	• Ability to detect Break Field low width/detection completion interrupt function • Control Field 0 and Control Field 1 data comparison/ match interrupt function • Ability to select between two data types for comparison (primary and secondary) in Control Field 1 • Ability to set priority interrupt bit in Control Field 1 • Support for Start Frames that do not include a Break Field • Support for Start Frames that do not include Control Field 0 • Bit rate measurement function
	I/O control function	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12
	Timer function	Usable as reload timer	Usable as reload timer

Item	RX66N (SCIj, SCIi, SCIh)	RX671 (SCIk, SCIm, SCIh)
Bit rate modulation function	Ability to reduce errors by correcting output from the on-chip baud rate generator	Ability to reduce errors by correcting output from the on-chip baud rate generator
Event link function (supported by SCI5 only)	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.55 Comparative Listing of Serial Communications Interface Channels

Item	RX66N (SCIj, SCIi, SCIh)	RX671 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
FIFO mode	SCI7 to SCI11	SCI10, SCI11
Data match detection	SCI0 to SCI11	SCI0 to SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0 to SCI6, SCI12 PCLKA: SCI7 to SCI11	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11

Table 2.56 Comparison of Serial Communications Interface Registers

Register	Bit	RX66N (SCIj, SCIi, SCIh)	RX671 (SCIk, SCIm, SCIh)
SEMR	ITE	—	Immediate transmit enable bit
SPTR	RXDMON	RXD line monitoring bit 0: RXDn pin is low-level 1: RXDn pin is high-level	RXD line monitoring bit When RINV = 0 0: RXDn pin is low-level 1: RXDn pin is high-level When RINV = 1 0: RXDn pin is high-level 1: RXDn pin is low-level
	SPB2DT SPB2IO	Serial port break data bit Serial port break I/O bit In clock-synchronous mode, the TXDn pins are controlled by the SCR.TE, SPB2DT, and SPB2IO bits in combination. For details, refer to Table 2.57.	Serial port break data bit Serial port break I/O bit The TXDn pins are controlled by the SCR.TE, SPB2DT, SPB2IO, and TINV bits in combination. For details, refer to Table 2.57. These settings take effect in clock-synchronous mode only.
	RINV	—	Receive input invert bit
	TINV	—	Transmit output invert bit
	RTADJ	—	Receive data sampling timing adjustment bit
	TTADJ	—	Transmit signal change timing adjustment bit
TMGR	—	—	Transmit/receive timing select register

Table 2.57 Comparison of TXDn Pin Control Settings

SCR.TE Bit Setting Value	SPB2IO Bit Setting Value	SPB2DT Bit Setting Value	TXDn Pin State	
			RX66N	RX671
0 (transmit disabled)	0 (input)	Any value	Hi-Z	Hi-Z
	1 (output)	0	Low-level output	When TINV bit = 0 Low-level output When TINV bit = 1 High-level output
		1	High-level output	When TINV bit = 0 High-level output When TINV bit = 1 Low-level output
1 (transmit enabled)	Any value	Any value	Transmit data output pin	Transmit data output pin

2.19 CAN Module

Table 2.58 is a comparative overview of the CAN modules.

Table 2.58 Comparative Overview of CAN Modules

Item	RX66N (CAN)	RX671 (CAN)
Number of channels	3 channels	2 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX66N (CAN)	RX671 (CAN)
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLKB), CANMCLK	Peripheral module clock (PCLKB), CANMCLK

Item	RX66N (CAN)	RX671 (CAN)
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.20 Serial Peripheral Interface

Table 2.59 is a comparative overview of the serial peripheral interfaces, and Table 2.60 is a comparison of serial peripheral interface registers.

Table 2.59 Comparative Overview of Serial Peripheral Interfaces

Item	RX66N (RSPIc)	RX671 (RSPId)
Number of channels	3 channels	3 channels
RSPI transfer functions	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Communication mode: Selectable between full-duplex and transmit-only • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Communication mode: Selectable between full-duplex and simplex (transmit-only or receive-only (in slave mode)) • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK
Data format	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame) • Ability to swap transmit and receive data in byte units	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame) • Ability to swap transmit/receive data in byte units • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX66N (RSPIc)	RX671 (RSPId)
SSL control function	• Four SSL pins (SSLx0 to SSLx3) per channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused. • In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLx0 to SSLx3) per channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused. • In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity
Control during master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt • Communication end interrupt

Item	RX66N (RSPIc)	RX671 (RSPId)
Event link function (output)	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Mode fault, overrun, underrun, or parity error event signal • RSPI idle event signal • Transmission-completed event signal	The following events can be output to the event link controller (RSPI0): • Receive buffer full events • Transmit buffer empty events • Error events (mode fault, overrun, underrun, parity error) • Idle events • Communication completion events
Other functions	• Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.60 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX66N (RSPIc)	RX671 (RSPId)
SPSR	SPCF	—	Communication completion flag
SPCR2	SPPE	Parity enable bit 0: No transmit data parity bit appended No parity checking is performed on receive data. 1: A transmit data parity bit is appended. Parity checking is performed on receive data.	Parity enable bit 0: No transmit data parity bit appended No parity checking is performed on receive data. 1: A transmit data parity bit is appended, and parity checking is performed on receive data (when SPCR.TXMD = 0). A parity bit is appended to transmit data, but no parity checking is performed on receive data (when SPCR.TXMD = 1).
SPDCR2	DINV	—	Transfer data invert bit
SPCR3	—	—	RSPI control register 3

2.21 Quad Serial Peripheral Interface/Quad SPI Memory Interface

Table 2.61 is a comparative overview of the quad serial peripheral interface and quad SPI memory interface, and Table 2.62 is a comparison of quad serial peripheral interface and quad SPI memory interface registers.

Table 2.61 Comparative Overview of Quad Serial Peripheral Interface and Quad SPI Memory Interface

Item	RX66N (QSPI)	RX671 (QSPIX)
Channels	1 channel	1 channel
SPI	• Ability to communicate with serial flash memory using single-, dual-, or quad-SPI operation • Ability to configure SPI modes 0 to 4	• Support for extended SPI, dual-SPI, and quad-SPI protocols • Ability to configure SPI modes 0 and 3 • Ability to select address width of 8, 16, 24, or 32 bits
Timing adjustment function	—	Ability to implement configurations supporting a variety of serial flash specifications
Memory mapped mode	—	• Support for read, fast read, fast read dual output, fast read dual I/O, fast read quad output, and fast read quad I/O instructions • Ability to substitute instruction codes • Ability to adjust dummy cycle count • Prefetch function • Polling processing • SPI bus cycle extension function
Indirect access mode	—	Flexible support using software control for various serial flash instructions/functions, including erase, write, ID read, and power down control
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • QSSL negate interrupt	• Error interrupt
Module stop function	Ability to transition to module stop state	Ability to reduce power consumption by enabling module stop state

Table 2.62 Comparison of Quad Serial Peripheral Interface and Quad SPI Memory Interface Registers

Register	Bit	RX66N (QSPI)	RX671 (QSPIX)
SPCR	—	QSPI control register	—
SSLP	—	QSPI slave select polarity register	—
SPPCR	—	QSPI pin control register	—
SPSR	—	QSPI status register SPSR is a 16-bit register.	SPI status register SPSR is a 32-bit register.
		Initial value after a reset differs.	
	SPSSLF	QSSL negate flag	—
	SPTEF	Transmit buffer empty flag	—
	TREND	Transmit end flag	—
	SPRFF	Receive buffer full flag	—
	BUSY	—	Bus busy flag
	ROMAE	—	ROM access error flag

Register	Bit	RX66N (QSPI)	RX671 (QSPIX)
SPDR	—	QSPI data register Writing to this register is accomplished by writing to the transmit buffer (SPTXB), and reading from this register is accomplished by reading from the receive buffer (SPRXB). This register can be accessed in byte, word, or longword units.	SPI data register Reads and writes to this register are converted into SPI bus cycles. When the AMOD bit is set to 1, this register can only be accessed in indirect access mode. In memory mapped mode, accesses to this register are ignored.
SPSCR	—	QSPI sequence control register	—
SPSSR	—	QSPI sequence status register	—
SPBR	—	QSPI bit rate register	—
SPDCR	TXDMY	Dummy data transmit enable bit	—
	DCYC[3:0]	—	Dummy cycle count setting bits
	XIPS	—	XIP status flag
	XIPE	—	XIP enable bit
	MODE[7:0]	—	Mode data bits
SPCKD	—	QSPI clock delay register	—
SSLND	—	QSPI slave select negate delay register	—
SPND	—	QSPI next access delay register	—
SPCMDn	—	QSPI command register n (n = 0 to 3)	—
SPBFCR	—	QSPI buffer control register	—
SPBDCR	—	QSP buffer data count setting register	—
SPBMULn	—	QSPI transfer data length multiple setting register n (n = 0 to 3)	—
SPMR0	—	—	Mode register 0
SPSSCR	—	—	Slave select signal control register
SPOCR	—	—	Operating clock control register
SPPFSR	—	—	Prefetch status register
SPMR1	—	—	Mode register 1
SPSR	—	—	SPI status register
SPRIR	—	—	Independent read instruction setting register
SPAMR	—	—	Address mode register
SPMR2	—	—	Mode register 2
SPPCR	—	—	Port control register
SPUAR	—	—	Upper-bit address register

2.22 Serial Sound Interface

Table 2.63 is a comparative overview of the serial sound interfaces.

Table 2.63 Comparative Overview of Serial Sound Interfaces

Item		RX66N (SSIE)	RX671 (SSIE)
Number of channels		2 channels (SSIE0 and SSIE1)	1 channel (SSIE0)
Transfer modes		• Master/slave • Transmission, reception, or transception (transception on SSIE0 only)	• Master/slave • Transmission, reception, or transception
Data formats		• I^2S format • Left-justified format • Right-justified format • Monaural format • TDM format	• I^2S format • Left-justified format • Right-justified format • Monaural format • TDM format
Serial data		• Fixed at MSB first • System word length: Selectable among 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: Selectable among 8, 16, 18, 20, 22, 24, or 32 bits • Polarity of the padding bits is selectable. • Mute function	• Fixed at MSB first • System word length: Selectable among 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: Selectable among 8, 16, 18, 20, 22, 24, or 32 bits • Polarity of the padding bits is selectable. • Mute function
Bit clock (BCK)	In master mode	• Clock source: AUDIO_CLK • Frequency: Selectable among: 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128 of the AUDIO_CLK frequency • Ability to select supply or stop while data transfer is halted	• Clock source: AUDIO_CLK • Frequency: Selectable among: 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128 of the AUDIO_CLK frequency • Ability to select supply or stop while data transfer is halted
	In master and slave modes	Ability to select polarity (rising or falling edge)	Ability to select polarity (rising or falling edge)
LR clock (LRCK)		• Ability to select polarity (low or high) • Ability to select supply or stop while data transfer is halted	• Ability to select polarity (low or high) • Ability to select supply or stop while data transfer is halted
FIFO	Capacity	• Transmit FIFO: 4 bytes × 32 stages • Receive FIFO: 4 bytes × 32 stages	• Transmit FIFO: 4 bytes × 32 stages • Receive FIFO: 4 bytes × 32 stages
	Data alignment	Ability to select alignment of data (left-justified or right-justified) in the FIFO	Ability to select alignment of data (left-justified or right-justified) in the FIFO
Interrupts		• Data transfer error/idle state • Receive data full • Transmit data empty	• Data transfer error/idle state • Receive data full • Transmit data empty
Low power consumption function		• Module stop function • Master clock (MCK) supply stop function	• Module stop function • Master clock (MCK) supply stop function

2.23 Boundary Scan

Table 2.64 is a comparative overview of the boundary scan functions, and Table 2.65 is a comparison of boundary scan registers.

Table 2.64 Comparative Overview of Boundary Scan Functions

Item	RX66N	RX671
Boundary scan enable/disable	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	The following pins are used exclusively by the JTAG when the boundary scan function is enabled: TDO, TCK, TDI, TMS, and TRST# 224-pin LFBGA and 176-pin LFBGA products: PF0, PF1, PF2, PF3, and PF4 145-pin TFLGA products: P26, P27, P30, P31, and P34	The following pins are used exclusively by the JTAG when the boundary scan function is enabled: TDO, TCK, TDI, TMS, and TRST# 145-pin TFLGA and 64-pin TFBGA products: P26, P27, P30, P31, and P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

Table 2.65 Comparison of Boundary Scan Registers

Register	Bit	RX66N	RX671
JTIDR	—	ID code register	ID code register
		Initial value after a reset differs.	

2.24 12-Bit A/D Converter

Table 2.66 is a comparative overview of the 12-bit A/D converters, Table 2.67 is a comparison of 12-bit A/D converter registers, Table 2.68 is a comparison of A/D conversion start triggers that can be set in the ADSTRGR register, and Table 2.69 is a comparison of A/D conversion start triggers that can be set in the ADGCTRGR register.

Table 2.66 Comparative Overview of 12-Bit A/D Converters

Item	RX66N (S12ADFa)	RX671 (S12ADFa)
Number of units	2 units (S12AD, S12AD1)	2 units (S12AD, S12AD1)
Input channels	S12AD: 8 channels S12AD1: 21 channels + 1 extension	S12AD: 8 channels S12AD1: 12 channels + 1 extension
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.48 µs per channel (12-bit conversion mode) 0.45 µs per channel (10-bit conversion mode) 0.42 µs per channel (8-bit conversion mode) (When A/D conversion clock (ADCLK) = 60 MHz)	0.48 µs per channel (12-bit conversion mode) 0.45 µs per channel (10-bit conversion mode) 0.42 µs per channel (8-bit conversion mode) (When A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.
Data registers	• 29 registers for analog input (eight for S12AD and 21 for S12AD1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD1) • One register for internal reference (S12AD1) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • Support for output of A/D conversion results at 8-, 10-, or 12-bit accuracy • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.	• 20 registers for analog input (eight for S12AD and 12 for S12AD1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD1) • One register for internal reference (S12AD1) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • Support for output of A/D conversion results at 8-, 10-, or 12-bit accuracy • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX66N (S12ADFa)	RX671 (S12ADFa)
Data registers	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	Operating modes can be set independently for two units. • Single scan mode: — A/D conversion is performed only once on the analog inputs arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (S12AD1). — A/D conversion is performed only once on the internal reference voltage (S12AD1). — A/D conversion is performed only once on the extended analog input (S12AD1). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog input, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) of an arbitrarily selected channel. — A/D conversion is performed repeatedly on the extended analog input (S12AD1). • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.	Operating modes can be set independently for two units. • Single scan mode: — A/D conversion is performed only once on the analog inputs arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (S12AD1). — A/D conversion is performed only once on the internal reference voltage (S12AD1). — A/D conversion is performed only once on the extended analog input (S12AD1). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog input, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) of an arbitrarily selected channel. — A/D conversion is performed repeatedly on the extended analog input (S12AD1). • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.

Item	RX66N (S12ADFa)	RX671 (S12ADFa)
Operating modes	— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.	— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger: Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC). • Asynchronous trigger: A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) or ADTRG1# (S12AD1) pin (independently for two units).	• Software trigger • Synchronous trigger: Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC). • Asynchronous trigger: A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) or ADTRG1# (S12AD1) pin (independently for two units).
Functions	• Channel-dedicated sample-and-hold function (three channels for S12AD only) • Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-/10-/8-bit conversion switching • Automatic clear function of A/D data registers • Extended analog input • Comparison function (windows A and B)	• Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-/10-/8-bit conversion switching • Automatic clear function of A/D data registers • Extended analog input • Comparison function (windows A and B)

Item	RX66N (S12ADFa)	RX671 (S12ADFa)
Interrupt sources	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (Independently for two units). • In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. (Independently for two units). • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan, whereas a group B–exclusive scan end interrupt request (S12GBADI or S12GBADI1) can be generated on completion of a group B scan, and a group C–exclusive scan end interrupt request (S12GCADI or S12GCADI1) can be generated on completion of a group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan of group A, and a scan end interrupt request exclusive to the corresponding group (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1, S12GBADI/S12GBADI1, and S12GCADI/S12GCADI1 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (Independently for two units). • In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. (Independently for two units). • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan, whereas a group B–exclusive scan end interrupt request (S12GBADI or S12GBADI1) can be generated on completion of a group B scan, and a group C–exclusive scan end interrupt request (S12GCADI or S12GCADI1) can be generated on completion of a group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan of group A, and a scan end interrupt request exclusive to the corresponding group (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1, S12GBADI/S12GBADI1, and S12GCADI/S12GCADI1 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).
Event linking function	• The ELC event signal is generated when all scans are finished. • Able to start scanning by a trigger from the ELC.	• The ELC event signal is generated when all scans are finished. • Able to start scanning by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.67 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX66N (S12ADFa)	RX671 (S12ADFa)
ADDRy	—	A/D data registers y (y = 0 to 7: S12AD, y = 0 to 20: S12AD1)	A/D data registers y (y = 0 to 11)
S12AD1. ADANSA0	ANSA012 to ANSA015	A/D conversion channel select bits	—
ADANSA1	—	A/D channel select register A1	—
S12AD1. ADANSB0	ANSB012 to ANSB015	A/D conversion channel select bits	—
ADANSB1	—	A/D channel select register B1	—
S12AD1. ADANSC0	ANSC012 to ANSC015	A/D conversion channel select bits	—
ADANSC1	—	A/D channel select register C1	—
S12AD1. ADADS0	ADS012 to ADS015	A/D-converted value addition/average channel select bits	—
ADADS1	—	A/D-converted value addition/ average function channel select register 1	—
ADSTRGR	TRSB[5:0]	A/D conversion start trigger select bits for group B Refer to Table 2.68 for details.	A/D conversion start trigger select bits for group B Refer to Table 2.68 for details.
	TRSA[5:0]	A/D conversion start trigger select bits Refer to Table 2.68 for details.	A/D conversion start trigger select bits Refer to Table 2.68 for details.
ADGCTRGR	TRSC[5:0]	A/D conversion start trigger select bits for group C Refer to Table 2.69 for details.	A/D conversion start trigger select bits for group C Refer to Table 2.69 for details.
ADSSTRn	—	A/D sampling state register n (n = 0 to 15, L, T, O)	A/D sampling state register n (n = 0 to 11, T, O)
ADSHCR	—	A/D sample-and-hold circuit control register	—
ADSHMSR	—	A/D sample-and-hold operating mode select register	—
S12AD1. ADCMPANSR0	CMPCHA012 to CMPCHA015	Comparison window A channel select bits	—
ADCMPANSR1	—	A/D comparison function window A channel select register 1	—
S12AD1. ADCMPLR0	CMPLCHA012 to CMPLCHA015	Comparison window A comparison condition select bits	—
ADCMPLR1	—	A/D comparison function window A comparison condition setting register 1	—
S12AD1. ADCMPSR0	CMPSTCHA012 to CMPSTCHA015	Comparison window A flags	—
ADCMPSR1	—	A/D comparison function window A channel status register 1	—

Table 2.68 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register

Bit	RX66N (S12ADFa)	RX671 (S12ADFa)
TRSB[5:0]	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 0 1 0 0 0 1: ELCTRG00N/ELCTRG10N 0 1 0 0 1 0: ELCTRG01N/ELCTRG11N 0 1 1 0 0 1: ELCTRG00N or ELCTRG01N/ELCTRG10N or ELCTRG11N	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 1 1 0 0 0 0: ELCTRG0N/ELCTRG1N

Bit	RX66N (S12ADFa)	RX671 (S12ADFa)
TRSA[5:0]	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 0 1 0 0 0 1: ELCTRG00N/ELCTRG10N 0 1 0 0 1 0: ELCTRG01N/ELCTRG11N 0 1 1 0 0 1: ELCTRG00N or ELCTRG01N/ELCTRG10N or ELCTRG11N	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 1 1 0 0 0 0: ELCTRG0N/ELCTRG1N

Table 2.69 Comparison of A/D Conversion Start Triggers Set in ADGCTRGR Register

Bit	RX66N (S12ADFa)	RX671 (S12ADFa)
TRSC[5:0]	Group C A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 0 1 0 0 0 1: ELCTRG00N/ELCTRG10N 0 1 0 0 1 0: ELCTRG01N/ELCTRG11N 0 1 1 0 0 1: ELCTRG00N or ELCTRG01N/ELCTRG10N or ELCTRG11N	Group C A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 1 1 0 0 0 0: ELCTRG0N/ELCTRG1N

2.25 Data Operation Circuit

Table 2.70 is a comparative overview of data operation circuit, and Table 2.71 is a comparison of data operation circuit registers.

Table 2.70 Comparative Overview of Data Operation Circuit

Item	RX66N (DOC)	RX671 (DOCA)
Data operation functions	• 16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32-bit data
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event linking function (output)	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.71 Comparison of Data Operation Circuit Registers

Register	Bit	RX66N (DOC)	RX671 (DOCA)
DOCR	DCSEL (RX66N) DCSEL[2:0] (RX671)	Detection condition select bit (b2) Data comparison result 0: Detect mismatches 1: Detect matches	Detection condition select bits (b6 to b4) b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPSZ	—	Data operation size select bit
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register DODIR is a 16-bit register.	DOC data input register DODIR is a 32-bit register. Access this register in units equal to the data operation size specified by the DOCR.DOPSZ bit.
DODSR (RX66N) DODSR0/ DODSR1 (RX671)	—	DOC data setting register DODSR is a 16-bit register.	DOC data setting registers 0 and 1 DODSR0 and DODSR1 are 32-bit registers. Access these registers in units equal to the data operation size specified by the DOCR.DOPSZ bit.

2.26 RAM

Table 2.72 is a comparative overview of RAM, and Table 2.73 is a comparison of RAM registers.

Table 2.72 Comparative Overview of RAM

Item	RX66N			RX671
	RAM	Expansion RAM	ECCRAM	RAM
Capacity	512 KB	512 KB	32 KB	384 KB
Address	0000 0000h to 0007 FFFFh	0080 0000h to 0087 FFFFh	00FF 8000h to 00FF FFFFh	0000 0000h to 0005 FFFFh
Memory bus	Memory bus 1	Memory bus 3	Memory bus 3	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• The Expansion RAM can be enabled or disabled. • Single-cycle access is possible for both reading and writing	• The ECCRAM can be enabled or disabled. • When the ECC function is disabled, read or write access requires two cycles. • When the ECC function is enabled (and there are no errors), read or write access requires two cycles. • When the ECC function is enabled (and an error occurs), read or write access requires three cycles.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Data retention function	Not available in deep software standby mode			Not available in deep software standby mode
Low power consumption function	Transition to module stop state can be enabled separately for RAM, expansion RAM, and ECCRAM.			Ability to transition to the module stop state
Error checking	• Parity checking: 1-bit error detection • A non-maskable interrupt or interrupt is generated in response to an error.		• ECC error correction: —Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• Parity checking: 1-bit error detection • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.73 Comparison of RAM Registers

Register	Bit	RX66N	RX671
EXRAMMODE	—	Expansion RAM operating mode control register	—
EXRAMSTS	—	Expansion RAM error status register	—
EXRAMECAD	—	Expansion RAM error address capture register	—
EXRAMPRCR	—	Expansion RAM protection register	—
ECCRAMMODE	—	ECCRAM operating mode control register	—
ECCRAM2STS	—	ECCRAM 2-bit error status register	—
ECCRAM1STSEN	—	ECCRAM 1-bit error information update enable register	—
ECCRAM1STS	—	ECCRAM 1-bit error status register	—
ECCRAMPRCR	—	ECCRAM protection register	—
ECCRAM2ECAD	—	ECCRAM 2-bit error address capture register	—
ECCRAM1ECAD	—	ECCRAM 1-bit error address capture register	—
ECCRAMPRCR2	—	ECCRAM protection register 2	—
ECCRAMETST	—	ECCRAM test control register	—

2.27 Standby RAM

Table 2.74 is a comparative overview of standby RAM.

Table 2.74 Comparative Overview of Standby RAM

Item	RX66N	RX671
RAM capacity	8 KB	4 KB
RAM address	000A 4000h to 000A 5FFFh	000A 4000h to 000A 4FFFh
Access	• Read and write operations require three or four cycles of PCLKB when ICLK ≥ PCLKB and two or three cycles of ICLK when ICLK < PCLKB. • Ability to enable or disable RAM access • The endian order conforms to the endian setting of the chip. • Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.	• Read and write operations require two or three cycles of PCLKB when ICLK ≥ PCLKB and two cycles of ICLK when ICLK < PCLKB. • Ability to enable or disable RAM access • The endian order conforms to the endian setting of the chip. • Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.
Data retention function	Data can be retained in deep software standby mode.	Data can be retained in deep software standby mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

2.28 Flash Memory

Table 2.75 is a comparative overview of flash memory, and Table 2.76 is a comparison of flash memory registers.

Table 2.75 Comparative Overview of Flash Memory

Item	RX66N (FLASH)		RX671 (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	User area: Up to 4 MB	Data area: 32 KB	User area: Up to 2 MB	Data area: 8 KB
Address	• When capacity is 4 MB: FFC0 0000h to FFFF FFFFh • When capacity is 2 MB: FFE0 0000h to FFFF FFFFh	0010 0000h to 0010 7FFFh	• When capacity is 2 MB: FFE0 0000h to FFFF FFFFh • When capacity is 1.5 MB: FFE8 0000h to FFFF FFFFh • When capacity is 1 MB: FFF0 0000h to FFFF FFFFh	0010 0000h to 0010 1FFFh
ROM cache	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—
Read cycles	• While ROM cache operation is enabled: — When the cache is hit: One cycle — When the cache is missed: One or two cycles • When ROM cache operation is disabled: One cycle	Reading proceeds in every cycle of FCLK.	• While ROM cache operation is enabled: — When the cache is hit: One cycle — When the cache is missed: One or two cycles when ICLK ≤ 60 MHz; two or three cycles when ICLK > 60 MHz • When ROM cache operation is disabled: — One cycle when ICLK ≤ 60 MHz — Two cycles when ICLK > 60 MHz	Reading proceeds in every cycle of FCLK.
Value after erasure	FFh	Undefined	FFh	Undefined

Item	RX66N (FLASH)		RX671 (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Programming/ erasing method	• Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACI commands specified in the FACI command issuing area (007E 0000h) (self-programming) • Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)		• Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACI commands specified in the FACI command issuing area (007E 0000h) (self-programming) • Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)	
Security function	Protects against illicit tampering or reading of data in flash memory		Protects against illicit tampering or reading of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory (software protection, error protection, startup program protection function, area protection, and dual-bank function)		Protects against erroneous rewriting of the flash memory (software protection, error protection, startup program protection function, area protection, and dual-bank function)	
Dual bank function	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	—	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	—
Trusted memory (TM) function	Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 78, and 79	—	Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 46, and 47	—
Background operation (BGO)	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.		• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes
Other functions	• Interrupts can be accepted during self-programming. • The initial settings of the MCU can be specified in the option-setting memory.		• Interrupts can be accepted during self-programming. • The initial settings of the MCU can be specified in the option-setting memory.	

Item	RX66N (FLASH)		RX671 (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
On-board programming (serial programming/ self-programming)	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming or erasure by self-programming — Programming and erasure can be performed without resetting the system.		• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming and erasure in single-chip mode — Programming and erasure can be performed by a code flash memory or data flash memory programming routine in a user program.	
Off-board programming	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.	Programming or erasure of the data flash memory by using a parallel programmer is not possible.	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.	Programming or erasure of the data flash memory by using a parallel programmer is not possible.
Unique ID	A 16-byte ID code is provided for each MCU.		A 16-byte ID code is provided for each MCU.	

Table 2.76 Comparison of Flash Memory Registers

Register	Bit	RX66N (FLASH)	RX671 (FLASH)
NCRCn	NCSZ[16:0]	Non-cacheable area size specification bits These bits specify the size of the non-cacheable area. b20 b4 0 0000 0000 0000 0000: 16 bytes 0 0000 0000 0000 0001: 32 bytes 0 0000 0000 0000 0011: 64 bytes 0 0000 0000 0000 0111: 128 bytes 0 0000 0000 0000 1111: 256 bytes 0 0000 0000 0001 1111: 512 bytes 0 0000 0000 0011 1111: 1 KB 0 0000 0000 0111 1111: 2 KB 0 0000 0000 1111 1111: 4 KB 0 0000 0001 1111 1111: 8 KB 0 0000 0011 1111 1111: 16 KB 0 0000 0111 1111 1111: 32 KB 0 0000 1111 1111 1111: 64 KB 0 0001 1111 1111 1111: 128 KB 0 0011 1111 1111 1111: 256 KB 0 0111 1111 1111 1111: 512 KB 0 1111 1111 1111 1111: 1 MB 1 1111 1111 1111 1111: 2 MB Other than above: Setting prohibited.	Non-cacheable area size specification bits These bits specify the size of the non-cacheable area. b20 b4 0 0000 0000 0000 0000: 16 bytes 0 0000 0000 0000 0001: 32 bytes 0 0000 0000 0000 0011: 64 bytes 0 0000 0000 0000 0111: 128 bytes 0 0000 0000 0000 1111: 256 bytes 0 0000 0000 0001 1111: 512 bytes 0 0000 0000 0011 1111: 1 KB 0 0000 0000 0111 1111: 2 KB 0 0000 0000 1111 1111: 4 KB 0 0000 0001 1111 1111: 8 KB 0 0000 0011 1111 1111: 16 KB 0 0000 0111 1111 1111: 32 KB 0 0000 1111 1111 1111: 64 KB 0 0001 1111 1111 1111: 128 KB 0 0011 1111 1111 1111: 256 KB 0 0111 1111 1111 1111: 512 KB 0 1111 1111 1111 1111: 1 MB Other than above: Setting prohibited.

2.29 Packages

As indicated in Table 2.77, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.77 Comparison of Packages

Package Type	Renesas Code	
	RX66N	RX671
224-pin LFBGA	○	×
176-pin LFBGA	○	×
176-pin LFQFP	○	×
145-pin TFLGA	PTLG0145KA-A	PTLG0145JC-A, PTLG0145KB-A
100-pin TFLGA	×	○
64-pin TFBGA	×	○
64-pin LFQFP	×	○
48-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 145-Pin TFLGA Package (RX671: 0.65 mm Pin Pitch)

Table 3.1 is a comparative listing of the pin functions of 145-pin TFLGA package (RX671: 0.65 mm pin pitch) products.

Table 3.1 Comparative Listing of 145-Pin TFLGA Package Pin Functions (RX671: 0.65 mm Pin Pitch)

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/ AN108
A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
A8	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
A10	VSS	VSS
A11	P62/RAS#/D1[A1/D1]/CS2#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
A12	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2-B/ MMC_D5-B/LCD_DATA15-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A13	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
B1	AVCC1	AVCC1
B2	AVCC0	AVCC0
B3	P05/SSILRCK1/IRQ13/DA1	P05/IRQ13
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN115	P91/A17/SCK7/IRQ9
B8	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
B10	VCC	VCC
B11	P61/SDCS#/D0[A0/D0]/CS1#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
B12	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
C1	AVSS1	AVSS1
C2	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	P02/TMCI1/SCK6/IRQ10/AN109
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS
C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
C8	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/ AN104
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
C10	P63/CAS#/D2[A2/D2]/CS3#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
C11	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
C12	P70/SDCLK	P70/SDCLK/IRQ0
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
D2	PF5/WAIT#/SSILRCK0/IRQ4	PF5/IRQ4
D3	P03/SSIDATA1/IRQ11/DA0	P03/IRQ11
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
D5	VCC	VCC
D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
D8	P60/CS0#	P60/CS0#/IRQ0
D9	P64/WE#/D3[A3/D3]/CS4#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
D10	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D11	VCC	VCC
D12	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
D13	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
E1	VSS	VSS
E2	VCL	VCL
E3	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
E10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E11	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	P66/CS6#/DQM0/MTIOC7D/IRQ14
E12	P65/CKE/CS5#	P65/CS5#/CKE/IRQ13
E13	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS
F11	VSS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
F13	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/ IRQ10
G1	XTAL/P37	XTAL/P37
G2	RES#	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
G12	VCC	VSS_USB
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS	USB1_DP
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
H4	UPSEL/P35/NMI	UPSEL/P35/NMI
H10	P72/A19/CS2#/ET0_MDC/PMGI0_MDC	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12
H11	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12	VCC_USB
H13	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	USB1_DM
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
J11	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
K1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
K5	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ MOSIC-B/IRQ4
K6	P53*1/BCLK	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ USB1_EXICEN/SDHI_WP/QIO2-A/IRQ8
K10	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
L1	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
L6	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
L8	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
L9	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP
L11	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
L12	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/USB1_VBUS/ USB1_VBUSEN/USB1_OVRCURB/IRQ8
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
M3	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/IRQ14
M4	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
M8	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/USB1_OVRCURB/ SDHI_CD/QIO3-A/IRQ9
M10	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/MMC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/USB1_ID/SDHI_CLK-A/QSPCLK-A/ IRQ7
M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/ SSDA011/TXDA011/SSL02-A/IRQ12/TS15
M13	VCC	VCC
N1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8

145-Pin TFLGA	RX66N	RX671 (0.65 mm Pin Pitch)
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
N3	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
N5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
N6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
N7	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
N8	VSS	VSS
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ SSITXD0/SMOSI010/SSDA010/TXD010/ MISO0-A/IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/USB1_VBUSEN/IRQ2
N11	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
N12	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/ USB1_OVRCURA/SDHI_D2-A/IRQ13
N13	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/USB1_VBUSEN/ IRQ12

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.2 145-Pin TFLGA Package (RX671: 0.50 mm Pin Pitch)

Table 3.2 is a comparative listing of the pin functions of 145-pin TFLGA package (RX671: 0.50 mm pin pitch) products.

Table 3.2 Comparative Listing of 145-Pin TFLGA Package Pin Functions (RX671: 0.50 mm Pin Pitch)

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/ AN108
A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
A8	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
A10	VSS	VSS
A11	P62/RAS#/D1[A1/D1]/CS2#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
A12	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A13	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
B1	AVCC1	AVCC1
B2	AVCC0	AVCC0
B3	P05/SSILRCK1/IRQ13/DA1	P05/IRQ13
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN115	P91/A17/SCK7/IRQ9
B8	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
B10	VCC	VCC
B11	P61/SDCS#/D0[A0/D0]/CS1#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
B12	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
B13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
C1	AVSS1	AVSS1
C2	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	P02/TMCI1/SCK6/IRQ10/AN109
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS
C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
C8	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/ AN104
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
C10	P63/CAS#/D2[A2/D2]/CS3#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
C11	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
C12	P70/SDCLK	P70/SDCLK/IRQ0
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
D2	PF5/WAIT#/SSILRCK0/IRQ4	PF5/IRQ4
D3	P03/SSIDATA1/IRQ11/DA0	P03/IRQ11
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
D5	VCC	VCC
D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
D8	P60/CS0#	P60/CS0#/IRQ0
D9	P64/WE#/D3[A3/D3]/CS4#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
D10	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D11	VCC	VCC
D12	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
D13	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
E1	VSS	VSS
E2	VCL	VCL
E3	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
E10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E11	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	P66/CS6#/DQM0/MTIOC7D/IRQ14
E12	P65/CKE/CS5#	P65/CS5#/CKE/IRQ13
E13	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
F11	VSS	VSS
F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
F13	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/ IRQ10
G1	XTAL/P37	XTAL/P37
G2	RES#	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
G12	VCC	VCC
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS
H4	UPSEL/P35/NMI	UPSEL/P35/NMI
H10	P72/A19/CS2#/ET0_MDC/PMGI0_MDC	P72/A19/CS2#/IRQ10
H11	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	P71/A18/CS1#/IRQ1
H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
H13	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
J11	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
K1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/ PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
K5	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
K6	P53*1/BCLK	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ SDHI_WP/QIO2-A/IRQ8
K10	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
L1	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/ TCLKC/TMO2/PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ SCL2-DS/USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
L6	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
L8	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
L9	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/ IRQ12/TSCAP
L11	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
L12	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/IRQ8
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
M3	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/IRQ14
M4	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
M8	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9
M10	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7
M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
M13	VCC	VCC
N1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
N3	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
N5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
N6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
N7	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
N8	VSS	VSS

145-Pin TFLGA	RX66N	RX671 (0.50 mm Pin Pitch)
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ SSITXD0/SMOSI010/SSDA010/TXD010/ MISO0-A/IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/IRQ2
N11	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
N12	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/SDHI_D2-A/IRQ13
N13	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/IRQ12

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.3 144-Pin LFQFP Package

Table 3.3 is a comparative listing of the pin functions of 144-pin LFQFP package products.

Table 3.3 Comparative Listing of 144-Pin LFQFP Package Pin Functions

144-Pin LFQFP	RX66N	RX671
1	AVSS0	AVSS0
2	P05/SSILRCK1/IRQ13/DA1	P05/IRQ13
3	AVCC1	AVCC1
4	P03/SSIDATA1/IRQ11/DA0	P03/IRQ11
5	AVSS1	AVSS1
6	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	P02/TMCI1/SCK6/IRQ10/AN109
7	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
9	PF5/WAIT#/SSILRCK0/IRQ4	PF5/IRQ4
10	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
14	VCL	VCL
15	VBATT	VBATT
16	MD/FINED	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES#	RES#
20	XTAL/P37	XTAL/P37
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36
23	VCC	VCC
24	UPSEL/P35/NMI	UPSEL/P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
26	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
30	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2

144-Pin LFQFP	RX66N	RX671
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
32	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
34	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
35	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
36	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
38	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
39	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
41	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/IRQ14
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
45	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
46	VCC_USB	VCC_USB
47	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1

144-Pin LFQFP	RX66N	RX671
48	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
49	VSS_USB	VSS_USB
50	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
51	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
52	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
53	P53*1/CLK	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
57	VSS	VSS
58	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
59	VCC	VCC
60	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ SSITXD0/SMOSI010/SSDA010/TXD010/ MISO0-A/IRQ14
61	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
62	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
63	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/IRQ2
64	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/SDHI_CD/ MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ SDHI_WP/QIO2-A/IRQ8
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP

144-Pin LFQFP	RX66N	RX671
67	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
68	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/RMII0_RX_ER/ QSPCLK-A/SDHI_CLK-A/MC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7
69	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
70	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
71	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/SDHI_D2-A/IRQ13
72	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/IRQ12
73	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
74	VCC	VCC
75	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
76	VSS	VSS
77	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/IRQ8
78	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
79	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
81	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
83	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
85	P72/A19/CS2#/ET0_MDC/PMGI0_MDC	P72/A19/CS2#/IRQ10
86	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	P71/A18/CS1#/IRQ1

144-Pin LFQFP	RX66N	RX671
87	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12
88	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
90	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
95	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/ IRQ10
96	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
97	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
98	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	P66/CS6#/DQM0/MTIOC7D/IRQ14
100	P65/CKE/CS5#	P65/CS5#/CKE/IRQ13
101	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
102	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
103	VCC	VCC
104	P70/SDCLK	P70/SDCLK/IRQ0
105	VSS	VSS
106	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
107	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12

144-Pin LFQFP	RX66N	RX671
108	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
109	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
110	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
111	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
112	P64/WE#/D3[A3/D3]/CS4#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
113	P63/CAS#/D2[A2/D2]/CS3#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
114	P62/RAS#/D1[A1/D1]/CS2#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
115	P61/SDCS#/D0[A0/D0]/CS1#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
116	VSS	VSS
117	P60/CS0#	P60/CS0#/IRQ0
118	VCC	VCC
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
120	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
121	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
122	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ QSSL-B/SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ SDHI_CMD-B/QSSL-B/IRQ4/AN103
123	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
124	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
125	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
126	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
127	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
128	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
129	P91/A17/SCK7/AN115	P91/A17/SCK7/IRQ9
130	VSS	VSS
131	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/AN108

144-Pin LFQFP	RX66N	RX671
132	VCC	VCC
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.4 100-Pin LFQFP Package

Table 3.4 is a comparative listing of the pin functions of 100-pin LFQFP package products.

Table 3.4 Comparative Listing of 100-Pin LFQFP Package Pin Functions

100-Pin LFQFP	RX66N	RX671
1	AVCC1	AVCC1
2	EMLE	EMLE
3	AVSS1	AVSS1
4	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
5	VCL	VCL
6	VBATT	VBATT
7	MD/FINED	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	UPSEL/P35/NMI	UPSEL/P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
17	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
21	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
23	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
25	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6

100-Pin LFQFP	RX66N	RX671
26	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
27	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSILRCK0/SCL1/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/SDA1/ IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
34	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
37	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
38	VSS_USB	VSS_USB
39	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET0_EXOUT/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/MISOC-B/IRQ10
40	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/MOSIC-B/ IRQ4
41	P53*1/BCLK	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSL B1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ SSITXD0/SMOSI010/SSDA010/TXD010/ MISO0-A/IRQ14

100-Pin LFQFP	RX66N	RX671
46	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
47	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP
49	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
50	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/ SDHI_D3-A/IRQ10
51	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
52	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/ SMISO011/SSCL011/SSL01-A/IRQ14/TS16
53	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
54	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
56	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ PMC0-DS/IRQ3
58	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/ET0_RX_CLK/REF50CK0/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/IRQ2
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/LCD_TCON3-B/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/IRQ12
62	VSS	VSS

100-Pin LFQFP	RX66N	RX671
63	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
65	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/ TMRI0/PO20/TXD5/SMOSI5/SSDA5/ SSLA0-B/SSL00-B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ5-DS
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS
68	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/IRQ10
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
70	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
71	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
72	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
73	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
74	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
75	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
76	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
77	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2-B/ MMC_D5-B/LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
78	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0

100-Pin LFQFP	RX66N	RX671
79	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
80	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
81	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN102
82	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
83	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/ AN104
84	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
85	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
86	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/SSILRCK1/IRQ13/DA1	P05/IRQ13

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

4. Notes on Migration

This section presents important information regarding differences between the RX671 Group and RX66N Group.

4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX66N Group is compatible with the RX671 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX671 Group and RX66N Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 Note on RX671 Group 48-Pin Package Products

On the RX671 Group the sub-clock and RTC cannot be used on 48-pin package products. After a cold start the state of the sub-clock control circuit is unstable, so do not fail to set these bits following a cold start. For details, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.1.2 Current Flow to VBATT Pin

On the RX671 Group, when the VCC voltage rises to VBATT + 0.6 V or higher while operating in battery backup mode, a current flows from the VCC pin, via a parasitic diode in the power switch on the VCC side, to the VBATT pin. If this presents a problem, insert a low-dropout diode between the backup power supply and the VBATT pin.

4.1.3 Port Direction Register (PDR) Initialization

The method for initializing the PDR register differs even on products with the same pin count.

4.1.4 Quad Serial Peripheral Interface/Quad SPI Memory Interface

The quad SPI memory interface registers on the RX671 Group incorporate significant changes compared to the quad serial peripheral interface registers on the RX66N Group. This results in a reduction in software compatibility.

4.1.5 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time of the 12-bit A/D converter differs on the RX66N Group and RX671 Group. The scan conversion time (t_{SCAN}) for single scan operation where the number of selected channels is n is shown below for each group. For details, refer to the description of "Analog Input Sampling Time and Scan Conversion Time" in the User's Manual: Hardware of each group, listed in 5, Reference Documents

RX66N: $t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX671: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_D: Start-of-scanning-delay time

t_{SPLSH}: Channel-dedicated sample-and-hold circuit processing time

t_{DIS}: Disconnection detection assistance processing time

t_{DIAG}: Self-diagnosis A/D conversion processing time

t_{CONV}: A/D conversion processing time

t_{ED}: End-of-scanning-delay time

5. Reference Documents

User's Manual: Hardware

RX66N Group User's Manual: Hardware, Rev.1.11 (R01UH0825EJ0111)
(The latest version can be downloaded from the Renesas Electronics website.)

RX671 Group User's Manual: Hardware, Rev. 1.10 (R01UH0899EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A0227A/E
- TN-RX*-A0233A/E
- TN-RX*-A0235B/E
- TN-RX*-A0257A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 7, 2021	—	First edition issued
1.10	May. 20, 2022	14	*Revised:* Table 2.4 Comparison of Clock Generation Circuit Registers
		130	*Revised:* Table 2.77 Comparison of Packages

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.