RX66N Group, RX65N/RX651 Group

Differences Between the RX66N Group and the RX65N Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX66N Group and RX65N Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 224-pin package version of the RX66N Group and the 177-pin package version of the RX65N Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX66N Group and RX65N Group

Contents

1. Comparison of Built-In Functions of RX66N Group and RX65N Group

A comparison of the built-in functions of the RX66N Group and RX65N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX66N Group and RX65N Group.

Table 1.1 Comparison of Built-In Functions of RX66N Group and RX65N Group

Function	RX65N		RX66N
	Code Flash 1.0 MB or less	Code Flash more than 1.5 MB	
CPU	●		
Operating mode	●		
Address space	▲		
Resets	○		
Option-setting memory (OFSM)	●		
Voltage detection circuit (LVDA)	○		
Clock generation circuit	●		
Clock frequency accuracy measurement circuit (CAC)	●		
Low power consumption function	●		
Battery backup function	○		
Register write protection function	●		
Exception handling	●		
Interrupt controller (ICUB): RX65N, (ICUD): RX66N	●		
Buses	●		
Memory-protection unit (MPU)	○		
DMA controller (DMACAa)	○		
EXDMA controlle (EXDMACa)	○		
Data transfer controller (DTCb)	○		
Event link controller (ELC)	●		
I/O ports	●		
Multi-function pin controller (MPC)	●		
Multi-function timer pulse unit 3 (MTU3a)	○		
Port output enable 3 (POE3a)	○		
General PWM timer (GPTW)	×		○
GPTW port output enable (POEG)	×		○
16-bit timer pulse unit (TPUa)	○		
Programmable pulse generator (PPG)	○		
8-bit timer (TMR)	○		
Compare match timer (CMT)	○		
Compare match timer W (CMTW)	○		
Realtime clock (RTCd)	○		
Watchdog timer (WDTA)	○		
Independent watchdog timer (IWDTa)	○		
Ethernet controller (ETHERC)	○		
DMA controller for the ethernet controller (EDMACa)	○		
PHY management interface (PMGI)	×		○
USB 2.0 FS Host/Function module (USBb)	○		

Function	RX65N		RX66N
	Code Flash 1.0 MB or less	Code Flash more than 1.5 MB	
Serial communications interface (SCIg, SCIi, SCIh): RX65N, (SCIj, SCIi, SCIh): RX66N	●/▲		
I²C bus interface (RIICa)	○		
CAN module (CAN)	●		
Serial peripheral interface (RSPIc)	○		
Quad serial peripheral interface (QSPI)	○		
CRC calculator (CRCA)	○		
Enhanced serial sound interface (SSIE)	×		○
SD host interface (SDHI)	○		
SD slave interfaces (SDSI)	○		×
Multimedia card interface (MMCIF)	○		
Parallel data capture unit (PDC)	○		
Graphic LCD controller (GLCDC)	×	○	
2D drawing engine (DRW2D)	×	○	
Boundary scan	○		
AESa	○	×	
RNG	○	×	
Trusted Secure IP (TSIP)	×	○	
12-bit A/D converter (S12ADFa)	▲		
12-bit D/A converter (R12DAa)	○		
Temperature sensor (TEMPS)	○		
Data operation circuit (DOC)	○		
RAM	●		
Standby RAM	▲		
Flash memory	●		
Packages	■		

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX65N	RX66N
CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit register • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Item	RX65N	RX66N
Double-precision floating point coprocessor	—	• Double-precision floating-point register set — Double-precision floating-point data registers: 64-bit × 16 — Double-precision floating-point control registers: 32-bit × 4 • Double-precision floating-point processing instructions: 21 • Function for notifying the interrupt controller of double-precision floating-point exceptions
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

Table 2.2 Comparison of CPU Registers

Register	Bit	RX65N	RX66N
DR0 to DR15	—	—	Double-precision floating-point data registers
DPSW	—	—	Double-precision floating-point status word
DCMR	—	—	Double-precision floating-point comparison result register
DECNT	—	—	Double-precision floating-point exception handling control register
DEPC	—	—	Double-precision floating-point exception program counter

2.2 Operating Modes

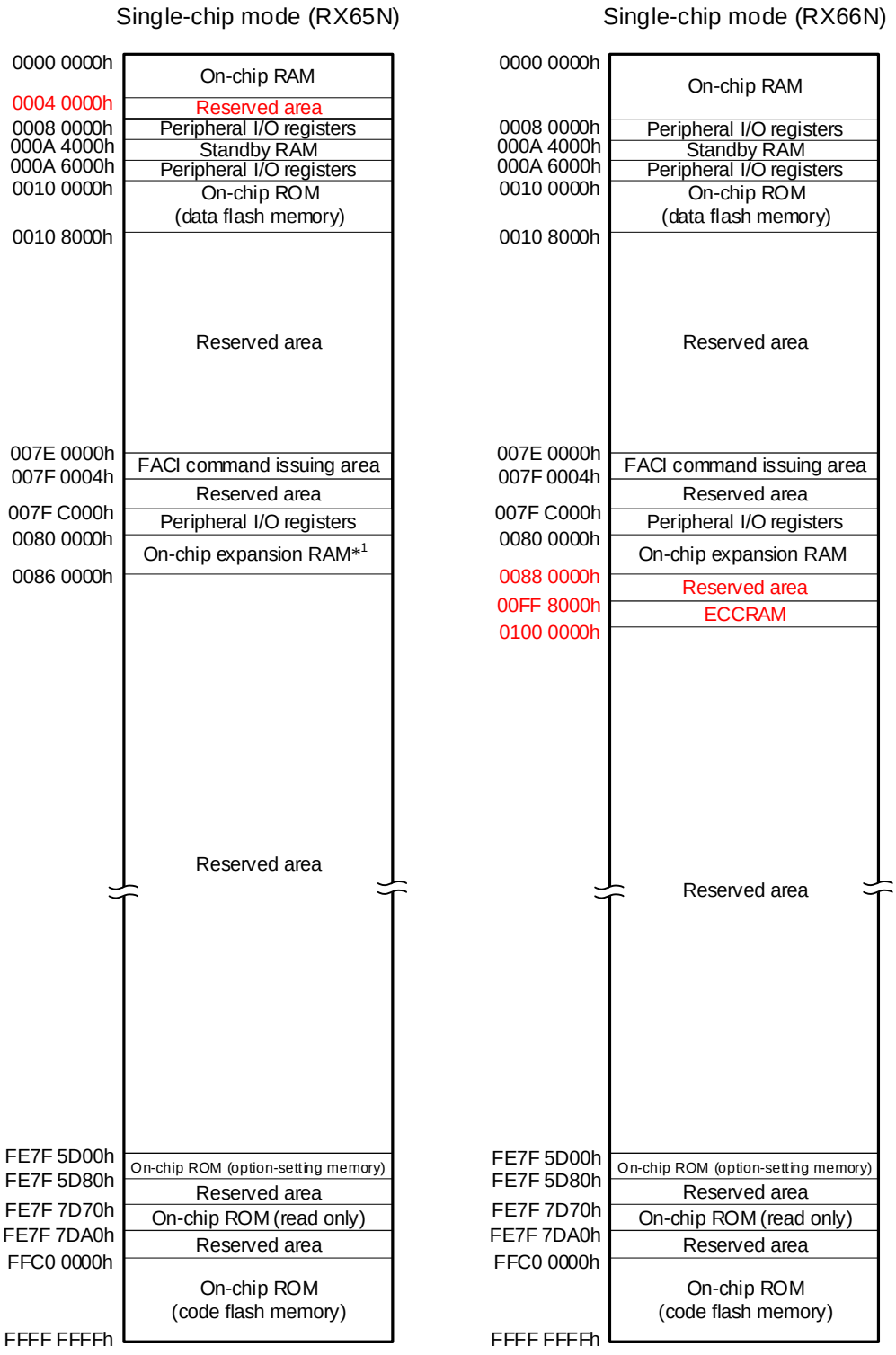
Table 2.3 is a comparison of operating mode registers.

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX65N	RX66N
SYSCR1	ECCRAME	—	ECCRAM enable bit

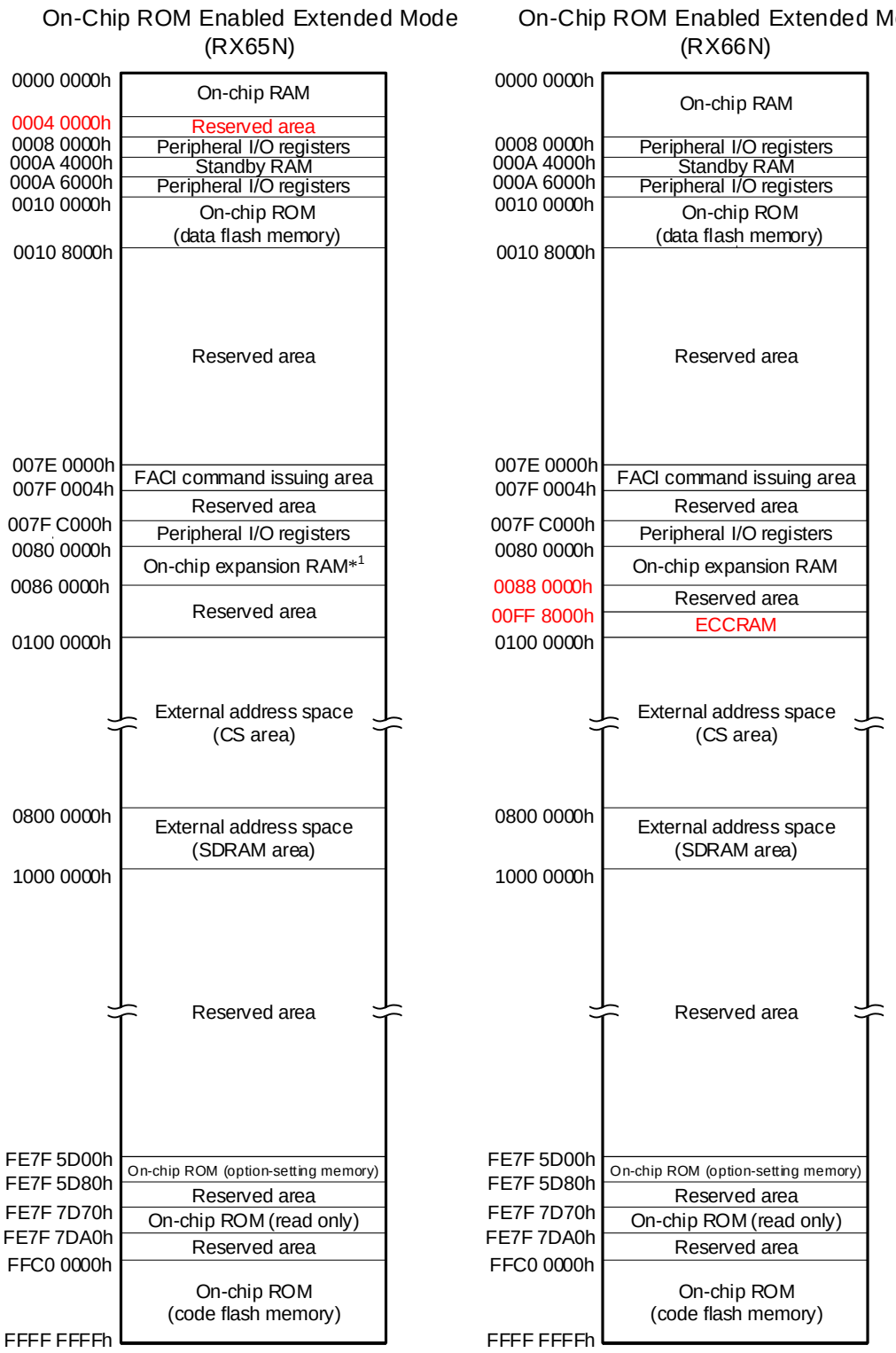
2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode, Figure 2.2 is a comparative memory map of on-chip ROM enabled extended mode, and Figure 2.3 is a comparative memory map of on-chip ROM disabled extended mode.



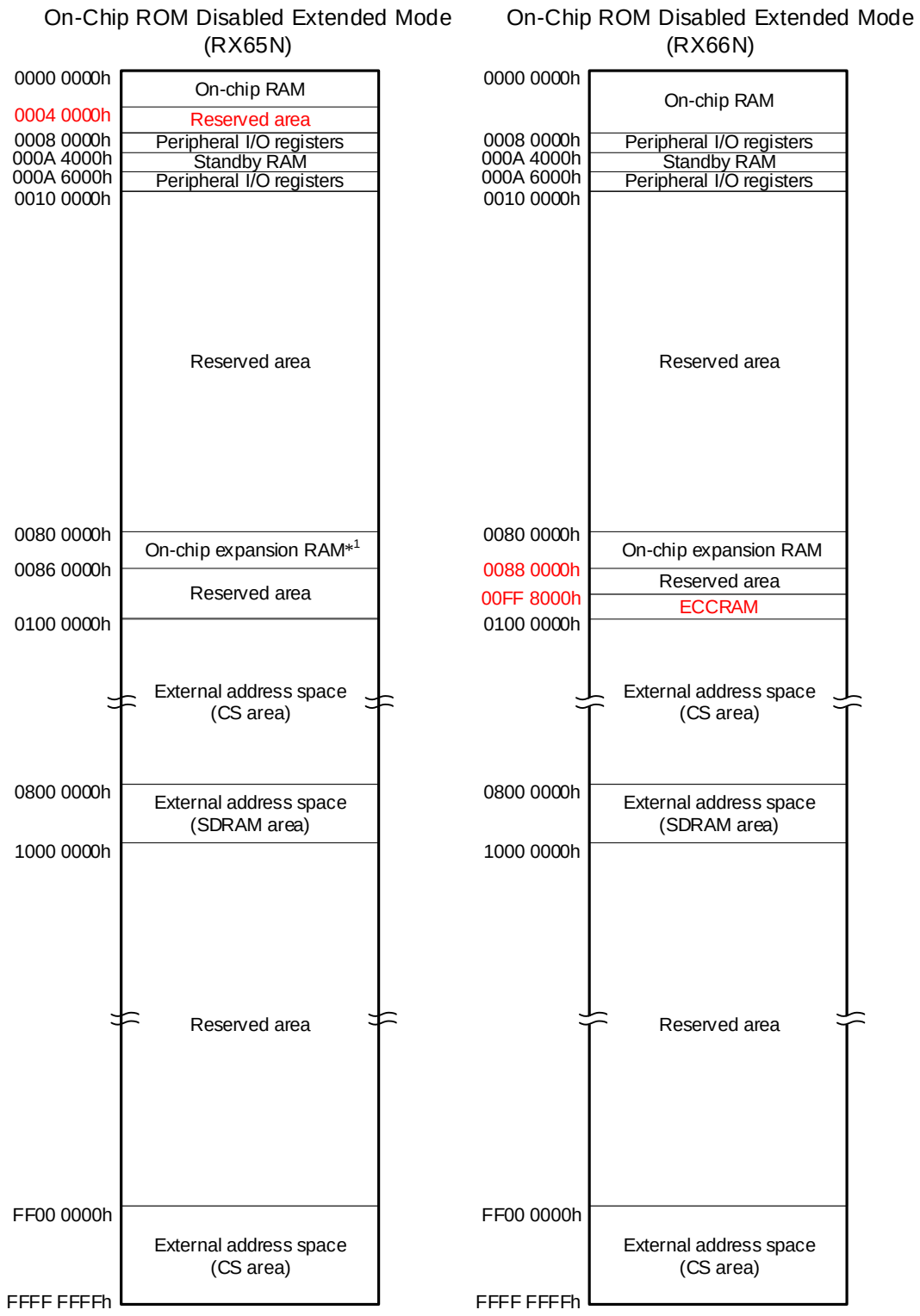
Note: 1. Products with 1.5 MB or more of flash memory (code flash) only.

Figure 2.1 Comparative Memory Map of Single-Chip Mode



Note: 1. Products with 1.5 MB or more of flash memory (code flash) only.

Figure 2.2 Comparative Memory Map of On-Chip ROM Enabled Extended Mode



Note: 1. Products with 1.5 MB or more of flash memory (code flash) only.

Figure 2.3 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

2.4 Option-Setting Memory

Table 2.4 is a comparison of option-setting memory registers.

Table 2.4 Comparison of Option-Setting Memory Registers

Register	Bit	RX65N (OFSM)	RX66N (OFSM)
TMEF	TMEFDB [2:0]	Dual-bank TM enable bits*1 b30 b28 0 0 0: The TM function is enabled for blocks 46 and 47 in the code flash memory. 1 1 1: The TM function is disabled for blocks 46 and 47 in the code flash memory.	Dual-bank TM enable bits b30 b28 0 0 0: The TM function is enabled for blocks 78 and 79 in the code flash memory. 1 1 1: The TM function is disabled for blocks 78 and 79 in the code flash memory.
BANKSEL*2	BANKSWP [2:0]	Startup bank switch bits b2 b0 0 0 0: The address range of bank 1 is specified as FFF0 0000h to FFFF FFFFh and of bank 0 as FFE0 0000h to FFEF FFFFh. 1 1 1: The address range of bank 1 is specified as FFE0 0000h to FFEF FFFFh and of bank 0 as FFF0 0000h to FFFF FFFFh.	Startup bank switch bits b2 b0 0 0 0: The address range of bank 1 is specified as FFE0 0000h to FFFF FFFFh and of bank 0 as FFC0 0000h to FFDF FFFFh. 1 1 1: The address range of bank 1 is specified as FFC0 0000h to FFDF FFFFh and of bank 0 as FFE0 0000h to FFFF FFFFh.

Notes: 1. These bits are reserved on products with 1 MB or less of code flash.
2. This is a reserved area on RX65N Group products with a code flash memory capacity of 1 MB or less. The BANKSEL register can only be used on products with a code flash memory capacity of 1.5 MB or more.

2.5 Clock Generation Circuit

Table 2.5 is a comparative overview of the clock generation circuits, and Table 2.6 is a comparison of clock generation circuit registers.

Table 2.5 Comparative Overview of Clock Generation Circuits

Item	RX65N	RX66N
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, AES*1, GLCDC*2, and DRW2D*2. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU, GLCDC, DRW2D, PMGI, and GPTW. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to the S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX65N	RX66N
Operating frequency	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory*2) — 60 MHz (max.) (for reading from the data flash memory)*2 • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 80 MHz (max.) • SDCLK pin output: 80 MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT25M pin output: 25 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU3 pin can be forcedly driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 30 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and the MTU and GPTW pins can be forcedly driven high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT

Item	RX65N	RX66N
PLL frequency synthesizer (PLL)	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
PLL frequency synthesizer for specific purposes (PPLL)	—	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2
Control of output on SDCLK pin	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Notes: 1. Implemented only on products with a code flash memory capacity of 1 MB or less.
2. Implemented only on products with a code flash memory capacity of 1.5 MB or more.

Table 2.6 Comparison of Clock Generation Circuit Registers

Register	Bit	RX65N	RX66N
SCKCR	BCK[3:0]	External bus clock (BCLK) select bits b19 b16 0 0 0 0: 1/1 0 0 0 1: 1/2 0 0 1 0: 1/4 0 0 1 1: 1/8 0 1 0 0: 1/16 0 1 0 1: 1/32 0 1 1 0: 1/64 Settings other than the above are prohibited.	External bus clock (BCLK) select bits b19 b16 0 0 0 0: 1/1 0 0 0 1: 1/2 0 0 1 0: 1/4 0 0 1 1: 1/8 0 1 0 0: 1/16 0 1 0 1: 1/32 0 1 1 0: 1/64 1 0 0 1: 1/3 Settings other than the above are prohibited.
ROMWT	—	ROM wait cycle setting register	—
OSCOVFSR	PPLOVF	—	PPLL clock oscillation stabilization flag
CKOCR	—	—	CLKOUT output control register
PACKCR	—	—	Specific-use clock control register
PPLLCR	—	—	PPLL control register
PPLLCR2	—	—	PPLL control register 2
PPLLCR3	—	—	PPLL control register 3

2.6 Clock Frequency Accuracy Measurement Circuit

Table 2.7 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.8 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.7 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX65N (CAC)	RX66N (CAC)
Measurement target clocks	• Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)	• Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)
Measurement reference clocks	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.8 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX65N (CAC)	RX66N (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M) Settings other than the above are prohibited.

2.7 Low Power Consumption

Table 2.9 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.10 is a comparison of low power consumption registers.

Table 2.9 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX66N
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PPLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM and expansion RAM: RX65N RAM, expansion RAM, and ECCRAM: RX66N	Operation possible (retained)	Operation possible (retained)
	Standby RAM	Operation possible (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USB 2.0 Host/Function module (USBb): RX65N, (USB): RX66N	Operation possible	Operation possible
	Watchdog timer (WDTA): RX65N, (WDT): RX66N	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Voltage detection circuit (LVDA): RX65N, (LVD): RX66N	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX66N
All-module clock stop mode	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PPLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM and expansion RAM: RX65N RAM, expansion RAM, and ECCRAM: RX66N	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb): RX65N, (USB): RX66N	Stopped	Stopped
	Watchdog timer (WDTA): RX65N, (WDT): RX66N	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible*1	Operation possible*1
	Voltage detection circuit (LVDA): RX65N, (LVD): RX66N	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	retained	retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	PPLL	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM and expansion RAM: RX65N RAM, expansion RAM, and ECCRAM: RX66N	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb): RX65N, (USB): RX66N	Stopped	Stopped
	Watchdog timer (WDTA): RX65N, (WDT): RX66N	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX66N
Software standby mode	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVDA): RX65N, (LVD): RX66N	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)
	PLL	Stopped	Stopped
	PPLL	—	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM and expansion RAM: RX65N RAM, expansion RAM, and ECCRAM: RX66N	Stopped (undefined)	Stopped (undefined)
	Standby RAM	Stopped (retained/undefined)	Stopped (retained/undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb): RX65N, (USB): RX66N	Stopped (retained/undefined)	Stopped (retained/undefined)
	Watchdog timer (WDTA): RX65N, (WDT): RX66N	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE)	Stopped (undefined)	Stopped (undefined)
	Voltage detection circuit (LVDA): RX65N, (LVD): RX66N	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

Table 2.10 Comparison of Low Power Consumption Registers

Register	Bit	RX65N	RX66N
MSTPCRA	MSTPA7	—	General PWM timer/GPTW dedicated port output enable module stop bit
MSTPCRB	MSTPB2	—	CAN module 2 module stop bit
	MSTPB15	Ethernet Controller and Ethernet controller DMA controller (channel 0) modules stop bit Target modules: ETHER and EDMAC (channel 0)	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 0) modules stop bit Target modules: ETHERC, EDMAC, and PMGI (channel 0)
MSTPCRC	MSTPC6	—	ECCRAM module stop bit
MSTPCRD	MSTPD13	SD slave interface module stop bit	—
	MSTPD14	—	Extended serial sound interface 1 module stop bit
	MSTPD15	—	Extended serial sound interface 0 module stop bit

2.8 Register Write Protection Function

Table 2.11 is a comparative overview of the register write protection functions.

Table 2.11 Comparative Overview of Register Write Protection Functions

Item	RX65N	RX66N
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PACKCR, PLLCR, PLLCR2, PPLLCR, PPLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, CKOCR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Exception Handling

Table 2.12 is a comparative overview of exception handling, Table 2.13 is a comparative listing of vector tables, and Table 2.14 is a comparative listing of return from exception handling routine instructions.

Table 2.12 Comparative Overview of Exception Handling

Item	RX65N	RX66N
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Address exception • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.13 Comparative Listing of Vector Tables

Item		RX65N	RX66N
Undefined instruction exception		Exception vector table (EXTB)	Exception vector table (EXTB)
Privileged instruction exception		Exception vector table (EXTB)	Exception vector table (EXTB)
Access exception		Exception vector table (EXTB)	Exception vector table (EXTB)
Address exception		—	Exception vector table (EXTB)
Floating-point exception (RX65N)/ single-precision floating-point exception (RX66N)		Exception vector table (EXTB)	Exception vector table (EXTB)
Reset		Exception vector table (EXTB)	Exception vector table (EXTB)
Non-maskable interrupt		Exception vector table (EXTB)	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Interrupt vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Interrupt vector table (INTB)	Interrupt vector table (INTB)

Table 2.14 Comparative Listing of Return from Exception Handling Routine Instructions

Item		RX65N	RX66N
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Address exception		—	RTE
Floating-point exception (RX65N)/ single-precision floating-point exception (RX66N)		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Prohibited	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controller

Table 2.15 is a comparative overview of the interrupt controllers, and Table 2.16 is a comparison of interrupt controller registers.

Table 2.15 Comparative Overview of Interrupt Controllers

Item		RX65N (ICUB)	RX66N (ICUD)
Interrupts	Peripheral function interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupts: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupts: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupts: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupts: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX65N (ICUB)	RX66N (ICUD)
Interrupts	External pin interrupts	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of sources: 2	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority	The priority level is set by writing to interrupt source priority register r (IPRr).	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt occurs at detection of main clock oscillation having stopped.	Interrupt occurs at detection of main clock oscillation having stopped.
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.

Item		RX65N (ICUB)	RX66N (ICUD)
Non-maskable interrupts	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in the RAM (including the expansion RAM).	Interrupt occurs when a parity check error is detected in the RAM (including the expansion RAM) or an ECC error is detected in the ECCRAM.
	Double-precision floating-point exceptions	—	Exceptions from double-precision floating-point coprocessor
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.16 Comparison of Interrupt Controller Registers

Register	Bit	RX65N (ICUB)	RX66N (ICUD)
NMISR	RAMST (RX65N) EXNMIST (RX66N)	RAM error interrupt status flag	Expanded non-maskable interrupt status flag
NMIER	RAMEN (RX65N) EXNMIEN (RX66N)	RAM error interrupt enable bit	Expanded non-maskable interrupt enable bit
EXNMISR	—	—	Expanded non-maskable interrupt status register
EXNMIER	—	—	Expanded non-maskable interrupt enable register
EXNMICLR	—	—	Expanded non-maskable interrupt status clear register
GRPIE0	—	—	Group IE0 interrupt request register
GENIE0	—	—	Group IE0 interrupt request enable register
GCRIE0	—	—	Group IE0 interrupt clear register
PIARk	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh)	Software configurable interrupt A request register k (k = 0h to Ah, Ch)

2.11 Buses

Table 2.17 is a comparative overview of the buses, and Table 2.18 is a comparison of bus registers.

Table 2.17 Comparative Overview of Buses

Item		RX65N	RX66N
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Connected to expansion RAM*1	Connected to expansion RAM and ECCRAM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC, DTC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, and extended bus master • Connected to on-chip memory (RAM, expansion RAM, ECCRAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1 and 3 to 5) • Operates in synchronization with the peripheral module clock (PCLKB)

Item		RX65N	RX66N
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES*2) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (EDMAC, ETHERC, PMGI, GPTW, MTU, SCIi, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	• Connected to peripheral modules (GLCDC and DRW2D)*1 • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (GLCDC and DRW2D) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash (in P/E) and data flash memory*1 • Operates in synchronization with the Flash-IF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the Flash-IF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

Notes: 1. Implemented only on products with a code flash memory capacity of 1.5 MB or more.
2. Implemented only on products with a code flash memory capacity of 1 MB or less.

Table 2.18 Comparison of Bus Registers

Register	Bit	RX65N	RX66N
BUSPRI	BPRA[1:0]	Memory bus 1 and 3 (RAM/expansion RAM) priority control bits	Memory bus 1 and 3 (RAM/expansion RAM/ECCRAM) priority control bits
EBMAPCR	RPSTOP	Rendering stop bit	—

2.12 Event Link Controller

Table 2.19 is a comparative overview of the event link controllers, Table 2.20 is a comparison of event link controller registers, Table 2.21 lists correspondences between ELSRn registers and peripheral modules, and Table 2.22 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.19 Comparative Overview of Event Link Controllers

Item	RX65N (ELC)	RX66N (ELC)
Event link function	• 82 event signals can be directly connected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be enabled on a single port corresponding to the specified bit. — Port group*1: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.	• 123 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be specified on a single port. — Port group*1: Event linkage operation can be specified by grouping multiple designated ports among up to eight ports.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Note: 1. An event is generated when the corresponding input signal on a single port or port group set to input changes.

Table 2.20 Comparison of Event Link Controller Registers

Register	Bit	RX65N (ELC)	RX66N (ELC)
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, and 45)	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45, and 48 to 57)
	ELS[7:0]	Event link select bits 00h: Event output to the corresponding peripheral module is disabled. 01h to BDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.

Table 2.21 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX65N (ELC)	RX66N (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR15	S12AD (ELCTRG0N)	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR33	CMTW0	CMTW0
ELSR35	TPU0	TPU0
ELSR36	TPU1	TPU1
ELSR37	TPU2	TPU2
ELSR38	TPU3	TPU3
ELSR45	S12AD1 (ELCTRG1N)	S12AD1 (ELCTRG10N)
ELSR48	—	GPTW event source A (common to all channels)
ELSR49	—	GPTW event source B (common to all channels)
ELSR50	—	GPTW event source C (common to all channels)
ELSR51	—	GPTW event source D (common to all channels)
ELSR52	—	GPTW event source E (common to all channels)
ELSR53	—	GPTW event source F (common to all channels)
ELSR54	—	GPTW event source G (common to all channels)
ELSR55	—	GPTW event source H (common to all channels)
ELSR56	—	S12AD (ELCTRG01N)
ELSR57	—	S12AD1 (ELCTRG11N)

Table 2.22 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX66N (ELC)
01h	Multifunction timer pulse unit 3	MTU0 compare match 0A	MTU0 compare match 0A
02h		MTU0 compare match 0B	MTU0 compare match 0B
03h		MTU0 compare match 0C	MTU0 compare match 0C
04h		MTU0 compare match 0D	MTU0 compare match 0D
05h		MTU0 compare match 0E	MTU0 compare match 0E
06h		MTU0 compare match 0F	MTU0 compare match 0F
07h		MTU0 overflow	MTU0 overflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
25h		TMR1 compare match A1	TMR1 compare match A1
26h		TMR1 compare match B1	TMR1 compare match B1
27h		TMR1 overflow	TMR1 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Bh		TMR3 compare match A3	TMR3 compare match A3
2Ch		TMR3 compare match B3	TMR3 compare match B3
2Dh		TMR3 overflow	TMR3 overflow
2Eh	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX66N (ELC)
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h		RSPI0 idle	RSPI0 idle
54h		RSPI0 receive data full	RSPI0 receive data full
55h		RSPI0 transmit data empty	RSPI0 transmit data empty
56h		RSPI0 transmit end	RSPI0 transmit end
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit
63h	I/O ports	Input edge detection of input port group 1	Input edge detection of input port group 1
64h		Input edge detection of input port group 2	Input edge detection of input port group 2
65h		Input edge detection of single input port 0	Input edge detection of single input port 0
66h		Input edge detection of single input port 1	Input edge detection of single input port 1
67h		Input edge detection of single input port 2	Input edge detection of single input port 2
68h		Input edge detection of single input port 3	Input edge detection of single input port 3
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met
6Ch	12-bit A/D converter	S12AD1 A/D conversion end	S12AD1 A/D conversion end
7Eh	Compare match timer W	CMTW channel 0 compare match	CMTW channel 0 compare match
80h	General PWM timer	—	GPTW0 compare match A
81h		—	GPTW0 compare match B
82h		—	GPTW0 compare match C
83h		—	GPTW0 compare match D
84h		—	GPTW0 compare match E
85h		—	GPTW0 compare match F
86h		—	GPTW0 overflow
87h		—	GPTW0 underflow
88h		—	GPTW1 compare match A
89h		—	GPTW1 compare match B
8Ah		—	GPTW1 compare match C
8Bh		—	GPTW1 compare match D

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX66N (ELC)
8Ch	General PWM timer	—	GPTW1 compare match E
8Dh		—	GPTW1 compare match F
8Eh		—	GPTW1 overflow
8Fh		—	GPTW1 underflow
90h		—	GPTW2 compare match A
91h		—	GPTW2 compare match B
92h		—	GPTW2 compare match C
93h		—	GPTW2 compare match D
94h		—	GPTW2 compare match E
95h		—	GPTW2 compare match F
96h		—	GPTW2 overflow
97h		—	GPTW2 underflow
98h		—	GPTW3 compare match A
99h		—	GPTW3 compare match B
9Ah		—	GPTW3 compare match C
9Bh		—	GPTW3 compare match D
9Ch		—	GPTW3 compare match E
9Dh		—	GPTW3 compare match F
9Eh		—	GPTW3 overflow
9Fh		—	GPTW3 underflow
ACh	16-bit timer pulse unit	TPU0 compare match A	TPU0 compare match A
ADh		TPU0 compare match B	TPU0 compare match B
AEh		TPU0 compare match C	TPU0 compare match C
AFh		TPU0 compare match D	TPU0 compare match D
B0h		TPU0 overflow	TPU0 overflow
B1h		TPU1 compare match A	TPU1 compare match A
B2h		TPU1 compare match B	TPU1 compare match B
B3h		TPU1 overflow	TPU1 overflow
B4h		TPU1 underflow	TPU1 underflow
B5h		TPU2 compare match A	TPU2 compare match A
B6h		TPU2 compare match B	TPU2 compare match B
B7h		TPU2 overflow	TPU2 overflow
B8h		TPU2 underflow	TPU2 underflow
B9h		TPU3 compare match A	TPU3 compare match A
BAh		TPU3 compare match B	TPU3 compare match B
BBh		TPU3 compare match C	TPU3 compare match C
BCh		TPU3 compare match D	TPU3 compare match D
BDh		TPU3 overflow	TPU3 overflow
C6h	General PWM timer	—	GPTW0 A/D converter start request A
C7h		—	GPTW0 A/D converter start request B
C8h		—	GPTW1 A/D converter start request A
C9h		—	GPTW1 A/D converter start request B
CAh		—	GPTW2 A/D converter start request A
CBh		—	GPTW2 A/D converter start request B

Value of ELS[7:0] Bits	Peripheral Module	RX65N (ELC)	RX66N (ELC)
CCh	General PWM timer	—	GPTW3 A/D converter start request A
CDh		—	GPTW3 A/D converter start request B
Settings other than the above are prohibited.			

2.13 I/O Ports

Table 2.23 is comparison of I/O port functions on RX65N products with a code flash memory capacity of 1 MB or less, Table 2.24 is comparison of I/O port functions on RX65N products with a code flash memory capacity of 1.5 MB or more, and Table 2.25 is a comparison of I/O port registers.

Table 2.23 Comparison of I/O Port Functions (Products with Code Flash Memory Capacity of 1 MB or Less (RX65N))

Item	Port Symbol	RX65N	RX66N
Input pull-up	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P12 to P17	P10 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P57
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P87
	PORT9	P90 to P93	P90 to P97
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5	PF0 to PF5
	PORTG	—	PG0 to PG7
	PORTH	—	PH0 to PH7
	PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5
	PORTK	—	PK0 to PK7
	PORTL	—	PL0 to PL7
	PORTM	—	PM0 to PM7
	PORTN	—	PN0 to PN5
	PORTQ	—	PQ0 to PQ7
Open-drain output	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P12 to P17	P10 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P57
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P87
	PORT9	P90 to P93	P90 to P97
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5	PF0 to PF5
	PORTG	—	PG0 to PG7
	PORTH	—	PH0 to PH7
	PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5

Item	Port Symbol	RX65N	RX66N
Open-drain output	PORTK	—	PK0 to PK7
	PORTL	—	PL0 to PL7
	PORTM	—	PM0 to PM7
	PORTN	—	PN0 to PN5
	PORTQ	—	PQ0 to PQ7
Driving ability switching	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P12 to P17	P10 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P57
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P83, P86, P87	P80 to P87
	PORT9	P90 to P93	P90 to P97
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5	PF0 to PF5
	PORTG	—	PG0 to PG7
	PORTH	—	PH0 to PH7
	PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5
	PORTK	—	PK0 to PK7
	PORTL	—	PL0 to PL7
	PORTM	—	PM0 to PM7
	PORTN	—	PN0 to PN5
	PORTQ	—	PQ0 to PQ7
5 V tolerant	PORT0	P07	P07
	PORT1	P12 to P17	P11 to P17
	PORT2	P20, P21	P20, P21
	PORT3	P30 to P33	P30 to P33
	PORT6	P67	P67
	PORTC	PC0 to PC3	PC0 to PC3

Table 2.24 Comparison of I/O Port Functions (Products with Code Flash Memory Capacity of 1.5 MB or More (RX65N))

Item	Port Symbol	RX65N	RX66N
Input pull-up	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P10 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P57
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P87
	PORT9	P90 to P97	P90 to P97
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF0 to PF5
	PORTG	PG0 to PG7	PG0 to PG7
	PORTH	—	PH0 to PH7
	PORTJ	PJ0 to PJ3, PJ5	PJ0 to PJ3, PJ5
	PORTK	—	PK0 to PK7
	PORTL	—	PL0 to PL7
	PORTM	—	PM0 to PM7
	PORTN	—	PN0 to PN5
	PORTQ	—	PQ0 to PQ7
Open-drain output	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P10 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P57
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P87
	PORT9	P90 to P97	P90 to P97
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF0 to PF5
	PORTG	PG0 to PG7	PG0 to PG7
	PORTH	—	PH0 to PH7
	PORTJ	PJ0 to PJ3, PJ5	PJ0 to PJ3, PJ5
	PORTK	—	PK0 to PK7
	PORTL	—	PL0 to PL7
	PORTM	—	PM0 to PM7
	PORTN	—	PN0 to PN5
	PORTQ	—	PQ0 to PQ7

Item	Port Symbol	RX65N	RX66N
Driving ability switching	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P10 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P57
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P87
	PORT9	P90 to P97	P90 to P97
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF0 to PF5
	PORTG	PG0 to PG7	PG0 to PG7
	PORTH	—	PH0 to PH7
	PORTJ	PJ0 to PJ3, PJ5	PJ0 to PJ3, PJ5
	PORTK	—	PK0 to PK7
	PORTL	—	PL0 to PL7
	PORTM	—	PM0 to PM7
	PORTN	—	PN0 to PN5
	PORTQ	—	PQ0 to PQ7
5 V tolerant	PORT0	P07	P07
	PORT1	P11 to P17	P11 to P17
	PORT2	P20, P21	P20, P21
	PORT3	P30 to P33	P30 to P33
	PORT6	P67	P67
	PORTC	PC0 to PC3	PC0 to PC3

Table 2.25 Comparison of I/O Port Registers

Register	Bit	RX65N	RX66N
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, J to N, Q)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to H, J to N, Q)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 bits (m = 0 to 9, A to H, J to N, Q)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to H, J to N, Q)
ODR0	B0	Pm0 output type select bit (m = 0 to 9, A to G, J)	Pm0 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B2	Pm1 output type select bit (m = 0 to 9, A to G, J)	Pm1 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B3	PE1 output type select bit (m = 0 to 9, A to G, J)	PE1 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B4	Pm2 output type select bit (m = 0 to 9, A to G, J)	Pm2 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B6	Pm3 output type select bit (m = 0 to 9, A to G, J)	Pm3 output type select bit (m = 0 to 9, A to H, J to N, Q)
ODR1	B0	Pm4 output type select bit (m = 0 to 9, A to G, J)	Pm4 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B2	Pm5 output type select bit (m = 0 to 9, A to G, J)	Pm5 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B4	Pm6 output type select bit (m = 0 to 9, A to G, J)	Pm6 output type select bit (m = 0 to 9, A to H, J to N, Q)
	B6	Pm7 output type select bit (m = 0 to 9, A to G, J)	Pm7 output type select bit (m = 0 to 9, A to H, J to N, Q)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to H, J to N, Q)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, G, J)	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, G, H, J to N, Q)
DSCR2	B0 to B7	Pm0 to Pm7 drive capacity control bits 2 (m = 0 to 3, 5, 7 to 9, A to E, G, J)	Pm0 to Pm7 drive capacity control bits 2 (m = 0 to 3, 5, 7 to 9, A to E, G, H, J to N, Q)

2.14 Multi-Function Pin Controller

Table 2.26 is a comparison of the assignments of multiplexed pins, and Table 2.27 to Table 2.47 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX66N Group only and **orange text** pins that exist on the RX65N Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.26 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
EXDMA controller	EDREQ0 (input)	P22	○	○	○	○	○	○
		P55	○	○	○	○	○	○
		P80	○	○	×	○	○	×
	EDACK0 (output)	P23	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		P81	○	○	×	○	○	×
	EDREQ1 (input)	P24	○	○	○	○	○	○
		P33	○	○	○	○	○	○
		P82	○	○	×	○	○	×
	EDACK1 (output)	P25	○	○	○	○	○	○
		P56	○	○	×	○	○	×
		P83	○	○	×	○	○	×
		PJ3	○	○	○	○	○	○
Interrupt	IRQ0-DS (input)	P30	○	○	○	○	○	○
	IRQ0 (input)	P10	○	×	×	○	×	×
		PD0	○	○	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○
	IRQ1 (input)	P11	○	×	×	○	×	×
		PD1	○	○	○	○	○	○
	IRQ2-DS (input)	P32	○	○	○	○	○	○
	IRQ2 (input)	P12	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
	IRQ3-DS (input)	P33	○	○	○	○	○	○
	IRQ3 (input)	P13	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
	IRQ4-DS (input)	PB1	○	○	○	○	○	○
	IRQ4 (input)	P14	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
		PF5	○	○	×	○	○	×
	IRQ5-DS (input)	PA4	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	IRQ6-DS (input)	PA3	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Interrupt	IRQ6 (input)	P16	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
	IRQ7-DS (input)	PE2	○	○	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
	IRQ8-DS (input)	P40	○	○	○	○	○	○
	IRQ8 (input)	P00	○	○	×	○	○	×
		P20	○	○	○	○	○	○
	IRQ9-DS (input)	P41	○	○	○	○	○	○
	IRQ9 (input)	P01	○	○	×	○	○	×
		P21	○	○	○	○	○	○
	IRQ10-DS (input)	P42	○	○	○	○	○	○
	IRQ10 (input)	P02	○	○	×	○	○	×
		P55	○	○	○	○	○	○
	IRQ11-DS (input)	P43	○	○	○	○	○	○
	IRQ11 (input)	P03	○	○	×	○	○	×
		PA1	○	○	○	○	○	○
	IRQ12-DS (input)	P44	○	○	○	○	○	○
	IRQ12 (input)	PB0	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
	IRQ13-DS (input)	P45	○	○	○	○	○	○
	IRQ13 (input)	P05	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	IRQ14-DS (input)	P46	○	○	○	○	○	○
	IRQ14 (input)	PC0	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	IRQ15-DS (input)	P47	○	○	○	○	○	○
	IRQ15 (input)	P07	○	○	○	○	○	○
		P67	○	○	×	○	○	×
Multi-function timer pulse unit 3	MTIOC0A (input/output)	P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	MTIOC0B (input/output)	P13	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	MTIOC0D (input/output)	P33	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Multi-function timer pulse unit 3	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	○	○	○	○	○
		P80	○	○	×	○	○	×
		PB7	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		P56	○	○	×	○	○	×
		PC0	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	○	○	○	○	○
		P81	○	○	×	○	○	×
		PB6	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
	MTIOC4A (input/output)	P21	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		P82	○	○	×	○	○	×
		PA0	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	MTIOC4B (input/output)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	MTIOC4C (input/output)	P25	○	○	○	○	○	○
		P83	○	○	×	○	○	×
		P87	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	○	○	○	○
		P86	○	○	×	○	○	×
		PC3	○	○	○	○	○	○
		PD2	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	MTIC5U (input)	P12	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PD7	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Multi-function timer pulse unit 3	MTIC5V (input)	P11	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PD6	○	○	○	○	○	○
	MTIC5W (input)	P10	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	MTIOC6A (input/output)	PE7	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	MTIOC6B (input/output)	PA5	○	○	○	○	○	○
		PJ0	○	×	×	○	×	×
	MTIOC6C (input/output)	PE6	○	○	○	○	○	○
		P85	○	×	×	○	×	×
	MTIOC6D (input/output)	PA0	○	○	○	○	○	○
		P84	○	×	×	○	×	×
	MTIOC7A (input/output)	PA2	○	○	○	○	○	○
	MTIOC7B (input/output)	PA1	○	○	○	○	○	○
	MTIOC7C (input/output)	P67	○	○	×	○	○	×
	MTIOC7D (input/output)	P66	○	○	×	○	○	×
	MTIOC8A (input/output)	PD6	○	○	○	○	○	○
	MTIOC8B (input/output)	PD4	○	○	○	○	○	○
	MTIOC8C (input/output)	PD5	○	○	○	○	○	○
	MTIOC8D (input/output)	PD3	○	○	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
		PD5	×	×	×	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		P25	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 3	POE0# (input)	P32	○	○	○	○	○	○
		P93	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
		PD7	○	○	○	○	○	○
	POE4# (input)	P33	○	○	○	○	○	○
		P92	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
		PD0	○	○	○	○	○	○
		PD6	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Port output enable 3	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
		PJ5	○	○	×	○	○	×
	POE10# (input)	P32	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PD5	○	○	○	○	○	○
	POE11# (input)	P33	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PD4	○	○	○	○	○	○
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	○	×	○	○	×
		PA0	○	○	○	○	○	○
	TIOCB0 (input/output)	P17	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	TIOCC0 (input/output)	P32	○	○	○	○	○	○
		P85	○	×	×	○	×	×
	TIOCD0 (input/output)	P33	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
	TIOCA1 (input/output)	P56	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
	TIOCB1 (input/output)	P16	○	○	○	○	○	○
		PA5	○	○	○	○	○	○
	TIOCA2 (input/output)	P87	○	○	×	○	○	×
		PA6	○	○	○	○	○	○
	TIOCB2 (input/output)	P15	○	○	○	○	○	○
		PA7	○	○	○	○	○	○
	TIOCA3 (input/output)	P21	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
	TIOCB3 (input/output)	P20	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	TIOCC3 (input/output)	P22	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
	TIOCD3 (input/output)	P23	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	TIOCA4 (input/output)	P25	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	TIOCB4 (input/output)	P24	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	TIOCA5 (input/output)	P13	○	○	○	○	○	○
		PB6	○	○	○	○	○	○
	TIOCB5 (input/output)	P14	○	○	○	○	○	○
		PB7	○	○	○	○	○	○
	TCLKA (input)	P14	○	○	○	○	○	○
		PC2	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
16-bit timer pulse unit	TCLKB (input)	P15	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
	TCLKC (input)	P16	○	○	○	○	○	○
		PB2	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	TCLKD (input)	P17	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
Programmable pulse generator	PO0 (output)	P20	○	○	○	○	○	○
	PO1 (output)	P21	○	○	○	○	○	○
	PO2 (output)	P22	○	○	○	○	○	○
	PO3 (output)	P23	○	○	○	○	○	○
	PO4 (output)	P24	○	○	○	○	○	○
	PO5 (output)	P25	○	○	○	○	○	○
	PO6 (output)	P26	○	○	○	○	○	○
	PO7 (output)	P27	○	○	○	○	○	○
	PO8 (output)	P30	○	○	○	○	○	○
	PO9 (output)	P31	○	○	○	○	○	○
	PO10 (output)	P32	○	○	○	○	○	○
	PO11 (output)	P33	○	○	○	○	○	○
	PO12 (output)	P34	○	○	○	○	○	○
	PO13 (output)	P13	○	○	○	○	○	○
		P15	○	○	○	○	○	○
	PO14 (output)	P16	○	○	○	○	○	○
	PO15 (output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
	PO16 (output)	P73	○	○	×	○	○	×
		PA0	○	○	○	○	○	○
	PO17 (output)	PA1	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	PO18 (output)	PA2	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	PO19 (output)	P74	○	○	×	○	○	×
		PA3	○	○	○	○	○	○
	PO20 (output)	P75	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
	PO21 (output)	PA5	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	PO22 (output)	P76	○	○	×	○	○	×
		PA6	○	○	○	○	○	○
	PO23 (output)	P77	○	○	×	○	○	×
		PA7	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	PO24 (output)	PB0	○	○	○	○	○	○
		PC3	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Programmable pulse generator	PO25 (output)	PB1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	PO26 (output)	P80	○	○	×	○	○	×
		PB2	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	PO27 (output)	P81	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
	PO28 (output)	P82	○	○	×	○	○	×
		PB4	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	PO29 (output)	PB5	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	PO30 (output)	PB6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	PO31 (output)	PB7	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
8-bit timer	TMO0 (output)	P22	○	○	○	○	○	○
		PB3	○	○	○	○	○	○
	TMCI0 (input)	P01	○	○	×	○	○	×
		P21	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	TMRI0 (input)	P00	○	○	×	○	○	×
		P20	○	○	○	○	○	○
		PA4	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P02	○	○	×	○	○	×
		P12	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	○	○	○	○
		P32	○	○	○	○	○	○
		P55	○	○	○	○	○	○
	TMCI3 (input)	P11	○	×	×	○	×	×
		P27	○	○	○	○	○	○
		P34	○	○	○	○	○	○
		PA6	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
8-bit timer	TMRI3 (input)	P10	○	×	×	○	×	×
		P30	○	○	○	○	○	○
		P33	○	○	○	○	○	○
Compare match timer W	TOC0 (output)	PC7	○	○	○	○	○	○
	TIC0 (input)	PC6	○	○	○	○	○	○
	TOC1 (output)	PE7	○	○	○	○	○	○
	TIC1 (input)	PE6	○	○	○	○	○	○
	TOC2 (output)	PD3	○	○	○	○	○	○
	TIC2 (input)	PD2	○	○	○	○	○	○
	TOC3 (output)	PE3	○	○	○	○	○	○
	TIC3 (input)	PE2	○	○	○	○	○	○
Ethernet controller	REF50CK0 (input)	P76	○	○	×	○	○	×
		PB2	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	RMII0_CRS_DV (input)	P83	○	○	×	○	○	×
		PB7	○	○	○	○	○	○
	RMII0_TXD0 (output)	P81	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	RMII0_TXD1 (output)	P82	○	○	×	○	○	×
		PB6	○	○	○	○	○	○
	RMII0_RXD0 (input)	P75	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
	RMII0_RXD1 (input)	P74	○	○	×	○	○	×
		PB0	○	○	○	○	○	○
	RMII0_TXD_EN (output)	P80	○	○	×	○	○	×
		PA0	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	RMII0_RX_ER (input)	P77	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
	ET0_CRS (input)	P83	○	○	×	○	○	×
		PB7	○	○	○	○	○	○
	ET0_RX_DV (input)	PC2	○	○	○	○	○	○
	ET0_EXOUT (output)	P55	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	ET0_LINKSTA (input)	P34	○	○	○	○	○	○
		P54	○	○	○	○	○	○
		PA5	○	○	○	○	○	○
	ET0_ETXD0 (output)	P81	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	ET0_ETXD1 (output)	P82	○	○	×	○	○	×
		PB6	○	○	○	○	○	○
	ET0_ETXD2 (output)	PC5	○	○	○	○	○	○
	ET0_ETXD3 (output)	PC6	○	○	○	○	○	○
	ET0_ERXD0 (input)	P75	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
	ET0_ERXD1 (input)	P74	○	○	×	○	○	×
		PB0	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Ethernet controller	ET0_ERXD2 (input)	PC1	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	ET0_ERXD3 (input)	PC0	○	○	○	○	○	○
		PE3	○	○	○	○	○	○
	ET0_TX_EN (output)	P80	○	○	×	○	○	×
		PA0	○	○	○	○	○	○
		PB4	○	○	○	○	○	○
	ET0_TX_ER (output)	PC3	○	○	○	○	○	○
	ET0_RX_ER (input)	P77	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
	ET0_TX_CLK (input)	PC4	○	○	○	○	○	○
	ET0_RX_CLK (input)	P76	○	○	×	○	○	×
		PB2	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	ET0_COL (input)	PC7	○	○	○	○	○	○
	ET0_WOL (output)	P73	○	○	×	○	○	×
		PA1	○	○	○	○	○	○
		PA7	○	○	○	○	○	○
	ET0_MDC (output)	P72	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
	ET0_MDIO (input/output)	P71	○	○	×	○	○	×
		PA3	○	○	○	○	○	○
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	○	○	○	○
		P33	○	○	○	○	○	○
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	SCK0 (input/output)	P22	○	○	○	○	○	○
		P34	○	○	○	○	○	○
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PF2	○	×	×	○	×	×
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
		PF0	○	×	×	○	×	×
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
		PF1	○	×	×	○	×	×
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	○	○	○	○	○
		P52	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Serial communications interface	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	○	○	○	○	○	○
		P50	○	○	○	○	○	○
	SCK2 (input/output)	P11	○	×	×	○	×	×
		P51	○	○	○	○	○	○
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	○	○	○	○	○
		PJ5	○	○	×	○	○	×
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	○	○	○	○
		P25	○	○	○	○	○	○
	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	○	○	○	○	○	○
		P23	○	○	○	○	○	○
	SCK3 (input/output)	P15	○	○	○	○	○	○
		P24	○	○	○	○	○	○
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	○	○	○	○
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	○	×	○	○	×
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	○	○	×	○	○	×
	SCK4 (input/output)	PB3	○	○	×	○	○	×
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	○	×	○	○	×
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	○	○	○	○
		PA3	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	○	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	○	○	×	○	○	×
		P33	○	○	○	○	○	○
		PB0	○	○	○	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P00	○	○	×	○	○	×
		P32	○	○	○	○	○	○
		PB1	○	○	○	○	○	○
	SCK6 (input/output)	P02	○	○	×	○	○	×
		P34	○	○	○	○	○	○
		PB3	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Serial communications interface	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	○	○	○	○
		PJ3	○	○	○	○	○	○
	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P57	○	×	×	○	×	×
		P92	○	○	×	○	○	×
	TXD7 (output)/ SMOSI7 (input/output)/ SSDA7 (input/output)	P55	○	○*2	×	○	○	×
		P90	○	○	×	○	○	×
	SCK7 (input/output)	P56	○	○*2	×	○	○	×
		P91	○	○	×	○	○	×
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	○	○	×	○	○	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○	○	○
		PJ2	○	×	×	○	×	×
	RTS8# (output)/ SCK8 (input/output)	PC5	○	○	○	○	○	○
	SCK8 (input/output)	PJ0	○	×	×	○	×	×
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	○	○	○
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	○	○	○	○
	RTS9# (output)/ SCK9 (input/output)	PB5	○	○	○	○	○	○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	○	○	○	○	○
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	○	○	×	○	○	×
		P86	○	○	×	○	○	×
		PC6	○	○	○	○	○	○
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	P82	○	○	×	○	○	×
		P87	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
	SCK10 (input/output)	PC5	○	○	○	○	○	○
	RTS10# (output)/ SCK10 (input/output)	P80	○	○	×	○	○	×
	CTS10# (input)/ SCK10 (input/output)/ SS10# (input)	P83	○	○	×	○	○	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Serial communications interface	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	○	○	○	○	○	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	○	○	×	○	○	×
		PB6	○	○	○	○	○	○
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	P77	○	○	×	○	○	×
		PB7	○	○	○	○	○	○
	SCK11 (input/output)	PB5	○	○	○	○	○	○
	RTS11# (output)/ SCK11 (input/output)	P75	○	○	×	○	○	×
	CTS11# (input)/ SS11# (input)	P74	○	○	×	○	○	×
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4	○	○	○	○	○	○
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○	○	○	○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○	○	○
	SCK12 (input/output)	PE0	○	○	○	○	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○	○	○
I^2C bus interface	SCL0[FM+] (input/output)	P12	○	○	○	○	○	○
	SDA0[FM+] (input/output)	P13	○	○	○	○	○	○
	SCL1 (input/output)*2	P21	○	○	○	○	○	○
	SDA1 (input/output)*2	P20	○	○	○	○	○	○
	SCL2-DS (input/output)	P16	○	○	○	○	○	○
	SDA2-DS (input/output)	P17	○	○	○	○	○	○
USB 2.0 FS Host/Function module	USB0_VBUS (input)	P16	○	○	○	○	○	○
	USB0_EXICEN (output)	P21	○	○	○	○	○	○
	USB0_VBUSEN (output)	P16	○	○	○	○	○	○
		P24	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	USB0_OVRCURA (input)/ USB0_OVRCURA-DS (input)	P14	○	○	○	○	○	○
	USB0_OVRCURB (input)	P16	○	○	○	○	○	○
		P22	○	○	○	○	○	○
	USB0_ID (input)	P20	○	○	○	○	○	○
CAN module	CRX0 (input)	P33	○	○	○	○	○	○
		PD2	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
CAN module	CTX0 (output)	P32	○	○	○	○	○	○
		PD1	○	○	○	○	○	○
	CRX1-DS (input)	P15	○	○	○	○	○	○
	CRX1 (input)	P55	○	○	○	○	○	○
	CTX1 (output)	P14	○	○	○	○	○	○
		P23	×	×	×	○	○	○
		P54	○	○	○	○	○	○
	CRX2 (input)	P67				○	○	×
	CTX2 (output)	P66				○	○	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	PA7	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	○	○	○
		PC0	○	○	○	○	○	○
	SSLA2 (output)	PA1	○	○	○	○	○	○
		PC1	○	○	○	○	○	○
	SSLA3 (output)	PA2	○	○	○	○	○	○
		PC2	○	○	○	○	○	○
	RSPCKB (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	○	○	○	○
	MOSIB (input/output)	P26	○	○	○	○	○	○
		PE6	○	○	○	○	○	○
	MISOB (input/output)	P30	○	○	○	○	○	○
		PE7	○	○	○	○	○	○
	SSLB0 (input/output)	P31	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
	SSLB1 (output)	P50	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
	SSLB2 (output)	P51	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
	SSLB3 (output)	P52	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	RSPCKC (input/output)	P56	○	×	×	○	×	×
		PD3	○	○	○	○	○	○
	MOSIC (input/output)	P54	○	×	×	○	×	×
		PD1	○	○	○	○	○	○
	MISOC (input/output)	P55	○	×	×	○	×	×
		PD2	○	○	○	○	○	○
	SSLC0 (input/output)	P57	○	×	×	○	×	×
		PD4	○	○	○	○	○	○
	SSLC1 (output)	PD5	○	○	○	○	○	○
		PJ0	○	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Serial peripheral interface	SSLC2 (output)	PD6	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	SSLC3 (output)	PD7	○	○	○	○	○	○
		PJ2	○	×	×	○	×	×
Realtime clock	RTCOUT (output)	P16	○	○	○	○	○	○
		P32	○	○	○	○	○	○
	RTCIC0 (input)*1	P30	○	○	○	○	○	○
	RTCIC1 (input)*1	P31	○	○	○	○	○	○
	RTCIC2 (input)*1	P32	○	○	○	○	○	○
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	○	○	○
	AN004 (input)*1	P44	○	○	○	○	○	○
	AN005 (input)*1	P45	○	○	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	○	○	○	○
	ADTRG0# (input)	P07	○	○	○	○	○	○
		P16	○	○	○	○	○	○
		P25	○	○	○	○	○	○
	AN100 (input)*1	PE2	○	○	○	○	○	○
	AN101 (input)*1	PE3	○	○	○	○	○	○
	AN102 (input)*1	PE4	○	○	○	○	○	○
	AN103 (input)*1	PE5	○	○	○	○	○	○
	AN104 (input)*1	PE6	○	○	○	○	○	○
	AN105 (input)*1	PE7	○	○	○	○	○	○
	AN106 (input)*1	PD6	○	○	○	○	○	○
	AN107 (input)*1	PD7	○	○	○	○	○	○
	AN108 (input)*1	PD0	○	○	○	○	○	○
	AN109 (input)*1	PD1	○	○	○	○	○	○
	AN110 (input)*1	PD2	○	○	○	○	○	○
	AN111 (input)*1	PD3	○	○	○	○	○	○
	AN112 (input)*1	PD4	○	○	○	○	○	○
	AN113 (input)*1	PD5	○	○	○	○	○	○
	AN114 (input)*1	P90	○	○	×	○	○	×
	AN115 (input)*1	P91	○	○	×	○	○	×
	AN116 (input)*1	P92	○	○	×	○	○	×
	AN117 (input)*1	P93	○	○	×	○	○	×
	AN118 (input)*1	P00	○	○	×	○	○	×
	AN119 (input)*1	P01	○	○	×	○	○	×
	AN120 (input)*1	P02	○	○	×	○	○	×
	ANEX0 (output)*1	PE0	○	○	○	○	○	○
	ANEX1 (input)*1	PE1	○	○	○	○	○	○
	ADTRG1# (input)	P13	○	○	○	○	○	○
		P17	○	○	○	○	○	○
12-bit D/A converter	DA0 (output)*1	P03	○	○	×	○	○	×
	DA1 (output)*1	P05	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Parallel data capture unit	PIXCLK (input)	P24	○	○	×	○	○	×
	VSYNC (input)	P32	○	○	×	○	○	×
	HSYNC (input)	P25	○	○	×	○	○	×
	PIXD0 (input)	P15	○	○	×	○	○	×
	PIXD1 (input)	P86	○	○	×	○	○	×
	PIXD2 (input)	P87	○	○	×	○	○	×
	PIXD3 (input)	P17	○	○	×	○	○	×
	PIXD4 (input)	P20	○	○	×	○	○	×
	PIXD5 (input)	P21	○	○	×	○	○	×
	PIXD6 (input)	P22	○	○	×	○	○	×
	PIXD7 (input)	P23	○	○	×	○	○	×
	PCKO (output)	P33	○	○	×	○	○	×
MultiMediaCard interface	MMC_RES# (output)	P75	○	○	×	○	○	×
		PE7	○	○	○	○	○	○
	MMC_CLK (output)	P77	○	○	×	○	○	×
		PD5	○	○	○	○	○	○
	MMC_CD (input)	PC2	○	○	×	○	○	×
		PE6	○	○	○	○	○	○
	MMC_CMD (input/output)	P76	○	○	×	○	○	×
		PD4	○	○	○	○	○	○
	MMC_D0 (input/output)	PC3	○	○	×	○	○	×
		PD6	○	○	○	○	○	○
	MMC_D1 (input/output)	PC4	○	○	×	○	○	×
		PD7	○	○	○	○	○	○
	MMC_D2 (input/output)	P80	○	○	×	○	○	×
		PD2	○	○	○	○	○	○
	MMC_D3 (input/output)	P81	○	○	×	○	○	×
		PD3	○	○	○	○	○	○
	MMC_D4 (input/output)	P82	○	○	×	○	○	×
		PE0	○	○	○	○	○	○
	MMC_D5 (input/output)	PC5	○	○	×	○	○	×
		PE1	○	○	○	○	○	○
	MMC_D6 (input/output)	PC6	○	○	×	○	○	×
		PE2	○	○	○	○	○	○
	MMC_D7 (input/output)	PC7	○	○	×	○	○	×
		PE3	○	○	○	○	○	○
SD host interface	SDHI_CLK (output)	P21	○	○*2	×	○	○	×
		P77	○	○	×	○	○	×
		PD5	○	○	○	○	○	○
	SDHI_CMD (input/output)	P20	○	○*2	×	○	○	×
		P76	○	○	×	○	○	×
		PD4	○	○	○	○	○	○
	SDHI_CD (input)	P25	○	○*2	×	○	○	×
		P81	○	○	×	○	○	×
		PE6	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
SD host interface	SDHI_WP (input)	P24	○	○*2	×	○	○	×
		P80	○	○	×	○	○	×
		PE7	○	○	○	○	○	○
	SDHI_D0 (input/output)	P22	○	○*2	×	○	○	×
		PC3	○	○	×	○	○	×
		PD6	○	○	○	○	○	○
	SDHI_D1 (input/output)	P23	○	○*2	×	○	○	×
		PC4	○	○	×	○	○	×
		PD7	○	○	○	○	○	○
	SDHI_D2 (input/output)	P75	○	○	×	○	○	×
		P87	○	○*2	×	○	○	×
		PD2	○	○	○	○	○	○
	SDHI_D3 (input/output)	P17	○	○*2	×	○	○	×
		PC2	○	○	×	○	○	×
		PD3	○	○	○	○	○	○
SD slave interface	SDSI_CLK (input)	P77	○	○	×			
		PB5	○	○	○			
	SDSI_CMD (input/output)	P76	○	○	×			
		PB4	○	○	○			
	SDSI_D0 (input/output)	PC3	○	○	×			
		PB6	○	○	○			
	SDSI_D1 (input/output)	PC4	○	○	×			
		PB7	○	○	○			
	SDSI_D2 (input/output)	P75	○	○	×			
		PB2	○	○	○			
	SDSI_D3 (input/output)	PC2	○	○	×			
		PB3	○	○	○			
Clock frequency measurement circuit	CACREF (input)	PC7	○	○	○	○	○	○
		PA0	○	○	○	○	○	○
Quad serial peripheral interface	QSPCLK (output)	P77	○	○	×	○	○	×
		PD5	○	○	○	○	○	○
	QSSL (output)	P76	○	○	×	○	○	×
		PD4	○	○	○	○	○	○
	QMO/QIO0 (input/output)	PC3	○	○	×	○	○	×
		PD6	○	○	○	○	○	○
	QMI/QIO1 (input/output)	PC4	○	○	×	○	○	×
		PD7	○	○	○	○	○	○
	QIO2 (input/output)	P80	○	○	×	○	○	×
		PD2	○	○	○	○	○	○
	QIO3 (input/output)	P81	○	○	×	○	○	×
		PD3	○	○	○	○	○	○
Graphic LCD controller*2	LCD_EXTCLK (input)	P73	○	×	×	○	×	×
		PD0	○	○	○	○	○	○
	LCD_CLK (output)	P14	○	×	×	○	×	×
		PB5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Graphic LCD controller*2	LCD_TCON0 (output)	P13	○	×	×	○	×	×
		PB4	○	○	○	○	○	○
	LCD_TCON1 (output)	P12	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
	LCD_TCON2 (output)	PB2	○	○	○	○	○	○
		PJ2	○	×	×	○	×	×
	LCD_TCON3 (output)	PB1	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	LCD_DATA0 (output)	PB0	○	○	○	○	○	○
		PJ0	○	×	×	○	×	×
	LCD_DATA1 (output)	P85	○	×	×	○	×	×
		PA7	○	○	○	○	○	○
	LCD_DATA2 (output)	P84	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	LCD_DATA3 (output)	P57	○	×	×	○	×	×
		PA5	○	○	○	○	○	○
	LCD_DATA4 (output)	P56	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
	LCD_DATA5 (output)	P55	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
	LCD_DATA6 (output)	P54	○	×	×	○	×	×
		PA2	○	○	○	○	○	○
	LCD_DATA7 (output)	P11	○	×	×	○	×	×
		PA1	○	○	○	○	○	○
	LCD_DATA8 (output)	P83	○	×	×	○	×	×
		PA0	○	○	○	○	○	○
	LCD_DATA9 (output)	PC7	○	×	×	○	×	×
		PE7	○	○	○	○	○	○
	LCD_DATA10 (output)	PC6	○	×	×	○	×	×
		PE6	○	○	○	○	○	○
	LCD_DATA11 (output)	PC5	○	×	×	○	×	×
		PE5	○	○	○	○	○	○
	LCD_DATA12 (output)	P82	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	LCD_DATA13 (output)	P81	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
	LCD_DATA14 (output)	P80	○	×	×	○	×	×
		PE2	○	○	○	○	○	○
	LCD_DATA15 (output)	PC4	○	×	×	○	×	×
		PE1	○	○	○	○	○	○
	LCD_DATA16 (output)	PC3	○	×	×	○	×	×
		PE0	○	○	○	○	○	○
	LCD_DATA17 (output)	P77	○	×	×	○	×	×
		PD7	○	○	○	○	○	○
	LCD_DATA18 (output)	P76	○	×	×	○	×	×
		PD6	○	○	○	○	○	○
	LCD_DATA19 (output)	PC2	○	×	×	○	×	×
		PD5	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Graphic LCD controller*2	LCD_DATA20 (output)	P75	○	×	×	○	×	×
		PD4	○	○	○	○	○	○
	LCD_DATA21 (output)	P74	○	×	×	○	×	×
		PD3	○	○	○	○	○	○
	LCD_DATA22 (output)	PC1	○	×	×	○	×	×
		PD2	○	○	○	○	○	○
	LCD_DATA23 (output)	P72	○	×	×	○	×	×
		PD1	○	○	○	○	○	○
General PWM timer W	GTADSM0 (output)	P12				○	○	○
	GTADSM1 (output)	P13				○	○	○
	GTETRGA (input)	P15				○	○	○
	GTETRGB (input)	PA6				○	○	○
	GTETRGC (input)	PC4				○	○	○
	GTETRGD (input)	P14				○	○	○
	GTIOC0A (input/output)	P23				○	○	○
		P83				○	○	×
		PA5				○	○	○
		PD3				○	○	○
		PE5				○	○	○
	GTIOC0B (input/output)	P17				○	○	○
		P81				○	○	×
		PA0				○	○	○
		PD2				○	○	○
		PE2				○	○	○
	GTIOC1A (input/output)	P22				○	○	○
		PA2				○	○	○
		PC5				○	○	○
		PD1				○	○	○
		PE4				○	○	○
	GTIOC1B (input/output)	P67				○	○	×
		P87				○	○	×
		PC3				○	○	○
		PD0				○	○	○
		PE1				○	○	○
	GTIOC2A (input/output)	P21				○	○	○
		P82				○	○	×
		PA1				○	○	○
		PE3				○	○	○
	GTIOC2B (input/output)	P66				○	○	×
		P86				○	○	×
		PC2				○	○	○
		PE0				○	○	○
	GTIOC3A (input/output)	PC7				○	○	○
		PE7				○	○	○
	GTIOC3B (input/output)	PC6				○	○	○
		PE6				○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX66N		
			176-Pin	145-/144-Pin	100-Pin	176-Pin	145-/144-Pin	100-Pin
Ethernet PHY management interface	PMGI0_MDC (output)	P72				○	○	×
		PA4				○	○	○
	PMGI0_MDIO (input/output)	P71				○	○	×
		PA3				○	○	○
Extended serial sound interface	AUDIO_CLK (input)	P00				○	○	×
		P22				○	○	○
	SSIBCK0 (input/output)	P01				○	○	×
		P23				○	○	○
	SSILRCK0 (input/output)	P21				○	○	○
		PF5				○	○	×
	SSIRXD0 (input)	P20				○	○	○
		PJ5				○	○	×
	SSITXD0 (output)	P17				○	○	○
		PJ3				○	○	○
	SSIBCK1 (input/output)	P02				○	○	×
		P24				○	○	○
	SSILRCK1 (input/output)	P05				○	○	○
		P15				○	○	○
	SSIDATA1 (input/output)	P03				○	○	×
		P25				○	○	○
Clock generation circuit	CLKOUT (output)	P25				○	○	○
	CLKOUT25M (output)	P56				○	○	×
		PJ2				○	×	×

Notes: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).
2. Not supported on RX65N Group products with a code flash memory capacity of 1 MB or less.

Table 2.27 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX65N (MPC) (n = 0 to 3, 5, 7)	RX66N (MPC) (n = 0 to 3, 5, 7)
P00PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/SSDA6	Pin function select bits 000000b: Hi-Z 000101b: TMRI0 001010b: TXD6/SMOSI6/SSDA6 010111b: AUDIO_CLK 011011b: QIO2-C
P01PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/SSCL6	Pin function select bits 000000b: Hi-Z 000101b: TMCI0 001010b: RXD6/SMISO6/SSCL6 010111b: SSIBCK0 011011b: QIO3-C
P02PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6	Pin function select bits 000000b: Hi-Z 000101b: TMCI1 001010b: SCK6 010111b: SSIBCK1
P03PFS	PSEL[5:0]	—	Pin function select bits
P05PFS	PSEL[5:0]	—	Pin function select bits

Table 2.28 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
P12PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 100101b: LCD_TCON1-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 011110b: GTADSM0 100101b: LCD_TCON1-A
P13PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 100101b: LCD_TCON0-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 011110b: GTADSM1 100101b: LCD_TCON0-A
P14PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 100101b: LCD_CLK-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA-DS 011110b: GTETRGD 100101b: LCD_CLK-A
P15PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 011100b: PIXD0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 010111b: SSILRCK1 011100b: PIXD0 011110b: GTETRGA

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
P17PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS 011010b: SDHI_D3-C*1 011100b: PIXD3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS 010111b: SSITXD0 011010b: SDHI_D3-C 011100b: PIXD3 011110b: GTIOC0B

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.29 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
P20PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRI0 000110b: PO0 001010b: TXD0/SMOSI0/SSDA0 001111b: SDA1*1 010011b: USB0_ID 011010b: SDHI_CMD-C*1 011100b: PIXD4	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRI0 000110b: PO0 001010b: TXD0/SMOSI0/SSDA0 001111b: SDA1 010011b: USB0_ID 010111b: SSIRXD0 011010b: SDHI_CMD-C 011100b: PIXD4
P21PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCI0 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1*1 010011b: USB0_EXICEN 011010b: SDHI_CLK-C*1 011100b: PIXD5	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCI0 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1 010011b: USB0_EXICEN 010111b: SSILRCK0 011010b: SDHI_CLK-C 011100b: PIXD5 011110b: GTIOC2A
P22PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB 011000b: EDREQ0 011010b: SDHI_D0-C*1 011100b: PIXD6	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB 010111b: AUDIO_CLK 011000b: EDREQ0 011010b: SDHI_D0-C 011100b: PIXD6 011110b: GTIOC1A

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
P23PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 011000b: EDACK0 011010b: SDHI_D1-C*1 011100b: PIXD7	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 010000b: CTX1 010111b: SSIBCK0 011000b: EDACK0 011010b: SDHI_D1-C 011100b: PIXD7 011110b: GTIOC0A
P24PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 011000b: EDREQ1 011010b: SDHI_WP*1 011100b: PIXCLK	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 010111b: SSIBCK1 011000b: EDREQ1 011010b: SDHI_WP 011100b: PIXCLK
P25PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 011000b: EDACK1 011010b: SDHI_CD*1 011100b: HSYNC	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 010111b: SSIDATA1 011000b: EDACK1 011010b: SDHI_CD 011100b: HSYNC 101010b: CLKOUT

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.30 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX65N (MPC) (n = 0 to 2, 4 to 7)	RX66N (MPC) (n = 0 to 2, 4 to 7)
P56PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7*1 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A 101010b: CLKOUT25M

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.31 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX65N (MPC) (n = 6, 7)	RX66N (MPC) (n = 6, 7)
P66PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7D	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7D 010000b: CTX2 011110b: GTIOC2B
P67PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7C 010000b: CRX2 011110b: GTIOC1B

Table 2.32 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX65N (MPC) (n = 1 to 7)	RX66N (MPC) (n = 1 to 7)
P71PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDIO 101000b: PMGI0_MDIO
P72PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDC 100101b: LCD_DATA23-A*1	Pin function select bits 000000b: Hi-Z 010001b: ET0_MDC 100101b: LCD_DATA23-A 101000b: PMGI0_MDC
P75PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100011b: SDSI_D2 100101b: LCD_DATA20-A*1	Pin function select bits 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100101b: LCD_DATA20-A
P76PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: RXD11/SMISO11/ SSCL11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100011b: SDSI_CMD 100101b: LCD_DATA18-A*1	Pin function select bits 000000b: Hi-Z 000110b: PO22 001010b: SMISO11/SSCL11/ RXD11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100101b: LCD_DATA18-A
P77PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: TXD11/SMOSI11/ SSDA11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100011b: SDSI_CLK 100101b: LCD_DATA17-A*1	Pin function select bits 000000b: Hi-Z 000110b: PO23 001010b: SMOSI11/SSDA11/ TXD11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100101b: LCD_DATA17-A

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.33 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
P81PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: RXD10/SMISO10/ SSCL10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD 011011b: QIO3-A 100101b: LCD_DATA13-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: SMISO10/SSCL10/ RXD10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD 011011b: QIO3-A 011110b: GTIOC0B 100101b: LCD_DATA13-A
P82PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: TXD10/SMOSI10/ SSDA10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 100101b: LCD_DATA12-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: SMOSI10/SSDA10/ TXD10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 011110b: GTIOC2A 100101b: LCD_DATA12-A
P83PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011000b: EDACK1 100101b: LCD_DATA8-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: SS10#/CTS10# 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011000b: EDACK1 011110b: GTIOC0A 100101b: LCD_DATA8-A
P86PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: RXD10/SMISO10/ SSCL10 011100b: PIXD1	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: SMISO10/SSCL10/ RXD10 011100b: PIXD1 011110b: GTIOC2B

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
P87PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: TXD10/SMOSI10/ SSDA10 011010b: SDHI_D2-C*1 011100b: PIXD2	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: SMOSI10/SSDA10/ TXD10 011010b: SDHI_D2-C 011100b: PIXD2 011110b: GTIOC1B

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.34 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PA0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100101b: LCD_DATA8-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011110b: GTIOC0B 100101b: LCD_DATA8-B
PA1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001101b: SSLA2-B 010001b: ET0_WOL 100101b: LCD_DATA7-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001101b: SSLA2-B 010001b: ET0_WOL 011110b: GTIOC2A 100101b: LCD_DATA7-B
PA2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 100101b: LCD_DATA6-B*1	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 011110b: GTIOC1A 100101b: LCD_DATA6-B
PA3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B 101000b: PMGI0_MDIO

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PA4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B 101000b: PMGI0_MDC
PA5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 100101b: LCD_DATA3-B*1	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKSTA 011110b: GTIOC0A 100101b: LCD_DATA3-B
PA6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 100101b: LCD_DATA2-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 011110b: GTETRGB 100101b: LCD_DATA2-B

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.35 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PB2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100011b: SDSI_D2 100101b: LCD_TCON2-B*1	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_TCON2-B
PB3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100011b: SDSI_D3 100101b: LCD_TCON1-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100101b: LCD_TCON1-B
PB4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: CTS9#/RTS9#/SS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100011b: SDSI_CMD 100100b: CTS11#/RTS11#/SS11# 100101b: LCD_TCON0-B*1	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: SS9#/CTS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100100b: SS11#/CTS11#/RTS11# 100101b: LCD_TCON0-B

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PB5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100011b: SDSI_CLK 100100b: SCK11 100101b: LCD_CLK-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 001011b: RTS9# 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100100b: SCK11 100101b: LCD_CLK-B
PB6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100011b: SDSI_D0 100100b: RXD11/SMISO11/ SSCL11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100100b: SMISO11/SSCL11/ RXD11
PB7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_DV 100011b: SDSI_D1 100100b: TXD11/SMOSI11/ SSDA11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_DV 100100b: SMOSI11/SSDA11/ TXD11

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.36 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PC2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 100011b: SDSI_D3 100101b: LCD_DATA19-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A 011010b: SDHI_D3-A 011110b: GTIOC2B 100101b: LCD_DATA19-A
PC3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QIO0-A/QMO-A 100011b: SDSI_D0 100101b: LCD_DATA16-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A 011010b: SDHI_D0-A 011011b: QMO/QIO0 011110b: GTIOC1B 100101b: LCD_DATA16-A
PC4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QIO1-A/QMI-A 100011b: SDSI_D1 100100b: CTS10#/RTS10#/SS10# 100101b: LCD_DATA15-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: SS8#/CTS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A 011010b: SDHI_D1-A 011011b: QMI/QIO1 011110b: GTETRGC 100100b: SS10#/CTS10#/RTS10# 100101b: LCD_DATA15-A

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PC5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A 100100b: SCK10 100101b: LCD_DATA11-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001011b: RTS8# 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A 011110b: GTIOC1A 100100b: SCK10 100101b: LCD_DATA11-A
PC6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A 011101b: TIC0 100100b: RXD10/SMISO10/ SSCL10 100101b: LCD_DATA10-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A 011101b: TIC0 011110b: GTIOC3B 100100b: SMISO10/SSCL10/ RXD10 100101b: LCD_DATA10-A
PC7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000110b: PO31 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA-A 010001b: ET0_COL 011001b: MMC_D7-A 011101b: TOC0 100100b: TXD10/SMOSI10/ SSDA10 100101b: LCD_DATA9-A*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000110b: PO31 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA-A 010001b: ET0_COL 011001b: MMC_D7-A 011101b: TOC0 011110b: GTIOC3A 100100b: SMOSI10/SSDA10/ TXD10 100101b: LCD_DATA9-A

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.37 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PD0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: POE4# 100101b: LCD_EXTCLK-B*1	Pin function select bits 000000b: Hi-Z 001000b: POE4# 011110b: GTIOC1B 100101b: LCD_EXTCLK-B
PD1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0 100101b: LCD_DATA23-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0 011110b: GTIOC1A 100101b: LCD_DATA23-B
PD2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 100101b: LCD_DATA22-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 011110b: GTIOC0B 100101b: LCD_DATA22-B
PD3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 100101b: LCD_DATA21-B*1	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 011110b: GTIOC0A 100101b: LCD_DATA21-B
PD5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKA 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PD6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QIO0-B/QMO-B 100101b: LCD_DATA18-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QMO/QIO0 100101b: LCD_DATA18-B
PD7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QIO1-B/QMI-B 100101b: LCD_DATA17-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QMI/QIO1 100101b: LCD_DATA17-B

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.38 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PE0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B 011001b: MMC_D4-B 100101b: LCD_DATA16-B*1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B 011001b: MMC_D4-B 011110b: GTIOC2B 100101b: LCD_DATA16-B
PE1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001101b: SSLB2-B 011001b: MMC_D5-B 100101b: LCD_DATA15-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001101b: SSLB2-B 011001b: MMC_D5-B 011110b: GTIOC1B 100101b: LCD_DATA15-B
PE2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLB3-B 011001b: MMC_D6-B 011101b: TIC3 100101b: LCD_DATA14-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLB3-B 011001b: MMC_D6-B 011101b: TIC3 011110b: GTIOC0B 100101b: LCD_DATA14-B
PE3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 100101b: LCD_DATA13-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 011110b: GTIOC2A 100101b: LCD_DATA13-B

Register	Bit	RX65N (MPC) (n = 0 to 7)	RX66N (MPC) (n = 0 to 7)
PE4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 100101b: LCD_DATA12-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 011110b: GTIOC1A 100101b: LCD_DATA12-B
PE5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_DATA11-B*1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 011110b: GTIOC0A 100101b: LCD_DATA11-B
PE6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD 011101b: TIC1 100101b: LCD_DATA10-B*1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD 011101b: TIC1 011110b: GTIOC3B 100101b: LCD_DATA10-B
PE7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP 011101b: TOC1 100101b: LCD_DATA9-B*1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#-B 011010b: SDHI_WP 011101b: TOC1 011110b: GTIOC3A 100101b: LCD_DATA9-B

Note: 1. Not supported on products with a code flash memory capacity of 1 MB or less.

Table 2.39 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 2, 5)	RX66N (MPC) (n = 0 to 2, 5)
PF5PFS	PSEL[5:0]	—	Pin function select bits

Table 2.40 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX65N (MPC)	RX66N (MPC)
PHnPFS	—	—	PHn pin function control register (n = 0 to 7)

Table 2.41 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX65N (MPC) (n = 0 to 3, 5)	RX66N (MPC) (n = 0 to 3, 5)
PJ2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: TXD8/SMOSI8/SSDA8 001101b: SSLC3-B 100101b: LCD_TCON2-A	Pin function select bits 000000b: Hi-Z 001010b: TXD8/SMOSI8/SSDA8 001101b: SSLC3-B 100101b: LCD_TCON2-A 101010b: CLKOUT25M
PJ3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 011000b: EDACK1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 010111b: SSITXD0 011000b: EDACK1 011011b: QMO-C/QIO0-C
PJ5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 100001b: POE8#	Pin function select bits 000000b: Hi-Z 001011b: CTS2#/RTS2#/SS2# 010111b: SSIRXD0 011011b: QMI-C/QIO1-C 100001b: POE8#

Table 2.42 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX65N (MPC)	RX66N (MPC)
PKnPFS	—	—	PKn pin function control register (n = 0 to 7)

Table 2.43 Comparison of PLn Pin Function Control Register (PLnPFS)

Register	Bit	RX65N (MPC)	RX66N (MPC)
PLnPFS	—	—	PLn pin function control register (n = 0 to 7)

Table 2.44 Comparison of PMn Pin Function Control Register (PMnPFS)

Register	Bit	RX65N (MPC)	RX66N (MPC)
PMnPFS	—	—	PMn pin function control register (n = 0 to 7)

Table 2.45 Comparison of PNn Pin Function Control Register (PNnPFS)

Register	Bit	RX65N (MPC)	RX66N (MPC)
PNnPFS	—	—	PNn pin function control register (n = 4, 5)

Table 2.46 Comparison of PQn Pin Function Control Register (PQnPFS)

Register	Bit	RX65N (MPC)	RX66N (MPC)
PQnPFS	—	—	PQn pin function control register (n = 0 to 3)

Table 2.47 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX65N (MPC)	RX66N (MPC)
PFBCR0	ADRHMS ADRHMS2	A16 to A23 output enable bit A16 to A23 output enable 2 bit ADRHMS / ADRHMS2 0 / 0: Set PC0 to PC7. 0 / 1: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 / 0: Products with 1.5 MB or more of code flash memory: Set P90 to P97. Products with 1 MB or less of code flash memory: Set P90 to P93 (A20 to A23 not assigned). 1 / 1: Setting prohibited.	A16 to A23 output enable bit A16 to A23 output enable 2 bit ADRHMS / ADRHMS2 0 / 0: Set PC0 to PC7. 0 / 1: Set PC0, PC1, P71, P72, P74, and PC5 to PC7. 1 / 0: 224- and 176-pin products: Set P90 to P97. 145- and 144-pin products: Set P90 to P93 (A20 to A23 not assigned). 1 / 1: Setting prohibited. On 100-pin products, set these bits to 00b.
PFBCR1	WAITS[1:0]	WAIT select bits b1 b0 0 0: Setting invalid 0 1: Set P55 as WAIT# input pin. 1 0: Set PC5 as WAIT# input pin. 1 1: Set P51 as WAIT# input pin.	WAIT select bits • PFBCR3.WAITS2 bit = 0 b1 b0 0 0: Setting prohibited. 0 1: Set P55 as WAIT# input pin. 1 0: Set PC5 as WAIT# input pin. 1 1: Set P51 as WAIT# input pin. • PFBCR3.WAITS2 bit = 1 b1 b0 0 0: Set PF5 as WAIT# input pin. 0 1: Setting prohibited. 1 x: Setting prohibited.
PFBCR3	SDCLKDRV	—	SDCLK pin drive select bit
	WAITS2	—	WAIT select bit 2

2.15 Serial Communications Interface

Table 2.48 is a comparative overview of the serial communications interfaces, Table 2.49 is a comparison of SCI channel functions, and Table 2.50 is a comparison of serial communications interface registers.

Table 2.48 Comparative Overview of Serial Communications Interfaces

Item		RX65N (SCIg, SCIi, SCIh)	RX66N (SCIj, SCIi, SCIh)
Number of channels		• SCIg: 10 channels • SCIi: 2 channels • SCIh: 1 channel	• SCIj: 7 channels • SCIi: 5 channels • SCIh: 1 channel
Serial communication modes		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.
Full-duplex communication		• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering	• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering
Data transfer		Selectable between LSB-first and MSB-first*1	Selectable between LSB-first and MSB-first*1
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI10, SCI11), completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI7 to SCI11), data match (SCI0 to SCI11), completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		Ability to transition individual channels to the module stop state	Ability to transition individual channels to the module stop state
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Data match detection	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI10, SCI11)	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI0 to SCI11)
	Start-bit detection	Selectable between low level and falling edge	Selectable between low level and falling edge

Item		RX65N (SCIg, SCIi, SCIh)	RX66N (SCIj, SCIi, SCIh)
Asynchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.
	Clock source	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)
	Double-speed mode	Ability to select baud rate generator double-speed mode	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	The input signal paths from the RXDn pins incorporate digital noise filters.	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
Smart card interface mode	Error processing	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Support for fast mode	Support for fast mode
	Noise cancellation	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.
	Clock settings	Ability to select among four clock phase and clock polarity settings	Ability to select among four clock phase and clock polarity settings

Item		RX65N (SCIg, SCIi, SCIh)	RX66N (SCIj, SCIi, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Ability to output break field low width/output completion interrupt function • Bus collision detection function/detection interrupt function	• Ability to output break field low width/output completion interrupt function • Bus collision detection function/detection interrupt function
	Start frame reception	• Ability to detect break field low width/detection completion interrupt function • Control field 0 and control field 1 data comparison/match interrupt function • Ability to select between two data types for comparison (primary and secondary) in control field 1 • Ability to set priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Bit rate measurement function	• Ability to detect break field low width/detection completion interrupt function • Control field 0 and control field 1 data comparison/match interrupt function • Ability to select between two data types for comparison (primary and secondary) in control field 1 • Ability to set priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Bit rate measurement function
	I/O control function	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12
	Timer function	Usable as reload timer	Usable as reload timer
Bit rate modulation function		Ability to reduce errors by correcting output from the on-chip baud rate generator	Ability to reduce errors by correcting output from the on-chip baud rate generator
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Note: 1. Simple I^2C mode can only be used with MSB-first data transfer.

Table 2.49 Comparison of SCI Channel Functions

Item	RX65N (SCIg, SCIi, SCIh)	RX66N (SCIj, SCIi, SCIh)
Asynchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
FIFO mode	SCI10, SCI11	SCI7 to SCI11
Data match detection	SCI10, SCI11	SCI0 to SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11	PCLKB: SCI0 to SCI6, SCI12 PCLKA: SCI7 to SCI11

Table 2.50 Comparison of Serial Communications Interface Registers

Register	Bit	RX65N	RX66N
SEMR	ABCSE	—	Asynchronous mode base clock select extended bit*1

Note: 1. This bit is reserved on SCI12. It is read as 0. The write value should be 0.

2.16 CAN Module

Table 2.51 shows a comparative overview of the CAN module specifications.

Table 2.51 Comparative Overview of CAN Module

Item	RX65N (CAN)	RX66N (CAN)
Number of channels	2 channels	3 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX65N (CAN)	RX66N (CAN)
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program
Error status monitoring	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLKB), CANMCLK	Peripheral module clock (PCLKB), CANMCLK

Item	RX65N (CAN)	RX66N (CAN)
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Ability to specify module stop state.	Ability to specify module stop state.

2.17 12-Bit A/D Converter

Table 2.52 is a comparative overview of 12-bit A/D converter functions.

Table 2.52 Comparative Overview of 12-Bit A/D Converter Functions

Item			RX65N (S12ADFa)		RX66N (S12ADFa)	
			Unit 0 (S12AD)	Unit 1 (S12AD1)	Unit 0 (S12AD)	Unit 1 (S12AD1)
Analog input channels			AN000 to AN007	AN100 to AN120, internal reference voltage, temperature sensor output, extended input	AN000 to AN007	AN100 to AN120, internal reference voltage, temperature sensor output, extended input
Conditions for A/D conversion start	Software	Software trigger	Enabled		Enabled	
	Asynchronous trigger	Trigger input pin	ADTRG0#	ADTRG1#	ADTRG0#	ADTRG1#
	Synchronous trigger	Compare match/ input capture from MTU0.TGRA	TRGA0N		TRGA0N	
		Compare match/ input capture from MTU1.TGRA	TRGA1N		TRGA1N	
		Compare match/ input capture from MTU2.TGRA	TRGA2N		TRGA2N	
		Compare match/ input capture from MTU3.TGRA	TRGA3N		TRGA3N	
		Compare match/ input capture from MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	TRGA4N		TRGA4N	
		Compare match/ input capture from MTU6.TGRA	TRGA6N		TRGA6N	
		Compare match/ input capture from MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	TRGA7N		TRGA7N	
		Compare match from MTU0.TGRE	TRG0N		TRG0N	
		Compare match between MTU4.TADCORA and MTU4.TCNT	TRG4AN		TRG4AN	
		Compare match between MTU4.TADCORB and MTU4.TCNT	TRG4BN		TRG4BN	

Item			RX65N (S12ADFa)		RX66N (S12ADFa)	
			Unit 0 (S12AD)	Unit 1 (S12AD1)	Unit 0 (S12AD)	Unit 1 (S12AD1)
Conditions for A/D conversion start	Synchronous trigger	Compare match between MTU4.TADCORA and MTU4.TCNT or compare match between MTU4.TADCORB and MTU4.TCNT	TRG4AN or TRG4BN		TRG4AN or TRG4BN	
		Compare match between MTU4.TADCORA and MTU4.TCNT, and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	TRG4ABN		TRG4ABN	
		Compare match between MTU7.TADCORA and MTU7.TCNT	TRG7AN		TRG7AN	
		Compare match between MTU7.TADCORB and MTU7.TCNT	TRG7BN		TRG7BN	
		Compare match between MTU7.TADCORA and MTU7.TCNT or compare match between MTU7.TADCORB and MTU7.TCNT	TRG7AN or TRG7BN		TRG7AN or TRG7BN	
		Compare match between MTU7.TADCORA and MTU7.TCNT, and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	TRG7ABN		TRG7ABN	
		Compare match between TMR0.TCORA and TMR0.TCNT	TMTRG0AN_0		TMTRG0AN_0	
		Compare match between TMR2.TCORA and TMR2.TCNT	TMTRG0AN_1		TMTRG0AN_1	

Item			RX65N (S12ADFa)		RX66N (S12ADFa)	
			Unit 0 (S12AD)	Unit 1 (S12AD1)	Unit 0 (S12AD)	Unit 1 (S12AD1)
Conditions for A/D conversion start	Synchronous trigger	Input capture/ compare match from TPU0.TGRA or input capture/ compare match from TPU1.TGRA or input capture/ compare match from TPU2.TGRA or input capture/ compare match from TPU3.TGRA or input capture/ compare match from TPU4.TGRA	TPTRGAN		TPTRGAN	
		Input capture/ compare match from TPU0.TGRA0	TPTRG0AN		TPTRG0AN	
		ELC trigger	ELCTRG0N	ELCTRG1N	ELCTRG00N /ELC TRG01N/EL CTRG 00N or ELCTRG01N	ELCTRG10N /ELC TRG11N/EL CTRG 10N or ELCTRG11N
Channel-dedicated sample-and-hold function		Target channels	AN000 to AN002	—	AN000 to AN002	—
Interrupts			S12ADI, GBADI, GCADI, S12CMPAI, and S12CMPBI interrupts	S12ADI1, GBADI1, GCADI1, S12CMPAI1, and S12CMPBI1 interrupts	S12ADI, GBADI, GCADI, S12CMPAI, and S12CMPBI interrupts	S12ADI1, GBADI1, GCADI1, S12CMPAI1, and S12CMPBI1 interrupts
Setting of module stop function			MSTPCRA.M STPA17 bit	MSTPCRA.M STPA16 bit	MSTPCRA.M STPA17 bit	MSTPCRA.M STPA16 bit

2.18 RAM

Table 2.53 is a comparative overview of RAM, and Table 2.54 is a comparison of RAM registers.

Table 2.53 Comparative Overview of RAM

Item	RX65N		RX66N		
	RAM	Expansion RAM*1	RAM	Expansion RAM*1	ECCRAM
Capacity	256 KB	384 KB	512 KB	512 KB	32 KB
Address	0000 0000h to 0003 FFFFh	0080 0000h to 0085 FFFFh	0000 0000h to 0007 FFFFh	0080 0000h to 0087 FFFFh	00FF 8000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 3	Memory bus 1	Memory bus 3	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.		• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • Expansion RAM can be enabled or disabled.	• The ECCRAM function can be enabled or disabled. • The ECC function is disabled: Access takes two cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles for reading or writing.
Data retention function	Not available in deep software standby mode		Not available in deep software standby mode		
Low power consumption function	Transition to module stop state can be enabled separately for RAM and expansion RAM*1.		Transition to module stop state can be enabled separately for RAM, expansion RAM, and ECCRAM.		
Error checking	• Parity checking: 1-bit error detection • A non-maskable interrupt or interrupt is generated in response to an error.		• Parity checking: 1-bit error detection • A non-maskable interrupt or interrupt is generated in response to an error.		• ECC error correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Note: 1. Only on products with a code flash memory capacity of 1.5 MB or more.

Table 2.54 Comparison of RAM Registers

Register	Bit	RX65N	RX66N
ECCRAMMODE	—	—	ECCRAM operating mode control register
ECCRAM2STS	—	—	ECCRAM2 bit error status register
ECCRAM1STSEN	—	—	ECCRAM1 bit error information update enable register
ECCRAM1STS	—	—	ECCRAM1 bit error status register
ECCRAMPRCR	—	—	ECCRAM protect register
ECCRAM2ECAD	—	—	ECCRAM2 bit error address capture register
ECCRAM1ECAD	—	—	ECCRAM1 bit error address capture register
ECCRAMPRCR2	—	—	ECCRAM protect register 2
ECCRAMETST	—	—	ECCRAM test control register

2.19 Standby RAM

Table 2.55 is a comparative overview of standby RAM.

Table 2.55 Comparative Overview of Standby RAM

Item	RX65N	RX66N
RAM capacity	8 KB	8 KB
RAM address	000A 4000h to 000A 5FFFh	000A 4000h to 000A 5FFFh
Access	• Both read and write operations take 2 or 3 cycles of PCLKB when ICLK ≥ PCLKB; 2 cycles of ICLK are needed when ICLK < PCLKB. • Ability to enable or disable RAM access • The endian order conforms to the endian setting of the chip. • Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.	• Both read and write operations take 3 or 4 cycles of PCLKB when ICLK ≥ PCLKB; 2 or 3 cycles of ICLK are needed when ICLK < PCLKB. • Ability to enable or disable RAM access • The endian order conforms to the endian setting of the chip. • Non-aligned access is prohibited. Correct operation is not guaranteed if non-aligned access is attempted.
Data retention function	Data can be retained in deep software standby mode.	Data can be retained in deep software standby mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

2.20 Flash Memory

Table 2.56 is a comparative overview of flash memory, and Table 2.57 is a comparison of flash memory registers.

Table 2.56 Comparative Overview of Flash Memory

Item	RX65N		RX66N (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	User area: Up to 2 MB	Data area: 32 KB	User area: Up to 4 MB	Data area: 32 KB
Address	• When capacity is 2 MB: FFE0 0000h to FFFF FFFFh • When capacity is 1.5 MB: FFE8 0000h to FFFF FFFFh • When capacity is 1 MB: FFF0 0000h to FFFF FFFFh • When capacity is 768 KB: FFF4 0000h to FFFF FFFFh • When capacity is 512 KB: FFF8 0000h to FFFF FFFFh	0010 0000h to 0010 7FFFh	• When capacity is 4 MB: FFC0 0000h to FFFF FFFFh • When capacity is 2 MB: FFE0 0000h to FFFF FFFFh	0010 0000h to 0010 FFFFh
ROM cache	• Capacity: Up to 256 Bytes • Mapping method: 8-way set associative • Replace method: LRU algorithm • Line size: 16 bytes	—	• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—

Item	RX65N		RX66N (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Read cycle	• When the cache is hit: One cycle • When the cache is missed while ROM cache operation is enabled, or when ROM cache operation is disabled: — ICLK ≤ 50 MHz One cycle — 50 MHz < ICLK ≤ 100 MHz Two cycles — ICLK > 100 MHz Three cycles	Reading proceeds in every cycle of FCLK.	• While ROM cache operation is enabled: — When the cache is hit: One cycle — when the cache is missed: One to two cycles • When ROM cache operation is disabled: One cycle	Reading proceeds in every cycle of FCLK.
Value after erasure	FFh	Undefined	FFh	Undefined
Programming/ erasing method	• Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACI commands specified in the FACI command issuing area (007E 0000h) (self-programming) • Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)		• Programming or erasure of the code flash memory and data flash memory, and programming of the option-setting memory, by means of FACI commands specified in the FACI command issuing area (007E 0000h) (self-programming) • Programming or erasure through transfer by a serial-programmer via a serial interface (serial programming)	
Security function	Protects against illicit tampering or reading of data in flash memory		Protects against illicit tampering or reading of data in flash memory	
Protection function	Protects against erroneous rewriting of the flash memory		Protects against erroneous rewriting of the flash memory	
Dual bank function	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	—	The dual-bank configuration enables safe updating in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	—
Trusted memory (TM) function	Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 46, and 47	—	Protects against unauthorized reading of the code flash memory. • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 78, and 79	—

Item	RX65N		RX66N (FLASH)	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Background operation (BGO)	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.		• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes	• Unit of programming for the user area: 128 bytes • Unit of erasure for the user area: Block	• Unit of programming for data area: 4 bytes • Unit of erasure for data area: 64, 128, or 256 bytes
Other functions	• Interrupts can be accepted during self-programming. • The initial settings of the MCU can be specified in the option-setting memory.		• Interrupts can be accepted during self-programming. • The initial settings of the MCU can be specified in the option-setting memory.	
On-board programming (serial programming/ self-programming)	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming or erasure by self-programming — Programming and erasure can be performed without resetting the system, and it is possible to read data from the code flash memory while erasure is in progress.		• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming or erasure by self-programming — Programming and erasure can be performed without resetting the system, and it is possible to read data from the code flash memory while erasure is in progress.	
Off-board programming	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.*1	Programming or erasure of the data flash memory by using a parallel programmer is not possible.*1	Programming or erasure of the code flash memory or option-setting memory are possible by using a parallel programmer.	Programming or erasure of the data flash memory by using a parallel programmer is not possible.
Unique ID	A 16-byte ID code is provided for each MCU.		A 16-byte ID code is provided for each MCU.	

Note: 1. Not supported on 64-pin products.

Table 2.57 Comparison of Flash Memory Registers

Register	Bit	RX65N	RX66N
NCRGn	—	—	Non-cacheable area n address register (n = 0 or 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0 or 1)
FWEPROR	FLWE[1:0]	Flash programming and erasure enable bits Products with 1.5 MB or more of code flash memory: b1 b0 0 0: Disables programming and erasure, and blank checking. 0 1: Enables programming and erasure, and blank checking. 1 0: Disables programming and erasure, and blank checking. 1 1: Disables programming and erasure, and blank checking. Products with 1 MB or less of code flash memory: b1 b0 0 0: Disables programming and erasure. 0 1: Enables programming and erasure. 1 0: Disables programming and erasure. 1 1: Disables programming and erasure.	Flash programming and erasure enable bits b1 b0 0 0: Disables programming and erasure, and blank checking. 0 1: Enables programming and erasure, and blank checking. 1 0: Disables programming and erasure, and blank checking. 1 1: Disables programming and erasure, and blank checking.

2.21 Packages

As indicated in Table 2.58, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to RX Family Design Guide for Migration between RX Family: Differences in Package External Form (R01AN4591EJ).

Table 2.58 Comparison of Packages

Package Type	Renesas Code	
	RX65N	RX66N
224-pin LFBGA	×	○
177-pin TFLGA	○	×
176-pin LFQFP	PLQP0176KB-A	PLQP0176KB-C
100-pin TFLGA	○	×
64-pin TFBGA	○	×
64-pin LFQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 176-Pin LFBGA Package

Table 3.1 is a comparative listing of the pin functions of 176-pin LFBGA package products.

Table 3.1 Comparative Listing of 176-Pin LFBGA Package Pin Functions

176-Pin LFBGA	RX65N	RX66N
A1	AVSS0	AVSS0
A2	AVCC0	AVCC0
A3	VREFL0	VREFL0
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
A6	VCC	VCC
A7	VSS	VSS
A8	P94/D20/A20	P94/D20/A20
A9	VCC	VCC
A10	TRSYNC1/P97/D23/A23	TRSYNC1/P97/D23/A23
A11	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
A12	P60/CS0#	P60/CS0#
A13	P63/CAS#/D2[A2/D2]/CS3#	P63/CAS#/D2[A2/D2]/CS3#
A14	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
A15	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
B1	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
B2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
B3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
B4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
B5	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B6	P91/D17/A17/SCK7/AN115	P91/D17/A17/SCK7/AN115
B7	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
B8	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
B9	TRDATA5/P96/D22/A22	TRDATA5/P96/D22/A22
B10	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
B11	TRDATA7/PG1/D25	TRDATA7/PG1/D25

176-Pin LFBGA	RX65N	RX66N
B12	VSS	VSS
B13	P64/WE#/D3[A3/D3]/CS4#	P64/WE#/D3[A3/D3]/CS4#
B14	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
B15	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/ RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
C1	AVSS1	AVSS1
C2	AVCC1	AVCC1
C3	VREFH0	VREFH0
C4	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
C5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
C6	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114
C7	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
C8	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
C9	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
C10	TRDATA6/PG0/D24	TRDATA6/PG0/D24
C11	VCC	VCC
C12	P62/RAS#/D1[A1/D1]/CS2#	P62/RAS#/D1[A1/D1]/CS2#
C13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
C14	VSS	VSS
C15	P70/SDCLK	P70/SDCLK
D1	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
D2	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
D3	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
D5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
D6	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117
D7	TRDATA4/P95/D21/A21	TRDATA4/P95/D21/A21
D8	VSS	VSS
D9	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
D10	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
D11	P61/SDCS#/D0[A0/D0]/CS1#	P61/SDCS#/D0[A0/D0]/CS1#

176-Pin LFBGA	RX65N	RX66N
D12	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/ET0_RX_CLK/REF50CK0/ RSPCKB-B/LCD_DATA11-B/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
D13	VCC	VCC
D14	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
D15	P65/CKE/CS5#	P65/CKE/CS5#
E1	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
E2	EMLE	EMLE
E3	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
E4	VSS	VSS
E12	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
E13	TRDATA0/PG2/D26	TRDATA0/PG2/D26
E14	TRDATA1/PG3/D27	TRDATA1/PG3/D27
E15	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
F1	VBATT	VBATT
F2	VCL	VCL
F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
F4	BSCANP	BSCANP
F12	P66/DQM0/CS6#/MTIOC7D	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
F13	TRSYNC/PG4/D28	TRSYNC/PG4/D28
F14	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
F15	VSS	VSS
G1	XCIN	XCIN
G2	XCOUT	XCOUT
G3	MD/FINED	MD/FINED
G4	TRST#/PF4	TRST#/PF4
G12	TRCLK/PG5/D29	TRCLK/PG5/D29
G13	TRDATA2/PG6/D30	TRDATA2/PG6/D30
G14	PA1/DQM3/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/ SSLA2-B/LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/LCD_DATA7-B/IRQ11
G15	VCC	VCC
H1	XTAL/P37	XTAL/P37
H2	VSS	VSS
H3	RES#	RES#
H4	UPSEL/P35/NMI	UPSEL/P35/NMI
H12	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS

176-Pin LFBGA	RX65N	RX66N
H13	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
H14	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
H15	TRDATA3/PG7/D31	TRDATA3/PG7/D31
J1	EXTAL/P36	EXTAL/P36
J2	VCC	VCC
J3	P34/MTIOC0A/TMCI3/PO12/POE10#/ ET0_LINKSTA/SCK6/SCK0/IRQ4	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4
J4	TMS/PF3	TMS/PF3
J12	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
J13	VSS	VSS
J14	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
J15	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
K1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
K2	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
K3	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
K4	TCK/PF1/SCK1	TCK/PF1/SCK1
K12	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
K13	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
K14	VCC	VCC
K15	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
L1	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS
L2	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
L3	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
L4	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
L12	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1

176-Pin LFBGA	RX65N	RX66N
L13	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/ LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
L14	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
L15	P72/A19/CS2#/ET0_MDC/LCD_DATA23-A	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A
M1	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A
M2	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
M3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
M4	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
M5	PJ2/TXD8/SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A
M6	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/ SSLC2-B/LCD_TCON3-A	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/ SSLC2-B/LCD_TCON3-A
M7	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	P85/MTIOC6C/TIOCC0/LCD_DATA1-A
M8	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/ET0_EXOUT/TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/LCD_DATA5-A/IRQ10	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/ CRX1/ET0_EXOUT/LCD_DATA5-A/IRQ10
M9	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
M10	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/ SCK10/RSPCKA-A/MMC_D5-A/ LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A
M11	P81/EDACK0/MTIOC3D/PO27/ET0_ETXD0/ RMII0_TXD0/SMISO10/SSCL10/RXD10/ QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A
M12	P77/CS7#/PO23/ET0_RX_ER/ RMII0_RX_ER/SMOSI11/SSDA11/TXD11/ QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/ MMC_CLK-A/LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A
M13	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
M14	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
M15	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B

176-Pin LFBGA	RX65N	RX66N
N1	VCC	VCC
N2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
N3	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ SDHI_D0-C/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6
N4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5
N5	P12/WR3#/BC3#/MTIC5U/TMCI1/RXD2/ SMISO2/SSCL2/SCL0[FM+]/LCD_TCON1-A/ IRQ2	P12/WR3#/BC3#/MTIC5U/TMCI1/ GTADSM0/RXD2/SMISO2/SSCL2/ SCL0[FM+]/LCD_TCON1-A/IRQ2
N6	PJ0/MTIOC6B/SCK8/SSLC1-B/ LCD_DATA0-A	PJ0/MTIOC6B/SCK8/SSLC1-B/ LCD_DATA0-A
N7	P84/MTIOC6D/LCD_DATA2-A	P84/MTIOC6D/LCD_DATA2-A
N8	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/ TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/LCD_DATA6-A
N9	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
N10	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/MMC_D7-A/ LCD_DATA9-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ LCD_DATA9-A/IRQ14
N11	P82/EDREQ1/MTIOC4A/PO28/ET0_ETXD1/ RMII0_TXD1/SMOSI10/SSDA10/TXD10/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A
N12	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/ QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A
N13	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
N14	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A
N15	VSS	VSS
P1	VSS	VSS
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C/ PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
P3	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/ IRQ4
P5	VCC_USB	VCC_USB

176-Pin LFBGA	RX65N	RX66N
P6	VSS_USB	VSS_USB
P7	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A
P8	P10/ALE/MTIC5W/TMRI3/IRQ0	P10/ALE/MTIC5W/TMRI3/IRQ0
P9	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
P10	P83/EDACK1/MTIOC4C/ET0_CRS/ RMII0_CRS_DV/SCK10/SS10#/CTS10#/ LCD_DATA8-A	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ LCD_DATA8-A
P11	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/MMC_D6-A/ LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13
P12	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/ SDSI_D1-A/MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A
P13	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A/SDHI_D3-A/SDSI_D3-A/ MMC_CD-A/LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A
P14	P75/CS5#/PO20/ET0_ERXD0/RMII0_RXD0/ SCK11/RTS11#/SDHI_D2-A/SDSI_D2-A/ MMC_RES#-A/LCD_DATA20-A	P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A
P15	VCC	VCC
R1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
R2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/ SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
R4	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ADTRG1#	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#
R5	USB0_DM	USB0_DM
R6	USB0_DP	USB0_DP
R7	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7/RSPCKC-B/LCD_DATA4-A
R8	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/ IRQ1	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/ IRQ1
R9	P53*1/BCLK	P53*1/BCLK
R10	VSS	VSS
R11	VCC	VCC

176-Pin LFBGA	RX65N	RX66N
R12	P80/EDREQ0/MTIOC3B/PO26/ET0_TX_EN/ RMII0_TXD_EN/SCK10/RTS10#/QIO2-A/ SDHI_WP/MMC_D2-A/LCD_DATA14-A	P80/EDREQ0/MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/RMII0_TXD_EN/ QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A
R13	P76/CS6#/PO22/ET0_RX_CLK/REF50CK0/ SMISO11/SSCL11/RXD11/QSSL-A/ SDHI_CMD-A/SDSI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A
R14	P74/A20/CS4#/PO19/ET0_ERXD1/ RMII0_RXD1/SS11#/CTS11#/ LCD_DATA21-A	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A
R15	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/ IRQ12

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.2 176-Pin LFQFP Package

Table 3.2 is a comparative listing of the pin functions of 176-pin LFQFP package products.

Table 3.2 Comparative Listing of 176-Pin LFQFP Package Pin Functions

176-Pin LFQFP	RX65N	RX66N
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
3	AVCC1	AVCC1
4	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
5	AVSS1	AVSS1
6	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
9	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
10	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
12	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
14	VCL	VCL
15	VBATT	VBATT
16	NC	NC
17	TRST#/PF4	TRST#/PF4
18	MD/FINED	MD/FINED
19	XCIN	XCIN
20	XCOUT	XCOUT
21	RES#	RES#
22	XTAL/P37	XTAL/P37
23	VSS	VSS
24	EXTAL/P36	EXTAL/P36
25	VCC	VCC
26	UPSEL/P35/NMI	UPSEL/P35/NMI
27	P34/MTIOC0A/TMCI3/PO12/POE10#/ ET0_LINKSTA/SCK6/SCK0/IRQ4	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4
28	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
29	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
30	TMS/PF3	TMS/PF3
31	TDI/PF2/RXD1/SMISO1/SSCL1	TDI/PF2/RXD1/SMISO1/SSCL1
32	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS
33	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS

176-Pin LFQFP	RX65N	RX66N
34	TCK/PF1/SCK1	TCK/PF1/SCK1
35	TDO/PF0/TXD1/SMOSI1/SSDA1	TDO/PF0/TXD1/SMOSI1/SSDA1
36	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A
37	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
38	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
39	VCC	VCC
40	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
41	VSS	VSS
42	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
43	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ SDHI_D0-C/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6
44	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SDHI_CLK-C/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
45	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/ SDHI_CMD-C/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
46	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C/ PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
47	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SDHI_D2-C/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
48	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
49	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
50	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5
51	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/ IRQ4

176-Pin LFQFP	RX65N	RX66N
52	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ADTRG1#	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#
53	P12/WR3#/BC3#/MTIC5U/TMCI1/RXD2/ SMISO2/SSCL2/SCL0[FM+]/LCD_TCON1-A/ IRQ2	P12/WR3#/BC3#/MTIC5U/TMCI1/ GTADSM0/RXD2/SMISO2/SSCL2/ SCL0[FM+]/LCD_TCON1-A/IRQ2
54	VCC_USB	VCC_USB
55	USB0_DM	USB0_DM
56	USB0_DP	USB0_DP
57	VSS_USB	VSS_USB
58	PJ2/TXD8/SMOSI8/SSDA8/SSLC3-B/ LCD_TCON2-A	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A
59	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/ SSLC2-B/LCD_TCON3-A	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/ SSLC2-B/LCD_TCON3-A
60	PJ0/MTIOC6B/SCK8/SSLC1-B/ LCD_DATA0-A	PJ0/MTIOC6B/SCK8/SSLC1-B/ LCD_DATA0-A
61	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	P85/MTIOC6C/TIOCC0/LCD_DATA1-A
62	P84/MTIOC6D/LCD_DATA2-A	P84/MTIOC6D/LCD_DATA2-A
63	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A
64	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/LCD_DATA4-A	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7/RSPCKC-B/LCD_DATA4-A
65	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/ET0_EXOUT/TXD7/SMOSI7/SSDA7/ MISOC-B/CRX1/LCD_DATA5-A/IRQ10	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/ CRX1/ET0_EXOUT/LCD_DATA5-A/IRQ10
66	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/ TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/ MOSIC-B/CTX1/LCD_DATA6-A	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/LCD_DATA6-A
67	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/ IRQ1	P11/MTIC5V/TMCI3/SCK2/LCD_DATA7-A/ IRQ1
68	P10/ALE/MTIC5W/TMRI3/IRQ0	P10/ALE/MTIC5W/TMRI3/IRQ0
69	P53*1/BCLK	P53*1/BCLK
70	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
71	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
72	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
73	VSS	VSS
74	P83/EDACK1/MTIOC4C/ET0_CRS/ RMII0_CRS_DV/SCK10/SS10#/CTS10#/ LCD_DATA8-A	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ LCD_DATA8-A
75	VCC	VCC
76	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/MMC_D7-A/ LCD_DATA9-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ LCD_DATA9-A/IRQ14
77	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/MMC_D6-A/ LCD_DATA10-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ LCD_DATA10-A/IRQ13

176-Pin LFQFP	RX65N	RX66N
78	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/ SCK10/RSPCKA-A/MMC_D5-A/ LCD_DATA11-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A/LCD_DATA11-A
79	P82/EDREQ1/MTIOC4A/PO28/ET0_ETXD1/ RMII0_TXD1/SMOSI10/SSDA10/TXD10/ MMC_D4-A/LCD_DATA12-A	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A
80	P81/EDACK0/MTIOC3D/PO27/ET0_ETXD0/ RMII0_TXD0/SMISO10/SSCL10/RXD10/ QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A
81	P80/EDREQ0/MTIOC3B/PO26/ET0_TX_EN/ RMII0_TXD_EN/SCK10/RTS10#/QIO2-A/ SDHI_WP/MMC_D2-A/LCD_DATA14-A	P80/EDREQ0/MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/RMII0_TXD_EN/ QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A
82	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/ SDSI_D1-A/MMC_D1-A/LCD_DATA15-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A/LCD_DATA15-A
83	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/ QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A
84	P77/CS7#/PO23/ET0_RX_ER/ RMII0_RX_ER/SMOSI11/SSDA11/TXD11/ QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/ MMC_CLK-A/LCD_DATA17-A	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/ LCD_DATA17-A
85	P76/CS6#/PO22/ET0_RX_CLK/REF50CK0/ SMISO11/SSCL11/RXD11/QSSL-A/ SDHI_CMD-A/SDSI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/ SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A
86	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A/SDHI_D3-A/SDSI_D3-A/ MMC_CD-A/LCD_DATA19-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A
87	P75/CS5#/PO20/ET0_ERXD0/RMII0_RXD0/ SCK11/RTS11#/SDHI_D2-A/SDSI_D2-A/ MMC_RES#-A/LCD_DATA20-A	P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A
88	P74/A20/CS4#/PO19/ET0_ERXD1/ RMII0_RXD1/SS11#/CTS11#/ LCD_DATA21-A	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A
89	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/ LCD_DATA22-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/ IRQ12
90	VCC	VCC
91	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
92	VSS	VSS
93	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A

176-Pin LFQFP	RX65N	RX66N
94	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
95	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
96	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
97	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
98	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/ LCD_TCON1-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
99	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/ LCD_TCON2-B	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
100	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/LCD_TCON3-B/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
101	P72/A19/CS2#/ET0_MDC/LCD_DATA23-A	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A
102	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
103	VCC	VCC
104	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ LCD_DATA0-B/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
105	VSS	VSS
106	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/ LCD_DATA1-B	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
107	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
108	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/LCD_DATA3-B	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
109	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
110	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
111	TRDATA3/PG7/D31	TRDATA3/PG7/D31

176-Pin LFQFP	RX65N	RX66N
112	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
113	TRDATA2/PG6/D30	TRDATA2/PG6/D30
114	PA1/DQM3/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/ SSLA2-B/LCD_DATA7-B/IRQ11	PA1/DQM3/A1/MTIOC0B/MTCLKC/ MTIOC7B/TIOCB0/PO17/GTIOC2A/SCK5/ SSLA2-B/ET0_WOL/LCD_DATA7-B/IRQ11
115	VCC	VCC
116	TRCLK/PG5/D29	TRCLK/PG5/D29
117	VSS	VSS
118	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/ LCD_DATA8-B
119	TRSYNC/PG4/D28	TRSYNC/PG4/D28
120	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
121	TRDATA1/PG3/D27	TRDATA1/PG3/D27
122	P66/DQM0/CS6#/MTIOC7D	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/ CTX2
123	TRDATA0/PG2/D26	TRDATA0/PG2/D26
124	P65/CKE/CS5#	P65/CKE/CS5#
125	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
126	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
127	VCC	VCC
128	P70/SDCLK	P70/SDCLK
129	VSS	VSS
130	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/ET0_RX_CLK/REF50CK0/ RSPCKB-B/LCD_DATA11-B/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
131	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/ LCD_DATA12-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
132	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/ RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
133	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
134	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
135	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0

176-Pin LFQFP	RX65N	RX66N
136	P64/WE#/D3[A3/D3]/CS4#	P64/WE#/D3[A3/D3]/CS4#
137	P63/CAS#/D2[A2/D2]/CS3#	P63/CAS#/D2[A2/D2]/CS3#
138	P62/RAS#/D1[A1/D1]/CS2#	P62/RAS#/D1[A1/D1]/CS2#
139	P61/SDCS#/D0[A0/D0]/CS1#	P61/SDCS#/D0[A0/D0]/CS1#
140	VSS	VSS
141	P60/CS0#	P60/CS0#
142	VCC	VCC
143	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
144	TRDATA7/PG1/D25	TRDATA7/PG1/D25
145	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
146	TRDATA6/PG0/D24	TRDATA6/PG0/D24
147	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
148	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
149	TRSYNC1/P97/D23/A23	TRSYNC1/P97/D23/A23
150	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
151	VSS	VSS
152	TRDATA5/P96/D22/A22	TRDATA5/P96/D22/A22
153	VCC	VCC
154	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
155	TRDATA4/P95/D21/A21	TRDATA4/P95/D21/A21
156	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ CTX0/LCD_DATA23-B/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
157	P94/D20/A20	P94/D20/A20
158	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
159	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117
160	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
161	P91/D17/A17/SCK7/AN115	P91/D17/A17/SCK7/AN115
162	VSS	VSS
163	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114	P90/D16/A16/TXD7/SMOSI7/SSDA7/AN114
164	VCC	VCC
165	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
166	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
167	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
168	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
169	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003

176-Pin LFQFP	RX65N	RX66N
170	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
171	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
172	VREFL0	VREFL0
173	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
174	VREFH0	VREFH0
175	AVCC0	AVCC0
176	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.3 145-Pin TFLGA Package

Table 3.3 is a comparative listing of the pin functions of 145-pin TFLGA package products.

Table 3.3 Comparative Listing of 145-Pin TFLGA Package Pin Functions

145-Pin TFLGA	RX65N	RX66N
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/AN114
A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
A8	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B*1/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/ LCD_DATA18-B*1/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
A10	VSS	VSS
A11	P62/RAS#/D1[A1/D1]*1/CS2#	P62/RAS#/D1[A1/D1]/CS2#
A12	PE1/D9[A9/D9]/D1[A1/D1]*1/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B*1/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
A13	PE3/D11[A11/D11]/D3[A3/D3]*1/MTIOC4B/ PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/ RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B*1/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
B1	AVCC1	AVCC1
B2	AVCC0	AVCC0
B3	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
B8	PD0/D0[A0/D0]/POE4#/ LCD_EXTCLK-B*1/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B*1/ IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
B10	VCC	VCC
B11	P61/SDCS#/D0[A0/D0]*1/CS1#	P61/SDCS#/D0[A0/D0]/CS1#

145-Pin TFLGA	RX65N	RX66N
B12	PE2/D10[A10/D10]/D2[A2/D2]*1/ MTIOC4A/PO23/TIC3/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B*1/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/ MTIOC4A/PO23/TIC3/GTIOC0B/RXD12/ SMISO12/SSCL12/RXDX12/SSLB3-B/ MMC_D6-B/LCD_DATA14-B/IRQ7-DS/ AN100
B13	PE4/D12[A12/D12]/D4[A4/D4]*1/ MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/ SSLB0-B/LCD_DATA12-B*1/AN102	PE4/D12[A12/D12]/D4[A4/D4]/ MTIOC4D/MTIOC1A/PO28/GTIOC1A/ SSLB0-B/ET0_ERXD2/LCD_DATA12-B/ AN102
C1	AVSS1	AVSS1
C2	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS
C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ CTX0/LCD_DATA23-B*1/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
C8	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B*1/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B*1/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
C10	P63/CAS#/D2[A2/D2]*1/CS3#	P63/CAS#/D2[A2/D2]/CS3#
C11	PE0/D8[A8/D8]/D0[A0/D0]*1/MTIOC3D/ SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B*1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
C12	P70/SDCLK	P70/SDCLK
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
D2	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
D3	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119
D5	VCC	VCC
D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B*1/IRQ5/ AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
D8	P60/CS0#	P60/CS0#
D9	P64/WE#/D3[A3/D3]*1/CS4#	P64/WE#/D3[A3/D3]/CS4#
D10	PE7/D15[A15/D15]/D7[A7/D7]*1/ MTIOC6A/TOC1/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B*1/IRQ7/ AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
D11	VCC	VCC

145-Pin TFLGA	RX65N	RX66N
D12	PE5/D13[A13/D13]/D5[A5/D5]*1/ MTIOC4C/MTIOC2B/ET0_RX_CLK/ REF50CK0/RSPCKB-B/ LCD_DATA11-B*1/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
D13	PE6/D14[A14/D14]/D6[A6/D6]*1/ MTIOC6C/TIC1/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B*1/ IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
E1	VSS	VSS
E2	VCL	VCL
E3	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
E10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/ LCD_DATA8-B*1	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
E11	P66/DQM0/CS6#/MTIOC7D	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
E12	P65/CKE/CS5#	P65/CKE/CS5#
E13	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6# /CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B*1/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
F11	VSS	VSS
F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/ LCD_DATA7-B*1/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
F13	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B*1	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
G1	XTAL/P37	XTAL/P37
G2	RES#	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B*1	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B*1	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
G12	VCC	VCC
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B*1/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS

145-Pin TFLGA	RX65N	RX66N
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS
H4	UPSEL/P35/NMI	UPSEL/P35/NMI
H10	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC
H11	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
H12	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ LCD_DATA0-B*1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
H13	PA7/A7/TIOCB2/PO23/ET0_WOL/ MISOA-B/LCD_DATA1-B*1	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/ LCD_TCON1-B*1	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
J11	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B*1	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
J12	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/ LCD_TCON2-B*1	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/LCD_TCON3-B*1/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
K1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS

145-Pin TFLGA	RX65N	RX66N
K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/ PIXD0/IRQ5
K5	TRDATA2/P54/ALE/D1[A1/D1]*1/ EDACK0/MTIOC4B/TMCI1/ET0_LINKSTA/ CTS2#/RTS2#/SS2#/CTX1	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA
K6	P53*2/BCLK	P53*2/BCLK
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ ET0_TX_EN/RMII0_TXD_EN/SCK10/ RTS10#/QIO2-A/SDHI_WP/MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A
K10	TRDATA6/P76/CS6#/PO22/ET0_RX_CLK/ REF50CK0/SMISO11/SSCL11/RXD11/ QSSL-A/SDHI_CMD-A/SDSI_CMD-A/ MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B*1	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/SDHI_D1-C/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/ TCLKC/TMO2/PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ SCL2-DS/USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/ TCLKC/TMO2/PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ SCL2-DS/USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
L6	P56/EDACK1/MTIOC3C/TIOCA1/SCK7*1	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7

145-Pin TFLGA	RX65N	RX66N
L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
L8	TRCLK/P83/EDACK1/MTIOC4C/ET0_CRS/ RMII0_CRS_DV/SCK10/SS10#/CTS10#	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV
L9	PC5/D3[A3/D3]*1/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/PO29/ ET0_ETXD2/SCK8/SCK10/RSPCKA-A/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2/ MMC_D5-A
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/ SDSI_D1-A/MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A
L11	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A/SDHI_D3-A/SDSI_D3-A/ MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A
L12	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/ET0_WOL
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ SDHI_D0-C*1/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6
M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/ SDHI_D3-C*1/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
M3	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
M4	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
M8	PC6/D2[A2/D2]*1/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13
M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ ET0_ETXD0/RMII0_TXD0/SMISO10/ SSCL10/RXD10/QIO3-A/SDHI_CD/ MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/SDHI_CD/ MMC_D3-A
M10	TRDATA7/P77/CS7#/PO23/ET0_RX_ER/ RMII0_RX_ER/SMOSI11/SSDA11/TXD11/ QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/ MMC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A

145-Pin TFLGA	RX65N	RX66N
M11	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
M12	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
M13	VCC	VCC
N1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1*1/ USB0_EXICEN/SDHI_CLK-C*1/PIXD5/ IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1*1/USB0_ID/ SDHI_CMD-C*1/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
N3	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SDHI_D2-C*1/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
N5	USB0_DM	USB0_DM
N6	USB0_DP	USB0_DP
N7	TRDATA3/P55/D0[A0/D0]*1/WAIT#/ EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/ TXD7*1/SMOSI7*1/SSDA7*1/CRX1/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10
N8	VSS	VSS
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/MMC_D7-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ ET0_ETXD1/RMII0_TXD1/SMOSI10/ SSDA10/TXD10/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A
N11	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/ QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A
N12	TRSYNC1/P75/CS5#/PO20/ET0_ERXD0/ RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/ SDSI_D2-A/MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A
N13	TRDATA5/P74/A20/CS4#/PO19/ ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1

Notes: 1. Valid only on products with a code flash memory capacity of 2 MB or 1.5 MB.
2. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.4 144-Pin LFQFP Package

Table 3.4 is a comparative listing of the pin functions of 144-pin LFQFP package products.

Table 3.4 Comparative Listing of 144-Pin LFQFP Package Pin Functions

144-Pin LFQFP	RX65N	RX66N
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1
3	AVCC1	AVCC1
4	P03/IRQ11/DA0	P03/SSIDATA1/IRQ11/DA0
5	AVSS1	AVSS1
6	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/ SSIBCK0/IRQ9/AN119
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/IRQ8/AN118
9	PF5/IRQ4	PF5/WAIT#/SSILRCK0/IRQ4
10	EMLE	EMLE
11	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0
12	VSS	VSS
13	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
14	VCL	VCL
15	VBATT	VBATT
16	MD/FINED	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES#	RES#
20	XTAL/P37	XTAL/P37
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36
23	VCC	VCC
24	UPSEL/P35/NMI	UPSEL/P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
26	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
30	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A

144-Pin LFQFP	RX65N	RX66N
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
32	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD*1/HSYNC/ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/SDHI_CD/HSYNC/ ADTRG0#
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP*1/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1/SDHI_WP/PIXCLK
34	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/SDHI_D1-C*1/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/ SDHI_D1-C/PIXD7
35	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ SDHI_D0-C*1/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/ PIXD6
36	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1*1/ USB0_EXICEN/SDHI_CLK-C*1/PIXD5/ IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ PIXD5/IRQ9
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1*1/USB0_ID/ SDHI_CMD-C*1/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8
38	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C*1/ PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#
39	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SDHI_D2-C*1/PIXD2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/SDHI_D2-C/PIXD2
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
41	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/PIXD1	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/ IRQ5
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
45	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2

144-Pin LFQFP	RX65N	RX66N
46	VCC_USB	VCC_USB
47	USB0_DM	USB0_DM
48	USB0_DP	USB0_DP
49	VSS_USB	VSS_USB
50	P56/EDACK1/MTIOC3C/TIOCA1/SCK7*1	CLKOUT25M/P56/EDACK1/MTIOC3C/ TIOCA1/SCK7
51	TRDATA3/P55/D0[A0/D0]*1/WAIT#/ EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/ TXD7*1/SMOSI7*1/SSDA7*1/CRX1/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/ET0_EXOUT/IRQ10
52	TRDATA2/P54/ALE/D1[A1/D1]*1/EDACK0/ MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA
53	P53*2/BCLK	P53*2/BCLK
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
57	VSS	VSS
58	TRCLK/P83/EDACK1/MTIOC4C/ET0_CRS/ RMII0_CRS_DV/SCK10/SS10#/CTS10#	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV
59	VCC	VCC
60	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/MMC_D7-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/MMC_D7-A/ IRQ14
61	PC6/D2[A2/D2]*1/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/MMC_D6-A/ IRQ13
62	PC5/D3[A3/D3]*1/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/PO29/ ET0_ETXD2/SCK8/SCK10/RSPCKA-A/ MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/PO29/ GTIOC1A/SCK8/RTS8#/SCK10/RSPCKA-A/ ET0_ETXD2/MMC_D5-A
63	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ ET0_ETXD1/RMII0_TXD1/SMOSI10/ SSDA10/TXD10/MMC_D4-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A
64	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ ET0_ETXD0/RMII0_TXD0/SMISO10/ SSCL10/RXD10/QIO3-A/SDHI_CD/ MMC_D3-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/ SDHI_CD/MMC_D3-A
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ ET0_TX_EN/RMII0_TXD_EN/SCK10/ RTS10#/QIO2-A/SDHI_WP/MMC_D2-A	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/ RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A

144-Pin LFQFP	RX65N	RX66N
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/ SDSI_D1-A/MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A
67	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/ QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/ GTIOC1B/TXD5/SMOSI5/SSDA5/ ET0_TX_ER/QMO-A/QIO0-A/SDHI_D0-A/ MMC_D0-A
68	TRDATA7/P77/CS7#/PO23/ET0_RX_ER/ RMII0_RX_ER/SMOSI11/SSDA11/TXD11/ QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/ MMC_CLK-A	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/ET0_RX_ER/ RMII0_RX_ER/QSPCLK-A/SDHI_CLK-A/ MMC_CLK-A
69	TRDATA6/P76/CS6#/PO22/ET0_RX_CLK/ REF50CK0/SMISO11/SSCL11/RXD11/ QSSL-A/SDHI_CMD-A/SDSI_CMD-A/ MMC_CMD-A	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/ET0_RX_CLK/REF50CK0/ QSSL-A/SDHI_CMD-A/MMC_CMD-A
70	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A/SDHI_D3-A/SDSI_D3-A/ MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV/SDHI_D3-A/MMC_CD-A
71	TRSYNC1/P75/CS5#/PO20/ET0_ERXD0/ RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/ SDSI_D2-A/MMC_RES#-A	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A
72	TRDATA5/P74/A20/CS4#/PO19/ ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1
73	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
74	VCC	VCC
75	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
76	VSS	VSS
77	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4/P73/CS3#/PO16/ET0_WOL
78	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
79	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B*[1]	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
81	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B*[1]	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B

144-Pin LFQFP	RX65N	RX66N
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/ LCD_TCON1-B*1	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
83	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/ LCD_TCON2-B*1	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/SS4#/CTS6#/RTS6#/SS6#/ ET0_RX_CLK/REF50CK0/LCD_TCON2-B
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/LCD_TCON3-B*1/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS
85	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC/PMGI0_MDC
86	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO
87	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ LCD_DATA0-B*1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ ET0_ERXD1/RMII0_RXD1/LCD_DATA0-B/ IRQ12
88	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/ LCD_DATA1-B*1	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B*1	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
90	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B*1	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B*1/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B*1/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
95	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B*1	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
96	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/ LCD_DATA7-B*1/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
97	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B*1	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
98	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/ CRX2/IRQ15
99	P66/DQM0/CS6#/MTIOC7D	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2
100	P65/CKE/CS5#	P65/CKE/CS5#
101	PE7/D15[A15/D15]/D7[A7/D7]*1/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B*1/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105

144-Pin LFQFP	RX65N	RX66N
102	PE6/D14[A14/D14]/D6[A6/D6]*1/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B*1/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
103	VCC	VCC
104	P70/SDCLK	P70/SDCLK
105	VSS	VSS
106	PE5/D13[A13/D13]/D5[A5/D5]*1/ MTIOC4C/MTIOC2B/ET0_RX_CLK/ REF50CK0/RSPCKB-B/ LCD_DATA11-B*1/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
107	PE4/D12[A12/D12]/D4[A4/D4]*1/ MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/ SSLB0-B/LCD_DATA12-B*1/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
108	PE3/D11[A11/D11]/D3[A3/D3]*1/ MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/ CTS12#/RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B*1/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
109	PE2/D10[A10/D10]/D2[A2/D2]*1/ MTIOC4A/PO23/TIC3/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B*1/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
110	PE1/D9[A9/D9]/D1[A1/D1]*1/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B*1/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2-B/ MMC_D5-B/LCD_DATA15-B/ANEX1
111	PE0/D8[A8/D8]/D0[A0/D0]*1/MTIOC3D/ SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B*1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
112	P64/WE#/D3[A3/D3]*1/CS4#	P64/WE#/D3[A3/D3]/CS4#
113	P63/CAS#/D2[A2/D2]*1/CS3#	P63/CAS#/D2[A2/D2]/CS3#
114	P62/RAS#/D1[A1/D1]*1/CS2#	P62/RAS#/D1[A1/D1]/CS2#
115	P61/SDCS#/D0[A0/D0]*1/CS1#	P61/SDCS#/D0[A0/D0]/CS1#
116	VSS	VSS
117	P60/CS0#	P60/CS0#
118	VCC	VCC
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B*1/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
120	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B*1/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
121	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B*1/IRQ5/ AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
122	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B*1/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112

144-Pin LFQFP	RX65N	RX66N
123	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B*1/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
124	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B*1/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
125	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ CTX0/LCD_DATA23-B*1/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
126	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B*1/ IRQ0/AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
127	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
128	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
129	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
130	VSS	VSS
131	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/AN114
132	VCC	VCC
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. Valid only on products with a code flash memory capacity of 2 MB or 1.5 MB.
2. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.5 100-Pin LFQFP Package

Table 3.5 is a comparative listing of the pin functions of 100-pin LFQFP package products.

Table 3.5 Comparative Listing of 100-Pin LFQFP Package Pin Functions

100-Pin LFQFP	RX65N	RX66N
1	AVCC1	AVCC1
2	EMLE	EMLE
3	AVSS1	AVSS1
4	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/ SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ ET0_EXOUT
5	VCL	VCL
6	VBATT	VBATT
7	MD/FINED	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	UPSEL/P35/NMI	UPSEL/P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS
21	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A
23	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ ADTRG0#	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/ SSCL3/SSIDATA1/ADTRG0#
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SSIBCK1

100-Pin LFQFP	RX65N	RX66N
25	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/CTX1/SSIBCK0
26	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/ USB0_OVRCURB/AUDIO_CLK
27	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1*1/ USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/GTIOC2A/RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSILRCK0/SCL1/IRQ9
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1*1/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/SDA1/ IRQ8
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/ SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/ SSITXD0/IRQ7/ADTRG1#
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1-DS/SSILRCK1/IRQ5
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/ SS1#/CTX1/USB0_OVRCURA/IRQ4
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/IRQ3/ADTRG1#
34	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/GTADSM0/RXD2/SMISO2/ SSCL2/SCL0[FM+]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	USB0_DM
37	USB0_DP	USB0_DP
38	VSS_USB	VSS_USB
39	P55/D0[A0/D0]*1/WAIT#/EDREQ0/ MTIOC4D/TMO3/ET0_EXOUT/CRX1/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10
40	P54/ALE/D1[A1/D1]*1/EDACK0/MTIOC4B/ TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/ CTX1	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA
41	P53*2/BCLK	P53*2/BCLK
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/GTIOC3A/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/ET0_COL/IRQ14

100-Pin LFQFP	RX65N	RX66N
46	PC6/D2[A2/D2]*1/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/GTIOC3B/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/ET0_ETXD3/IRQ13
47	PC5/D3[A3/D3]*1/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/PO29/ ET0_ETXD2/SCK8/SCK10/RSPCKA-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/ RTS8#/SCK10/RSPCKA-A/ET0_ETXD2
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/CTS8#/ SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK
49	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ ET0_RX_DV
51	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12
52	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV
54	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B*1	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/LCD_CLK-B
56	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B*1	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/ SS11#/CTS11#/RTS11#/ET0_TX_EN/ RMII0_TXD_EN/LCD_TCON0-B
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK6/SDSI_D3-B/ LCD_TCON1-B*1	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ ET0_RX_ER/RMII0_RX_ER/LCD_TCON1-B
58	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS6#/RTS6#/ SS6#/SDSI_D2-B/LCD_TCON2-B*1	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/ET0_RX_CLK/REF50CK0/ LCD_TCON2-B
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD6/SMOSI6/SSDA6/LCD_TCON3-B*1/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ ET0_ERXD0/RMII0_RXD0/LCD_TCON3-B/ IRQ4-DS
60	VCC	VCC

100-Pin LFQFP	RX65N	RX66N
61	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD6/SMISO6/ SSCL6/LCD_DATA0-B*1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/ LCD_DATA1-B*1	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/ SS5#/MOSIA-B/LCD_DATA2-B*1	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/ SS5#/MOSIA-B/ET0_EXOUT/LCD_DATA2-B
65	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B*1	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B*1/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/PMGI0_MDC/LCD_DATA4-B/ IRQ5-DS
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B*1/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS
68	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B*1	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/ LCD_DATA7-B*1/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11
70	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B*1	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B
71	PE7/D15[A15/D15]/D7[A7/D7]*1/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B*1/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/GTIOC3A/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
72	PE6/D14[A14/D14]/D6[A6/D6]*1/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B*1/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/GTIOC3B/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
73	PE5/D13[A13/D13]/D5[A5/D5]*1/MTIOC4C/ MTIOC2B/ET0_RX_CLK/REF50CK0/ RSPCKB-B/LCD_DATA11-B*1/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ ET0_RX_CLK/REF50CK0/LCD_DATA11-B/ IRQ5/AN103
74	PE4/D12[A12/D12]/D4[A4/D4]*1/MTIOC4D/ MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/ LCD_DATA12-B*1/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102
75	PE3/D11[A11/D11]/D3[A3/D3]*1/MTIOC4B/ PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/ RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B*1/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/TOC3/POE8#/GTIOC2A/CTS12#/ RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101
76	PE2/D10[A10/D10]/D2[A2/D2]*1/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B*1/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/GTIOC0B/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100

100-Pin LFQFP	RX65N	RX66N
77	PE1/D9[A9/D9]/D1[A1/D1]*1/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B*1/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/GTIOC1B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/LCD_DATA15-B/ ANEX1
78	PE0/D8[A8/D8]/D0[A0/D0]*1/MTIOC3D/ SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B*1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
79	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B*1/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107
80	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B*1/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
81	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B*1/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ MTCLKA/POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/ IRQ5/AN113
82	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B*1/IRQ4/ AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
83	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B*1/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
84	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B*1/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/ MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
85	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ CTX0/LCD_DATA23-B*1/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/ AN109
86	PD0/D0[A0/D0]/POE4#/ LCD_EXTCLK-B*1/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/SSILRCK1/IRQ13/DA1

Notes: 1. Valid only on products with a code flash memory capacity of 2 MB or 1.5 MB.
2. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

4. Notes on Migration

This section presents important information regarding differences between the RX66N Group and RX65N Group.

4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

4.1.1 Serial Communication Interface RTS8# Pin

The RTS8# pin of the serial communication interface is assigned to PC4 on the RX65N Group and multiplexed to PC5 and PK3 on the RX66N Group. Bear this in mind when designing your system.

4.1.2 Serial Communication Interface RTS9# Pin

The RTS9# pin of the serial communication interface is assigned to PB4 on the RX65N Group and multiplexed to PB5 and PL3 on the RX66N Group. Bear this in mind when designing your system.

4.2 Notes on Functional Design

Some software that runs on the RX65N Group is compatible with the RX66N Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX66N Group and RX65N Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.2.1 Running RAM Self-Diagnostics on Register Save Banks

On the RX66N Group the register save banks are configured in the RAM. The register save banks are buffered, so writing to a bank with the SAVE instruction and then reading from the same bank with the RSTR instruction immediately afterwards may result in data being read from the buffer rather than from the RAM memory cells. When running RAM self-diagnostics on a register save bank, follow the steps below to ensure that the previously written data is read from the RAM rather than from the buffer.

(1) Use the SAVE instruction to write data to the bank on which self-diagnostics will be run.
(2) Use the SAVE instruction to write data to a bank other than that written to in step (1).
(3) Use the RSTR instruction to read data from the bank written to in step (1).

4.2.2 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the MCU, but this processing it not needed on the RX66N Group.

4.2.3 Clock Frequency Restrictions When Using ETHERC

When using the ETHERC on the RX65N Group the clock frequency is restricted to the range "12.5 MHz ≤ PCLKA ≤ 120 MHz" and the PCLKA frequency must equal the ICLK frequency, but on the RX66N Group it is not necessary that the PCLKA frequency be equal to the ICLK frequency.

4.2.4 Clock Frequency Settings

The RX65N Group and the RX66N Group have different limits on clock frequency settings. Refer to Table 4.1 for details.

Table 4.1 Comparison of Limits on Clock Frequency Settings

Item	RX65N	RX66N
Clock frequency setting limits	ICLK ≥ BCLK PCLKA ≥ PCLKB PCLKB ≥ PCLKC PCLKB ≥ PCLKD	ICLK ≥ BCLK PCLKA ≥ PCLKB PCLKB ≥ PCLKC PCLKB ≥ PCLKD
Clock frequency ratio limits	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N ICLK:BCLK = N:1

4.2.5 Note on Changing the ICLK Frequency

On the RX66N Group, when changing the ICLK frequency from less than 70 MHz to 70 MHz or higher, and if the ratio of the frequencies before and after the change is greater than 4×, it is necessary to set the frequency once to 1/4 of the frequency after the change, wait 3 µs, and then set the target frequency.

In addition, when changing the ICLK frequency from 70 MHz or higher to less than 70 MHz, and if the ratio of the frequencies before and after the change is less than 1/4, it is necessary to set the frequency once to 1/4 of the frequency before the change, wait 3 µs, and then set the target frequency.

4.2.6 Note on Software Reset of ETHERC and EDMAC

On the RX66N Group the data in the address range from 0000 0000h to 0000 001Fh may be corrupted if 1 is written to the EDMR.SWR bit while the EDMAC is operating. Do not use the address range from 0000 0000h to 0000 001Fh while the Ethernet controller is in use.

4.2.7 Initialization of the Port Direction Register (PDR)

Initialization of the PDR registers differs even when using RX66N Group or RX65N/RX651 Group products with the same pin count.

5. Reference Documents

User's Manual: Hardware

RX65N Group, RX651 Group User's Manual: Hardware, Rev. 2.30 (R01UH0590EJ0230)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface,
Rev. 2.10 (R01UH0602EJ0210)
(The latest version can be downloaded from the Renesas Electronics website.)

RX66N Group User's Manual: Hardware, Rev. 1.00 (R01UH0825EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

TN-RX*-A0215A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 16, 2019	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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