RX24T/RX24U Group, RX23T Group

Differences Between the RX24T/RX24U Group and the RX23T Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX24T/RX24U Group and RX23T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX24T Group, the 144-pin package version of the RX24U Group, and the 64-pin package version of the RX23T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX24T Group, RX24U Group, and RX23T Group

Contents

1. Comparison of Built-In Functions of RX24T/RX24U Group and RX23T Group

A comparison of the built-in functions of the RX24T/RX24U Group and RX23T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX24T/RX24U Group and RX23T Group.

Table 1.1 Comparison of Built-In Functions of RX24T/RX24U Group and RX23T Group

Function	RX23T	RX24T Chip Version A	RX24T Chip Version B	RX24U
CPU	●			
Operating modes	○			
Address space	▲			
Resets	○			
Option-setting memory	●			
Voltage detection circuit (LVDAb)	▲			
Clock generation circuit	●			
Clock frequency accuracy measurement circuit (CAC)	○			
Low power consumption	●			
Register write protection function	●			
Exception handling	○			
Interrupt controller (ICUb)	●			
Buses	●			
Memory-protection unit (MPU)	○			
Data transfer controller (DTCa)	○			
I/O ports	●			
Multi-function pin controller (MPC)	●			
Multi-function timer pulse unit 3 (MTU3c): RX23T, (MTU3d): RX24T/RX24U	●			
Port output enable 3 (POE3b): RX23T, (POE3b, POE3A): RX24T, (POE3A): RX24U	●*1			
General PWM timer (GPTB)	×		○	
8-bit timer (TMR)	●			
Compare match timer (CMT)	○			
Independent watchdog timer (IWDTa)	○			
Serial communications interface (SCIg)	●			
I²C bus interface (RIICa)	○			
CAN module (RSCAN)	×		○	
Serial peripheral interface (RSPIa): RX23T, (RSPIb): RX24T/RX24U	●			
CRC calculator (CRC)	○			
12-bit A/D converter (S12ADE): RX23T, (S12ADF): RX24T/RX24U	●			
D/A converter for generating comparator C reference voltage (DA): RX23T, D/A converter (DA, DAa): RX24T, (DAa): RX24U	●*2			
Comparator C (CMPC)	●			
Data operation circuit (DOC)	○			
RAM	●			
Flash memory	●			
Packages	●/■			

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Notes: 1. On the RX24T Group, chip version A is provided with the POE3b and chip version B with the POE3A.
2. On the RX24T Group, chip version A is provided with the DA and chip version B with the DAa.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX23T	RX24T/RX24U
CPU	• Maximum operating frequency: 40 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU) • ROM cache: 2 KB (disabled by default)
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

2.2 Address space

Figure 2.1 is a comparative memory map of single-chip mode.

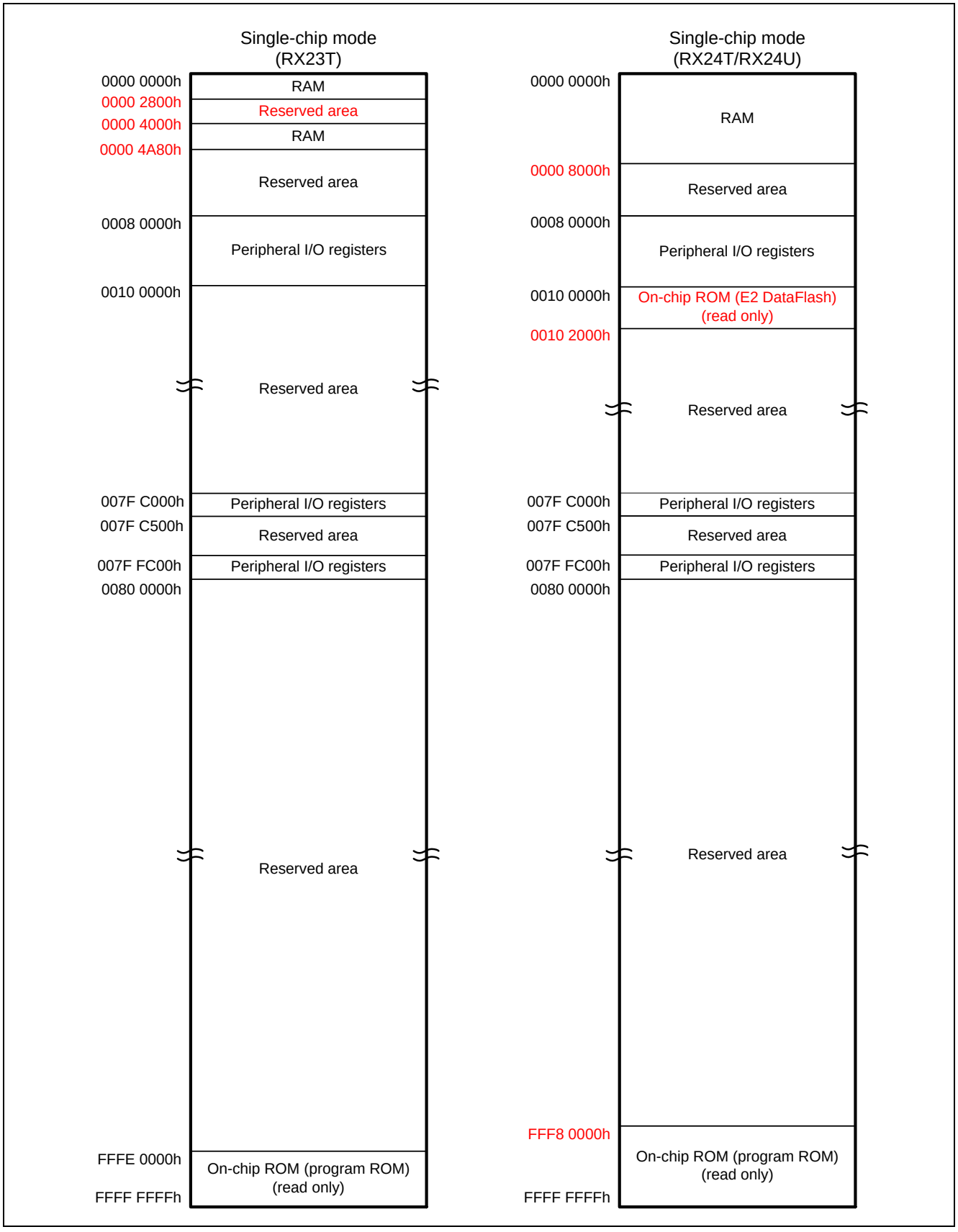

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Option-Setting Memory

Table 2.2 is a comparison of option-setting memory registers.

Table 2.2 Comparison of Option-Setting Memory Registers

Register	Bit	RX23T	RX24T/RX24U
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 1 0: 2.51 V is selected Do not set a value other than those above when using the voltage detection 0 circuit.	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Do not set a value other than those above when using the voltage detection 0 circuit.

2.4 Voltage Detection Circuit

Table 2.3 is a comparative overview of the voltage detection circuits.

Table 2.3 Comparative Overview of Voltage Detection Circuits

Item		RX23T (LVDAb)			RX24T (LVDAb)/RX24U (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	Voltage selectable from two levels using OFS1 register	Voltage selectable from nine levels using the LVDLVLR.LVD1 LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2 LVL[1:0] bits	Voltage selectable from three levels using OFS1 register	Voltage selectable from nine levels using the LVDLVLR.LVD1 LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2 LVL[1:0] bits
	Monitor flag	—	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection		LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable is selectable	Non-maskable or maskable is selectable		Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either

2.5 Clock Generation Circuit

Table 2.4 is a comparative overview of the clock generation circuits, and Table 2.5 is a comparison of clock generation circuit registers.

Table 2.4 Comparative Overview of Clock Generation Circuits

Item	RX23T	RX24T	RX24U
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules. The peripheral module clock (PCLKA) is the operating clock for the MTU3, the peripheral module clock (PCLKD) is the operating clock for the S12AD, and the peripheral module clock (PCLKB) is the operating clock for modules other MTU3 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules. The peripheral module clock (PCLKA) is the operating clock for the MTU and GPT, the peripheral module clock (PCLKD) is the operating clock for the S12AD, and the peripheral module clock (PCLKB) is the operating clock for the other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules. The peripheral module clock (PCLKA) is the operating clock for the MTU, GPT, and SCI11, the peripheral module clock (PCLKD) is the operating clock for the S12AD, and the peripheral module clock (PCLKB) is the operating clock for the other modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN.
Operating frequency	• ICLK: 40 MHz (max.) • PCLKA: 40 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 to 32 MHz (ROM) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 to 32 MHz (ROM) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 to 32 MHz (ROM) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)

Item	RX23T	RX24T	RX24U
Main clock oscillator	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU and GPT pin output is stopped. • Drive capacity switching function	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU and GPT pin output is stopped. • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 10 (increments of 0.5) • Oscillation frequency: 24 to 40 MHz	• Input clock source: Main clock, and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 40 to 80 MHz	• Input clock source: Main clock, and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 40 to 80 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 32 MHz, 64 MHz	Oscillation frequency: 32 MHz, 64 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Table 2.5 Comparison of Clock Generation Circuit Registers

Register	Bit	RX23T	RX24T/RX24U
SCKCR	—	Reserved bits (b19 to b16) Set these bits to match the setting value of the ICK[3:0] or PCKB[3:0] bits, whichever corresponds to a higher frequency.	Reserved bits (b19 to b16) Set these bits to match the setting value of the PCKB[3:0] bits.
PLLCR	PLLSRCSEL	—	PLL clock source selection bit
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5 Settings other than the above are prohibited.
HOCOCR2	—	—	High-speed on-chip oscillator control register 2

Register	Bit	RX23T	RX24T/RX24U
HOCOWTCR	HSTS[2:0]	High-speed on-chip oscillator oscillation stabilization wait time setting bits b2 b0 1 0 0: Wait time = 78 cycles 1 0 1: Wait time = 142 cycles Settings other than the above are prohibited.	High-speed on-chip oscillator oscillation stabilization wait time setting bits b2 b0 1 0 1: Wait time = 142 cycles (when HOCO oscillation frequency is set to 32 MHz) 1 1 0: Wait time = 270 cycles (when HOCO oscillation frequency is set to 64 MHz) Settings other than the above are prohibited.
MEMWAIT	MEMWAIT (RX23T) MEMWAIT[1:0] (RX24T/RX24U)	Memory wait cycle setting bits (b0) 0 0: No wait states 0 1: Wait states	Memory wait cycle setting bits (b1 and b0) 0 0: No wait states 0 1: Wait states (ICLK ≤ 64 MHz) 1 0: Wait states (ICLK ≤ 80 MHz) Settings other than the above are prohibited.

2.6 Low Power Consumption

Table 2.6 is a comparison of low power consumption registers.

Table 2.6 Comparison of Low Power Consumption Registers

Register	Bit	RX23T	RX24T	RX24U
MSTPCRA	MSTPA2	—	8-bit timer 7 and 6 (unit 3) module stop bit	8-bit timer 7 and 6 (unit 3) module stop bit
	MSTPA3	—	8-bit timer 5 and 4 (unit 2) module stop bit	8-bit timer 5 and 4 (unit 2) module stop bit
	MSTPA7	—	General PWM timer module stop bit	General PWM timer module stop bit
	MSTPA16	—	12-bit A/D converter 1 module stop bit	12-bit A/D converter 1 module stop bit
	MSTPA23	—	12-bit A/D converter 2 module stop bit	12-bit A/D converter 2 module stop bit
MSTPCRB	MSTPB0	—	RSCAN module stop bit*1	RSCAN module stop bit*1
	MSTPB25	—	Serial communication interface 6 module stop bit	Serial communication interface 6 module stop bit
MSTPCRC	MSTPC24	—	—	Serial communication interface 11 module stop bit
	MSTPC26	—	—	Serial communication interface 9 module stop bit
	MSTPC27	—	—	Serial communication interface 8 module stop bit

Note: 1. Overwrite this bit when the oscillation of the clock controlled by it is stable. Before entering software standby mode after overwriting this bit, wait 2 cycles of CANMCLK after overwriting, and execute a WAIT instruction.

2.7 Register Write Protection Function

Table 2.7 is a comparative overview of the register write protection functions.

Table 2.7 Comparative Overview of Register Write Protection Functions

Item	RX23T	RX24T/RX24U
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, MEMWAIT	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the clock generation circuit: HOCOWTCR	Registers related to the clock generation circuit: HOCOWTCR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.8 Interrupt Controller

Table 2.8 is a comparative overview of interrupt controller, and Table 2.9 is a comparison of interrupt controller registers.

Table 2.8 Comparative Overview of Interrupt Controller

Item		RX23T (ICUb)	RX24T (ICUb)/RX24U (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ5 • Number of sources: 6 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • One interrupt source	• Interrupt generated by writing to a register. • One interrupt source
	Interrupt priority level	Specified by registers.	Specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC control	The DTC can be activated by interrupt sources.	The DTC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item	RX23T (ICUb)	RX24T (ICUb)/RX24U (ICUb)
Return from low power consumption modes	• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts and interrupts IRQ0 to IRQ5.	• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts and interrupts IRQ0 to IRQ7.

Table 2.9 Comparison of Interrupt Controller Registers

Register	Bit	RX23T (ICUb)	RX24T (ICUb)	RX24U (ICUb)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 253)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 250)
DTCERn*1	—	DTC activation enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 027 to 252)
IRQCRi		IRQ control register i (i = 0 to 5)	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0 to 7)
IRQFLTE0	FLTEN6	—	IRQ6 digital filter enable bit	IRQ6 digital filter enable bit
	FLTEN7	—	IRQ7 digital filter enable bit	IRQ7 digital filter enable bit
IRQFLTC0	FCLKSEL6 [1:0]	—	IRQ6 digital filter sampling clock setting bits	IRQ6 digital filter sampling clock setting bits
	FCLKSEL7 [1:0]	—	IRQ7 digital filter sampling clock setting bits	IRQ7 digital filter sampling clock setting bits

Note: 1. On the RX23T Group and RX24T Group n = 250 to 255, and on the RX24U Group n = 254 and 255, are reserved areas.

2.9 Buses

Table 2.10 is a comparative overview of the buses.

Table 2.10 Comparative Overview of Buses

Bus Type		RX23T	RX24T	RX24U
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)

Bus Type		RX23T	RX24T	RX24U
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (RSCAN and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (RSCAN and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU and GPT) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, GPT, and SCI11) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to the flash control module • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to the flash control module and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to the flash control module and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)

2.10 I/O Ports

Table 2.11 is a comparative overview of the I/O ports of 100-pin products, and Table 2.12 is a comparative overview of the I/O ports of 64-pin products. Table 2.13 is a comparison of I/O port functions, and Table 2.14 is a comparison of I/O port registers.

Table 2.11 Comparative Overview of I/O Ports of 100-Pin Products

Port Symbol	RX24T (100-Pin)	RX24U (100-Pin)
PORT0	P00 to P02	P00 to P02
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5

Table 2.12 Comparative Overview of I/O Ports of 64-Pin Products

Port Symbol	RX23T (64-Pin)	RX24T (64-Pin)
PORT0	P00 to P02	P00 to P02
PORT1	P10, P11	P11
PORT2	P22 to P24	P21 to P24
PORT3	P30 to P33, P36, P37	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P42, P44 to P46
PORT5	—	P50 to P54
PORT7	P70 to P76	P70 to P76
PORT9	P91 to P94	P90 to P96
PORTA	PA2 to PA5	—
PORTB	PB0 to PB7	PB1 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2

Table 2.13 Comparison of I/O Port Functions

Item	Port Symbol	RX23T	RX24T	RX24U
Input pull-up function	PORT0	P00 to P02	P00 to P02	P00 to P02
	PORT1	P10, P11	P10, P11	P10 to P17
	PORT2	P22 to P24	P20 to P24	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P37
	PORT4	P40 to P47	P40 to P47	P40 to P47
	PORT5	—	P50 to P55	P50 to P55
	PORT6	—	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	—	P80 to P82	P80 to P84
	PORT9	P91 to P94	P90 to P96	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA5	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	—	PC0 to PC6
	PORTD	PD3 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6
	PORTF	—	—	PF0 to PF3
	PORTG	—	—	PG0 to PG2
Open-drain output function	PORT0	P00 to P02	P00 to P02	P00 to P02
	PORT1	P10, P11	P10, P11	P10 to P17
	PORT2	P22 to P24	P20 to P24	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P37
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	—	P80 to P82	P80 to P84
	PORT9	P91 to P94	P90 to P96	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA5	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	—	PC0 to PC6
	PORTD	PD3 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6
	PORTF	—	—	PF0 to PF3
	PORTG	—	—	PG0 to PG2
Drive capacity switching function	PORT0	P00 to P02	P00 to P02	P00 to P02
	PORT1	P10, P11	P10, P11	P10 to P17
	PORT2	P22 to P24	P20 to P24	P20 to P27
	PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P37
	PORT4	P40 to P47	P40 to P47	P40 to P47
	PORT5	—	P50 to P55	P50 to P55
	PORT6	—	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	—	P80 to P82	P80 to P84
	PORT9	P91 to P94	P90 to P96	P90 to P96
	PORTA	PA2 to PA5	PA0 to PA5	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	—	PC0 to PC6
	PORTD	PD3 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6
	PORTF	—	—	PF0 to PF3
	PORTG	—	—	PG0 to PG2

Item	Port Symbol	RX23T	RX24T	RX24U
Large-voltage pins	PORT7	P71 to P76	P71 to P76	P71 to P76
	PORT8	—	P81	P81
	PORT9	—	P90 to P95	P90 to P95
	PORTB	PB5	PB5	PB5
	PORTD	PD3	PD3	PD3
5 V tolerant	PORTB	PB1, PB2	PB1, PB2	PB1, PB2

Table 2.14 Comparison of I/O Port Registers

Register	Bit	RX23T	RX24T	RX24U
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 4, 7, 9, A, B, D, E)	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 bits (m = 0 to 9, A to G)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7, 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7 to 9, A to G)
ODR0	B0	Pm0 output type select bit (m = 0 to 3, 7, 9, A, B, D)	Pm0 output type select bit (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 output type select bit (m = 0 to 3, 7 to 9, A to G)
	B2	Pm1 output type select bit (m = 0 to 3, 7, 9, A, B, D)	Pm1 output type select bit (m = 0 to 3, 7 to 9, A, B, D, E)	Pm1 output type select bit (m = 0 to 3, 7 to 9, A to G)
	B4	Pm2 output type select bit (m = 0 to 3, 7, 9, A, B, D)	Pm2 output type select bit (m = 0 to 3, 7 to 9, A, B, D, E)	Pm2 output type select bit (m = 0 to 3, 7 to 9, A to G)
	B6	Pm3 output type select bit (m = 0 to 3, 7, 9, A, B, D)	Pm3 output type select bit (m = 0 to 3, 7 to 9, A, B, D, E)	Pm3 output type select bit (m = 0 to 3, 7 to 9, A to G)
ODR1	B0	Pm4 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm4 output type select bit (m = 2, 7, 9, A, B, D, E)	Pm4 output type select bit (m = 1 to 3, 7 to 9, A to E)
	B2	Pm5 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm5 output type select bit (m = 2, 7, 9, A, B, D, E)	Pm5 output type select bit (m = 1 to 3, 7 to 9, A to E)
	B4	Pm6 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm6 output type select bit (m = 2, 7, 9, A, B, D, E)	Pm6 output type select bit (m = 1 to 3, 7 to 9, A to E)
	B6	Pm7 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm7 output type select bit (m = 2, 7, 9, A, B, D, E)	Pm7 output type select bit (m = 1 to 3, 7 to 9, A to E)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7, 9, A, B, D)	Pm0 to Pm7 drive capacity control bits (m =0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A to G)

2.11 Multi-Function Pin Controller

Table 2.15 and Table 2.16 are comparisons of the assignments of multiplexed pins, and Table 2.17 to Table 2.33 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist only on the comparison source (100-pin: RX24T Group, 64-pin: RX23T Group) and **orange text** pins that exist only on the comparison target (100-pin: RX24U Group, 64-pin: RX24T Group). A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.15 Comparison of Multiplexed Pin Assignments (100-Pin)

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin
Interrupt	IRQ0 (input)	P10	○	○	○
		P52	○	○	○
		PE5	○	○	○
	IRQ1 (input)	P11	○	○	○
		P53	○	○	○
		PA5	○	○	○
		PE4	○	○	○
	IRQ2 (input)	P00	○	○	○
		P54	○	○	○
		PD4	○	○	○
		PE3	○	○	○
	IRQ3 (input)	P55	○	○	○
		PB4	○	○	○
		PD5	○	○	○
	IRQ4 (input)	P01	○	○	○
		P60	○	○	○
		P96	○	○	○
	IRQ5 (input)	P02	○	○	○
		P61	○	○	○
		P70	○	○	○
		PB6	○	○	○
		PD6	○	○	○
	IRQ6 (input)	P21	○	○	○
		P31	○	○	○
		P62	○	○	○
	IRQ7 (input)	P20	○	○	○
		P30	○	○	○
		P63	○	○	○
	NMI (input)	PE2	○	○	○
Multi-function timer unit 3	MTIOC0A (input/output) / MTIOC0A# (input/output)	P31	○	○	○
		PB3	○	○	○
	MTIOC0B (input/output) / MTIOC0B# (input/output)	P30	○	○	○
		PB2	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
Multi-function timer unit 3	MTIOC0C (input/output) / MTIOC0C# (input/output)	PB1	○	○	○
	MTIOC0D (input/output) / MTIOC0D# (input/output)	PB0	○	○	○
	MTIOC1A (input/output) / MTIOC1A# (input/output)	PA5	○	○	○
		P27	×	×	○
	MTIOC1B (input/output) / MTIOC1B# (input/output)	PA4	○	○	○
	MTIOC2A (input/output) / MTIOC2A# (input/output)	PA3	○	○	○
	MTIOC2B (input/output) / MTIOC2B# (input/output)	PA2	○	○	○
	MTIOC3A (input/output) / MTIOC3A# (input/output)	P11	○	○	○
		P33	○	○	○
	MTIOC3B (input/output) / MTIOC3B# (input/output)	P71	○	○	○
	MTIOC3C (input/output) / MTIOC3C# (input/output)	P32	○	○	○
	MTIOC3D (input/output) / MTIOC3D# (input/output)	P74	○	○	○
	MTIOC4A (input/output) / MTIOC4A# (input/output)	P72	○	○	○
	MTIOC4B (input/output) / MTIOC4B# (input/output)	P73	○	○	○
	MTIOC4C (input/output) / MTIOC4C# (input/output)	P75	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
Multi-function timer unit 3	MTIOC4D (input/output) / MTIOC4D# (input/output)	P76	○	○	○
	MTIC5U (input) / MTIC5U# (input)	P24	○	○	○
		P82	○	○	○
	MTIC5V (input) / MTIC5V# (input)	P23	○	○	○
		P81	○	○	○
	MTIC5W (input) / MTIC5W# (input)	P22	○	○	○
		P80	○	○	○
	MTIOC6A (input/output) / MTIOC6A# (input/output)	PA1	○	○	○
	MTIOC6B (input/output) / MTIOC6B# (input/output)	P95	○	○	○
	MTIOC6C (input/output) / MTIOC6C# (input/output)	PA0	○	○	○
	MTIOC6D (input/output) / MTIOC6D# (input/output)	P92	○	○	○
	MTIOC7A (input/output) / MTIOC7A# (input/output)	P94	○	○	○
	MTIOC7B (input/output) / MTIOC7B# (input/output)	P93	○	○	○
	MTIOC7C (input/output) / MTIOC7C# (input/output)	P91	○	○	○
	MTIOC7D (input/output) / MTIOC7D# (input/output)	P90	○	○	○
	MTIOC9A (input/output) / MTIOC9A# (input/output)	P21	○	○	○
		PD7	○	○	○
	MTIOC9B (input/output) / MTIOC9B# (input/output)	P10	○	○	○
		PE0	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
Multi-function timer unit 3	MTIOC9C (input/output) / MTIOC9C# (input/output)	P20	○	○	○
		PD6	○	○	○
	MTIOC9D (input/output) / MTIOC9D# (input/output)	P02	○	○	○
		PE1	○	○	○
	MTCLKA (input) / MTCLKA# (input)	P21	○	○	○
		P33	○	○	○
	MTCLKB (input) / MTCLKB# (input)	P20	○	○	○
		P32	○	○	○
	MTCLKC (input) / MTCLKC# (input)	P11	○	○	○
		P31	○	○	○
		PE4	○	○	○
	MTCLKD (input) / MTCLKD# (input)	P10	○	○	○
		P30	○	○	○
		PE3	○	○	○
	ADSM0 (output)	PB2	○	○	○
	ADSM1 (output)	PB1	○	○	○
General PWM timer	GTIOC0A (input/output) / GTIOC0A# (input/output)	P71		○	○
		PD2		○	○
	GTIOC0B (input/output) / GTIOC0B# (input/output)	P74		○	○
		PD1		○	○
	GTIOC1A (input/output) / GTIOC1A# (input/output)	P72		○	○
		PD0		○	○
	GTIOC1B (input/output) / GTIOC1B# (input/output)	P75		○	○
		PB7		○	○
	GTIOC2A (input/output) / GTIOC2A# (input/output)	P73		○	○
		PB6		○	○
	GTIOC2B (input/output) / GTIOC2B# (input/output)	P76		○	○
		PB5		○	○
	GTIOC3A (input/output) / GTIOC3A# (input/output)	PD7		○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
General PWM timer	GTIOC3B (input/output) / GTIOC3B# (input/output)	PD6		○	○
	GTECLKA (input)	PD5		○	○
	GTECLKB (input)	PD4		○	○
	GTECLKC (input)	PD3		○	○
	GTECLKD (input)	PB4		○	○
	GTETRG (input)	PB4		○	○
	GTADSM0 (output)	PA3		○	○
	GTADSM1 (output)	PA2		○	○
8-bit timer	TMO0 (output)	PD3	○	○	○
		P33	○	○	○
		PB0	○	○	○
	TMCI0 (input)	PD4	○	○	○
		PB1	○	○	○
	TMRI0 (input)	PD5	○	○	○
		PB2	○	○	○
	TMO1 (output)	PD6	○	○	○
	TMCI1 (input)	PD2	○	○	○
		PE0	○	○	○
	TMRI1 (input)	PD7	○	○	○
	TMO2 (output)	P23	○	○	○
		PA0	○	○	○
		PD1	○	○	○
	TMCI2 (input)	P24	○	○	○
	TMRI2 (input)	P22	○	○	○
	TMO3 (output)	P11	○	○	○
	TMCI3 (input)	PA5	○	○	○
	TMRI3 (input)	P10	○	○	○
	TMO4 (output)	P22	○	○	○
		P82	○	○	○
		PA1	○	○	○
		PD2	○	○	○
	TMCI4 (input)	P21	○	○	○
		P81	○	○	○
	TMRI4 (input)	P20	○	○	○
		P80	○	○	○
	TMO5 (output)	PE1	○	○	○
	TMCI5 (input)	PE0	○	○	○
	TMRI5 (input)	PD7	○	○	○
	TMO6 (output)	P24	○	○	○
		P32	○	○	○
		PD0	○	○	○
	TMCI6 (input)	P30	○	○	○
		PD4	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
8-bit timer	TMRI6 (input)	P31	○	○	○
		PD5	○	○	○
	TMO7 (output)	PA2	○	○	○
	TMCI7 (input)	PA4	○	○	○
	TMRI7 (input)	PA3	○	○	○
CAN module	CTXD0 (output)	PA0		○	○
	CRXD0 (input)	PA1		○	○
Port output enable 3	POE0# (input)	P70	○	○	○
	POE4# (input)	P96	○	○	○
	POE8# (input)	PB4	○	○	○
	POE10# (input)	PE2	○	○	○
		PE4	○	○	○
	POE11# (input)	PE3	○	○	○
	POE12# (input)	P01	○	○	○
		P10	○	○	○
Serial communications interface	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	PD5	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	PD3	○	○	○
	SCK1 (input/output)	PD4	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P02	○	○	○
		PD6	○	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PB6	○	○	○
		PE0	×	○	○
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PB5	○	○	○
		PD7	×	○	○
	SCK5 (input/output)	PB7	○	○	○
		PD2	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PB4	○	○	○
		PE1	○	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	P80	○	○	○
		PA5	○	○	○
		PB1	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
Serial communications interface	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P81	○	○	○
		PB0	○	○	○
		PB2	○	○	○
	SCK6 (input/output)	P82	○	○	○
		PA4	○	○	○
		PB3	○	○	○
	CTS6# (input) / RTS6# (output) / SS6# (input)	P10	○	○	○
		PA2	○	○	○
	RXD11 (input) / SMISO11 (input/output) / SSCL11 (input/output)	PD5			○
	TXD11 (output) / SMOSI11 (input/output) / SSDA11 (input/output)	PD3			○
	SCK11 (input/output)	PD4			○
	CTS11# (input) / RTS11# (output) / SS11# (input)	PD6			○
I²C bus interface	SCL0 (input/output)	PB1	○	○	○
	SDA0 (input/output)	PB2	○	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○	○	○
		PA4	○	○	○
		PB3	○	○	○
		PD0	○	○	○
	MOSIA (input/output)	P23	○	○	○
		PB0	○	○	○
		PD2	○	○	○
	MISOA (input/output)	P22	○	○	○
		PA5	○	○	○
		PD1	○	○	○
	SSLA0 (input/output)	P30	○	○	○
		PA3	○	○	○
		PD6	○	○	○
	SSLA1 (output)	P31	○	○	○
		PA2	○	○	○
		PD7	○	○	○
	SSLA2 (output)	P32	○	○	○
		PA1	○	○	○
		PE0	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
Serial peripheral interface	SSLA3 (output)	P33	○	○	○
		PA0	○	○	○
		PE1	○	○	○
12-bit A/D converter	AN000 (input)	P40	○	○	○
	AN001 (input)	P41	○	○	○
	AN002 (input)	P42	○	○	○
	AN003 (input)	P43	○	○	○
	AN016 (input)	P20	○	○	○
	AN100 (input)	P44	○	○	○
	AN101 (input)	P45	○	○	○
	AN102 (input)	P46	○	○	○
	AN103 (input)	P47	○	○	○
	AN116 (input)	P21	○	○	○
	AN200 (input)	P60	○	○	○
	AN201 (input)	P61	○	○	○
	AN202 (input)	P62	○	○	○
	AN203 (input)	P63	○	○	○
	AN204 (input)	P64	○	○	○
	AN205 (input)	P65	○	○	○
	AN206 (input)	P50	○	○	○
	AN207 (input)	P51	○	○	○
	AN208 (input)	P52	○	○	○
	AN209 (input)	P53	○	○	○
	AN210 (input)	P54	○	○	○
	AN211 (input)	P55	○	○	○
	ADTRG0# (input)	PA4	○	○	○
		P20	○	○	○
		PA1	○	○	○
	ADTRG1# (input)	P21	○	○	○
		PA5	○	○	○
	ADTRG2# (input)	P22	○	○	○
		PB0	○	○	○
	ADST0 (output)	P02	○	○	○
		PD6	○	○	○
	ADST1 (output)	P00	○	○	○
	ADST2 (output)	P01	○	○	○
8-bit D/A converter	DA0	P24		○	○
	DA1	P23		○	○
Clock frequency accuracy measurement circuit	CACREF (input)	P23	○	○	○
		PB3	○	○	○
Comparator	COMP0 (output)	P24	○	○	○
	COMP1 (output)	P23	○	○	○
	COMP2 (output)	P22	○	○	○
	COMP3 (output)	P30	○	○	○
	CVREFC0 (input)	P20	○	×	×
	CVREFC1 (input)	P21	○	×	×

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)
			100-Pin		
			Chip Version A	Chip Version B	100-Pin
Comparator	CMPC00 (input)	P40	○	○	○
	CMPC01 (input)	P40	○	○	○
	CMPC02 (input)	P45	○	○	○
	CMPC03 (input)	P45	○	○	○
	CMPC10 (input)	P44	○	○	○
	CMPC11 (input)	P44	○	○	○
	CMPC12 (input)	P46	○	○	○
	CMPC13 (input)	P46	○	○	○
	CMPC20 (input)	P45	○	○	○
	CMPC21 (input)	P45	○	○	○
	CMPC22 (input)	P40	○	○	○
	CMPC23 (input)	P40	○	○	○
	CMPC30 (input)	P46	○	○	○
	CMPC31 (input)	P46	○	○	○
	CMPC32 (input)	P44	○	○	○
	CMPC33 (input)	P44	○	○	○

Table 2.16 Comparison of Multiplexed Pin Assignments (64-Pin)

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX24T (MPC) 64-Pin
Interrupt	NMI (input)	PE2	○	○
	IRQ0 (input)	P10	○	×
		P93	○	×
		P52	×	○
	IRQ1 (input)	P11	○	○
		P94	○	×
		P53	×	○
	IRQ2 (input)	P00	○	○
		P22	○	×
		PB1	○	×
		PD4	○	○
		P54	×	○
	IRQ3 (input)	P24	○	×
		PB4	○	○
		PD5	○	○
	IRQ4 (input)	P01	○	○
		P23	○	×
		PA2	○	×
		P96	×	○
	IRQ5 (input)	P02	○	○
		P70	○	○
		PB6	○	○
		PD6	○	○
	IRQ6 (input)	P21		○
		P31		○
	IRQ7 (input)	P30		○
Multi-function timer unit 3	MTIOC0A (input/output) / MTIOC0A# (input/output)	P31	○	○
		PB3	○	○
	MTIOC0B (input/output) / MTIOC0B# (input/output)	P30	○	○
		P93	○	×
		PB2	○	○
	MTIOC0C (input/output) / MTIOC0C# (input/output)	P94	○	×
		PB1	○	○
	MTIOC0D (input/output)	PB0	○	×
	MTIOC1A (input/output)	PA5	○	×
	MTIOC1B (input/output)	PA4	○	×
	MTIOC2A (input/output)	PA3	○	×
	MTIOC2B (input/output)	PA2	○	×

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)	RX24T (MPC)
			64-Pin	64-Pin
Multi-function timer unit 3	MTIOC3A (input/output) / MTIOC3A# (input/output)	P11	○	○
		P33	○	×
	MTIOC3B (input/output) / MTIOC3B# (input/output)	P71	○	○
	MTIOC3C (input/output)	P32	○	×
	MTIOC3D (input/output) / MTIOC3D# (input/output)	P74	○	○
	MTIOC4A (input/output) / MTIOC4A# (input/output)	P72	○	○
	MTIOC4B (input/output) / MTIOC4B# (input/output)	P73	○	○
	MTIOC4C (input/output) / MTIOC4C# (input/output)	P75	○	○
	MTIOC4D (input/output) / MTIOC4D# (input/output)	P76	○	○
	MTIC5U (input) / MTIC5U# (input)	P24	○	○
	MTIC5V (input) / MTIC5V# (input)	P23	○	○
	MTIC5W (input) / MTIC5W# (input)	P22	○	○
	MTIOC6B (input/output) / MTIOC6B# (input/output)	P95		○
	MTIOC6D (input/output) / MTIOC6D# (input/output)	P92		○
	MTIOC7A (input/output) / MTIOC7A# (input/output)	P94		○
	MTIOC7B (input/output) / MTIOC7B# (input/output)	P93		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX24T (MPC) 64-Pin
Multi-function timer unit 3	MTIOC7C (input/output) / MTIOC7C# (input/output)	P91		○
	MTIOC7D (input/output) / MTIOC7D# (input/output)	P90		○
	MTIOC9A (input/output) / MTIOC9A# (input/output)	P21		○
		PD7		○
	MTIOC9C (input/output) / MTIOC9C# (input/output)	PD6		○
	MTIOC9D (input/output) / MTIOC9D# (input/output)	P02		○
	MTCLKA (input) / MTCLKA# (input)	P33	○	×
		P21	×	○
	MTCLKB (input)	P32	○	×
	MTCLKC (input) / MTCLKC# (input)	P11	○	○
		P31	○	○
	MTCLKD (input) / MTCLKD# (input)	P10	○	×
		P30	○	○
	ADSM0 (output)	PB2	○	○
	ADSM1 (output)	PB1		○
8-bit timer	TMO0 (output)	PD3	○	○
	TMCI0 (input)	PD4	○	○
		PB1	×	○
	TMRI0 (input)	PD5	○	○
		PB2	×	○
	TMO1 (output)	P94	○	×
		PD6	○	○
	TMCI1 (input)	P92	○	×
	TMRI1 (input)	P93	○	×
		PD7	○	○
	TMO2 (output)	P23	○	○
	TMCI2 (input)	P24	○	○
	TMRI2 (input)	P22	○	○
	TMO3 (output)	P11	○	○
	TMCI3 (input)	PA5	○	×
	TMRI3 (input)	P10	○	×
	TMO4 (output)	P22		○
	TMCI4 (input)	P21		○
	TMRI5 (input)	PD7		○
	TMO6 (output)	P24		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX24T (MPC) 64-Pin
8-bit timer	TMCI6 (input)	P30		○
		PD4		○
	TMRI6 (input)	P31		○
		PD5		○
Port output enable 3	POE0# (input)	P70	○	○
	POE4# (input)	P96		○
	POE8# (input)	PB4	○	○
	POE10# (input)	PE2	○	○
	POE12# (input)	P01		○
Serial communications interface	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	PD5	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	PD3	○	○
	SCK1 (input/output)	PD4	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P02	○	○
		PD6	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PB1	○	×
		PB6	○	○
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PB2	○	×
		PB5	○	○
	SCK5 (input/output)	P93	○	×
		PB3	○	×
		PB7	○	×
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA2	○	×
		PB4	×	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	PB1		○
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	PB2		○
	SCK6 (input/output)	PB3		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC)	RX24T (MPC)
			64-Pin	64-Pin
I²C bus interface	SCL0 (input/output)	PB1	○	○
	SDA0 (input/output)	PB2	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○	○
		P93	○	×
		PA4	○	×
		PB3	○	○
	MOSIA (input/output)	P23	○	○
		PB0	○	×
	MISOA (input/output)	P22	○	○
		P94	○	×
		PA5	○	×
	SSLA0 (input/output)	P30	○	○
		PA3	○	×
		PD6	○	○
	SSLA1 (output)	P31	○	○
		PA2	○	×
		PD7	○	○
	SSLA2 (output)	P32	○	×
		P92	○	×
	SSLA3 (output)	P33	○	×
		P91	○	×
12-bit A/D converter	AN000 (input)	P40	○	○
	AN001 (input)	P41	○	○
	AN002 (input)	P42	○	○
	AN003 (input)	P43	○	×
	AN004 (input)	P44	○	
	AN005 (input)	P45	○	
	AN006 (input)	P46	○	
	AN007 (input)	P47	○	
	AN016 (input)	P11	○	×
	AN017 (input)	P10	○	
	AN100 (input)	P44		○
	AN101 (input)	P45		○
	AN102 (input)	P46		○
	AN116 (input)	P21		○
	AN206 (input)	P50		○
	AN207 (input)	P51		○
	AN208 (input)	P52		○
	AN209 (input)	P53		○
	AN210 (input)	P54		○
	ADTRG0# (input)	PA4	○	×
	ADTRG1# (input)	P21		○
	ADTRG2# (input)	P22		○
	ADST0 (output)	P02	○	○
		PD6	○	○
	ADST1 (output)	P00		○
	ADST2 (output)	P01		○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 64-Pin	RX24T (MPC) 64-Pin
Clock frequency accuracy measurement circuit	CACREF (input)	P01	○	×
		P23	○	○
		PB3	○	○
Comparator	CMPC00 (input)	P40	○	○
	CMPC01 (input)	P43	○	×
		P40	×	○
	CMPC02 (input)	P46	○	×
		P45	×	○
	CMPC03 (input)	P45		○
	CMPC10 (input)	P41	○	×
		P44	×	○
	CMPC11 (input)	P44	○	○
	CMPC12 (input)	P47	○	×
		P46	×	○
	CMPC13 (input)	P46		○
	CMPC20 (input)	P42	○	×
		P45	×	○
	CMPC21 (input)	P45	○	○
	CMPC22 (input)	P47	○	×
		P40	×	○
	CMPC23 (input)	P40		○
	CMPC30 (input)	P46		○
	CMPC31 (input)	P46		○
	CMPC32 (input)	P44		○
	CMPC33 (input)	P44		○
	COMP0 (output)	P24	○	○
	COMP1 (output)	P23	○	○
	COMP2 (output)	P22	○	○
	COMP3 (output)	P30		○
	CVREFC0 (input)	P11	○	×
	CVREFC1 (input)	P10	○	×
		P21	×	○

Table 2.17 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX23T (n = 0 to 2)	RX24T (n = 0 to 2)		RX24U (n = 0 to 2)
			Chip Version A	Chip Version B	
P00PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
P01PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00111b: CACREF	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2
P02PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9D 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9D 00011b: MTIOC9D# 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9D 00011b: MTIOC9D# 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1#

Table 2.18 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX23T (n = 0, 1)	RX24T (n = 0, 1)		RX24U (n = 0 to 7)
			Chip Version A	Chip Version B	
P10PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKD 00101b: TMRI3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/ RTS6#/ SS6#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B# 00100b: MTCLKD# 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/ RTS6#/ SS6#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B# 00100b: MTCLKD# 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/ RTS6#/ SS6#
P11PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A# 00100b: MTCLKC# 00101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A# 00100b: MTCLKC# 00101b: TMO3
P12PFS	—	—	—	—	P12 pin function control register
P13PFS	—	—	—	—	P13 pin function control register
P14PFS	—	—	—	—	P14 pin function control register
P15PFS	—	—	—	—	P15 pin function control register
P16PFS	—	—	—	—	P16 pin function control register
P17PFS	—	—	—	—	P17 pin function control register
P1nPFS	ASEL	Analog input function select bit	—	—	—

Table 2.19 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX23T (n = 2 to 4)	RX24T (n = 0 to 4)		RX24U (n = 0 to 7)
			Chip Version A	Chip Version B	
P20PFS	—	—	P20 pin function control register	P20 pin function control register	P20 pin function control register
P21PFS	—	—	P21 pin function control register	P21 pin function control register	P21 pin function control register
P22PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00101b: TMRI2 01101b: MISOA 11110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 11110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 11110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 10110b: COMP2
P23PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMO2 00111b: CACREF 01101b: MOSIA 10110b: COMP1
P24PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI2 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 10110b: COMP0
P25PFS	—	—	—	—	P25 pin function control register
P26PFS	—	—	—	—	P26 pin function control register
P27PFS	—	—	—	—	P27 pin function control register
P2nPFS	ASEL	—	Analog input function select bit	Analog input function select bit	Analog input function select bit

Table 2.20 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX23T (n = 0 to 3)	RX24T (n = 0 to 3)		RX24U (n = 0 to 5)
			Chip Version A	Chip Version B	
P30PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00101b: TMCI6 01101b: SSLA0 11110b: COMP3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00011b: MTIOC0B# 00100b: MTCLKD# 00101b: TMCI6 01101b: SSLA0 11110b: COMP3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00011b: MTIOC0B# 00100b: MTCLKD# 00101b: TMCI6 01101b: SSLA0 11110b: COMP3
P31PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00101b: TMRI6 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00011b: MTIOC0A# 00100b: MTCLKC# 00101b: TMRI6 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00011b: MTIOC0A# 00100b: MTCLKC# 00101b: TMRI6 01101b: SSLA1
P32PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 01101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00101b: TMO6 01101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00011b: MTIOC3C# 00100b: MTCLKB# 00101b: TMO6 01101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00011b: MTIOC3C# 00100b: MTCLKB# 00101b: TMO6 01101b: SSLA2
P33PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 01101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMO0 01101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: MTIOC3A# 00100b: MTCLKA# 00101b: TMO0 01101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: MTIOC3A# 00100b: MTCLKA# 00101b: TMO0 01101b: SSLA3
P34PFS	—	—	—	—	P34 pin function control register
P35PFS	—	—	—	—	P35 pin function control register

Register	Bit	RX23T (n = 0 to 3)	RX24T (n = 0 to 3)		RX24U (n = 0 to 5)
			Chip Version A	Chip Version B	
P3nPFS	ISEL	—	Interrupt input function select bit	Interrupt input function select bit	Interrupt input function select bit

Table 2.21 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX23T (n = 0 to 7)	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)
P4nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin
		P40: AN000 (64/52/48-pin)	P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (100/80/64-pin)	P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (144/100-pin)
		P41: AN001 (64/52/48-pin)	P41: AN001 (100/80/64-pin)	P41: AN001 (144/100-pin)
		P42: AN002 (64/52/48-pin)	P42: AN002 (100/80/64-pin)	P42: AN002 (144/100-pin)
		P43: AN003 (64/52/48-pin)	P43: AN003 (100/80-pin)	P43: AN003 (144/100-pin)
		P44: AN004 (64/52/48-pin)	P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (100/80/64-pin)	P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (144/100-pin)
		P45: AN005 (64/52/48-pin)	P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (100/80/64-pin)	P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (144/100-pin)
		P46: AN006 (64/52/48-pin)	P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (100/80/64-pin)	P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (144/100-pin)
		P47: AN007 (64/52/48-pin)	P47: AN103 (100/80-pin)	P47: AN103 (144/100-pin)

Table 2.22 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX23T	RX24T	RX24U
P5nPFS	—	—	P5n pin function control register (n = 0 to 5)	P5n pin function control register (n = 0 to 5)

Table 2.23 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX23T	RX24T	RX24U
P6nPFS	—	—	P6n pin function control register (n = 0 to 5)	P6n pin function control register (n = 0 to 5)

Table 2.24 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX23T (n = 0 to 6)	RX24T (n = 0 to 6)		RX24U (n = 0 to 6)
			Chip Version A	Chip Version B	
P70PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0# 01010b: CTS9#/ RTS9#/ SS9#
P71PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B# 10100b: GTIOC0A 10110b: GTIOC0A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B# 10100b: GTIOC0A 10110b: GTIOC0A#
P72PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A# 10100b: GTIOC1A 10110b: GTIOC1A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A# 10100b: GTIOC1A 10110b: GTIOC1A#
P73PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B# 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B# 10100b: GTIOC2A 10110b: GTIOC2A#
P74PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D# 10100b: GTIOC0B 10110b: GTIOC0B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D# 10100b: GTIOC0B 10110b: GTIOC0B#

Register	Bit	RX23T (n = 0 to 6)	RX24T (n = 0 to 6)		RX24U (n = 0 to 6)
			Chip Version A	Chip Version B	
P75PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C# 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C# 10100b: GTIOC1B 10110b: GTIOC1B#
P76PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D# 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D# 10100b: GTIOC2B 10110b: GTIOC2B#

Table 2.25 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX23T	RX24T	RX24U
P8nPFS	—	—	P8n pin function control register (n = 0 to 2)	P8n pin function control register (n = 0 to 4)

Table 2.26 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX23T (n = 1 to 4)	RX24T (n = 0 to 6)		RX24U (n = 0 to 6)
			Chip Version A	Chip Version B	
P90PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
P91PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7C	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7C 00011b: MTIOC7C#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7C 00011b: MTIOC7C#
P92PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 01101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6D 00011b: MTIOC6D#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6D 00011b: MTIOC6D#

Register	Bit	RX23T (n = 1 to 4)	RX24T (n = 0 to 6) Chip Version A	RX24T (n = 0 to 6) Chip Version B	RX24U (n = 0 to 6)
P93PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMRI1 01010b: SCK5 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#
P94PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO1 01101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#
P95PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
P96PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ0 (64/52/48-pin) P94: IRQ1 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (100/80/64-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (144/100-pin)

Table 2.27 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX23T (n = 2 to 5)	RX24T (n = 0 to 5)		RX24U (n = 0 to 7)
			Chip Version A	Chip Version B	
PA0PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PA1PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PA2PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 01010b: CTS5#/ RTS5#/ SS5# 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMO7 01010b: CTS6#/ RTS6#/ SS6# 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTIOC2B# 00101b: TMO7 01010b: CTS6#/ RTS6#/ SS6# 01101b: SSLA1 10100b: GTADSM1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00011b: MTIOC2B# 00101b: TMO7 01010b: CTS6#/ RTS6#/ SS6# 01101b: SSLA1 10100b: GTADSM1
PA3PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMRI7 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC2A# 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00011b: MTIOC2A# 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0
PA4PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 01001b: ADTRG0# 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00010b: MTIOC1B# 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC1B# 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA

Register	Bit	RX23T (n = 2 to 5)	RX24T (n = 0 to 5) Chip Version A	RX24T (n = 0 to 5) Chip Version B	RX24U (n = 0 to 7)
PA5PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMCI3 01101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/ SMISO6/ SSCL6 01101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00010b: MTIOC1A# 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/ SMISO6/ SSCL6 01101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC1A# 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/ SMISO6/ SSCL6 01101b: MISOA
PA6PFS	PSEL [4:0]	—	—	—	Pin function select bits
PA7PFS	PSEL [4:0]	—	—	—	Pin function select bits
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA2: IRQ4 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (100/80-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (144/100-pin)

Table 2.28 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX23T (n = 0 to 7)	RX24T (n = 0 to 7) Chip Version A	RX24T (n = 0 to 7) Chip Version B	RX24U (n = 0 to 7)
PB0PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 01101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/ SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D# 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/ SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D# 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/ SMOSI6/ SSDA6 01101b: MOSIA

Register	Bit	RX23T (n = 0 to 7)	RX24T (n = 0 to 7) Chip Version A	RX24T (n = 0 to 7) Chip Version B	RX24U (n = 0 to 7)
PB1PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD5/ SMISO5/ SSCL5 01111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/ SMISO6/ SSCL6 01111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C# 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/ SMISO6/ SSCL6 01111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C# 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/ SMISO6/ SSCL6 01111b: SCL0
PB2PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 01001b: ADSM0 01010b: TXD5/ SMOSI5/ SSDA5 01111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/ SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B# 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/ SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B# 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/ SMOSI6/ SSDA6 01111b: SDA0
PB3PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A# 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A# 00111b: CACREF 01010b: SCK6 01101b: RSPCKA
PB4PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/ RTS5#/ SS5#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/ RTS5#/ SS5# 10100b: GTETRG 10101b: GTECLKD	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/ RTS5#/ SS5# 10100b: GTETRG 10101b: GTECLKD

Register	Bit	RX23T (n = 0 to 7)	RX24T (n = 0 to 7) Chip Version A	RX24T (n = 0 to 7) Chip Version B	RX24U (n = 0 to 7)
PB5PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/ SMOSI5/ SSDA5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/ SMOSI5/ SSDA5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/ SMOSI5/ SSDA5 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/ SMOSI5/ SSDA5 10100b: GTIOC2B 10110b: GTIOC2B#
PB6PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/ SMISO5/ SSCL5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/ SMISO5/ SSCL5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/ SMISO5/ SSCL5 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/ SMISO5/ SSCL5 10100b: GTIOC2A 10110b: GTIOC2A#
PB7PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B 10110b: GTIOC1B#
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (64/52/48-pin) PB4: IRQ3 (64/52/48-pin) PB6: IRQ5 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (100/80/64-pin) PB6: IRQ5 (100/80/64-pin)		Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (144/100-pin) PB6: IRQ5 (144/100-pin)

Table 2.29 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX23T	RX24T	RX24U
PCnPFS	—	—	—	PCn pin function control register (n = 0 to 6)

Table 2.30 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX23T (n = 3 to 7)	RX24T (n = 0 to 7)		RX24U (n = 0 to 7)
			Chip Version A	Chip Version B	
PD0PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PD1PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PD2PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PD3PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/ SMOSI1/ SSDA1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/ SMOSI1/ SSDA1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/ SMOSI1/ SSDA1 10101b: GTECLKC	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/ SMOSI1/ SSDA1 01011b: TXD11/ SMOSI11/ SSDA11 10101b: GTECLKC
PD4PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 01010b: SCK1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 10101b: GTECLKB	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 01011b: SCK11 10101b: GTECLKB
PD5PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 01010b: RXD1/ SMISO1/ SSCL1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/ SMISO1/ SSCL1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/ SMISO1/ SSCL1 10101b: GTECLKA	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/ SMISO1/ SSCL1 01011b: RXD11/ SMISO11/ SSCL11 10101b: GTECLKA

Register	Bit	RX23T (n = 3 to 7)	RX24T (n = 0 to 7) Chip Version A	RX24T (n = 0 to 7) Chip Version B	RX24U (n = 0 to 7)
PD6PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO1 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1# 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00101b: TMO1 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1# 01101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C# 00101b: TMO1 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1# 01101b: SSLA0 10100b: GTIOC3B 10110b: GTIOC3B#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C# 00101b: TMO1 01001b: ADST0 01010b: CTS1#/ RTS1#/ SS1# 01011b: CTS11#/ RTS11#/ SS11# 01101b: SSLA0 10100b: GTIOC3B 10110b: GTIOC3B#
PD7PFS	PSEL [4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI1 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00101b: TMRI1 00110b: TMRI5 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00011b: MTIOC9A# 00101b: TMRI1 00110b: TMRI5 01010b: TXD5/ SMOSI5/ SSDA5 01101b: SSLA1 10100b: GTIOC3A 10110b: GTIOC3A#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00011b: MTIOC9A# 00101b: TMRI1 00110b: TMRI5 01010b: TXD5/ SMOSI5/ SSDA5 01101b: SSLA1 10100b: GTIOC3A 10110b: GTIOC3A#

Table 2.31 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX23T (n = 2)	RX24T (n = 0 to 5)		RX24U (n = 0 to 6)
			Chip Version A	Chip Version B	
PE0PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PE1PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PE3PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PE4PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PE5PFS	PSEL [4:0]	—	Pin function select bits	Pin function select bits	Pin function select bits
PE6PFS	PSEL [4:0]	—	—	—	Pin function select bits
PEnPFS	ISEL	—	Interrupt input function select bit	Interrupt input function select bit	Interrupt input function select bit

Table 2.32 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX23T	RX24T	RX24U
PFnPFS	—	—	—	PFn pin function control register (n = 0 to 3)

Table 2.33 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX23T	RX24T	RX24U
PGnPFS	—	—	—	PGn pin function control register (n = 0 to 2)

2.12 Multi-Function Timer Pulse Unit 3

Table 2.34 is a comparative overview of multi-function timer pulse unit 3, and Table 2.35 is a comparison of multi-function timer pulse unit 3 registers.

Table 2.34 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX23T (MTU3c)	RX24T (MTU3d)/RX24U (MTU3d)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (when LWA = 1))	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (when LWA = 1))
Operating frequency	Up to 40 MHz	Up to 80 MHz
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4] • Ability to specify buffer operation	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available

Item	RX23T (MTU3c)	RX24T (MTU3d)/RX24U (MTU3d)
Available operations	[MTU3, MTU4] • Ability to output in complementary PWM and reset PWM operation positive and negative signals in six phases through interlocked operation of MTU3 and MTU4 • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer register (MTU4.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Ability to output in complementary PWM and reset PWM operation positive and negative signals in six phases (12 phases in total) through interlocked operation of MTU3/MTU4 and MTU6/MTU7 • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer registers (MTU4.TGRD and MTU7.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode
	[MTU3, MTU4] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0	[MTU3, MTU4] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0
	[MTU5] • Ability to use the MTU5 as a dead-time compensation counter	[MTU5] • Ability to use the MTU5 as a dead-time compensation counter
	—	[MTU6, MTU7] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU9
Interrupt skipping function	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.35 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX23T (MTU3c)	RX24T (MTU3d)/RX24U (MTU3d)
TMDR2B	—	—	Timer mode register 2
TSYCR	—	—	Timer synchronous clear register
TSTRA	CST9	—	Counter start 9 bit
TSTRB	—	—	Timer start register
TSYRA	SYNC9	—	Timer synchronous operation 9 bit
TSYRB	—	—	Timer synchronous register
TCSYSTR	SCH7	—	Synchronous start 7 bit
	SCH6	—	Synchronous start 6 bit
	SCH9	—	Synchronous start 9 bit
TRWERB	—	—	Timer read/write enable register
TOERB	—	—	Timer output master enable register
TOCR1B	—	—	Timer output control register 1
TOCR2B	—	—	Timer output control register 2
TOLBRB	—	—	Timer output level buffer register
TGCRB	—	—	Timer gate control register
TCNTSB	—	—	Timer subcounter
TCDRB	—	—	Timer period data register
TCBRB	—	—	Timer period buffer register
TDDRB	—	—	Timer dead time data register
TDERB	—	—	Timer dead time enable register
TBTERB	—	—	Timer buffer transfer set register
TWCRB	—	—	Timer waveform control register
NFCRn	—	Noise filter control register n (n = 0 to 4, C)	Noise filter control register n (n = 0 to 4, 6, 7, 9, C)
TITCR1B	—	—	Timer interrupt skipping set register 1
TITCNT1B	—	—	Timer interrupt skipping counter 1
TITCR2B	—	—	Timer interrupt skipping set register 2
TITCNT2B	—	—	Timer interrupt skipping counter 2

Register	Bit	RX23T (MTU3c)	RX24T (MTU3d)/RX24U (MTU3d)
TADSTRGR0	TADSTRS0 [4: 0]	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation bits b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation bits b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: TRGA9N 1 0 0 1 0: TRG9N 1 0 0 1 1: TRG9AEN 1 0 1 0 0: TRG0AEN 1 0 1 0 1: TRGA09N 1 0 1 1 0: TRG09N
TADSTRGR1	—	—	A/D conversion start request select register 1

2.13 Port Output Enable 3

Table 2.36 is a comparative overview of port output enable 3, and Table 2.37 is a comparison of port output enable 3 registers.

Table 2.36 Comparative Overview of Port Output Enable 3

Item	RX23T (POE3b)	RX24T (POE3b, POE3A)/RX23U (POE3A)
Pin status while output is disabled	• High-impedance	• High-impedance • General I/O port*1
Output disable control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins*1 — GPT0 pin (GTIOC0A, GTIOC0B) — GPT1 pin (GTIOC1A, GTIOC1B) — GPT2 pin (GTIOC2A, GTIOC2B) — GPT3 pin (GTIOC3A, GTIOC3B)
Conditions for generating output disable request	• Input pin change: Detection of signal input on POE0#, POE8#, or POE10# • Register setting • Detection of oscillation stop by clock oscillator • Detection of output from comparator (CMPC) • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D	• Input pin change: Detection of signal input on POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# • Register setting • Detection of oscillation stop by main clock oscillator • Detection of output from comparator C (CMPC) • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D

Item	RX23T (POE3b)	RX24T (POE3b, POE3A)/RX23U (POE3A)
Conditions for generating output disable request		[GPT output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B
Functions	• The POE0#, POE8#, and POE10# input pins can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.	• The POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# input pins can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.
	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state at falling-edge or low-level sampling of the POE0#, POE8#, or POE10# pins.	• Output on all the target pins can be disabled by falling-edge or low-level sampling of the POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# pin.
	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state when clock generator oscillation stop is detected.	• Output on all the target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.
	• MTU complementary PWM output pins can be placed in the high-impedance state when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.	• Output on the MTU complementary PWM output pins can be disabled when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.
		• Output on the GPT output pins can be disabled when output levels of GPT output pins (GPT0, GPT1, and GPT2) are compared and simultaneous active-level output continues for one cycle or more.
	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state at comparator detection by the comparator (CMPC).	• Output on all the target pins can be disabled at comparator detection by comparator C (CMPC).
	• MTU complementary PWM output pins and MTU0 pins can be placed in the high-impedance state by modifying the settings of the POE registers.	• Output on all the target pins can be disabled by modifying the settings of the POE registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.

Note: 1. On the RX24T Group, chip version B only.

Table 2.37 Comparison of Port Output Enable 3 Registers

Register	Bit	RX23T (POE3b)	RX24T (POE3b, POE3A)	RX23U (POE3A)
ICSR2	—	—	Input level control/ status register 2	Input level control/ status register 2
ICSR5	—	—	Input level control/ status register 5	Input level control/ status register 5
ICSR7	—	—	Input level control/ status register 7	Input level control/ status register 7
OCSR2	—	—	Output level control/ status register 2	Output level control/ status register 2
OCSR3	—	—	—	Output level control/ status register 3
ALR1	OLSG0A	MTIOC3B active level setting bit	MTIOC3B/GTIOC0A (P71) pin active level setting bit	MTIOC3B/GTIOC0A (P71) pin active level setting bit
	OLSG0B	MTIOC3D active level setting bit	MTIOC3D/GTIOC0B (P74) pin active level setting bit	MTIOC3D/GTIOC0B (P74) pin active level setting bit
	OLSG1A	MTIOC4A active level setting bit	MTIOC4A/GTIOC1A (P72) pin active level setting bit	MTIOC4A/GTIOC1A (P72) pin active level setting bit
	OLSG1B	MTIOC4C active level setting bit	MTIOC4C/GTIOC1B (P75) pin active level setting bit	MTIOC4C/GTIOC1B (P75) pin active level setting bit
	OLSG2A	MTIOC4B active level setting bit	MTIOC4B/GTIOC2A (P73) pin active level setting bit	MTIOC4B/GTIOC2A (P73) pin active level setting bit
	OLSG2B	MTIOC4D active level setting bit	MTIOC4D/GTIOC2B (P76) pin active level setting bit	MTIOC4D/GTIOC2B (P76) pin active level setting bit
ALR2	—	—	Active level register 2	Active level register 2
ALR3	—	—	—	Active level register 3
SPOER	MTUCH34HIZ	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit	MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit
	MTUCH67HIZ	—	MTU6 and MTU7 pin output disable bit	MTU6 and MTU7 pin output disable bit
	GPT02HIZ	—	—	GPT0 to GPT2 or MTU3, MTU4 pin output disable bit
	GPT03HIZ	—	GPT0 to GPT3 pin output disable bit*1	GPT0 to GPT3 pin output disable bit
	MTUCH9HIZ	—	MTU9 pin output disable bit	MTU9 pin output disable bit
POECR1	MTU0B2ZE	MTIOC0B P93 pin high-impedance enable bit	—	—
	MTU0C1ZE	MTIOC0C P94 pin high-impedance enable bit	—	—

Register	Bit	RX23T (POE3b)	RX24T (POE3b, POE3A)	RX23U (POE3A)
POECR2	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit	MTIOC6B/MTIOC6D pin high-impedance enable bit
POECR3	—	—	Port output enable control register 3*2	Port output enable control register 3
	GPT0AZE	—	—	GTIOC0A (P12) pin high-impedance enable bit
	GPT0BZE	—	—	GTIOC0B (P15) pin high-impedance enable bit
	GPT1AZE	—	—	GTIOC1A (P13) pin high-impedance enable bit
	GPT1BZE	—	—	GTIOC1B (P16) pin high-impedance enable bit
	GPT2AZE	—	—	GTIOC2A (P14) pin high-impedance enable bit
	GPT2BZE	—	—	GTIOC2B (P17) pin high-impedance enable bit
POECR4	IC2ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE4F add bit	MTU3 and MTU4 output disabling condition POE4F add bit
	IC5ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE11F add bit	MTU3 and MTU4 output disabling condition POE11F add bit
	IC6ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE12F add bit	MTU3 and MTU4 output disabling condition POE12F add bit
	CMADDMT67ZE	—	MTU6 and MTU7 output disabling condition CFLAG add bit	MTU6 and MTU7 output disabling condition CFLAG add bit
	IC1ADDMT67ZE	—	MTU6 and MTU7 output disabling condition POE0F add bit	MTU6 and MTU7 output disabling condition POE0F add bit
	IC3ADDMT67ZE	—	MTU6 and MTU7 output disabling condition POE8F add bit	MTU6 and MTU7 output disabling condition POE8F add bit

Register	Bit	RX23T (POE3b)	RX24T (POE3b, POE3A)	RX23U (POE3A)
POECR4	IC4ADDMT67ZE	—	MTU6 and MTU7 output disabling condition POE10F add bit	MTU6 and MTU7 output disabling condition POE10F add bit
	IC5ADDMT67ZE	—	MTU6 and MTU7 output disabling condition POE11F add bit	MTU6 and MTU7 output disabling condition POE11F add bit
	IC6ADDMT67ZE	—	MTU6 and MTU7 output disabling condition POE12F add bit	MTU6 and MTU7 output disabling condition POE12F add bit
POECR5	IC2ADDMT0ZE	—	MTU0 output disabling condition POE4F add bit	MTU0 output disabling condition POE4F add bit
	IC5ADDMT0ZE	—	MTU0 output disabling condition POE11F add bit	MTU0 output disabling condition POE11F add bit
	IC6ADDMT0ZE	—	MTU0 output disabling condition POE12F add bit	MTU0 output disabling condition POE12F add bit
POECR6	—	—	Port output enable control register 6*2	Port output enable control register 6
	CMADDGPT02ZE	—	—	GPT0 to GPT2 output disabling condition CFLAG add bit
	IC1ADDGPT02ZE	—	—	GPT0 to GPT2 output disabling condition POE0F add bit
	IC2ADDGPT02ZE	—	—	GPT0 to GPT2 output disabling condition POE4F add bit
	IC3ADDGPT02ZE	—	—	GPT0 to GPT2 output disabling condition POE8F add bit
	IC5ADDGPT02ZE	—	—	GPT0 to GPT2 output disabling condition POE11F add bit
	IC6ADDGPT02ZE	—	—	GPT0 to GPT2 output disabling condition POE12F add bit

Register	Bit	RX23T (POE3b)	RX24T (POE3b, POE3A)	RX23U (POE3A)
POECR7	—	—	Port output enable control register 7	Port output enable control register 7
	MTU9A2ZE	—	—	MTIOC9A (P26) pin high-impedance enable bit
	MTU9C2ZE	—	—	MTIOC9C (P25) pin high-impedance enable bit
POECR8	—	—	Port output enable control register 8	Port output enable control register 8
PMMCR0	—	—	Port mode mask control register 0*2	Port mode mask control register 0
PMMCR1	—	—	Port mode mask control register 1*2	Port mode mask control register 1
PMMCR2	—	—	Port mode mask control register 2*2	Port mode mask control register 2
	GPT0AME	—	—	GTIOC0A/MTIOC3B (P12) pin port mode mask enable bit
	GPT0BME	—	—	GTIOC0B/MTIOC3D (P15) pin port mode mask enable bit
	GPT1AME	—	—	GTIOC1A/MTIOC4A (P13) pin port mode mask enable bit
	GPT1BME	—	—	GTIOC1B/MTIOC4C (P16) pin port mode mask enable bit
	GPT2AME	—	—	GTIOC2A/MTIOC4B (P14) pin port mode mask enable bit
	GPT2BME	—	—	GTIOC2B/MTIOC4D (P17) pin port mode mask enable bit
PMMCR3	—	—	Port mode mask control register 3*2	Port mode mask control register 3
	MTU9A2ME	—	—	MTIOC9A (P26) pin port mode mask enable bit
	MTU9C2ME	—	—	MTIOC9C (P25) pin port mode mask enable bit
POECMPFR	C3FLAG	—	Comparator channel 3 output detection flag	Comparator channel 3 output detection flag
POECMPSEL	POEREQ3	—	Comparator channel 3 output disabling request enable bit	Comparator channel 3 output disabling request enable bit

Register	Bit	RX23T (POE3b)	RX24T (POE3b, POE3A)	RX23U (POE3A)
POECMPEXm	—	—	Port output enable comparator request extended selection register m (m = 0 to 2, 4, or 5)*2	Port output enable comparator request extended selection register m (m = 0 to 5)

Notes: 1. This bit is reserved on chip version A. The read value is 0 and the write value should be 0.
2. Only implemented on chip version B.

2.14 8-Bit Timer

Table 2.38 is a comparative overview of 8-bit timer.

Table 2.38 Comparative Overview of 8-Bit Timer

Item	RX23T (TMR)	RX24T (TMR)/RX24U (TMR)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, and TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, and TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0, TMR2, TMR4, or TMR6
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI	Generation of baud rate clock for SCI
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

2.15 Serial Communications Interface

Table 2.39 is a comparative overview of the serial communications interfaces, and Table 2.40 is a comparison of serial communications interface channel specifications.

Table 2.39 Comparative Overview of Serial Communications Interfaces

Item		RX23T (SCIg)	RX24T (SCIg)	RX24U (SCIg)
Number of channels		SCIg: 2 channels	SCIg: 3 channels	SCIg: 6 channels
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX23T (SCIg)	RX24T (SCIg)	RX24U (SCIg)
Asynchronous mode	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX23T (SCIg)	RX24T (SCIg)	RX24U (SCIg)
Simple I²C mode	Communication format	I²C bus format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.40 Comparison of Serial Communications Interface Channel Specifications

Item	RX23T (SCIg)	RX24T (SCIg)	RX24U (SCIg)
Synchronous mode	SCI1, SCI5	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Clock synchronous mode	SCI1, SCI5	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Smart card interface mode	SCI1, SCI5	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Simple I²C mode	SCI1, SCI5	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Simple SPI mode	SCI1, SCI5	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
TMR clock input	SCI5	SCI5, SCI6	SCI5, SCI6
Peripheral module clock	PCLKB: SCI1, SCI5	PCLKB: SCI1, SCI5, SCI6	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9 PCLKA: SCI11

2.16 Serial Peripheral Interface

Table 2.41 is a comparative overview of serial peripheral interface, and Table 2.42 is a comparison of serial peripheral interface registers.

Table 2.41 Comparative Overview of Serial Peripheral Interface

Item	RX23T (RSPIa)	RX24T (RSPIb)/RX24U (RSPIb)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4,096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX23T (RSPIa)	RX24T (RSPIb)/RX24U (RSPIb)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.42 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX23T (RSPIa)	RX24T (RSPIb)/RX24U (RSPIb)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode fault error flag 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	—	Underrun error flag*1

Note: 1. When clearing the UDRF flag to 0, clear the MODF flag to 0 at the same time.

2.17 12-Bit A/D Converter

Table 2.43 is a comparative overview of the 12-bit A/D converters, and Table 2.44 is a comparison of 12-bit A/D converter registers, and Table 2.45 is a comparison of A/D start triggers and corresponding ADSTRGR register settings.

Table 2.43 Comparative Overview of 12-Bit A/D Converters

Item	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
Number of units	1 unit (S12AD)	3 units (S12AD, S12AD1, S12AD2)
Input channels	S12AD: 10 channels	S12AD: 5 channels S12AD1: 5 channels S12AD2: 12 channels
Extended analog function	Internal reference voltage	Internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1 µs per channel (when A/D conversion clock ADCLK = 40 MHz)	1 µs per channel (when A/D conversion clock ADCLK = 40 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 10 registers for analog input, one for A/D-converted data duplication in double trigger mode, and two for A/D-converted data duplication during extended operation in double trigger mode • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.	• 22 registers for analog input (five for S12AD, five for S12AD1, and 12 for S12AD2), one for A/D-converted data duplication in double trigger mode, and two per unit for A/D-converted data duplication during extended operation in double trigger mode. • One register for internal reference (S12AD2) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
Data register	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 10 channels arbitrarily selected. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 10 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 10 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times.	The operating mode can be set independently for each of three units. • Single scan mode: — A/D conversion is performed only once on the analog inputs of the arbitrarily selected channels. — A/D conversion is performed only once on the internal reference voltage. (S12AD2) • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of the arbitrarily selected. • Group scan mode: — The number of groups used is selectable between two (groups A and B) and three (groups A, B, and C). (When two is selected as the number of groups, only group A and group B may be used in combination.) — Analog inputs of arbitrarily selected channels are divided into group A and group B, or group A, group B, and group C, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A, group B, and group C, allowing A/D conversion of the groups to start at different times.

Item	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
Operating modes	• Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.	• Group scan mode (when a group is given priority): — If a trigger is input for a higher-priority group during A/D conversion on a lower-priority group, A/D conversion on the lower-priority group is stopped and A/D conversion is performed on the higher-priority group. — The order of priority is group A (highest) > group B > group C (lowest). — Restart (rescan) of A/D conversion on the lower-priority group after completion of A/D conversion on the higher-priority group can be enabled. In addition, rescan can be set to start from the first of the selected channels or from the channels on which A/D conversion has not yet finished.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or 8-bit timer (TMR) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), general PWM timer (GPT), or 8-bit timer (TMR) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for each of three units).
Functions	• Channel-dedicated sample-and-hold function (three channels) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers	• Channel-dedicated sample-and-hold function (three channels: S12AD1 only) • Input signal amplification function using programmable gain amplifier (1channel: S12AD and 3 channels: S12AD1) • Variable sampling state count (independently settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers

Item	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (independently for each of three units). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (independently for each of three units). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI, GBADI1, or GBADI2) for group B can be generated on completion of group B scan. A dedicated group C scan end interrupt request (GCADI, GBADI1, or GBADI2) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, S12ADI2) can be generated on completion of double scan of group A. A dedicated group B or dedicated group C scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, or GBADI2/GCADI2) can be generated on completion of group B or group C scan, respectively. • The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.44 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
ADDRy	—	A/D data register y (y = 0 to 7, 16, 17)	A/D data register y (y = 0 to 3, 16: S12AD and S12AD1, y = 0 to 11: S12AD2)
ADCSR	ADST	A/D conversion start bit	A/D conversion start bit*1
S12AD. ADANSA0	ANSA0n	A/D conversion channel select bit (n = 00 to 07)	A/D conversion channel select bit (n = 00 to 03)
S12AD1. ADANSA0	—	—	A/D channel select register A0

Register	Bit	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
S12AD2. ADANSA0	—	—	A/D channel select register A0
S12AD. ADANSA1	ANSA1n	A/D conversion channel select bit (n = 00, 01)	A/D conversion channel select bit (n = 00)
S12AD1. ADANSA1	—	—	A/D channel select register A1
S12AD. ADANSB0	ANSB0n	A/D conversion channel select bit (n = 00 to 07)	A/D conversion channel select bit (n = 00 to 03)
S12AD1. ADANSB0	—	—	A/D channel select register B0
S12AD2. ADANSB0	—	—	A/D channel select register B0
S12AD. ADANSB1	ANSB1n	A/D conversion channel select bit (n = 00, 01)	A/D conversion channel select bit (n = 00)
S12AD1. ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
S12AD. ADADS0	ADS0n	A/D-converted value addition/ average channel select bit (n = 00 to 07)	A/D-converted value addition/ average channel select bit (n = 00 to 03)
S12AD1. ADADS0	—	—	A/D-converted value addition/ average function channel select register 0
S12AD2. ADADS0	—	—	A/D-converted value addition/ average function channel select register 0
S12AD. ADADS1	ADS1n	A/D-converted value addition/ average channel select bit (n = 00, 01)	A/D-converted value addition/ average channel select bit (n = 00)
S12AD1. ADADS1	—	—	A/D-converted value addition/ average function channel select register 1
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, O)	A/D sampling state register n (n = 0 to 11, L, O)
ADGSPCR	LGRRS	—	Restart channel select bit
ADHVREFCNT	—	A/D high-potential/low-potential reference voltage control register	—
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0

Note: 1. The ADST bit retains a value of 1 when group priority operation mode is enabled (bits ADCSR.ADCS[1:0] = 01b and bit ADGSPCR.PGS = 1) and the single scan continuous function is used (bit ADGSPCR.GBRP = 1).

Table 2.45 Comparison of A/D Start Triggers and Corresponding ADSTRGR Register Settings

Bit	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
TRSB[5:0]	A/D conversion start trigger select bits for group B b5 b0 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1	A/D conversion start trigger select bits for group B b5 b0 1 1 1 1 1 1: No trigger source selected. 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N

Bit	RX23T (S12ADE)	RX24T (S12ADF)/RX24U (S12ADF)
TRSA[5:0]	A/D conversion start trigger select bits	A/D conversion start trigger select bits
	b13 b8	b13 b8
	1 1 1 1 1 1: No trigger source selected.	1 1 1 1 1 1: No trigger source selected.*1
	0 0 0 0 0 0: ADTRG0#	
	0 0 0 0 0 1: TRGA0N	0 0 0 0 0 1: TRGA0N
	0 0 0 0 1 0: TRGA1N	0 0 0 0 1 0: TRGA1N
	0 0 0 0 1 1: TRGA2N	0 0 0 0 1 1: TRGA2N
	0 0 0 1 0 0: TRGA3N	0 0 0 1 0 0: TRGA3N
	0 0 0 1 0 1: TRGA4N	0 0 0 1 0 1: TRGA4N
		0 0 0 1 1 0: TRGA6N
		0 0 0 1 1 1: TRGA7N
	0 0 1 0 0 0: TRG0N	0 0 1 0 0 0: TRG0N
	0 0 1 0 0 1: TRG4AN	0 0 1 0 0 1: TRG4AN
	0 0 1 0 1 0: TRG4BN	0 0 1 0 1 0: TRG4BN
	0 0 1 0 1 1: TRG4AN or TRG4BN	0 0 1 0 1 1: TRG4AN or TRG4BN
	0 0 1 1 0 0: TRG4ABN	0 0 1 1 0 0: TRG4ABN
		0 0 1 1 0 1: TRG7AN
		0 0 1 1 1 0: TRG7BN
		0 0 1 1 1 1: TRG7AN or TRG7BN
		0 1 0 0 0 0: TRG7ABN
		0 1 0 0 1 1: TRGA9N
		0 1 0 1 0 0: TRG9N
		0 1 1 0 0 1: TRGA0N or TRG0N
		0 1 1 0 1 0: TRGA9N or TRG9N
		0 1 1 0 1 1: TRGA0N or TRGA9N
		0 1 1 1 0 0: TRG0N or TRG9N
	0 1 1 1 0 1: TMTRG0AN_0	0 1 1 1 0 1: TMTRG0AN_0
	0 1 1 1 1 0: TMTRG0AN_1	0 1 1 1 1 0: TMTRG0AN_1
		0 1 1 1 1 1: TMTRG0AN_2
		1 0 0 0 0 0: TMTRG0AN_3
		1 0 0 0 0 1: TRG9AEN
		1 0 0 0 1 0: TRG0AEN
		1 0 0 0 1 1: TRGA09N
		1 0 0 1 0 0: TRG09N
		1 1 0 0 1 0: GTADTRA0N
		1 1 0 0 1 1: GTADTRB0N
		1 1 0 1 0 0: GTADTRA1N
		1 1 0 1 0 1: GTADTRB1N
		1 1 0 1 1 0: GTADTRA2N
		1 1 0 1 1 1: GTADTRB2N
		1 1 1 0 0 0: GTADTRA3N
		1 1 1 0 0 1: GTADTRB3N
		1 1 1 0 1 0: GTADTRA0N or GTADTRB0N
		1 1 1 0 1 1: GTADTRA1N or GTADTRB1N
		1 1 1 1 0 0: GTADTRA2N or GTADTRB2N
		1 1 1 1 0 1: GTADTRA3N or GTADTRB3N

Note: 1. On the RX23T Group it is not possible to use an asynchronous trigger as the A/D conversion start trigger for group A in group scan mode, but on the RX24T/RX24U Group it is possible to use an asynchronous trigger for this purpose.

2.18 D/A Converter for Generating Comparator C Reference Voltage (DA) and D/A Converter (DAa)

Table 2.46 is a comparative overview of the D/A converters, and Table 2.47 is a comparison of D/A converter registers.

Table 2.46 Comparative Overview of D/A Converters

Item	RX23T (DA)	RX24T (DA, DAa)	RX24U (DAa)
Resolution	8 bits	8 bits	8 bits
Output channels	One channel	[Chip version A] One channel [Chip version B] Two channels	Two channels
Measure against mutual interference between analog modules	—	Measure against interference between D/A and A/D converters • D/A-converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling, by means of an enable signal, the timing at which the 8-bit D/A converter inrush current occurs.	Measure against interference between D/A and A/D converters • D/A-converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling, by means of an enable signal, the timing at which the 8-bit D/A converter inrush current occurs.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.47 Comparison of D/A Converter Registers

Register	Bit	RX23T (DA)	RX24T (DA, DAa)	RX24U (DAa)
DADRm	—	D/A data register m (m = 0)	D/A data register m (m = 0, 1)	D/A data register m (m = 0, 1)
DACR	DAOE1	—	D/A output enable 1 bit This bit is reserved on chip version A. The read value is 0 and the write value should be 0.	D/A output enable 1 bit
DADPR	—	DADRm format select register (m = 0)		DADRm format select register (m = 0 or 1)
DAADSCR	—	—	D/A A/D synchronous start control register Implemented in chip version B only.	D/A A/D synchronous start control register

2.19 Comparator C

Table 2.48 is a comparative overview of the comparator C modules, and Table 2.49 is a comparison of comparator C registers.

Table 2.48 Comparative Overview of Comparator C Modules

Item	RX23T (CMPC)	RX24T (CMPC)	RX24U (CMPC)
Number of channels	3 channels (comparator C0 to comparator C2)	4 channels (comparator C0 to comparator C3)	4 channels (comparator C0 to comparator C3)
Analog input voltage	• Input voltage to CMPCnm pin (n = channel number; m = 0 to 2) • Internal reference voltage	• Input voltage to CMPCnm pin (n = channel number; m = 0 to 3)	• Input voltage to CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	• Input voltage to CVREFC0 or CVREFC1 pin or on-chip D/A converter output voltage	[Chip version A] • Input voltage to CVREFC0 or CVREFC1 pin or on-chip D/A converter 0 output voltage [Chip version B] • Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	• Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and POE source output, and comparison results can be read from registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output, POE source output, and GPT internal trigger source output, and comparison results can be read from registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output, POE source output, and GPT internal trigger source output, and comparison results can be read from registers.
Interrupt request	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.49 Comparison of Comparator C Registers

Register	Bit	RX23T (CMPC)	RX24T (CMPC)	RX24U (CMPC)
CMPSEL0	CMPSEL [3:0]	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: Internal reference voltage selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: Internal reference voltage selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: Internal reference voltage selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: CMPC23 selected Settings other than the above are prohibited.

Register	Bit	RX23T (CMPC)	RX24T (CMPC)	RX24U (CMPC)
CMPSEL0	CMPSEL [3:0]		• Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.	• Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 selected 0 0 1 0: CMPC31 selected 0 1 0 0: CMPC32 selected 1 0 0 0: CMPC33 selected Settings other than the above are prohibited.
CMPSEL1	CVRS [1:0]	Reference input voltage select bits • Comparator C0 and comparator C1 b1 b0 0 0: No input 0 1: Input to CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter output selected as reference input voltage Settings other than the above are prohibited. • Comparator C2 b1 b0 0 0: No input 0 1: Input to CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter output selected as reference input voltage Settings other than the above are prohibited.	Reference input voltage select bits [Chip version A] • Comparator C1 to comparator C3 b1 b0 0 0: No input 0 1: Input to CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited. • Comparator C0 b1 b0 0 0: No input 0 1: Input to CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited.	Reference input voltage select bits

Register	Bit	RX23T (CMPC)	RX24T (CMPC)	RX24U (CMPC)
CMPSEL1	CVRS [1:0]		[Chip version B] b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited.	b1 b0 0 0: No input 0 1: On-chip D/A converter 1 output selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited.
CMPC0.CMPIOC	VREFEN	Internal reference voltage on/off control bit	—	—

2.20 RAM

Table 2.50 is a comparative overview of RAM.

Table 2.50 Comparative Overview of RAM

Item	RX23T	RX24T	RX24U
RAM capacity	12 KB (RAM0: 12 KB)	Up to 32 KB (RAM0: 32 KB)	32 KB (RAM0: 32 KB)
RAM address	RAM0: 0000 0000h to 0000 27FFh, 0000 4000h to 0000 4A7Fh	• When the RAM capacity is 32 KB RAM0: 0000 0000h to 0000 7FFFh • When the RAM capacity is 16 KB RAM0: 0000 0000h to 0000 3FFFh	RAM0: 0000 0000h to 0000 7FFFh
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to set module stop state for RAM0	Ability to set module stop state for RAM0	Ability to set module stop state for RAM0

2.21 Flash Memory

Table 2.51 is a comparative overview of flash memory, and Table 2.52 is a comparison of flash memory registers.

Table 2.51 Comparative Overview of Flash Memory

Item	RX23T	RX24T	RX24U
Memory capacity	• User area: Up to 128 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh
ROM cache	—	Capacity: 2 KB	Capacity: 2 KB
Software commands	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh

Item	RX23T	RX24T	RX24U
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area can be programmed. • Self-programming (single-chip mode) — The user area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.
Off-board programming	The user area can be programmed using a flash programmer compatible with the MCU.	The user area and data area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the MCU.	The user area and data area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the MCU.
ID codes protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes. • ROM codes can be used for control when connecting to a parallel programmer.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes. • ROM codes can be used for control when connecting to a parallel programmer.
Start-up program protection function	This function is used to safely program blocks 0 to 7.	This function is used to safely program blocks 0 to 7.	This function is used to safely program blocks 0 to 7.

Item	RX23T	RX24T	RX24U
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	—	Programs in the ROM can run while the E2 DataFlash is being programmed.	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.52 Comparison of Flash Memory Registers

Register	Bit	RX23T	RX24T/RX24U
DFLCTL	—	—	E2 data flash control register
FENTRYR	FENTRYD	—	E2 data flash P/E mode entry bit
FPMCR	FMS0	Flash operating mode select bit 0 FMS2 FMS1 FMS0 0 0 0: ROM read mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.	Flash operating mode select bit 0 FMS2 FMS1 FMS0 0 0 0: ROM/E2 data flash read mode 0 1 0: E2 data flash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.
FASR	EXS	Extra area select bit 0: User area 1: Extra area	Extra area select bit 0: User area, data area 1: Extra area
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register

2.22 Packages

As indicated in Table 2.53, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.53 Packages

Package Type	Renesas Code		
	RX23T	RX24T	RX24U
144-pin LFQFP	×	×	○
80-pin LQFP	×	○	×
80-pin LFQFP	×	○	×
64-pin LQFP	×	○	×
64-pin LFQFP	○	○	×
52-pin LQFP	○	×	×
48-pin LFQFP	○	×	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 100-Pin LFQFP Package (RX24T: Chip Version A)

Table 3.1 is comparative listing of the pin functions of 100-pin LFQFP package products (RX24T: chip version A). Note that the RX23T Group is not available in a 100-pin package version.

Table 3.1 Comparative Listing of 100-Pin LFQFP Package Pin Functions (RX24T: Chip Version A)

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
1	PE5/IRQ0	PE5/IRQ0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0
3	VSS	VSS
4	P00/IRQ2/ADST1	P00/IRQ2/ADST1
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/POE12#/IRQ4/ADST2
8	PE4/MTCLKC/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/SSLA1
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/IRQ3	PD5/TMRI0/TMRI6/GTECLKA/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ3
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/IRQ2
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	PD3/TMO0/GTECLKC/TXD1/SMOSI1/SSDA1/TXD11/SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/SCK5/MOSIA	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/SCK5/MOSIA
24	PD1/TMO2/MISOA	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA
25	PD0/TMO6/RSPCKA	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA
26	PB7/SCK5	PB7/GTIOC1B/GTIOC1B#/SCK5

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/SSCL5/IRQ5
28	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/SSDA5
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRG/GTECLKD/CTS5#/RTS5#/SS5#/IRQ3
31	VSS	VSS
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/RSPCKA
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/TXD6/SMOSI6/SSDA6/SDA0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/RXD6/SMISO6/SSCL6/SCL0
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/SMOSI6/SSDA6/MOSIA/ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ADTRG0#	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/RSPCKA/ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/GTADSM0/SSLA0
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/SSLA1	PA2/MTIOC2B/MTIOC2B#/TMO7/GTADSM1/CTS6#/RTS6#/SS6#/SSLA1
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/CRXD0/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/CTXD0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/POE4#/IRQ4
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#
51	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC2B#
52	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC1B#
53	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC0B#
54	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC2A#
55	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC1A#
56	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC0A#
57	P70/POE0#/IRQ5	P70/POE0#/IRQ5

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/ IRQ6	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/MTIOC1A/MTIOC1A#
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116
69	P65/AN205	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016
70	P64/AN204	P65/AN205
71	AVCC2	P64/AN204
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/AN203/IRQ7
75	P62/AN202/IRQ6	P62/AN202/IRQ6
76	P61/AN201/IRQ5	P61/AN201/IRQ5
77	P60/AN200/IRQ4	P60/AN200/IRQ4
78	P55/AN211/IRQ3	P55/AN211/IRQ3
79	P54/AN210/IRQ2	P54/AN210/IRQ2
80	P53/AN209/IRQ1	P53/AN209/IRQ1
81	P52/AN208/IRQ0	P52/AN208/IRQ0
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31
84	P47/AN103	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002
89	P42/AN002	P41/AN001
90	P41/AN001	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PGAVSS0

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/MTIC5U/MTIC5U#/TMO4/SCK6
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0

3.2 100-Pin LFQFP Package (RX24T: Chip Version B)

Table 3.2 is comparative listing of the pin functions of 100-pin LFQFP package products (RX24T: chip version B). Note that the RX23T Group is not available in a 100-pin package version.

Table 3.2 Comparative Listing of 100-Pin LFQFP Package Pin Functions (RX24T: Chip Version B)

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
1	PE5/IRQ0	PE5/IRQ0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/ SS1#/IRQ5/ADST0	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/ SS1#/IRQ5/ADST0
3	VSS	VSS
4	P00/IRQ2/ADST1	P00/IRQ2/ADST1
5	VCL	VCL
6	MD/FINED	MD/FINED
7	P01/POE12#/IRQ4/ADST2	P01/POE12#/IRQ4/ADST2
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/SSLA3	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/SSLA3
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ RXD5/SMISO5/SSCL5/SSLA2	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ RXD5/SMISO5/SSCL5/SSLA2
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/ GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/ SSLA1	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/ GTIOC3A/GTIOC3A#/TXD5/SMOSI5/SSDA5/ SSLA1
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/SSLA0/ IRQ5/ADST0	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/ RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/SSCL11/ IRQ3
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/ IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA
26	PB7/GTIOC1B/GTIOC1B#/SCK5	PB7/GTIOC1B/GTIOC1B#/SCK5
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5
29	VCC	VCC

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/POE4#/IRQ4
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC6B#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC7A#
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC7B#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6D#
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#
57	P70/POE0#/IRQ5	P70/POE0#/IRQ5
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2
60	VCC	VCC

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P27/MTIOC1A/MTIOC1A#
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116
69	P65/AN205	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016
70	P64/AN204	P65/AN205
71	AVCC2	P64/AN204
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/AN203/IRQ7
75	P62/AN202/IRQ6	P62/AN202/IRQ6
76	P61/AN201/IRQ5	P61/AN201/IRQ5
77	P60/AN200/IRQ4	P60/AN200/IRQ4
78	P55/AN211/IRQ3	P55/AN211/IRQ3
79	P54/AN210/IRQ2	P54/AN210/IRQ2
80	P53/AN209/IRQ1	P53/AN209/IRQ1
81	P52/AN208/IRQ0	P52/AN208/IRQ0
82	P51/AN207	P47/AN103
83	P50/AN206	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31
84	P47/AN103	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	PGAVSS1
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003
88	P43/AN003	P42/AN002
89	P42/AN002	P41/AN001
90	P41/AN001	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	PGAVSS0
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1

100-Pin LFQFP	RX24T (Chip Version A)	RX24U
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/MTIC5U/MTIC5U#/TMO4/SCK6
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0

3.3 64-Pin LFQFP Package

Table 3.3 is comparative listing of the pin functions of 64-pin LFQFP package products. Note that the RX24U Group is not available in a 64-pin package version.

Table 3.3 Comparative Listing of 64-Pin LFQFP Package Pin Functions

64-Pin LFQFP	RX23T	RX24T
1	P02/CTS1#/RTS1#/SS1#/ADST0/IRQ5	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ ADST0
2	P00/IRQ2	P00/IRQ2/ADST1
3	VCL	VCL
4	P01/CACREF/IRQ4	MD/FINED
5	MD/FINED	P01/POE12#/IRQ4/ADST2
6	RES#	RES#
7	XTAL/P37	XTAL/P37
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36
10	VCC	VCC
11	PE2/POE10#/NMI	PE2/POE10#/NMI
12	PD7/TMRI1/SSLA1	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1
13	PD6/TMO1/SSLA0/CTS1#/RTS1#/SS1#/ ADST0/IRQ5	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#
14	PD5/TMRI0/RXD1/SMISO1/SSCL1/IRQ3	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1
15	PD4/TMCI0/SCK1/IRQ2	PD4/TMCI0/TMCI6/SCK1/IRQ2
16	PD3/TMO0/TXD1/SMOSI1/SSDA1	PD3/TMO0/TXD1/SMOSI1/SSDA1
17	PB7/SCK5	PB6/RXD5/SMISO5/SSCL5/IRQ5
18	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB5/TXD5/SMOSI5/SSDA5
19	PB5/TXD5/SMOSI5/SSDA5	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3
20	VCC	PB3/MTIOC0A/CACREF/SCK6/RSPCKA
21	PB4/POE8#/IRQ3	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0
22	VSS	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0
23	PB3/MTIOC0A/CACREF/SCK5/RSPCKA	VCC
24	PB2/MTIOC0B/ADSM0/TXD5/SMOSI5/ SSDA5/SDA0	P96/POE4#/IRQ4
25	PB1/MTIOC0C/RXD5/SMISO5/SSCL5/ SCL0/IRQ2	VSS
26	PB0/MTIOC0D/MOSIA	P95/MTIOC6B
27	PA3/MTIOC2A/SSLA0	P94/MTIOC7A
28	PA2/MTIOC2B/CTS5#/RTS5#/SS5#/SSLA1/ IRQ4	P93/MTIOC7B
29	P94/MTIOC0C/TMO1/MISOA/IRQ1	P92/MTIOC6D
30	P93/MTIOC0B/TMRI1/SCK5/RSPCKA/IRQ0	P91/MTIOC7C
31	P92/TMCI1/SSLA2	P90/MTIOC7D
32	P91/SSLA3	P76/MTIOC4D
33	P76/MTIOC4D	P75/MTIOC4C
34	P75/MTIOC4C	P74/MTIOC3D
35	P74/MTIOC3D	P73/MTIOC4B
36	P73/MTIOC4B	P72/MTIOC4A
37	P72/MTIOC4A	P71/MTIOC3B

64-Pin LFQFP	RX23T	RX24T
38	P71/MTIOC3B	P70/POE0#/IRQ5
39	P70/POE0#/IRQ5	VCC
40	P33/MTIOC3A/MTCLKA/SSLA3	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/IRQ6
41	P32/MTIOC3C/MTCLKB/SSLA2	VSS
42	VCC	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3
43	P31/MTIOC0A/MTCLKC/SSLA1	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0
44	VSS	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1
45	P30/MTIOC0B/MTCLKD/SSLA0	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2
46	P24/MTIC5U/TMCI2/RSPCKA/COMP0/IRQ3	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1
47	P23/MTIC5V/CACREF/TMO2/MOSIA/ COMP1/IRQ4	AVCC2/VREF
48	P22/MTIC5W/TMRI2/MISOA/COMP2/IRQ2	AVSS2
49	P47/AN007/CMPC12/CMPC22	P54/AN210/IRQ2
50	P46/AN006/CMPC02	P53/AN209/IRQ1
51	P45/AN005/CMPC21	P52/AN208/IRQ0
52	P44/AN004/CMPC11	P51/AN207
53	P43/AN003/CMPC01	P50/AN206
54	P42/AN002/CMPC20	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31
55	P41/AN001/CMPC10	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21
56	P40/AN000/CMPC00	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33
57	AVCC0	P42/AN002
58	VREFH0	P41/AN001
59	VREFL0	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23
60	AVSS0	AVCC1
61	P11/MTIOC3A/MTCLKC/TMO3/IRQ1/ AN016/CVREFC0	AVCC0
62	P10/MTCLKD/TMRI3/IRQ0/AN017/ CVREFC1	AVSS0
63	PA5/MTIOC1A/TMCI3/MISOA	AVSS1
64	PA4/MTIOC1B/RSPCKA/ADTRG0#	P11/MTIOC3A/MTCLKC/TMO3/IRQ1

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX24T/RX24U Group and the RX23T Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

4.1.1 Inserting Decoupling Capacitor between AVCC and AVSS Pins

To prevent destruction of the RX24T/RX24U Group's analog input pins (AN000 to AN003, AN100 to AN103, AN200 to AN211, AN016, and AN116) by abnormal voltage such as an excessive surge, insert capacitors between AVCCn and AVSSn and between VREFHn and VREFLn, and connect a protective circuit to protect the analog input pins (AN000 to AN003, AN100 to AN103, AN200 to AN211, AN016, and AN116).

For details, refer to "Notes on Noise Prevention" in the 12-Bit A/D Converter section of RX24T/RX24U Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2 Notes on Functional Design

Some software that runs on the RX23T Group is compatible with the RX24T/RX24U Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX24T/RX24U Group and RX23T Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.2.1 Operation of Main Clock Oscillation Stop Detection Function

When the oscillation stop detection function detects that the main clock oscillator has stopped, it outputs a low-speed clock from the low-speed on-chip oscillator as the clock source of the system clock in place of the main clock.

Note that on the RX24T/RX24U Group, if the HOCO clock is selected as the PLL clock source and the PLL clock is selected as the clock source of the system clock, the system clock does not switch to the LOCO clock even if oscillation stop of the main clock is detected.

4.2.2 Initializing the Port Direction Register (PDR)

The method of initializing the PDR differs, even on products with the same pin count.

4.2.3 Buffer Register Setting Values in Complementary PWM Mode

When using the double buffering function in complementary PWM mode of multi-function timer pulse unit 3, the PWM output to the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) should be set to "duty value − 1" on the RX23T Group, but on the RX24T/RX24U Group a duty value should be specified for PWM output.

4.2.4 Control of Output Disabling Request Issuance by Port Output Enable 3

When an output disabling request is generated on the RX24T/RX24U Group, the pins for which the corresponding bits in the POECR1 to POECR3 and POECR7 registers have been set to 1 enter the high-impedance state and the pins for which the corresponding bits in the PMMCR0 to PMMCR3 registers have been set to 1 are switched to general I/O port operation.

If bits in both sets of registers corresponding to the same pins have been set to 1, the POECR1 to POECR3 and POECR7 registers take priority and the pins enter the high-impedance state.

After a switch to general I/O port operation, the pin state is determined by the settings of the PDR and PODR registers.

Note that on the RX24T Group the POECR3 and PMMCR0 to PMMCR3 registers are implemented on chip version B only.

4.2.5 Active Level Setting when MTU Inverted Output Is Specified

On the RX24T Group (chip version B) and RX24U Group the MPC.PmnPFS register can be used to select either non-inverted or inverted output from the MTU. When inverted output is selected, the active level set in the MTU.TOCR1j and MTU.TOCR2j registers (j = A and B), and the active level output on the pins, is inverted. In this case, when using the output short-circuit detection function on POE3, use the signals output on the pins as the standard when setting the active level in the ALR1 to ALR3 registers.

4.2.6 D/A Converter Voltage Relationships

On the RX24T Group (chip version B) the voltages of VREF and VCC, and on the RX24U Group the voltages of AVCC2 and VCC, can be set independently, subject to the following limitation:

- When using the P23 and P24 pins as the D/A converter output pins, ensure that the output voltage of the D/A converter is higher than the VCC voltage.
- This limitation does not apply when pins other than P23 and P24 are used as the D/A converter output pins.

4.2.7 Comparator C Operation with 12-Bit A/D Converter in Module Stop State

On the RX24T/RX24U Group both the programmable gain amplifier (PGA) and the 12-bit A/D converter are controlled by the same module stop signal, so comparator C cannot compare the PGA outputs listed below when the 12-bit A/D converter is in the module stop state.

- AN000 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

The analog pins listed below are connected directly to the comparator, so they can be compared even when the 12-bit A/D converter is in the module stop state.

- AN000 pin
- AN100 pin
- AN101 pin
- AN102 pin

4.2.8 ROM Cache

The RX24T/RX24U Group has a 2 KB ROM cache, but the operation of the ROM cache is disabled after a reset. To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

5. Reference Documents

User's Manual: Hardware

RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24T Group User's Manual: Hardware Rev.2.00 (R01UH0576EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24U Group User's Manual: Hardware Rev.1.00 (R01UH0658EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A151A/E

TN-RX*-A163A/E

TN-RX*-A173A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A200A/E

TN-RX*-A0206A/E

TN-RX*-A0213A/E

TN-RX*-A0216A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 20, 2020	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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