RX13T Group, RX23T Group

Differences Between the RX13T Group and the RX23T Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX13T Group and RX23T Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 48-pin package version of the RX13T Group and the 64-pin package version of the RX23T Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX13T Group and RX23T Group

Contents

1. Comparison of Built-In Functions of RX13T Group and RX23T Group

A comparison of the built-in functions of the RX13T Group and RX23T Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX13T Group and RX23T Group.

Table 1.1 Comparison of Built-In Functions of RX13T Group and RX23T Group

Function	RX23T	RX13T
CPU		■
Operating modes		○
Address space		▲
Resets		○
Option-setting memory (OFSM)		●
Voltage detection circuit (LVDAb)		●
Clock generation circuit		■
Clock frequency accuracy measurement circuit (CAC)		○
Low power consumption		▲
Register write protection function		●/■
Exception handling		■
Interrupt controller (ICUb)		▲
Buses		▲/■
Memory-protection unit (MPU)	○	×
Data transfer controller (DTCa): RX23T, (DTCb): RX13T		●
I/O ports		●
Multi-function pin controller (MPC)		●/▲/■
Multi-function timer pulse unit 3 (MTU3c)		■
Port output enable 3 (POE3b): RX23T, (POE3C): RX13T		▲
8-bit timer (TMR)	○	×
Compare match timer (CMT)		■
Independent watchdog timer (IWDTa)		○
Serial communications interface (SCIg): RX23T, (SCIg, SCIh): RX13T		●
I^2C bus interface (RIICa)		○
Serial peripheral interface (RSPIa)	○	×
CRC calculator (CRC)		○
12-bit A/D converter (S12ADE): RX23T, (S12ADF): RX13T		●/■
D/A converter for generating comparator C reference voltage (DA)		○
Comparator C (CMPC)		●/■
Data operation circuit (DOC)		○
RAM		▲
Flash memory (FLASH)		●
Packages		●/■

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX23T	RX13T
CPU	• Maximum operating frequency: 40 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit register • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit registers • Basic instructions: 73, variable-length instruction format • Floating point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX23T	RX13T
EXTB	—	Exception table register	—
ACC0, ACC1 (RX23T) ACC (RX13T)	—	Accumulator 0, accumulator 1	Accumulator

2.2 Address Space

Figure 2.1 is a comparative memory map of single-chip mode.

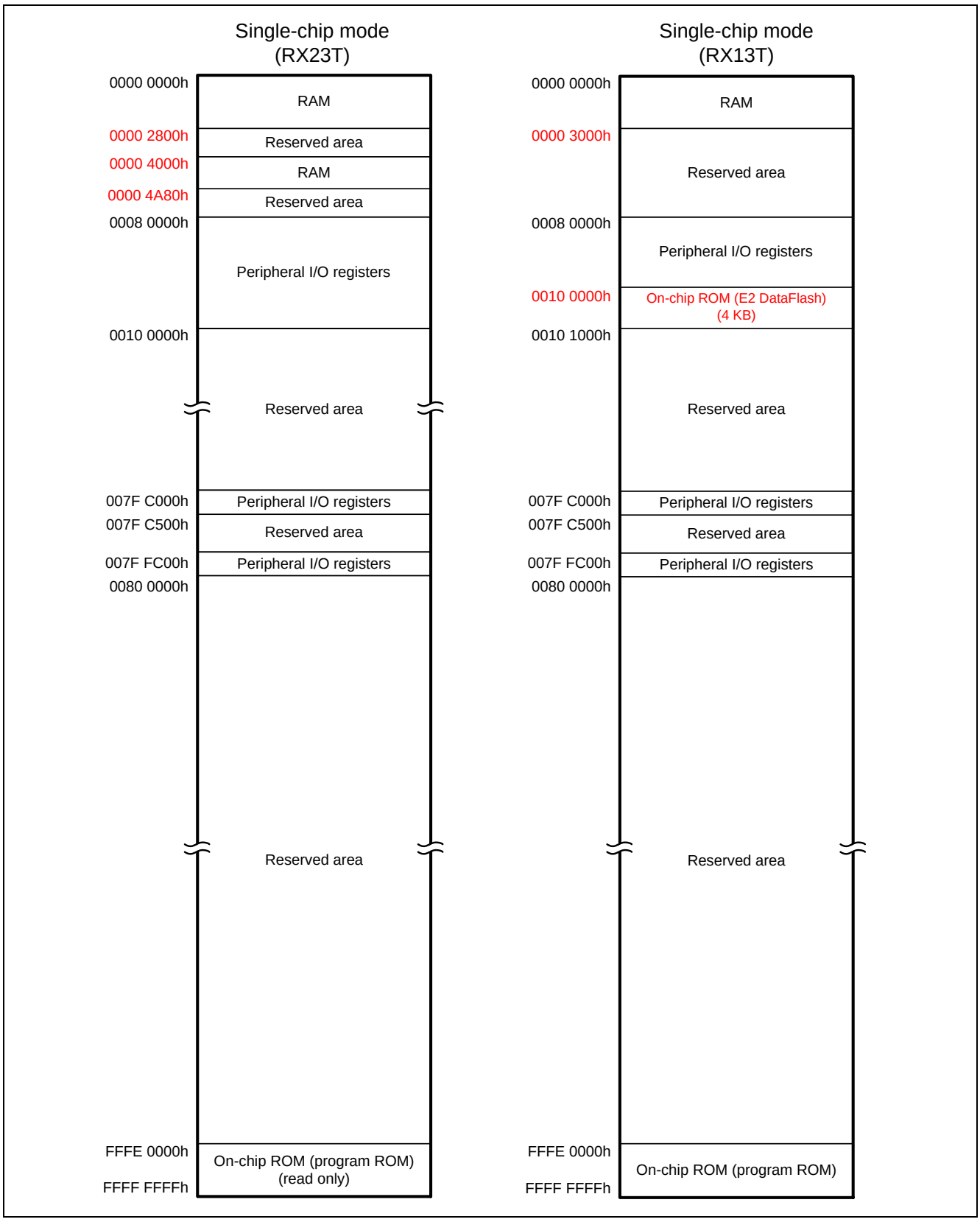

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Option-Setting Memory

Table 2.3 is a comparison of option-setting memory registers.

Table 2.3 Comparison of Option-Setting Memory Registers

Register	Bit	RX23T	RX13T (OFSM)
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 1 0: 2.51 V is selected Do not set a value other than those above when using the voltage detection 0 circuit.	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Do not set a value other than those above when using the voltage detection 0 circuit.

2.4 Voltage Detection Circuit

Table 2.4 is a comparative overview of the voltage detection circuits.

Table 2.4 Comparative Overview of Voltage Detection Circuits

Item		RX23T (LVDAb)			RX13T (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	Voltage selectable from two levels using OFS1 register	Voltage selectable from nine levels using the LVDLVLR.LVD1 LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2 LVL[1:0] bits	Voltage selectable from three levels using OFS1 register	Voltage selectable from nine levels using the LVDLVLR.LVD1 LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2 LVL[1:0] bits
	Monitor flag	—	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection		LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable is selectable	Non-maskable or maskable is selectable		Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either

2.5 Clock Generation Circuit

Table 2.5 is a comparative overview of the clock generation circuits, and Table 2.6 is a comparison of clock generation circuit registers.

Table 2.5 Comparative Overview of Clock Generation Circuits

Item	RX23T	RX13T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules, PCLKA is the operating clock for the MTU3, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than MTU3 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD and PCLKB is the operating clock for modules other than MTU2 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
Operating frequency	• ICLK: 40 MHz (max.) • PCLKA: 40 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz	• ICLK: 32 MHz (max.)*1 • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz
Main clock oscillator*2	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function

Item	RX23T	RX13T
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 10 (increments of 0.5) • Oscillation frequency: 24 MHz to 40 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Notes: 1. Make settings such that the division ratios for ICLK:FCLK, ICLK:PCLKB, and ICLK:PCLKD = 1:N (where N is an integer).
2. On the RX13T Group, set the main clock oscillator to 8 MHz or 16 MHz when the PLL is oscillating at 32 MHz.

Table 2.6 Comparison of Clock Generation Circuit Registers

Register	Bit	RX23T	RX13T
SCKCR	—	System clock control register	System clock control register
		The value after a reset differs.	
	PCKA[3:0]	Peripheral module clock A (PCLKA) select bits	—
	—	Reserved bits (b19 to b16) Set these bits to match the setting value of the ICK[3:0] or PCKB[3:0] bits, whichever corresponds to a higher frequency.	Reserved bits (b19 to b16) These bits are read as 0. The write value should be 0.
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Settings other than the above are prohibited.
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—
LOCOTRR	—	—	Low-speed on-chip oscillator trimming register
ILOCOTRR	—	—	IWDT dedicated on-chip oscillator trimming register
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0)
MEMWAIT	—	Main wait cycle setting register	—

2.6 Low Power Consumption

Table 2.7 is a comparative overview of the low power consumption functions, and Table 2.8 is a comparison of low power consumption registers.

Table 2.7 Comparative Overview of Low Power Consumption Functions

Item	RX23T	RX13T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode

Table 2.8 Comparison of Low Power Consumption Registers

Register	Bit	RX23T	RX13T
SBYCR	—	Reserved bit (b14) This bit is read as 1. The write value should be 1.	Reserved bit (b14) These bit is read as 0. The write value should be 0.
MSTPCRA	MSTPA4	8-bit timer 3 and 2 (unit 1) module stop bit	—
	MSTPA5	8-bit timer 1 and 0 (unit 0) module stop bit	—
	MSTPA14	Compare match timer 1 (unit 1) module stop bit	—
MSTPCRB	MSTPB4	—	Serial communication interface SCIh module stop bit
	MSTPB17	Serial peripheral interface 0 module stop bit	—

2.7 Register Write Protection Function

Table 2.9 is a comparative overview of the register write protection functions, and Table 2.10 is a comparison of register write protection function registers.

Table 2.9 Comparative Overview of Register Write Protection Functions

Item	RX23T	RX13T
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, MEMWAIT	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the clock generation circuit: HOCOWTCR	—
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.10 Comparison of Register Write Protection Function Registers

Register	Bit	RX23T	RX13T
PRCR	PRC2	Protect bit 2	—

2.8 Exception Handling

Table 2.11 is a comparative overview of exception handling, Table 2.12 is a comparison of vectors, and Table 2.13 is a comparison of instructions for returning from exception handling routines.

Table 2.11 Comparative Overview of Exception Handling

Item	RX23T	RX13T
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.12 Comparison of Vectors

Item		RX23T	RX13T
Undefined instruction exception		Exception vector table (EXTB)	Fixed vector table
Privileged instruction exception		Exception vector table (EXTB)	Fixed vector table
Access exception		Exception vector table (EXTB)	—
Floating-point exception		Exception vector table (EXTB)	Fixed vector table
Reset		Exception vector table (EXTB)	Fixed vector table
Non-maskable interrupt		Exception vector table (EXTB)	Fixed vector table
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Interrupt vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Interrupt vector table (INTB)	Relocatable vector table (INTB)

Table 2.13 Comparison of Instructions for Returning from Exception Handling Routines

Item		RX23T	RX13T
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	—
Floating-point exception		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Prohibited	Return not possible
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.9 Interrupt Controller

Table 2.14 is a comparison of interrupt controller registers.

Table 2.14 Comparison of Interrupt Controller Registers

Register	Bit	RX23T (ICUb)	RX13T (ICUb)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 255)
DTCERn*1	—	DTC activation enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 027 to 255)

Note: 1. On both the RX23T Group and RX13T Group n = 250 to 255 are reserved areas.

2.10 Buses

Table 2.15 is a comparative overview of the buses, and Table 2.16 is a comparison of bus registers.

Table 2.15 Comparative Overview of Buses

Bus Type		RX23T	RX13T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)
	Internal peripheral bus 3	• Connected to peripheral modules (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3) • Operates in synchronization with the peripheral-module clock (PCLKA)	—

Bus Type		RX23T	RX13T
Internal peripheral buses	Internal peripheral bus 6	• Connected to the flash control module • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.16 Comparison of Bus Registers

Register	Bit	RX23T	RX13T
BUSPRI	BPHB[1:0]	Internal peripheral bus 4 priority control bits	—

2.11 Data Transfer Controller

Table 2.17 is a comparative overview of the data transfer controllers, and Table 2.18 is a comparison of data transfer controller registers.

Table 2.17 Comparative Overview of Data Transfer Controllers

Item	RX23T (DTCa)	RX13T (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX23T (DTCa)	RX13T (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt sources	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Read skip	Ability to specify that reading of transfer information is skipped	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Ability to skip write-back of transferred data when the transfer source address or transfer destination address is fixed	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.18 Comparison of Data Transfer Controller Registers

Register	Bit	RX23T (DTCa)	RX13T (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.12 I/O Ports

Table 2.19 is a comparative overview of the I/O ports of 48-pin products, Table 2.20 is a comparison of I/O port functions, and Table 2.21 is a comparison of I/O port registers.

Table 2.19 Comparative Overview of I/O Ports of 48-Pin Products

Port Symbol	RX23T (48-Pin)	RX13T (48-Pin)
PORT1	P10, P11	P10, P11
PORT2	P22 to P24	P22 to P24
PORT3	P36, P37	P36, P37
PORT4	P40 to P47	P40 to P47
PORT7	P70 to P76	P70 to P76
PORT9	P93, P94	P93, P94
PORTA	PA2, PA3	PA2, PA3
PORTB	PB0 to PB6	PB0 to PB7
PORTD	PD3 to PD6	PD3 to PD6
PORTE	PE2	PE2

Table 2.20 Comparison of I/O Port Functions

Item	Port Symbol	RX23T	RX13T
Input pull-up function	PORT0	P00, P01, P02	—
	PORT1	P10, P11	P10, P11
	PORT2	P22, P23, P24	P22, P23, P24
	PORT3	P30 to P33, P36, P37	P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT7	P70 to P76	P70 to P76
	PORT9	P91 to P94	P93, P94
	PORTA	PA2 to PA5	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTD	PD3 to PD7	PD3 to PD6
Open-drain output function	PORT0	P00, P01, P02	—
	PORT1	P10, P11	P10, P11
	PORT2	P22, P23, P24	P22, P23, P24
	PORT3	P30 to P33, P36, P37	P36, P37
	PORT7	P70 to P76	P70 to P76
	PORT9	P91 to P94	P93, P94
	PORTA	PA2 to PA5	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTD	PD3 to PD7	PD3 to PD6
Drive capacity switching function	PORT0	P00, P01, P02	—
	PORT1	P10, P11	P10, P11
	PORT2	P22, P23, P24	P22, P23, P24
	PORT3	P30 to P33, P36, P37	—
	PORT4	P40 to P47	P40 to P47
	PORT7	P70 to P76	P70 to P76
	PORT9	P91 to P94	P93, P94
	PORTA	PA2 to PA5	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTD	PD3 to PD7	PD3 to PD6

Item	Port Symbol	RX23T	RX13T
High current pin	PORT7	P71 to P76	P71 to P76
	PORTB	PB5	PB6
	PORTD	PD3	—
5 V tolerant	PORTB	PB1, PB2	PB1, PB2

Table 2.21 Comparison of I/O Port Registers

Register	Bit	RX23T	RX13T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 I/O select bits (m = 1 to 4, 7, 9, A, B, D)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 output data store bits (m = 1 to 4, 7, 9, A, B, D)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 bits (m = 1 to 4, 7, 9, A, B, D)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 3, 7, 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 1 to 3, 7, 9, A, B, D, E)
ODR0	B0 (RX23T) B0, B1 (RX13T)	Pm0 output type select bit (m = 0 to 3, 7, 9, A, B, D) 0: CMOS output 1: N-channel open-drain	Pm0 output type select bit (m = 1, 2, 7, 9, A, B, D) • P10, P70 b0 0: CMOS output 1: N-channel open-drain b1 This bit is read as 0. The write value should be 0. • PB0 b1 b0 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z
	B2	Pm1 output type select bits (m = 0 to 3, 7, 9, A, B, D)	Pm1 output type select bits (m = 1, 2, 7, 9, A, B, D)
	B4	Pm2 output type select bit (m = 0 to 3, 7, 9, A, B, D)	Pm2 output type select bits (m = 1, 2, 7, 9, A, B, D)
	B6	Pm3 output type select bit (m = 0 to 3, 7, 9, A, B, D)	Pm3 output type select bit (m = 1, 2, 7, 9, A, B, D)
ODR1	B0	Pm4 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm4 output type select bit (m = 2, 3, 7, 9, B, D)
	B2	Pm5 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm5 output type select bit (m = 2, 3, 7, 9, B, D)
	B4	Pm6 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm6 output type select bit (m = 2, 3, 7, 9, B, D)
	B6	Pm7 output type select bit (m = 2, 3, 7, 9, A, B, D)	Pm7 output type select bit (m = 2, 3, 7, 9, B, D)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 4, 7, 9, A, B, D)	Pm0 to Pm7 input pull-up resistor control bits (m = 1 to 4, 7, 9, A, B, D)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7, 9, A, B, D)	Pm0 to Pm7 drive capacity control bits (m = 1, 2, 7, 9, A, B, D)

2.13 Multi-Function Pin Controller

Table 2.22 is a comparison of the assignments of multiplexed pins, and Table 2.23 to Table 2.32 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX13T Group only and **orange text** pins that exist on the RX23T Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.22 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 48-Pin	RX13T (MPC) 48-Pin
Interrupt	NMI (input)	PE2	○	○
	IRQ0 (input)	P10	○	○
		P93	○	○
		PE2	×	○
	IRQ1 (input)	P11	○	○
		P94	○	○
	IRQ2 (input)	P22	○	○
		PB1	○	○
		PD4	○	○
	IRQ3 (input)	P24	○	○
		PB4	○	○
		PD5	○	○
	IRQ4 (input)	P23	○	○
		PA2	○	○
	IRQ5 (input)	P70	○	○
		PB7	×	○
		PB6	○	×
		PD6	○	○
Multi-function timer unit 3	MTIOC0A (input/output)	PB3	○	○
		PD3	×	○
	MTIOC0B (input/output)	P93	○	×
		PB2	○	○
		PD4	×	○
	MTIOC0C (input/output)	P94	○	×
		PB1	○	○
		PD5	×	○
	MTIOC0D (input/output)	PB0	○	○
		PD6	×	○
	MTIOC1A (input/output)	P93	×	○
		PA2	×	○
	MTIOC1B (input/output)	PA3	×	○
		PB6	×	○
	MTIOC2A (input/output)	PA3	○	○
		PB0	×	○
	MTIOC2B (input/output)	PA2	○	○
		P94	×	○
	MTIOC3A (input/output)	P11	○	○
		PB6	×	○
	MTIOC3B (input/output)	P71	○	○
	MTIOC3C (input/output)	PB7	×	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 48-Pin	RX13T (MPC) 48-Pin
Multi-function timer unit 3	MTIOC3D (input/output)	P74	○	○
	MTIOC4A (input/output)	P72	○	○
	MTIOC4B (input/output)	P73	○	○
	MTIOC4C (input/output)	P75	○	○
	MTIOC4D (input/output)	P76	○	○
	MTIC5U (input)	P24	○	○
		P94	×	○
	MTIC5V (input)	P23	○	○
		P93	×	○
	MTIC5W (input)	P22	○	○
		PB1	×	○
	MTCLKA (input)	P11	×	○
		P94	×	○
		PB1	×	○
	MTCLKB (input)	P10	×	○
		PB0	×	○
	MTCLKC (input)	P11	○	×
		PB2	×	○
	MTCLKD (input)	P10	○	×
		PB7	×	○
	ADSM0 (output)	PB2	○	○
8-bit timer	TMO0 (output)	PD3	○	
	TMCI0 (input)	PD4	○	
		PD5	○	
	TMO1 (output)	P94	○	
		PD6	○	
	TMRI1 (input)	P93	○	
	TMO2 (output)	P23	○	
	TMCI2 (input)	P24	○	
	TMRI2 (input)	P22	○	
	TMO3 (output)	P11	○	
	TMRI3 (input)	P10	○	
Port output enable 3	POE0# (input)	P70	○	○
	POE8# (input)	PB4	○	○
		P11	×	○
	POE10# (input)	PE2	○	○
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○
		PB7	×	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○
		PB6	×	○
	SCK1 (input/output)	PD4	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	PD6	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PB1	○	○
		PB6	○	×
		PB7	×	○
		P24	×	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 48-Pin	RX13T (MPC) 48-Pin
Serial communications interface	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PB2	○	○
		PB5	○	×
		PB6	×	○
		P23	×	○
	SCK5 (input/output)	P93	○	○
		PB3	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA2	○	○
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P94		○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PB0		○
	SCK12 (input/output)	PB3		○
		P93		○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PA3		○
I²C bus interface	SCL0 (input/output)	PB1	○	○
	SDA0 (input/output)	PB2	○	○
Serial peripheral interface	RSPCKA (input/output)	P24	○	
		P93	○	
		PB3	○	
	MOSIA (input/output)	P23	○	
		PB0	○	
	MISOA (input/output)	P22	○	
		P94	○	
	SSLA0 (input/output)	PA3	○	
		PD6	○	
	SSLA1 (output)	PA2	○	
12-bit A/D converter	AN000 (input)	P40	○	○
	AN001 (input)	P41	○	○
	AN002 (input)	P42	○	○
	AN003 (input)	P43	○	○
	AN004 (input)	P44	○	○
	AN005 (input)	P45	○	○
	AN006 (input)	P46	○	○
	AN007 (input)	P47	○	○
	AN016 (input)	P11	○	
	AN017 (input)	P10	○	
	ADTRG0# (input)	P93	×	○
		PB5	×	○
	ADST0 (output)	PD6	○	○

Module/ Function	Pin Function	Port Allocation	RX23T (MPC) 48-Pin	RX13T (MPC) 48-Pin
Clock frequency accuracy measurement circuit	CACREF (input)	P23	○	○
		PB3	○	○
Comparator	CMPC00 (input)	P40	○	○
	CMPC01 (input)	P43	○	
	CMPC02 (input)	P46	○	×
		P43	×	○
	CMPC03 (input)	P46		○
	CMPC10 (input)	P41	○	○
	CMPC11 (input)	P44	○	
	CMPC12 (input)	P47	○	×
		P44	×	○
	CMPC13 (input)	P47		○
	CMPC20 (input)	P42	○	○
	CMPC21 (input)	P45	○	
	CMPC22 (input)	P47	○	×
		P45	×	○
	COMP0 (output)	P24	○	○
	COMP1 (output)	P23	○	○
	COMP2 (output)	P22	○	○
	CVREFC0 (input)	P11	○	○
	CVREFC1 (input)	P10	○	

Table 2.23 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX23T (MPC)	RX13T (MPC)
P0nPFS	—	P0n pin function control register (n = 0 to 2)	—

Table 2.24 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX23T (MPC) (n = 0, 1)	RX13T (MPC) (n = 0, 1)
P10PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTCLKD 00101b: TMRI3	Pin function select bits 00000b: Hi-Z 00010b: MTCLKB
P11PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00101b: TMO3	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00111b: POE8#

Register	Bit	RX23T (MPC) (n = 0, 1)	RX13T (MPC) (n = 0, 1)
P1nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P10: AN017, CVREFC1 (64/52/48-pin) P11: AN016, CVREFC0 (64/52/48-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P11: CVREFC0 (48/32-pin)

Table 2.25 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX23T (MPC) (n = 2 to 4)	RX13T (MPC) (n = 2 to 4)
P22PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00101b: TMRI2 01101b: MISOA 11110b: COMP2	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 11110b: COMP2
P23PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00111b: CACREF 01010b: TXD5/SMOSI5/SSDA5 11110b: COMP1
P24PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI2 01101b: RSPCKA 11110b: COMP0	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 01010b: RXD5/SMISO5/SSCL5 11110b: COMP0

Table 2.26 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX23T (MPC)	RX13T (MPC)
P3nPFS	—	P3 pin function select register (n = 0 to 3)	—

Table 2.27 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX23T (MPC) (n = 0 to 7)	RX13T (MPC) (n = 0 to 7)
P4nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (64/52/48-pin) P41: AN001 (64/52/48-pin) P42: AN002 (64/52/48-pin) P43: AN003 (64/52/48-pin) P44: AN004 (64/52/48-pin) P45: AN005 (64/52/48-pin) P46: AN006 (64/52/48-pin) P47: AN007 (64/52/48-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000/CMPC00 (48/32-pin) P41: AN001/CMPC10 (48/32-pin) P42: AN002/CMPC20 (48/32-pin) P43: AN003/CMPC02 (48/32-pin) P44: AN004/CMPC12 (48/32-pin) P45: AN005/CMPC22 (48-pin) P46: AN006/CMPC03 (48-pin) P47: AN007/CMPC13 (48-pin)

Table 2.28 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX23T (MPC) (n = 1 to 4)	RX13T (MPC) (n = 3, 4)
P91PFS	—	P91 pin function control register	—
P92PFS	—	P92 pin function control register	—
P93PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMRI1 01010b: SCK5 01101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIC5V 01001b: ADTRG0# 01010b: SCK5 01100b: SCK12
P94PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO1 01101b: MISOA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTCLKA 00011b: MTIC5U 01100b: RXD12/SMISO12/ SSCL12/RXDX12

Table 2.29 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX23T (MPC) (n = 2 to 5)	RX13T (MPC) (n = 2, 3)
PA2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 01010b: CTS5#/RTS5#/SS5# 01101b: SSLA1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC2B 01010b: CTS5#/RTS5#/SS5#
PA3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 01101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC2A 01100b: CTS12#/RTS12#/SS12#
PA4PFS	—	PA4 pin function control register	—
PA5PFS	—	PA5 pin function control register	—

Table 2.30 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX23T (MPC) (n = 0 to 7)	RX13T (MPC) (n = 0 to 7)
PB0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 01101b: MOSIA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKB 00011b: MTIOC2A 01100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12
PB1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD5/SMISO5/SSCL5 01111b: SCL0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTCLKA 00011b: MTIC5W 01010b: RXD5/SMISO5/SSCL5 01111b: SCL0
PB2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 01001b: ADSM0 01010b: TXD5/SMOSI5/SSDA5 01111b: SDA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: ADSM0 00111b: TXD5/SMOSI5/SSDA5 01111b: SDA0
PB3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01100b: SCK12
PB5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5	Pin function select bits 00000b: Hi-Z 01001b: ADTRG0#
PB6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC3A 01010b: TXD5/SMOSI5/SSDA5 01011b: TXD1/SMOSI1/SSDA1

Register	Bit	RX23T (MPC) (n = 0 to 7)	RX13T (MPC) (n = 0 to 7)
PB7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: SCK5	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKD 01010b: RXD5/SMISO5/SSCL5 01011b: RXD1/SMISO1/SSCL1
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (64/52/48-pin) PB4: IRQ3 (64/52/48-pin) PB6: IRQ5 (64/52/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (48/32-pin) PB4: IRQ3 (48-pin) PB7: IRQ5 (48/32-pin)

Table 2.31 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX23T (MPC) (n = 3 to 7)	RX13T (MPC) (n = 3 to 6)
PD3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/SSDA1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 01010b: TXD1/SMOSI1/SSDA1
PD4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 01010b: SCK1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 01010b: SCK1
PD5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMRI0 01010b: RXD1/SMISO1/SSCL1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD1/SMISO1/SSCL1
PD6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/SS1# 01101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 01001b: ADST0 01010b: CTS1#/RTS1#/SS1#
PD7PFS	—	PD7 pin function select register	—

Table 2.32 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX23T (MPC) (n = 2)	RX13T (MPC) (n = 2)
PE2PFS	ISEL	—	Interrupt input function select bit

2.14 Multi-Function Timer Pulse Unit 3

Table 2.33 is a comparison of multi-function timer pulse unit 3 registers.

Table 2.33 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX23T (MTU3c)	RX13T (MTU3c)
TADSTRGR0	TADSTRS0 [4:0]	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation bits b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN	A/D conversion start request select for ADSM0 pin output frame synchronization signal generation bits b4 b0 0 0 0 0 0: Source not selected. 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 1 0 0: TRG4ABN

2.15 Port Output Enable 3

Table 2.34 is a comparison of port output enable 3 registers.

Table 2.34 Comparison of Port Output Enable 3 Registers

Register	Bit	RX23T (POE3b)	RX13T (POE3C)
POECR1	MTU0A1ZE	MTIOC0A P31 pin high-impedance enable bit	MTIOC0A (PD3) pin high-impedance enable bit
	MTU0B1ZE	MTIOC0B P30 pin high-impedance enable bit	MTIOC0B (PD4) pin high-impedance enable bit
	MTU0B2ZE (RX23T) MTU0C1ZE (RX13T)	MTIOC0B P93 pin high-impedance enable bit	MTIOC0C (PD5) pin high-impedance enable bit
	MTU0C1ZE (RX23T) MTU0D1ZE (RX13T)	MTIOC0C P94 pin high-impedance enable bit	MTIOC0D (PD6) pin high-impedance enable bit

2.16 Compare Match Timer

Table 2.35 is a comparison of compare match timer registers.

Table 2.35 Comparison of Compare Match Timer Registers

Register	Bit	RX23T (CMT)	RX13T (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.17 Serial Communications Interface

Table 2.36 is a comparative overview of the serial communications interfaces, and Table 2.37 is a comparison of serial communications interface channel specifications, and Table 2.38 is a comparison of serial communications interface registers.

Table 2.36 Comparative Overview of Serial Communications Interfaces

Item		RX23T (SCIg)	RX13T (SCIg, SCIh)
Number of channels		• SCIg: 2 channels	• SCIg: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5).	• An internal or external clock can be selected. • Transfer rate clock input from the MTU can be used (SCI1 and SCI5).

Item		RX23T (SCIg)	RX13T (SCIg, SCIh)
Asynchronous mode	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX23T (SCIg)	RX13T (SCIg, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	—	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	—	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	—	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.37 Comparison of Serial Communications Interface Channel Specifications

Item	RX23T (SCIg)	RX13T (SCIg, SCIh)
Synchronous mode	SCI1, SCI5	SCI1, SCI5, SCI12
Clock synchronous mode	SCI1, SCI5	SCI1, SCI5, SCI12
Smart card interface mode	SCI1, SCI5	SCI1, SCI5, SCI12
Simple I^2C mode	SCI1, SCI5	SCI1, SCI5, SCI12
Simple SPI mode	SCI1, SCI5	SCI1, SCI5, SCI12
Extended serial mode	—	SCI12
TMR clock input (RX23T)/ MTU clock input (RX13T)	SCI5	SCI1, SCI5, SCI12

Table 2.38 Comparison of Serial Communications Interface Registers

Register	Bit	RX23T (SCIg)	RX13T (SCIg, SCIh)
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 only) Available compare match output varies among SCI channels.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from MTU
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control field 0 data register
CF0CR	—	—	Control field 0 compare enable register
CF0RR	—	—	Control field 0 receive data register
PCF1DR	—	—	Primary control field 1 data register
SCF1DR	—	—	Secondary control field 1 data register
CF1CR	—	—	Control field 1 compare enable register
CF1RR	—	—	Control field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.18 12-Bit A/D Converter

Table 2.39 is a comparative overview of the 12-bit A/D converters, Table 2.40 is a comparison of 12-bit A/D converter registers, and Table 2.41 is a comparison of A/D conversion start triggers that can be set in the ADSTRGR register.

Table 2.39 Comparative Overview of 12-Bit A/D Converters

Item	RX23T (S12ADE)	RX13T (S12ADF)
Number of units	1 unit	1 unit (S12AD)
Input channels	10 channels	S12AD: 8 channels
Extended analog function	Internal reference voltage	Internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 40 MHz)	1.4 µs per channel (when A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 10 registers for analog input, one for A/D-converted data duplication in double trigger mode, and two for A/D-converted data duplication during extended operation in double trigger mode • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• 8 registers for analog input, one for A/D-converted data duplication in double trigger mode, and two for A/D-converted data duplication during extended operation in double trigger mode • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX23T (S12ADE)	RX13T (S12ADF)
Data register	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 10 channels arbitrarily selected. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 10 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 10 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of the arbitrarily selected channels. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of the arbitrarily selected. • Group scan mode: — The number of groups used is selectable between two (groups A and B) and three (groups A, B, and C). (When two is selected as the number of groups, only group A and group B may be used in combination.) — Analog inputs of arbitrarily selected channels are divided into group A and group B, or group A, group B, and group C, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A, group B, and group C, allowing A/D conversion of the groups to start at different times. • Group scan mode (when a group is given priority): — If a trigger is input for a higher-priority group during A/D conversion on a lower-priority group, A/D conversion on the lower-priority group is stopped and A/D conversion is performed on the higher-priority group. — The order of priority is group A (highest) > group B > group C (lowest).

Item	RX23T (S12ADE)	RX13T (S12ADF)
Operating modes	— Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.	— Restart (rescan) of A/D conversion on the lower-priority group after completion of A/D conversion on the higher-priority group can be enabled. In addition, rescan can be set to start from the first of the selected channels or from the channels on which A/D conversion has not yet finished.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or 8-bit timer (TMR) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Channel-dedicated sample-and-hold function (three channels) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers	• Channel-dedicated sample-and-hold function (three channels) • Input signal amplification function using programmable gain amplifier (three channels) • Variable sampling state count (independently settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers

Item	RX23T (S12ADE)	RX13T (S12ADF)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. A dedicated group C scan end interrupt request (GCADI) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A. A dedicated group B or dedicated group C scan end interrupt request (GBADI or GCADI) can be generated on completion of group B or group C scan, respectively. • The S12ADI, GBADI, and GCADI interrupts can activate the data transfer controller (DTC).
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.40 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX23T (S12ADE)	RX13T (S12ADF)
ADDRy	—	A/D data register y (y = 0 to 7, 16, 17)	A/D data register y (y = 0 to 7)
ADCSR	ADST	A/D conversion start bit	A/D conversion start bit*1
ADANSA1	—	A/D channel select register A1	—
ADANSB1	—	A/D channel select register B1	—
ADANSC0	—	—	A/D channel select register C0
ADADS1	—	A/D-converted value addition/ average channel select register 1	—
ADSTRGR	TRSB[5:0]	A/D conversion start trigger select for group B bits Refer to Table 2.41 for details.	A/D conversion start trigger select for group B bits Refer to Table 2.41 for details.
	TRSA[5:0]	A/D conversion start trigger select bits*2 Refer to Table 2.41 for details.	A/D conversion start trigger select bits*2 Refer to Table 2.41 for details.
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, O)	A/D sampling state register n (n = 0 to 7, O)
ADGSPCR	LGRRS	—	Restart channel select bit
ADHVREFCNT	—	A/D high-potential/low-potential reference voltage control register	—
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0

Notes: 1. The ADST bit retains a value of 1 when group priority operation mode is enabled (bits ADCSR.ADCS[1:0] = 01b and bit ADGSPCR.PGS = 1) and the single scan continuous function is used (bit ADGSPCR.GBRP = 1).

2. On the RX23T Group it is not possible to use an asynchronous trigger as the A/D conversion start trigger for group A in group scan mode, but on the RX13T Group an asynchronous trigger may be used in such cases.

Table 2.41 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register

Bit	RX23T (S12ADE)	RX13T (S12ADF)
TRSB[5:0]	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN
TRSA[5:0]	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN

2.19 Comparator C

Table 2.42 is a comparative overview of the comparator C modules, and Table 2.43 is a comparison of comparator C registers.

Table 2.42 Comparative Overview of Comparator C Modules

Item	RX23T (CMPC)	RX13T (CMPC)
Number of channels	3 channels (comparator C0 to comparator C2)	3 channels (comparator C0 to comparator C2)
Analog input voltage	• Input voltage to CMPCnm pin (n = channel number; m = 0 to 2) • Internal reference voltage	• Input voltage to CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	Input voltage to CVREFC0 or CVREFC1 pin or on-chip D/A converter output voltage	Input voltage to CVREFC0 pin or on-chip D/A converter 0 output voltage
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and POE source output, and comparison results can be read from registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and POE source output, and comparison results can be read from registers.
Interrupt request	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.43 Comparison of Comparator C Registers

Register	Bit	RX23T (CMPC)	RX13T (CMPC)
CMPSEL0	CMPSEL [3:0]	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: Internal reference voltage selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: Internal reference voltage selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected 1 0 0 0: Internal reference voltage selected Settings other than the above are prohibited.	Comparator input select bits • Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 selected 0 0 1 0: CMPC01 selected 0 1 0 0: CMPC02 selected 1 0 0 0: CMPC03 selected Settings other than the above are prohibited. • Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 selected 0 0 1 0: CMPC11 selected 0 1 0 0: CMPC12 selected 1 0 0 0: CMPC13 selected Settings other than the above are prohibited. • Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 selected 0 0 1 0: CMPC21 selected 0 1 0 0: CMPC22 selected Settings other than the above are prohibited.

Register	Bit	RX23T (CMPC)	RX13T (CMPC)
CMPSEL1	CVRS [1:0]	Reference input voltage select bits • Comparator C0 and comparator C1 b1 b0 0 0: No input 0 1: Input to CVREFC1 pin selected as reference input voltage 1 0: On-chip D/A converter output selected as reference input voltage Settings other than the above are prohibited. • Comparator C2 b1 b0 0 0: No input 0 1: Input to CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter output selected as reference input voltage Settings other than the above are prohibited.	Reference input voltage select bits b1 b0 0 0: No input 0 1: Input to CVREFC0 pin selected as reference input voltage 1 0: On-chip D/A converter 0 output selected as reference input voltage Settings other than the above are prohibited.
CMPC0.CMPIOC	VREFEN	Internal reference voltage on/off control bit	—

2.20 RAM

Table 2.44 is a comparative overview of RAM.

Table 2.44 Comparative Overview of RAM

Item	RX23T	RX13T
RAM capacity	12 KB (RAM0: 12 KB)	12 KB
RAM address	RAM0: 0000 0000h to 0000 27FFh, 0000 4000h to 0000 4A7Fh	RAM0: 0000 0000h to 0000 2FFFh
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to set module stop state for RAM0	Ability to set module stop state for RAM0

2.21 Flash Memory

Table 2.45 is a comparative overview of flash memory, and Table 2.46 is a comparison of flash memory registers.

Table 2.45 Comparative Overview of Flash Memory

Item	RX23T	RX13T (FLASH)
Memory capacity	• User area: Up to 128 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 128 KB • Data area: 4 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh	• Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh
Software commands	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and unique ID read • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area can be programmed. • Self-programming (single-chip mode) — The user area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.
Off-board programming	The user area can be programmed using a flash programmer compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.

Item	RX23T	RX13T (FLASH)
ID codes protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 7.	This function is used to safely program blocks 0 to 15.
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	—	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.46 Comparison of Flash Memory Registers

Register	Bit	RX23T	RX13T
DFLCTL	—	—	E2 DataFlash control register
FENTRYR	FENTRYD	—	E2 DataFlash P/E mode entry bit
FPMCR	FMS0	Flash operating mode select bit 0 FMS2 FMS1 FMS0 0 0 0: ROM read mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.	Flash operating mode select bit 0 FMS2 FMS1 FMS0 0 0 0: ROM/E2 DataFlash read mode 0 1 0: E2 DataFlash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.
FASR	EXS	Extra area select bit 0: User area 1: Extra area	Extra area select bit 0: User area, data area 1: Extra area
FCR	CMD[3:0]	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than the above are prohibited.	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 0 1: Unique ID read Settings other than the above are prohibited.
	DRC	—	Data read complete bit

Register	Bit	RX23T	RX13T
FSARH	—	Flash processing start address register H FSARH is a 16-bit register. The flash memory address for programming or erasure is set in bits b31 to b25 and b20 to b16 in this register.	Flash processing start address register H FSARH is an 8-bit register. The flash memory address for programming or erasure is set in bits b19 to b16 in this register.
FSARL	—	Flash processing start address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b2 to b0 to 000b.	Flash processing start address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b1 to b0 to 00b.
FEARH	—	Flash processing end address register H FEARH is a 16-bit register. The flash memory address for programming or erasure is set in bits b31 to b25 and b20 to b16 in this register.	Flash processing end address register H FEARH is an 8-bit register. The flash memory address for programming or erasure is set in bits b19 to b16 in this register.
FEARL	—	Flash processing end address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b2 to b0 to 000b.	Flash processing end address register L The flash memory address for programming or erasure is set in bits b15 to b0 in this register. When the target is the ROM, set bits b1 to b0 to 00b.
FWBn (RX23T) FWBH, FWBL (RX13T)	—	Flash write buffer n register (n = 0 to 3)	Flash write buffer registers H and L
FRBH	—	—	Flash read buffer register H
FRBL	—	—	Flash read buffer register L
FSTATR1	DRRDY	—	Data read ready flag
FEAMH	—	Flash error address monitor register H FEAMH is a 16-bit register. This register stores bits b31 to b25 and b20 to b16 of the address where an error has occurred for the program command or blank check command, or it stores bits b31 to b25 and b20 to b16 of the start address of the area where an error has occurred for the block erase command or all-block erase command.	Flash error address monitor register H FEAMH is an 8-bit register. This register stores bits b19 to b16 of the address where an error has occurred for the program command or blank check command, or it stores bits b19 to b16 of the start address of the area where an error has occurred for the block erase command.

Register	Bit	RX23T	RX13T
FSCMR	—	Flash start-up setting monitor register	Flash start-up setting monitor register
		The value after a reset differs.	
FAWSMR	—	Flash access window start address monitor register In a blank product the value after a reset of bits b11 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b11 to b0 in the FWB0 register.	Flash access window start address monitor register In a blank product the value after a reset of bits b9 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b9 to b0 in the FWBL register.
FAWEMR	—	Flash access window end address monitor register In a blank product the value after a reset of bits b11 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b11 to b0 in the FWB1 register.	Flash access window end address monitor register In a blank product the value after a reset of bits b9 to b0 is 1. After the access window information program command is executed these bits are set to the same value as that set in bits b9 to b0 in the FWBH register.
UIDRn	—	Unique ID register n (n = 0 to 3) UIDRn is a 32-bit register.	Unique ID register n (n = 0 to 31) UIDRn is an 8-bit register.

2.22 Packages

As indicated in Table 2.47, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.47 Packages

Package Type	Renesas Code	
	RX23T	RX13T
64-pin LFQFP	○	×
52-pin LQFP	○	×
48-pin HWQFN	×	○
32-pin LQFP	×	○
32-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by blue text. Items that exists on both groups with different specifications are indicated by red text. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 48-Pin Package

Table 3.1 is a comparative listing of the pin functions of 48-pin package products.

Table 3.1 Comparative Listing of 48-Pin Package Pin Functions

48-Pin	RX23T (48-Pin LFQFP)	RX13T (48-Pin LFQFP)
1	VCL	VCL
2	MD/FINED	MD/FINED
3	RES#	RES#
4	XTAL/P37	XTAL/P37
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36
7	VCC	VCC
8	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
9	PD6/TMO1/SSLA0/CTS1#/RTS1#/SS1#/ ADST0/IRQ5	PD6/MTIOC0D/CTS1#/RTS1#/SS1#/IRQ5/ ADST0
10	PD5/TMRI0/RXD1/SMISO1/SSCL1/IRQ3	PD5/MTIOC0C/RXD1/SMISO1/SSCL1/IRQ3
11	PD4/TMCI0/SCK1/IRQ2	PD4/MTIOC0B/SCK1/IRQ2
12	PD3/TMO0/TXD1/SMOSI1/SSDA1	PD3/MTIOC0A/TXD1/SMOSI1/SSDA1
13	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB7/MTIOC3C/MTCLKD/RXD1/SMISO1/ SSCL1/RXD5/SMISO5/SSCL5/IRQ5
14	PB5/TXD5/SMOSI5/SSDA5	PB6/MTIOC1B/MTIOC3A/TXD1/SMOSI1/ SSDA1/TXD5/SMOSI5/SSDA5
15	VCC	PB5/ADTRG0#
16	PB4/POE8#/IRQ3	PB4/POE8#/IRQ3
17	PB3/MTIOC0A/CACREF/SCK5/RSPCKA	PB3/MTIOC0A/CACREF/SCK5/SCK12
18	PB2/MTIOC0B/ADSM0/TXD5/SMOSI5/ SSDA5/SDA0	PB2/MTIOC0B/MTCLKC/ADSM0/TXD5/ SMOSI5/SSDA5/SDA0
19	PB1/MTIOC0C/RXD5/SMISO5/SSCL5/SCL0/ IRQ2	PB1/MTIOC0C/MTIC5W/MTCLKA/RXD5/ SMISO5/SSCL5/SCL0/IRQ2
20	PB0/MTIOC0D/MOSIA	PB0/MTIOC0D/MTIOC2A/MTCLKB/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12
21	PA3/MTIOC2A/SSLA0	PA3/MTIOC1B/MTIOC2A/CTS12#/RTS12#/ SS12#
22	PA2/MTIOC2B/CTS5#/RTS5#/SS5#/SSLA1/ IRQ4	PA2/MTIOC1A/MTIOC2B/CTS5#/RTS5#/ SS5#/IRQ4
23	P94/MTIOC0C/TMO1/MISOA/IRQ1	P94/MTIOC2B/MTIC5U/MTCLKA/RXD12/ RXDX12/SMISO12/SSCL12/IRQ1
24	P93/MTIOC0B/TMRI1/SCK5/RSPCKA/IRQ0	P93/MTIOC1A/MTIC5V/SCK5/SCK12/IRQ0/ ADTRG0#
25	P76/MTIOC4D	P76/MTIOC4D
26	P75/MTIOC4C	P75/MTIOC4C
27	P74/MTIOC3D	P74/MTIOC3D
28	P73/MTIOC4B	P73/MTIOC4B
29	P72/MTIOC4A	P72/MTIOC4A
30	P71/MTIOC3B	P71/MTIOC3B

48-Pin	RX23T (48-Pin LFQFP)	RX13T (48-Pin LFQFP)
31	P70/POE0#/IRQ5	P70/POE0#/IRQ5
32	VCC	VCC
33	VSS	VSS
34	P24/MTIC5U/TMCI2/RSPCKA/COMP0/IRQ3	P24/MTIC5U/RXD5/SMISO5/SSCL5/IRQ3/ COMP0
35	P23/MTIC5V/CACREF/TMO2/MOSIA/ COMP1/IRQ4	P23/MTIC5V/CACREF/TXD5/SMOSI5/ SSDA5/IRQ4/COMP1
36	P22/MTIC5W/TMRI2/MISOA/COMP2/IRQ2	P22/MTIC5W/IRQ2/COMP2
37	P47/AN007/CMPC12/CMPC22	P47/AN007/CMPC13
38	P46/AN006/CMPC02	P46/AN006/CMPC03
39	P45/AN005/CMPC21	P45/AN005/CMPC22
40	P44/AN004/CMPC11	P44/AN004/CMPC12
41	P43/AN003/CMPC01	P43/AN003/CMPC02
42	P42/AN002/CMPC20	P42/AN002/CMPC20
43	P41/AN001/CMPC10	P41/AN001/CMPC10
44	P40/AN000/CMPC00	P40/AN000/CMPC00
45	AVCC0	AVCC0
46	AVSS0	AVSS0
47	P11/MTIOC3A/MTCLKC/TMO3/IRQ1/AN016/ CVREFC0	P11/MTIOC3A/MTCLKA/POE8#/IRQ1/ CVREFC0
48	P10/MTCLKD/TMRI3/IRQ0/AN017/CVREFC1	P10/MTCLKB/IRQ0

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX13T Group and the RX23T Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

4.1.1 Inserting Decoupling Capacitor between AVCC and AVSS Pins

To prevent destruction of the RX13T Group's analog input pins (AN000 to AN007) by abnormal voltage such as an excessive surge, insert capacitors between AVCC0 and AVSS0, and connect a protective circuit to protect the analog input pins (AN000 to AN007).

For details, refer to "Notes on Noise Prevention" in the 12-Bit A/D Converter section of RX13T Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2 Notes on Functional Design

Some software that runs on the RX23T Group is compatible with the RX13T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX13T Group and RX23T Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.2.1 Note on High-Speed Operating Mode

The maximum operating frequency when reading the flash memory in high-speed operating mode differs between the RX13T Group and RX23T Group. For details, refer to Table 4.1, Comparison of Maximum Operating Frequencies when Reading Flash Memory in High-Speed Operating Mode.

Table 4.1 Comparison of Maximum Operating Frequencies when Reading Flash Memory in High-Speed Operating Mode

Item		RX23T	RX13T
Flash memory read	ICLK	Up to 40 MHz	Up to 32 MHz
	FCLK	Up to 32 MHz	Up to 32 MHz
	PCLKD	Up to 40 MHz	Up to 32 MHz
	PCLKB	Up to 40 MHz	Up to 32 MHz
	PCLKA	Up to 40 MHz	—
Flash memory program/erase	FCLK	1 MHz to 32MHz	1 MHz to 32 MHz

4.2.2 Exception Vector Table

On the RX23T Group the vector addresses are relocatable using the value set in the exception table register (EXTB) as the start address, but addresses allocated in the vector table are fixed on the RX13T Group.

4.2.3 Initialization of the Port Direction Register (PDR)

Initialization of the PDR registers differs even when using RX13T Group or RX23T Group products with the same pin count.

4.2.4 Initial Buffer Register Settings in Complementary PWM Mode

When using the double buffering function in complementary PWM mode of multi-function timer pulse unit 3, the PWM output to the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) should be set to “duty value − 1” on the RX23T Group, but on the RX13T Group a duty value should be specified for PWM output.

4.2.5 MTIOC Pin Output Level when Counter Stopped

When operating with the MTIOC pin in the output state, clearing the CSTn bit in TSTRA or TSTR to 0 or causes the corresponding counter to stop. When this happens in complementary PWM mode or reset synchronous PWM mode on the RX13T Group, the initial output level set in the TOCR1A or TOCR2A register is output on the MTIOC pin.

When operating in other than complementary PWM mode or reset synchronous PWM mode, the output compare output level of the MTIOC is maintained.

4.2.6 Comparator C Operation with 12-Bit A/D Converter in Module Stop Mode

On the RX13T Group the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal. Therefore, comparison of the following PGA outputs is not possible while the 12-bit A/D converter is in module stop mode.

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output

The following analog pins are connected directly to the comparator, so they can be compared even when the 12-bit A/D converter is in module stop mode.

- AN000 pin
- AN001 pin
- AN002 pin
- AN003 pin
- AN004 pin
- AN005 pin
- AN006 pin
- AN007 pin

5. Reference Documents

User's Manual: Hardware

RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX13T Group User's Manual: Hardware Rev.1.00 (R01UH0822EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A151A/E

TN-RX*-A163A/E

TN-RX*-A173A/E

TN-RX*-A175A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A200A/E

TN-RX*-A0227A/E

TN-RX*-A0224B/E

TN-RX*-A0230A/E

TN-RX*-A0246A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 16, 2019	—	First edition issued
1.10	Dec. 9, 2020	4	1 Table 1.1 Comparison of Built-In Functions of RX13T Group and RX23T Group revised
		6, 7	2.2 Table 2.3 Comparative Memory Map of Single-Chip Mode deleted and Figure 2.1 Comparative Memory Map of Single-Chip Mode added
		14	2.8 Table 2.12 Comparison of Vectors and Table 2.13 Comparison of Instructions for Returning from Exception Handling Routines added
		15	2.9 Table 2.14 Comparison of Interrupt Controller Registers revised
		20	2.12 Table 2.20 Comparison of I/O Port Functions added
		22	2.13 Table 2.22 Comparison of Multiplexed Pin Assignments revised
		42	2.18 Table 2.40 Comparison of 12-Bit AID Converter Registers revised
		43	2.18 Table 2.41 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register added
		55	4.2.1 and 4.2.3 added
		56	4.2.5 and 4.2.6 added
		58	Related Technical Updates revised
1.20	Nov. 5, 2021	52	2.22 Table 2.47 Packages revised
		58	Related Technical Updates revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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