

Renesas Synergy™ Platform

Differences between R7FS7G2 Early Samples and Mass Production Devices

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Introduction

This application note describes the differences between early samples and mass production devices in the R7FS7G2 group.

Target Devices

The part numbers affected by this app note are marked as shown below. For more marking details see section 3.

- R7F5A00Z03CBG: Early sample
- R7FS7G27H2A01CBD: Mass production

Table 1. Parts used in hardware development tools

Tool Part Number	Device Marking/Part number	Revision
DK-S7G2	R7F5A00Z03CBG	1.x
DK-S7G2	R7F5A00Z03CBG	2.x
DK-S7G2	R7FS7G27H2A01CBD	3.0 or later
PE-HMI1	R7F5A00Z03CBG	1.x
PE-HMI1	R7FS7G27H2A01CBD	2.0 or later

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1. Differences from R7F5A00Z03CBG to R7FS7G27H2A01CBD

1.1 Pixel clock

The LCD pixel clock source is PLCKB. Divider definition is different between R7F5A00Z03CBG and R7FS7G27H2A01CBD.

System Control Block Version and Panel Clock Control Register

(SYSCNT_PANEL_CLK)

Table 2. R7FS7G27H2A01CBD input clock division

DCDR[5:0]	Division ratio	CLKSEL= 0 LCD_EXTCLK ($\leq 60\text{MHz}$)	CLKSEL = 1 PLL output (120 to 240MHz)
000000b	1/2	LCD_EXTCLK/2	-
000001b	1/1	-	-
000010b	1/2	LCD_EXTCLK/2	-
000011b	1/3	LCD_EXTCLK/3	-
000100b	1/4	LCD_EXTCLK/4	-
000101b	1/5	LCD_EXTCLK/5	PLL output/5
000110b	1/6	LCD_EXTCLK/6	PLL output/6
000111b	1/7	LCD_EXTCLK/7	PLL output/7
001000b	1/8	LCD_EXTCLK/8	PLL output/8
001001b	1/9	LCD_EXTCLK/9	PLL output/9
001100b	1/12	LCD_EXTCLK/12	PLL output/12
010000b	1/16	LCD_EXTCLK/16	PLL output/16
011000b	1/24	LCD_EXTCLK/24	PLL output/24
100000b	1/32	LCD_EXTCLK/32	PLL output/32

Note: See S7 Series User's Manual: Microcontrollers Electrical Characteristics for details.

Table 3. R7F5A00Z03CBG input clock division

DCDR[5:0]	Division ratio	CLKSEL= 0 LCD_EXTCLK ($\leq 60\text{MHz}$)	CLKSEL = 1 PCLKB ($\leq 60\text{MHz}$)
000000b	1/2	LCD_EXTCLK/2	-
000001b	1/1	-	-
000010b	1/2	LCD_EXTCLK/2	PCLKB/2
000011b	1/3	LCD_EXTCLK/3	PCLKB/3
000100b	1/4	LCD_EXTCLK/4	PCLKB/4
000101b	1/5	LCD_EXTCLK/5	PCLKB/5
000110b	1/6	LCD_EXTCLK/6	PCLKB/6
000111b	1/7	LCD_EXTCLK/7	PCLKB/7
001000b	1/8	LCD_EXTCLK/8	PCLKB/8
001001b	1/9	LCD_EXTCLK/9	PCLKB/9
001100b	1/12	LCD_EXTCLK/12	PCLKB/12
010000b	1/16	LCD_EXTCLK/16	PCLKB/16
011000b	1/24	LCD_EXTCLK/24	PCLKB/24
100000b	1/32	LCD_EXTCLK/32	PCLKB/32

1.2 MPC for SDRAM

Register settings for input/output pin function (PSEL[4:0]) have been changed.

R7FS7G27H2A01CBD:

PSEL[4:0] Settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
01011b	BUS	D0:I/O DQ0:I/O	D1:I/O DQ1:I/O	D2:I/O DQ2:I/O	D3:I/O DQ3:I/O	D4:I/O DQ4:I/O	D5:I/O DQ5:I/O	D6:I/O DQ6:I/O	D7:I/O DQ7:I/O				A5:O	A4:O	A3:O	A2:O	A1:O
11011b	cannot use																

PSEL[4:0] Settings	Function	pin															
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313	P314	P315
01011b	BUS		A6:O	A7:O	A8:O	A9:O	A10:O	A11:O	A12:O	A13:O	A14:O	A15:O	CS2#:O RAS#:O	CS3#:O CAS#:O	A20:O	A21:O	A22:O
11011b	cannot use																

PSEL[4:0] Settings	Function	pin															
		P600	P601	P602	P603	P604	P605	P606	P607	P608	P609	P610	P611	P612	P613	P614	P615
01011b	BUS	RD#:O	WR#:O WR0#:O DQM0:O	EBCLK:O SDCLK:O	D13:I/O DQ13:I/O	D12:I/O DQ12:I/O	D11:I/O DQ11:I/O			A0:O BC0:O DQM1:O	CS1#:O CKE:O	CS0#:O WE#:O	SDCS#:O	D8:I/O DQ8:I/O	D9:I/O DQ9:I/O	D10:I/O DQ10:I/O	
11011b	cannot use																

PSEL[4:0] Settings	Function	pin															
		P800	P801	P802	P803	P804	P805	P806	P807	P808	P809	P810	P811	P812	P813		
01011b	BUS	D14:I/O DQ14:I/O	D15:I/O DQ15:I/O														
11011b	cannot use																

R7F5A00Z03CBG:

PSEL[4:0] Settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
01011b	BUS	D0:I/O	D1:I/O	D2:I/O	D3:I/O	D4:I/O	D5:I/O	D6:I/O	D7:I/O				A5:O	A4:O	A3:O	A2:O	A1:O
11011b	SDRAM	DQ0:I/O	DQ1:I/O	DQ2:I/O	DQ3:I/O	DQ4:I/O	DQ5:I/O	DQ6:I/O	DQ7:I/O				A5:O	A4:O	A3:O	A2:O	A1:O

PSEL[4:0] Settings	Function	pin															
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313	P314	P315
01011b	BUS		A6:O	A7:O	A8:O	A9:O	A10:O	A11:O	A12:O	A13:O	A14:O	A15:O	CS2#:O	CS3#:O	A20:O	A21:O	A22:O
11011b	SDRAM		A6:O	A7:O	A8:O	A9:O	A10:O	A11:O	A12:O	A13:O	A14:O	A15:O	RAS#:O	CAS#:O			

PSEL[4:0] Settings	Function	pin															
		P600	P601	P602	P603	P604	P605	P606	P607	P608	P609	P610	P611	P612	P613	P614	P615
01011b	BUS	RD#:O	WR#:O WR0#:O	EBCLK:O	D13:I/O	D12:I/O	D11:I/O			A0:O BC0:O	CS1#:O CKE:O	CS0#:O		D8:I/O	D9:I/O	D10:I/O	
11011b	SDRAM	CKE:O	WE#:O	SDCLK:O	DQ13:I/O	DQ12:I/O	DQ11:I/O			A0:O	DQM1:O	DQM0:O	SDCS#	DQ8:I/O	DQ9:I/O	DQ10:I/O	

PSEL[4:0] Settings	Function	pin															
		P800	P801	P802	P803	P804	P805	P806	P807	P808	P809	P810	P811	P812	P813		
01011b	BUS	D14:I/O	D15:I/O														
11011b	SDRAM	DQ14:I/O	DQ15:I/O														

1.3 I/O port drive capability

The DSCR[1:0] value of P1_09 and P1_08 after reset has been changed.

Table 3. DSCR[1:0] meaning

DSCR[1:0]	Port Drive
0 0	Low drive
0 1	Middle drive
1 0	Setting prohibited
1 1	High drive

R7FS7G27H2A01CBD: DSCR[1:0] is “01” after reset

R7F5A00Z03CBG: DSCR[1:0] is “00” after reset

1.4 I/O pull-up control

R7FS7G27H2A01CBD: There is no effect on the port pull-up resistor when you select SDHI enable (PSEL= ‘10101b’).

R7F5A00Z03CBG: When you select SDHI enable (PSEL= ‘10101b’) for the pins below, the pull-up resistor is automatically ON, and the pull-up resistors cannot be cut by software.

Table 4: Effected ports

Port	Function	I/O
P9_3	SD0CD	Input
P4_12	SD0CMD	I/O
P4_11	SD0DAT0	I/O
P4_10	SD0DAT1	I/O
P2_6	SD0DAT2	I/O
P2_5	SD0DAT3	I/O
P2_4	SD0DAT4	I/O
P2_3	SD0DAT5	I/O
P2_2	SD0DAT6	I/O
P3_13	SD0DAT7	I/O
P4_14	SD0WP	Input
P5_6	SD1CD	Input
P5_1	SD1CMD	I/O
P5_2	SD1DAT0	I/O
P5_3	SD1DAT1	I/O
P5_4	SD1DAT2	I/O
P5_5	SD1DAT3	I/O
P8_1	SD1DAT4	I/O
P8_2	SD1DAT5	I/O
P8_3	SD1DAT6	I/O
P8_4	SD1DAT7	I/O
P5_7	SD1WP	Input

1.5 Bus access speed from CPU to SRAM

R7FS7G27H2A01CBD can get faster bus access from the CPU to SRAM0 and SRAM1 than R7F5A00Z03CBG for continuous write and read.

2. R7F5A00Z03CBG restrictions

2.1 Flash programing restriction

When the LSI flash memory is being programmed, at least one of PCLKA and PLCKB and PCLKC and PCLKD is faster than FCLK. If $ICLK \geq FCLK > PCLKA/B/D$, the FRDYI interrupt does not appear.

2.2 PCNTR3 register reading restriction

POSR_n in PCNTR3 cannot be accessed by 16-bit access. PCNTR3 register can only be accessed by 32-bit access.

2.3 EEP blank check restriction

Blank check for EEP cannot be executed while EEP or FLI programming are suspended.

2.4 RTC time capture function restriction

RTC time capture function might not work correctly after VCC resupply.

When output RTCIC-2=1, a power-on reset may occur.

Unexpected POR occurs when RTCIC[2:0] is toggled (0->1) as part of the wakeup function. A voltage surge during the toggle causes a voltage drop on VBATT resulting in POR.

The cause is insufficient current drive for VBATT regulator.

2.5 Bus arbitration function restriction

This product does not support round-robin bus arbitration.

You can only use fixed arbitration when resource conflict occurs.

2.6 Software Standby restriction

When SSTBY mode with port select uses USBHS, USBFS or Key interrupt and those interrupts are not permitted, an unexpected interrupt may occur after cancelling the SSTBY mode .

This occurs when all of the following conditions are met:

- SSTBY mode
- USB HS or USB FS or Key interrupt is selected for IO port by PSEL.
- USB HS or USB FS or Key interrupt (same as above (2) IP interrupt is not permitted

Under these conditions, an unexpected interrupt may occur after cancelling the SSTBY mode.

2.7 A/D group scan mode restriction

When using higher priority Group A, with the Group B trigger and restart function of Group B at PCLK > ADCLK, Group B conversion might occur twice even if only one Group B trigger occurs..

Specification: A/D group scan mode (when group A is given priority). If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B stops and A/D conversion is performed on group A. Restart of A/D conversion on group B after completion of group A can be set.

Issue: When a group A trigger occurs just before group B conversion is completed, the group B conversion will occur twice despite the single trigger on group B.

2.8 SSI (I2S) operation restriction

A false interrupt occurs as a result of clearing the SSI FIFO Status Register Receive Data Full Flag (RDF) and Transmit Data Empty Flag (TDE).

The follow sequence of events will result in a false interrupt:

1. When either RDF or TDE flags are asserted one after another
2. Before the CPU is able to clear the first flag, DMA or DTC accesses the bus (second bus master)
3. When the CPU clears the first flag, it causes a second interrupt (duplicated) from the second flag

The cause for this is a design flaw on the address decoder for FIFO Status Register (SSIFSR).

2.9 JTAG or SWD operation restriction

The pin function of JTAG or SWD may change unexpectedly after reset.

After reset, the system clock source is switched to MOCO. When a glitch occurs during this period, the PFS (Pin Function control register) may get corrupted.

2.10 SDRAM pins in Standby Mode restriction

In Software Standby Mode or Deep Software Standby Mode, even if SBYCR.OPE is set to 0, CE, DQM0, DQM1 pins retain the output state instead of high-impedance state.

3. Marking information of R7F5A00Z03CBG

These are the markings for R7F5A00Z03CBG.

SYNERGY R7F5A00Z03CBG WS1 441A100	SYNERGY R7F5A00Z03CBG WS1 441A101	SYNERGY R7F5A00Z03CBG WS1 445A100	SYNERGY R7F5A00Z03CBG WS1 502A100
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4. Reference Documents

User's Manual: Microcontrollers:

S7 Series User's Manual: Microcontrollers (R01UH0582EU0080)

The latest version can be downloaded from the Renesas Electronics website: <http://www.renesassynergy.com/docs>.

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Revision History

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