# R32C/118 Group and R32C/118A Group

Differences between R32C/118 and R32C/118A (144-pin Package)

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## 1. Abstract

This document is a reference to ascertain the changes in functions from the 144-pin package for the R32C/118 Group and the 144-pin package for the R32C/118A Group. For details on functions, refer to the hardware user's manual.

## 2. Introduction

This document applies to the following products:
R32C/118 Group 144-pin package and R32C/118A Group 144-pin package
R32C/117 Group 144-pin package and R32C/117A Group 144-pin package
R32C/116 Group 144-pin package and R32C/116A Group 144-pin package

# 3. Overview of Comparison

## 3.1 Overview of Functions

Table 3.1 lists the differences between products.

**Table 3.1 Comparison Chart: Overview of Functions**

| Item | R32C/118 | R32C/118A |
|---|---|---|
| Memory | Flash memory: 384 Kbytes to 1 Mbyte<br>RAM: 40/48/63 Kbytes | Flash memory: 512 Kbytes to 1 Mbyte<br>RAM: 96 Kbytes |
| Watchdog timer | — | Automatic timer start function is available |
| DMAC | Request sources: 57 | Request sources: 61 |
| I/O ports | 120 CMOS I/O ports (32 are 5 V tolerant) | • 124 CMOS I/O ports (40 are 5 V tolerant)<br>• Self test function |
| Serial interface | 9 channels (UART0 to UART8) | 11 channels (UART0 to UART10) |
| A/D converter | — | Self test/Open-circuit detection assist |
| Protect area | — | Available |
| Operating frequency | 50 MHz | 64 MHz |
| Flash memory | — | • Forcible erase function<br>• Standard serial I/O mode disable function |

## 3.2 Pin Characteristics

Table 3.2 lists pin characteristics and changes from the R32C/118.

**Table 3.2 Comparison Chart: Pin Characteristics**

| R32C/118 | R32C/118A | Changes |
|---|---|---|
| VCC | P14_7 | Added: P14_7<br>Deleted: VCC |
| VSS | P11_7 | Added: P11_7<br>Deleted: VSS |
| VCC | P11_6 | Added: P11_6<br>Deleted: VCC |
| VSS | P11_5 | Added: P11_5<br>Deleted: VSS |
| P2_7/AN2_7/A7(/D7) | P2_7/TXD10/AN2_7/A7(/D7) | Added: TXD10 |
| P2_6/AN2_6/A6(/D6) | P2_6/RXD10/AN2_6/A6(/D6) | Added: RXD10 |
| P2_5/AN2_5/A5(/D5) | P2_5/CLK10/AN2_5/A5(/D5) | Added: CLK10 |
| P2_4/AN2_4/A4(/D4) | P2_4/$\overline{\text{CTS10}}$/$\overline{\text{RTS10}}$/AN2_4/A4(/D4) | Added: $\overline{\text{CTS10}}$/$\overline{\text{RTS10}}$ |
| P2_3/AN2_3/A3(/D3) | P2_3/TXD9/AN2_3/A3(/D3) | Added: TXD9 |
| P2_2/AN2_2/A2(/D2) | P2_2/RXD9/AN2_2/A2(/D2) | Added: RXD9 |
| P2_1/AN2_1/A1(/D1)/$\overline{\text{BC2}}$(/D1) | P2_1/CLK9/AN2_1/A1(/D1)/$\overline{\text{BC2}}$(/D1) | Added: CLK9 |
| P2_0/AN2_0/A0(/D0)/$\overline{\text{BC0}}$(/D0) | P2_0/$\overline{\text{CTS9}}$/$\overline{\text{RTS9}}$/AN2_0/A0(/D0)/$\overline{\text{BC0}}$(/D0) | Added: $\overline{\text{CTS9}}$/$\overline{\text{RTS9}}$ |

# 4. Detailed Comparison

## 4.1 Clock

Table 4.1 lists the changes in SFRs associated with the clock.

**Table 4.1 Comparison Chart: Clock-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| PM2 | 40035h | 40035h | 2 | — | Watchdog timer count source protect bit |
| | | | 3 | — | Watchdog timer count source select bit |

## 4.2 Protection

Table 4.2 lists the changes in SFRs associated with protection.

**Table 4.2 Comparison Chart: Protection-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| PRR | 0007h | 0007h | — | Control the protection for registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23. | Control the protection for registers CCR, FMCR, PBC, FEBC, EBC0 to EBC3, CB01, CB12, and CB23. |
| PRCR4 | — | 4404Ch | — | — | Available only in the R32C/118A |

## 4.3 Interrupts

Table 4.3 lists the changes in SFRs associated with interrupts.
The relocatable vector tables and interrupt priority level select circuitry of each are different.

**Table 4.3 Comparison Chart: Interrupt-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| S9TIC | — | 00D9h | — | — | Available only in the R32C/118A |
| S10TIC | — | 00DBh | — | — | Available only in the R32C/118A |
| S9RIC | — | 00F9h | — | — | Available only in the R32C/118A |
| S10RIC | — | 00FBh | — | — | Available only in the R32C/118A |

## 4.4 Watchdog Timer

Table 4.4 and Table 4.5 list the changes in the watchdog timer and associated SFRs, respectively.

**Table 4.4 Comparison Chart: Watchdog Timer**

| Item | R32C/118 | R32C/118A |
|---|---|---|
| Clock source for watchdog timer | Peripheral bus clock | Peripheral bus clock, on-chip oscillator clock |
| Watchdog timer prescaler divide ratio | Divide-by-16 or -128 | When peripheral bus clock is selected: Divide-by-16 or -128<br>When on-chip oscillator clock is selected: Divide-by-1, -2, -4, -8, -16, -32, -64, -128, -256, -512, or -1024 |
| Automatic timer start function | — | Available |

**Table 4.5 Comparison Chart: Watchdog Timer-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| WDK | — | 4404Dh | — | — | Available only in the R32C/118A |
| WDC | 4404Fh | 4404Fh | 4 to 0 | Upper 5 bits of the watchdog timer (b14 to b10) | Upper 5 bits of the watchdog timer, when the peripheral bus clock is used: b14 to b10<br>When the on-chip oscillator is used: b10 to b6 (1) |
| OFS | — | FFFFFFEFh | — | — | Available only in the R32C/118A |

Note:
1. When the on-chip oscillator clock is used as the count source, the read value may be undefined due to a change in the count value while being read.

## 4.5 DMAC

Table 4.6 lists the changes in DMAC.

**Table 4.6 Comparison Chart: DMAC**

| Item | R32C/118 | R32C/118A |
|---|---|---|
| DMA request sources | UART0 to UART8 transmit/receive interrupt requests | UART0 to UART11 transmit/receive interrupt requests |

## 4.6 Serial Interface

Table 4.7 lists the changes in serial interface associated SFRs.

**Table 4.7 Comparison Chart: Serial Interface-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| U9MR | — | 40300h | — | — | Available only in the R32C/118A |
| U9BRG | — | 40301h | — | — | Available only in the R32C/118A |
| U9TB | — | 40303h to 40302h | — | — | Available only in the R32C/118A |
| U9C0 | — | 40304h | — | — | Available only in the R32C/118A |
| U9C1 | — | 40305h | — | — | Available only in the R32C/118A |
| U9RB | — | 40307h to 40306h | — | — | Available only in the R32C/118A |
| U10MR | — | 40308h | — | — | Available only in the R32C/118A |
| U10BRG | — | 40309h | — | — | Available only in the R32C/118A |
| U10TB | — | 4030Bh to 4030Ah | — | — | Available only in the R32C/118A |
| U10C0 | — | 4030Ch | — | — | Available only in the R32C/118A |
| U10C1 | — | 4030Dh | — | — | Available only in the R32C/118A |
| U10RB | — | 4030Fh to 4030Eh | — | — | Available only in the R32C/118A |
| U910CON | — | 40310h | — | — | Available only in the R32C/118A |

## 4.7 A/D Converter

Table 4.8 and Table 4.9 list the changes in A/D converter and associated SFRs, respectively.

**Table 4.8 Comparison Chart: A/D Converter**

| Item | R32C/118 | R32C/118A |
|---|---|---|
| Operating modes | — | Open-circuit detection, self-test mode |

**Table 4.9 Comparison Chart: A/D Converter-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| AD0CON5 | — | 0393h | — | — | Available only in the R32C/118A |

## 4.8 Protected Areas

The R32C/118A Group has five 32-bit areas protected from unexpected write accesses. Like RAM, the protected areas are randomly accessible. However, they are not rewritable while the protection is locked. Table 4.10 lists the address range of protected areas and Table 4.11 lists the protected area-associated SFRs.

**Table 4.10 Address Range of Protected Areas**

| Protected Area | Address Range |
|---|---|
| Protected Area 0 | 42000h to 4201Fh |
| Protected Area 1 | 42020h to 4203Fh |
| Protected Area 2 | 42040h to 4205Fh |
| Protected Area 3 | 42060h to 4207Fh |
| Protected Area 4 | 42080h to 4209Fh |

**Table 4.11 Comparison Chart: Protected Area-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| PAPR | — | 420F0h | — | — | Available only in the R32C/118A |
| PAWF | — | 420F2h | — | — | Available only in the R32C/118A |

## 4.9 I/O Pins

Table 4.12 and Table 4.13 list the changes in I/O pin-associated SFRs.

**Table 4.12 Comparison Chart: I/O Pin-associated SFRs (1/2)**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| P11 | 03D5h | 03D5h | 5 | — | Port P11_5 bit |
| | | | 6 | — | Port P11_6 bit |
| | | | 7 | — | Port P11_7 bit |
| P14 | 03DCh | 03DCh | 7 | — | Port P14_7 bit |
| PD11 | 03D7h | 03D7h | 5 | — | Port P11_5 direction bit (1) |
| | | | 6 | — | Port P11_6 direction bit (1) |
| | | | 7 | — | Port P11_7 direction bit (1) |
| PD14 | 03DEh | 03DEh | 7 | — | Port P14_7 direction bit (1) |
| PUR3 | 03F3h | 03F3h | 4 | P12_0 to P12_3 pull-up control bit | — |
| | | | 5 | P12_4 to P12_7 pull-up control bit | — |
| PUR4 | 03F4h | 03F4h | 7 | — | P17_4 to P17_7 pull-up control bit (2) |
| PUR5 | - | 03F5h | — | — | Available only in the R32C/118A (3) |
| PCR | 03FFh | 03FFh | 3 | — | Read data select bit |
| | | | 6 | — | PD11_5 to PD11_7, PD14_7 write enable bit |
| | | | 7 | Port P9_0, P9_2, P11 to P15 enable bit | Reserved |
| IFS3 | 4009Bh | 4009Bh | 4 | — | UART9 input pin switch bit (2) |
| | | | 5 | — | UART10 input pin switch bit (2) |

Notes:
1. Set the PDWE bit in the PCR register to 1 (write enabled) before rewriting this bit.
2. This bit should be set to 0 in the 144-pin package.
3. This register should be set to 00h in the 144-pin package.

**Table 4.13 Comparison Chart: I/O Pin-associated SFRs (2/2)**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| P2_0S | 400B0h | 400B0h | 6 | — | N-channel open drain output select bit |
| P2_1S | 400B2h | 400B2h | 6 | — | N-channel open drain output select bit |
| P2_2S | 400B4h | 400B4h | 6 | — | N-channel open drain output select bit |
| P2_3S | 400B6h | 400B6h | 6 | — | N-channel open drain output select bit |
| P2_4S | 400B8h | 400B8h | 6 | — | N-channel open drain output select bit |
| P2_5S | 400BAh | 400BAh | 6 | — | N-channel open drain output select bit |
| P2_6S | 400BCh | 400BCh | 6 | — | N-channel open drain output select bit |
| P2_7S | 400BEh | 400BEh | 6 | — | N-channel open drain output select bit |
| P11_5S | — | 400FBh | — | — | Available only in the R32C/118A |
| P11_6S | — | 400FDh | — | — | Available only in the R32C/118A |
| P11_7S | — | 400FFh | — | — | Available only in the R32C/118A |
| P12_4S | 40108h | 40108h | 6 | — | N-channel open drain output select bit |
| P12_5S | 4010Ah | 4010Ah | 6 | — | N-channel open drain output select bit |
| P12_6S | 4010Ch | 4010Ch | 6 | — | N-channel open drain output select bit |
| P12_7S | 4010Eh | 4010Eh | 6 | — | N-channel open drain output select bit |
| P14_7S | — | 4011Fh | — | — | Available only in the R32C/118A |

## 4.10 Flash Memory

Table 4.14 lists the changes in flash memory-associated SFRs, Table 4.15 lists the changes in registers in single-chip mode, and Table 4.16 lists the changes in registers in the memory expansion mode.

**Table 4.14 Comparison Chart: Flash Memory-associated SFRs**

| Symbol | Address | | Bit | R32C/118 | R32C/118A |
|---|---|---|---|---|---|
| | R32C/118 | R32C/118A | | | |
| FEBC | — | 0009h to 0008h | — | — | Available only in the R32C/118A |
| FEBC0 | 001Dh to 001Ch | — | — | Available only in the R32C/118 | — |
| FEBC3 | 0011h to 0010h | — | — | Available only in the R32C/118 | — |
| FMR0 | 40000h | 40000h | 6 | Reserved | Suspend request acknowledge flag |
| FMSR0 | 40001h | 40001h | 3 | Reserved | Program suspend status flag |
| | | | 6 | Reserved | Erase suspend status flag |
| FMR1 | 40009h | 40009h | 0 | Reserved | Suspend request interrupt level select bit |
| | | | 5 | Reserved | Suspend request bit |
| | | | 6 | Reserved | Suspended and ready flag |
| | | | 7 | Reserved | Suspend enable bit |

**Table 4.15 Comparison Chart: Registers in Single-chip Mode**

| Item | R32C/118 | R32C/118A |
|---|---|---|
| Bus setting in the program area | FEBC0 register | FEBC register |
| Bus setting in the data area | | |

**Table 4.16 Comparison Chart: Registers in Memory Expansion Mode**

| Item | R32C/118 | R32C/118A |
|---|---|---|
| Bus setting in the program area | FEBC0 register | FEBC register |
| Bus setting in the data area | FEBC3 register | |

# 5. Reference Documents

User's Manuals
R32C/118 Group User's Manual: Hardware Rev.1.00
R32C/118A Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
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| REVISION HISTORY | R32C/118 Group and R32C/118A Group<br>Differences between R32C/118 and R32C/118A (144-pin Package) |
|---|---|

| Rev. | Date | Description | |
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| | | | |

# General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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