M32C/87 Group, R32C/118 Group

Differences between M32C/87 and R32C/118

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1. Introduction

This document is a reference to confirm the functional changes from the M32C/87 (144-pin package version) to the R32C/118 (144-pin package version).
For details on functions, refer to the hardware and software manuals for each group.

2. Applicable MCUs

This document is applicable to the following products:
M32C/87, 144-pin package version and R32C/118, 144-pin package version

3. Overview of Comparison

3.1 Overview of Functions

Table 3.1 and Table 3.2 list the functions of each product.

Table 3.1 Comparison Chart: Overview of Functions (1/2)

Item	M32C/87	R32C/118
Basic instructions	108	108 (including 18 deleted, 18 added, and 5 changed)
Minimum instruction execution time	31.3 ns (f(CPU) = 32 MHz / VCC1 = 4.2 to 5.5 V)	20 ns (f(CPU) = 50 MHz)
Multiplier	16-bit × 16-bit→32-bit	32-bit × 32-bit→64-bit
Multiply-accumulate unit	16-bit × 16-bit + 48-bit→48-bit	32-bit × 32-bit + 64-bit→64-bit
FPU	N/A (1)	Single precision (compliant with IEEE-754)
Barrel shifter	16 bits	32 bits
Operating mode	Single-chip mode, memory expansion mode, microprocessor mode	Single-chip mode, memory expansion mode, microprocessor mode (optional (2))
Address space	16 Mbytes	4 Gbytes (available up to 64 Mbytes)
Low voltage detector	Vdet3 detection, Vdet4 detection, coldstart/warmstart determination	Low voltage detection interrupt (optional (2))
Clocks	• Main clock oscillation circuit: up to 32 MHz • PLL synthesizer: up to 32 MHz • Oscillation stop detector: main clock oscillation stop detection • Frequency divide circuit: divide-by-i selectable (i = 1, 2, 3, 4, 6, 8, 10, 12, 14, and 16)	• Main clock oscillation circuit: 4 to 16 MHz • PLL synthesizer: 96 to 128 MHz • Oscillation stop detector: main clock oscillation stop detection, re-oscillation detection • Frequency divide circuit: divide-by-2 to divide-by-24 selectable
Interrupts	Interrupt vectors: 70	Interrupt vectors: 261
DMAC	• 4 channels • Request sources: 43	• 4 channels • Request sources: 57
I/O ports	121 CMOS inputs/outputs, 1 input-only port	120 CMOS inputs/outputs, 2 input-only ports
Serial interface	• 7 channels (UART0 to UART6) -Synchronous serial interface -Asynchronous serial interface • 5 channels (UART0 to UART4) -I^2C bus, special mode 2, GCI mode, SIM mode, IEBus mode (optional (2)) • 1 channel (UART0) -IrDA mode	• 9 channels (UART0 to UART8) -Synchronous serial interface -Asynchronous serial interface • 7 channels (UART0 to UART6) -I^2C bus, special mode2, IEBus mode (optional (2))

Notes:
1. “Not applicable” and “not available” will hereinafter be referred to as “N/A” in tables.
2. Please contact a Renesas sales office to use the optional feature.

Table 3.2 Comparison Chart: Overview of Functions (2/2)

Item	M32C/87	R32C/118
Intelligent I/O	• Time measurement:16 bits × 8 • Waveform generation:16 bits × 16 • Serial interface: -Synchronous serial I/O mode -Asynchronous serial I/O mode -HDLC data processing mode -IEBus mode (optional (2)) -Two-phase pulse signal processing mode (Group 1)	• Time measurement:16 bits × 16 • Waveform generation:16 bits × 24 • Serial interface: -Variable-length synchronous serial I/O mode -IEBus mode (optional (2)) -Two-phase pulse signal processing mode (Groups 0 and 1)
CAN	CAN Specification 2.0B 16 slots X 2 channels	ISO11898-1 Specifications 32 mail box X 2 channels
Multi-master I^2C-bus Interface	N/A	1 channel
Flash memory	Erase and program voltage: 3.3 ± 0.3V, or 5.0 ± 0.5 V Erase and program endurance: 100 times (all areas)	Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Erase and program endurance: 1,000 times (program area) and 10,000 times (data area)
Operating frequency/ Supply voltage	• 32 MHz / VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 • 24 MHz / VCC1= 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1	50 MHz / VCC = 3.0 to 5.5 V,
Current consumption	• 32 mA (32 MHz / VCC1 = VCC2 = 5.0 V) • 23 mA (24 MHz / VCC1 = VCC2 = 3.3 V) • 45 µA (approx. 1 MHz / VCC1 = VCC2 = 3.3 V, when entering wait mode from on-chip oscillator low-power consumption mode) • 0.8 µA (VCC1 = VCC2 = 3.3 V in stop mode)	• 35 mA (VCC = 5.0 V, f(CPU) = 50 MHz) • 8 µA (VCC = 3.3 V to 5.0V, f(XCIN) = 32.768 kHz, in wait mode) • 5 µA (VCC = 3.3 to 5.0 V, when all clocks and main regulator are stopped)

Notes:
1. “Not applicable” and “not available” will hereinafter be referred to as “N/A” in tables.
2. Please contact a Renesas sales office to use the optional feature.

3.2 Pin Characteristics

Table 3.3 to Table 3.6 list each pin characteristics and changes from the M32C/87.

Table 3.3 Comparison Chart: Pin Characteristics (1/4)

M32C/87	R32C/118	Changes
P14_3/INPC1_7/OUTC1_7 (1)	P14_3	Deleted: INPC1_7/OUTC1_7
P14_2/INPC1_6/OUTC1_6 (1)	VDC0	Deleted: P14_2/INPC1_6/ OUTC1_6 Added: VDC0
P14_1/INPC1_5/OUTC1_5 (1)	P14_1	Deleted:INPC1_5/OUTC1_5
P14_0/INPC1_4/OUTC1_4 (1)	VDC1	Deleted: P14_0/INPC1_4/ OUTC1_4 Added: VDC1
BYTE	NSD	Deleted: BYTE Added: NSD
P8_3/$\overline{\text{INT1}}$/CAN0IN/CAN1IN	P8_3/$\overline{\text{INT1}}$/CAN0IN/$\overline{\text{CAN0WU}}$/ $\overline{\text{CAN1IN}}$/CAN1WU	Added: $\overline{\text{CAN0WU}}$/$\overline{\text{CAN1WU}}$
P8_1/TA4IN/$\overline{\text{U}}$/RTP2_3/$\overline{\text{CTS5}}$/ $\overline{\text{RTS5}}$/INPC1_5/OUTC1_5 (1)	P8_1/TA4IN/$\overline{\text{U}}$/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$/ IIO1_5/UD0B/UD1B (1)	Deleted: RTP2_3 Added: $\overline{\text{SS5}}$/UD0B/ UD1B
P8_0/TA4OUT/U/RXD5/ISRXD0	P8_0/TA4OUT/U/RXD5/SCL5/ STXD5/UD0A/UD1A	Deleted: ISRXD0 Added: SCL5/STXD5/UD0A/ UD1A
P7_7/TA3IN/RTP2_2/CLK5/ CAN0IN/INPC1_4/OUTC1_4/ ISCLK0 (1)	P7_7/TA3IN/CLK5/CAN0IN/ $\overline{\text{CAN0WU}}$/IIO1_4/UD0B/UD1B (1)	Deleted: RTP2_2/ISCLK0 Added: $\overline{\text{CAN0WU}}$/UD0B/UD1B
P7_6/TA3OUT/TXD5/CAN0OUT/ INPC1_3/OUTC1_3/ISTXD0 (1)	P7_6/TA3OUT/TXD5/SDA5/ SRXD5/$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$/CAN0OUT/ IIO1_3/UD0A/UD1A (1)	Deleted: ISTXD0 Added: SDA5/SRXD5/$\overline{\text{CTS8}}$/ $\overline{\text{RTS8}}$/UD0A/UD1A
P7_5/TA2IN/$\overline{\text{W}}$/RTP2_1/INPC1_2/ OUTC1_2/ISRXD1 (1)	P7_5/TA2IN/$\overline{\text{W}}$/RXD8/IIO1_2 (1)	Deleted: RTP2_1/ISRXD1 Added: RXD8
P7_4/TA2OUT/W/RTP2_0/ INPC1_1/OUTC1_1/ISCLK1 (1)	P7_4/TA2OUT/W/CLK8/IIO1_1 (1)	Deleted: RTP2_0/ISCLK1 Added: CLK8
P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/ INPC1_0/OUTC1_0/ISTXD1 (1)	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/ TXD8/IIO1_0 (1)	Deleted: ISTXD1 Added: TXD8
P7_1/TA0IN/TB5IN/RTP0_3/RXD2/ SCL2/STXD2/INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN (1)	P7_1/TA0IN/TB5IN/RXD2/SCL2/ STXD2/MSCL/IIO1_7/OUTC2_2/ ISRXD2/IEIN (1)	Deleted: RTP0_3 Added: MSCL

Note:
1. OUTC1_i (i = 1 to 7) and INPC1_i in the M32C/87 are merged into IIO1_i in the R32C/118

Table 3.4 Comparison Chart: Pin Characteristics (2/4)

M32C/87	R32C/118	Changes
P7_0/TA0OUT/RTP0_2/TXD2/ SDA2/SRXD2/INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT (1)	P7_0/TA0OUT/TXD2/SDA2/ SRXD2/MSDA/IIO1_6/OUTC2_0/ ISTXD2/IEOUT (1)	Deleted: RTP0_2 Added: MSDA
VCC1	VCC	Deleted: VCC1 Added: VCC
P6_3/TXD0/SDA0/IrDAOUT/ SRXD0	P6_3/TXD0/SDA0/SRXD0	Deleted: IrDAOUT
P6_2/RXD0/SCL0/STXD0/IrDAIN	P6_2/TB2IN/RXD0/SCL0/STXD0	Deleted: IrDAIN Added: TB2IN
P6_1/RTP0_1/CLK0	P6_1/TB1IN/CLK0	Deleted: RTP0_1 Added: TB1IN
P6_0/RTP0_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	P6_0/TB0IN/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	Deleted: RTP0_0 Added: TB0IN
P13_7/OUTC2_7	P13_7/OUTC2_7/D31	Added: D31
P13_6/OUTC2_1/ISCLK2	P13_6/OUTC2_1/ISCLK2/D30	Added: D30
P13_5/OUTC2_2/ISRXD2/IEIN	P13_5/OUTC2_2/ISRXD2/IEIN/ D29	Added: D29
P13_4/OUTC2_0/ISTXD2/IEOUT	P13_4/OUTC2_0/ISTXD2/IEOUT/ D28	Added: D28
P5_7/$\overline{\text{RDY}}$	P5_7/$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/$\overline{\text{RDY}}$/$\overline{\text{CS3}}$	Added: $\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/$\overline{\text{CS3}}$
P5_6/ALE	P5_6/RXD7/ALE/$\overline{\text{CS2}}$	Added: RXD7/$\overline{\text{CS2}}$
P5_5/$\overline{\text{HOLD}}$	P5_5/CLK7/$\overline{\text{HOLD}}$	Deleted: CLK7
P5_4/$\overline{\text{HLDA}}$/ALE	P5_4/TXD7/$\overline{\text{HLDA}}$/$\overline{\text{CS1}}$	Deleted: ALE Added: TXD7/$\overline{\text{CS1}}$
P13_3/OUTC2_3	P13_3/OUTC2_3/D27	Added: D27
P13_2/OUTC2_6	P13_2/OUTC2_6/D26	Added: D26
VCC2	VCC	Deleted: VCC2 Added: VCC
P13_1/OUTC2_5	P13_1/OUTC2_5/D25	Added: D25
P13_0/OUTC2_4	P13_0/OUTC2_4/D24	Added: D24
P5_3/CLKOUT/BCLK/ALE	P5_3/CLKOUT/BCLK	Deleted: ALE
P5_1/$\overline{\text{WRH}}$/$\overline{\text{BHE}}$ (2) (3)	P5_1/$\overline{\text{WR1}}$/$\overline{\text{BC1}}$ (2) (3)	
P5_0/$\overline{\text{WR}}$/$\overline{\text{WRL}}$ (4)	P5_0//$\overline{\text{WR}}$/$\overline{\text{WR0}}$ (4)	
P12_7	P12_7/D23	Added: D23
P12_6	P12_6/D22	Added: D22
P12_5	P12_5/D21	Added: D21

Notes:
1. OUTC1_i (i = 1 to 7) and INPC1_i in the M32C/87 are merged into IIO1_i in the R32C/118.
2. $\overline{\text{WRH}}$ in the M32C/87 is changed to $\overline{\text{WR1}}$ in the R32C/118.
3. $\overline{\text{BHE}}$ in the M32C/87 is changed to $\overline{\text{BC1}}$ in the R32C/118.
4. $\overline{\text{WRL}}$ in the M32C/87 is changed to $\overline{\text{WR0}}$ in the R32C/118.

Table 3.5 Comparison Chart: Pin Characteristics (3/4)

M32C/87	R32C/118	Changes
P4_7/$\overline{CS0}$/A23	P4_7/TXD6/SDA6/SRXD6/$\overline{CS0}$/A23	Added: TXD6/SDA6/SRXD6
P4_6/$\overline{CS1}$/A22	P4_6/RXD6/SCL6/STXD6/$\overline{CS1}$/A22	Added: RXD6/SCL6/STXD6
P4_5/$\overline{CS2}$/A21	P4_5/CLK6/$\overline{CS2}$/A21	Added: CLK6
P4_4/$\overline{CS3}$/A20	P4_4/$\overline{CS6}$/$\overline{RTS6}$/$\overline{SS6}$/$\overline{CS3}$/A20	Added: $\overline{CTS6}$/$\overline{RTS6}$/$\overline{SS6}$
P4_3/A19	P4_3/TXD3/SDA3/SRXD3/OUTC2_0/ISTXD2/IEOUT/A19	Added: TXD3/SDA3/SRXD3/OUTC2_0/ISTXD2/IEOUT
VCC2	VCC	Deleted: VCC2 Added: VCC
P4_2/A18	P4_2/RXD3/SCL3/STXD3/ISRXD2/IEIN/A18	Added: RXD3/SCL3/STXD3/ISRXD2/IEIN
P4_1/A17	P4_1/CLK3/A17	Added: CLK3
P4_0/A16	P4_0/$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$/A16	Added: $\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$
P3_7/A15, [A15/D15]	P3_7/TA4IN/$\overline{U}$/A15(/D15)	Added: TA4IN/$\overline{U}$
P3_6/A14, [A14/D14]	P3_6/TA4OUT/U/A14(/D14)	Added: TA4OUT/U
P3_5/A13, [A13/D13]	P3_5/TA2IN/$\overline{W}$/A13(/D13)	Added: TA2IN/$\overline{W}$
P3_4/A12, [A12/D12]	P3_4/TA2OUT/W/A12(/D12)	Added: TA2OUT/W
P3_3/A11, [A11/D11]	P3_3/TA1IN/$\overline{V}$/A11(/D11)	Added: TA1IN/$\overline{V}$
P3_2/A10, [A10/D10]	P3_2/TA1OUT/V/A10(/D10)	Added: TA1OUT/V
P3_1/A9, [A9/D9]	P3_1/TA3OUT/UD0B/UD1B/A9(/D9)	Added: TA3OUT/UD0B/UD1B
P12_4	P12_4/D20	Added: D20
P12_3/$\overline{CTS6}$/$\overline{RTS6}$	P12_3/$\overline{CTS6}$/$\overline{RTS6}$/$\overline{SS6}$/D19	Added: $\overline{SS6}$/D19
P12_2/RXD6	P12_2/RXD6/SCL6/STXD6/D18	Added: SCL6/STXD6/D18
P12_1/CLK6	P12_1/CLK6/D17	Added: D17
P12_0/TXD6	P12_0/TXD6/SDA6/SRXD6/D16	Added: SDA6/SRXD6/D16
P3_0/A8, [A8/D8]	P3_0/TA0OUT/UD0A/UD1A/A8(/D8)	Added: TA0OUT/UD0A/UD1A
P2_1/AN2_1/A1(/D1)	P2_1/AN2_1/A1(/D1)/$\overline{BC2}$(/D1)	Added: $\overline{BC2}$(/D1)
P2_0/AN2_0/A0(/D0)	P2_0/AN2_0/A0(/D0)/$\overline{BC0}$(/D0)	Added: $\overline{BC0}$(/D0)
P1_7/$\overline{INT5}$/D15	P1_7/$\overline{INT5}$/D15/IIO0_7/IIO1_7	Added: IIO0_7/IIO1_7
P1_6/$\overline{INT4}$/D14	P1_6/$\overline{INT4}$/D14/IIO0_6/IIO1_6	Added: IIO0_6/IIO1_6
P1_5/$\overline{INT3}$/D13	P1_5/$\overline{INT3}$/D13/IIO0_5/IIO1_5	Added: IIO0_5/IIO1_5
P1_4/D12	P1_4/D12/IIO0_4/IIO1_4	Added: IIO0_4/IIO1_4
P1_3/D11	P1_3/D11/IIO0_3/IIO1_3	Added: IIO0_3/IIO1_3
P1_2/D10	P1_2/D10/IIO0_2/IIO1_2	Added: IIO0_2/IIO1_2
P1_1/D9	P1_1/D9/IIO0_1/IIO1_1	Added: IIO0_1/IIO1_1
P1_0/D8	P1_0/D8/IIO0_0/IIO1_0	Added: IIO0_0/IIO1_0
P11_4	P11_4/$\overline{BC3}$/$\overline{WR3}$	Added: $\overline{BC3}$/$\overline{WR3}$

Table 3.6 Comparison Chart: Pin Characteristics (4/4)

M32C/87	R32C/118	Changes
P11_3/INPC1_3/OUTC1_3 (1)	P11_3/$\overline{\text{RTS8}}$/$\overline{\text{CTS8}}$/IIO1_3/$\overline{\text{CS3}}$/ $\overline{\text{WR2}}$ (1)	Added: $\overline{\text{RTS8}}$/$\overline{\text{CTS8}}$/$\overline{\text{CS3}}$/$\overline{\text{WR2}}$
P11_2/INPC1_2/OUTC1_2/ ISRXD1 (1)	P11_2/RXD8/IIO1_2/$\overline{\text{CS2}}$ (1)	Deleted: ISRXD1 Added: RXD8/$\overline{\text{CS2}}$
P11_1/INPC1_1/OUTC1_1/ISCLK1 (1)	P11_1/CLK8/IIO1_1/$\overline{\text{CS1}}$ (1)	Deleted: ISCLK1 Added: CLK8/$\overline{\text{CS1}}$
P11_0/INPC1_0/OUTC1_0/ISTXD1 (1)	P11_0/TXD8/IIO1_0/$\overline{\text{CS0}}$ (1)	Deleted: ISTXD1 Added: TXD8/$\overline{\text{CS0}}$
P15_7/$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/AN15_7	P15_7/$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$/IIO0_7/ AN15_7	Added: $\overline{\text{SS6}}$/IIO0_7
P15_6/CLK6/AN15_6	P15_6/CLK6/IIO0_6/AN15_6	Added: IIO0_6
P15_5/RXD6/AN15_5	P15_5/RXD6/SCL6/STXD6/IIO0_5/ AN15_5	Added: SCL6/STXD6/IIO0_5
P15_4/TXD6/AN15_4	P15_4/TXD6/SDA6/SRXD6/ IIO0_4/AN15_4	Added: SDA6/SRXD6/IIO0_4
P15_3/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/AN15_3	P15_3/$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/IIO0_3/AN15_3	Deleted: $\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$ Added: $\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/IIO0_3
P15_2/RXD5/ISRXD0/AN15_2	P15_2/RXD7/IIO0_2/AN15_2	Deleted: RXD5/ISRXD0 Added: RXD7/IIO0_2
P15_1/CLK5/ISCLK0/AN15_1	P15_1/CLK7/IIO0_1/AN15_1	Deleted: CLK5/ISCLK0 Added: CLK7/IIO0_1
P15_0/TXD5/ISTXD0/AN15_0	P15_0/TXD7/IIO0_0/AN15_0	Deleted: TXD5/ISTXD0 Added: TXD7/IIO0_0
VCC1	VCC	Deleted: VCC1 Added: VCC
P10_7/$\overline{\text{KI3}}$/RTP3_3/AN_7	P10_7/$\overline{\text{KI3}}$/AN_7	Deleted: RTP3_3
P10_6/$\overline{\text{KI2}}$/RTP3_2/AN_6	P10_6/$\overline{\text{KI2}}$/AN_6	Deleted: RTP3_2
P10_5/$\overline{\text{KI1}}$/RTP3_1/AN_5	P10_5/$\overline{\text{KI1}}$/AN_5	Deleted: RTP3_1
P10_4/$\overline{\text{KI0}}$/RTP3_0/AN_4	P10_4/$\overline{\text{KI0}}$/AN_4	Deleted: RTP3_0
P10_3/RTP1_3/AN_3	P10_3/AN_3	Deleted: RTP1_3
P10_2/RTP1_2/AN_2	P10_2/AN_2	Deleted: RTP1_2
P10_1/RTP1_1/AN_1	P10_1/AN_1	Deleted: RTP1_1
P10_0/RTP1_0/AN_0	P10_0/AN_0	Deleted: RTP1_0

Note:
1. OUTC1_i (i = 1 to 7) and INPC1_i in the M32C/87 are merged into IIO1_i in the R32C/118.

4. Detailed Comparison

4.1 CPU Function

Table 4.1 to Table 4.4 list the changes from the R32C/118 on instructions, bit length of internal registers, and flags.

Table 4.1 Chart: R32C/118 Instructions

Item	R32C/118
Added instructions	ADDF, ADSF, CMPF, CNVIF, DIVF, DIV (1), DIVU (1), DIVX (1), EXITI, MUL (1), MULU (1), MULX, MULF, ROUND, STOP, SUBF, SUNTIL, and SWHILE
Mnemonic changed instructions	EDIV (from DIV), EDIVU (from DIVU), EDIVX (from DIVX), EMUL (from MUL), and EMULU (from MULU)
Deleted instructions	ADDX, ADJNZ, BAND, BNAND, BNOR, BNTST, BNXOR, BOR, BXOR, CMPX, JMPS, JSRS, MOVX, MULEX, SBJNZ, SHANC, SHLNC, and SUBX

Note:
1. These instructions are newly added with existing mnemonics. (Refer to Table 4.2).

Table 4.2 Comparison Chart: Mnemonic Changed Instructions and Their Bit Length (reference)

Mnemonic	M32C/87	R32C/118
DIV, DIVU, DIVX	16 bits ÷ 8 bits = 8 bits (for byte) 32 bits ÷16 bits = 16 bits (for word) 64 bits ÷ 32 bits = 32 bits (for long word)	8 bits ÷ 8 bits = 8 bits (for byte) 16 bits ÷16 bits = 16 bits (for word) 32 bits ÷ 32 bits = 32 bits (for long word)
MUL, MULU	8 bits × 8 bits = 16 bits (for byte) 16 bits ×16 bits = 32 bits (for word) 32 bits × 32 bits = 64 bits (for long word)	8 bits × 8 bits = 8 bits (for byte) 16 bits ×16 bits = 16 bits (for word) 32 bits × 32 bits = 32 bits (for long word)

Table 4.3 Comparison Chart: Bit Length of Internal Registers

Internal Register	M32C/87		R32C/118	
	Register	Bit length	Register	Bit length
Flag register	FLG	16 bits	FLG	32 bits
Data registers (1)	R0, R1, R2, R3	16 bits Registers R0 and R1 can be respectively divided into upper and lower 8-bit registers. Registers R2 and R0, R3 and R1 can be respectively merged into one 32-bit register.	R0, R1, R2, R3	16 bits Registers R0, R1, R2, and R3 can be respectively divided into upper and lower 8-bit registers. Registers R2 and R0, R3 and R1 can be respectively merged into one 32-bit register
			R4, R5, R6, R7	16 bits Registers R7 and R5, R6 and R4 can be respectively merged into one 32-bit register
Address register (1)	A0, A1	24 bits	A0, A1, A2, A3	32 bits
Static base register (1)	SB		SB	
Frame base register (1)	FB		FB	
User stack pointer	USP		USP	
Interrupt table register	INTB		INTB	
Program counter	PC		PC	
Fast interrupt registers	SVF	16 bits	SVF	
	SVP	24 bits	SVP	
	VCT		VCT	
DMAC-associated registers (In the M32C/87, if 3 or more DMAC channels are to be used, the register bank 1 and fast interrupt registers function as DMAC registers.)	DMD0, DMD1	8 bits	DMD0, DMD1, DMD2, DMD3	
	DCT, DCT1, DCT2(R0), DCT3(R1)	16 bits	DCT0, DCT1, DCT2, DCT3	
	DRC0, DRC1, DRC1(R2), DRC2(R3)		DCR0, DCR1, DCR2, DCR3	
	DMA0, DMA1, DMA2(A0), DMA3(A1), DSA0, DSA1, DSA2(SB), DSA3(FB)	24 bits	DSA0, DSA1, DSA2, DSA3	
			DDA0, DDA1, DDA2, DDA3	
	DRA0, DRA1, DRA2(SVP), DRA3(VCT)		DSR0, DSR1, DSR2, DSR3	
			DDR0, DDR1, DDR2, DDR3	

Note:
1. There are two banks of these registers.

Table 4.4 Comparison Chart: Flag Registers

Item	M32C/87		R32C/118	
	Flag	Bit position	Flag	Bit position
Floating-point underflow flag	N/A	N/A	FU	b8
Floating-point overflow flag	N/A	N/A	FO	b9
Fixed-point designation flag	N/A	N/A	DP	b16
Floating-point round mode	N/A	N/A	RND	b19 and b18

4.2 Resets

Hardware reset 1, low voltage detection (hardware reset 2), software reset, and watchdog timer reset are implemented to reset the MCU. However, the low voltage detection is available only in the M32C/87.
Some SFRs remain uninitialized even after a reset operation.
Table 4.5 to Table 4.7 list the changes from the M32C/87 on reset operations.

Table 4.5 Comparison Chart: Non-reset Registers

Item	Register	State after reset	
		M32C/87	R32C/118
Hardware reset 1	WDC	WDC5 bit is not initialized	N/A
Low voltage detection (hardware reset 2) (available only in the M32C/87)	WDC	WDC5 bit is not initialized	N/A
Software reset	PM0	Bits PM01 and PM00 are not initialized	
	TCSPR	Not initialized	Initialized
	WDC	WDC5 bit is not initialized	N/A
Watchdog timer reset	PM0	Bits PM01 and PM00 are not initialized	
	TCSPR	Not initialized	Initialized
	WDC	WDC5 bit is not initialized	N/A

Table 4.6 Comparison Chart: Clock Source and Divide Ratio After a Reset

Item	M32C/87	R32C/118
Clock source	Main clock	PLL self oscillation mode
CPU clock	Divide-by-8	Divide-by-12
Peripheral bus clock	Divide-by-8	Divide-by-12
Other clocks	N/A	• Base clock: divide-by-6 • CPU clock: base clock divide-by-2 • Peripheral bus clock: base clock divide-by-2

Table 4.7 Comparison Chart: Clock Source Before a Software Reset

Item	M32C/87	R32C/118
Clock source	Main clock	PLL clock

4.3 Voltage Regulator

The internal voltage of the R32C/118 is generated by reducing the input voltage from the VCC pin with the voltage regulator(s). To stabilize the internal voltage, a decoupling capacitor should be connected between pins VDC1 and VDC0. The M32C/87 does not require any decoupling capacitor. Table 4.8 lists the change on the voltage regulator control register.

Table 4.8 Comparison Chart: Voltage Regulator Control Register

Symbol	Address		Bit	M32C/87	R32C/118
	M32C/87	R32C/118			
VRCR	N/A	40060h	-	N/A	Available only in the R32C/118

4.4 Low Voltage Detection

Table 4.9 lists the changes on SFRs associated with low voltage detection.

Table 4.9 Comparison Chart: Low Voltage Detection-associated SFRs

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
VCR1	001Bh	N/A	-	Available only in the M32C/87	N/A
VCR2	0017h	N/A	-	Available only in the M32C/87	N/A
D4INT	002Fh	N/A	-	Available only in the M32C/87	N/A
WDC	000Fh	4404Fh	5	Coldstart/warmstart determination flag	Reserved
LVDC	N/A	40062h	-	N/A	Available only in the R32C/118
DVCR	N/A	40064h	-	N/A	Available only in the R32C/118

4.5 Processor Modes

Table 4.10 lists the changes on SFRs associated with processor mode.

Table 4.10 Comparison Chart: Processor Mode-associated SFRs

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
			-	Address changed	
PM0	0004h	40044h	5, 4	Multiplexed bus space select bits	Reserved
PM1	0005h	N/A	-	Available only in the M32C/87	N/A

4.6 Clocks

Table 4.11 to Table 4.13 respectively list the changes on clock characteristics, settings, and associated SFRs.

Table 4.11 Comparison Chart: Clock Characteristics

Item	M32C/87	R32C/118
CPU clock after reset	Main clock divided by 8	PLL frequency synthesizer (self-oscillation mode) divided by 12
XIN-XOUT drive power	Unswitchable	Switchable
Main clock division	Selectable from 1, 2, 3, 4, 6, 8, 12, and 16	Selectable from 1, 2, 3, and 4
Base clock division	N/A	Selectable from 2, 3, 4, and 6
CPU clock division	N/A	Selectable from 1, 2, 3, and 4
Peripheral bus clock division	N/A	Selectable from 2, 3, and 4
PLL multiplexed ratio	Selectable from 6/2, 8/2, 6/3, and 8/3	Selectable from values specified in the hardware manual
Stop mode	Each has its own procedure to enter stop mode	
Transition from main clock mode to stop mode or wait mode	Enabled	N/A
Transition from PLL mode (high/medium speed) to stop mode or wait mode	N/A	Disabled
Transition from PLL self-oscillation mode to wait mode	N/A	Enabled
Transition from low speed mode to stop mode	Disabled	Enabled
Transition from low power mode to stop mode or wait mode	Disabled	Enabled
Exit from wait mode by serial interface interrupt	Enabled by every UART channel	Enabled by UART channels except UART7, and UART8
CPU clock when exiting from stop mode	Main clock divided by 8	Divide ratio of CPU clock when the STOP instruction is executed

Table 4.12 Comparison Chart: Clock-associated Settings

Item	M32C/87	R32C/118
XIN-XOUT drive power	N/A	Bits CM15 and CM16 in the CM1 register
Main clock division	Bits MCD0 to MCD4 in the MCD register	Bits CCD0 and CCD1 in the CCR register
Base clock division	N/A	Bits BCD0 and BCD1 in the CCR register
Peripheral bus clock division	N/A	Bits PCD0 and PCD1 in the CCR register
PLL multiplexed ratio	• Bits PLC0 to PLC02 in the PLC0 register • PLC12 bit in the PLC1 register	Setting value of registers PLC0 and PLC1 specified in the hardware manual

Table 4.13 Comparison Chart: Clock-associated SFRs

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
CCR	N/A	0004h	-	N/A	Available only in the R32C/118
PBC	N/A	001Fh-001Eh	-	N/A	Available only in the R32C/118
CM0	0006h	40046h	-	Address changed	
			7	CPU clock select bit 0	Reserved
CM1	0007h	40047h	-	Address changed	
			0	All clock stop control bit	PLL clock oscillator stop bit
			6, 5	Reserved	XIN-XOUT drive power select bits
			7	CPU clock select bit 1	Reserved
MCD	000Ch	N/A	-	Available only in the M32C/87	N/A
CM2	000Dh	4004Dh	-	Address changed	
			1	CPU clock select bit	Reserved
PLC0	0026h	40020h	-	Address changed	
			2 to 0	Programmable counter select bits (PLC02, PLC01, PLC00)	Main counter divide ratio setting bit (MCV2, MCV1, MCV0)
			4, 3	Reserved	Main counter divide ratio setting bit (MCV4, MCV3)
			6, 5	Reserved	Swallow counter divide ratio setting bit (SVC1, SVC0)
			7	Operation enable bit (PLC07)	Swallow counter divide ratio setting bit (SVC2)
PLC1	0027h	40021h	-	Address changed	
			1, 0	Reserved	Reference counter divide ratio setting bits (RCV1, RCV0)
			2	PLL clock division select bit (PLC12)	Reference counter divide ratio setting bit (RCV2)
			3	Reserved	Reference counter divide ratio setting bit (RCV3)
			4	Reserved	Self-oscillation mode setting bit (SEO)
PM2	0013h	40053h	-	Address changed	
			2	WDT count source protect bit	Reserved
			4	CPU clock select bit 3	NMI enable bit
			5	CAN clock select bit	Reserved
			6	f2n clock source select bit	f2n clock source select bit
			7	f2n clock source select bit	Reserved
CM3	N/A	4005Ah	-	N/A	Available only in the R32C/118
PM3	N/A	40048h	-	N/A	Available only in the R32C/118

4.7 Bus

Table 4.14 to Table 4.18 respectively list the changes on bus characteristics, settings, bus control pins, and associated SFRs.

Table 4.14 Comparison Chart: Bus Characteristics

Item	M32C/87	R32C/118
Address space	16 Mbytes	4 Gbytes (available up to 64 Mbytes)
External space wait states	1 to 7 wait states based on BCLK cycle	1 to 28 wait states based on base clock cycle
Recovery cycle insert (Address hold time after read/write)	Available (selectable)	Available
SFR area wait states	1 or 2 wait states	No wait state, Settable by the CCR register (divide-by-1, 2, 3, or 4)

Table 4.15 Comparison Chart: Bus Settings

Item	M32C/87	R32C/118
Data bus width	• Each external space bus width is set by bits DS0 to DS3 in the DS register; 0: 8 bits 1: 16 bits • Bus width after a reset is set by the BYTE pin (applicable to external space 3 only); H: 8 bits L: 16 bits	• Each external space bus width is set by bits BW0 and BW1 in registers EBC0 to EBC3; 00b: 8 bits as width 01b: 16 bits as width 10b: 32 bits as width • Maximum width of each external space bus is set by bits EXBW0 and EXBW1 in the PBC register; 00b: 8 bits as maximum width 01b: 16 bits as maximum width 10b: 32 bits as maximum width • Bus width after a reset is set by the lower two bits of reset vector (applicable to external space CS0 only); 11b: 8 bits 10b: 16 bits 00b: 32 bits
Chip select signals	Bits PM10 and PM11 in the PM1 register	Registers CSOP0 and CSOP2
SFR area bus timing	PM13 bit in the PM1 register	PBC register
External space bus timing	Bits EWCRi00 to EWCRi04 in the EWCRi register (i = 0 to 3)	EBCi register (i = 0 to 3)
Recovery cycle insert (Address hold time after read/write)	EWCRi06 bit in the EWCRi register (i = 0 to 3)	N/A
BCLK output	• PM07 bit in the PM0 register • Bits PM14 and PM15 bits in the PM1 register • Bits CM00 and CM01 in the CM0 register	• PM07 bit in the PM0 register • Bits CM00 and CM01 in the CM0 register

Table 4.16 Comparison Chart: Bus Control Pins (when $\overline{RD}$, $\overline{WR0}$, to $\overline{WR3}$ outputs are selected)

Bus Control Signal	Output Pins	
	M32C/87	R32C/118
$\overline{CS3}$	P4_4 (A20) (1)	P4_4 (A20) (1)
		P5_7 ($\overline{RDY}$) (1)
		P11_3 (1)
$\overline{CS2}$	P4_5 (A21) (1)	P4_5 (A21) (1)
		P5_6 (ALE) (1)
		P11_2
$\overline{CS1}$	P4_6 (A22) (1)	P4_6 (A22) (1)
		P5_4 ($\overline{HLDA}$) (1)
		P11_1
ALE	P5_6	P5_6 ($\overline{CS2}$) (1)
	P5_4 ($\overline{HLDA}$) (1)	
	P5_3 (BCLK) (1)	
$\overline{WR3}$	N/A	P11_4
$\overline{WR2}$	N/A	P11_3 ($\overline{CS3}$) (1)
$\overline{WRH}$/$\overline{WR1}$ (2)	P5_1	P5_1
$\overline{WRL}$/$\overline{WR0}$ (3)	P5_0	P5_0
$\overline{A23}$	P4_7 ($\overline{CS0}$) (1)	P4_7 (A23) ($\overline{CS0}$) (1)

Notes:
1. A control pin in parentheses above shares an output pin with a corresponding bus control pin. Either of them should be selected for using.
2. $\overline{WRH}$ in the M32C/87 is changed to $\overline{WR1}$ in the R32C/118.
3. $\overline{WRL}$ in the M32C/87 is changed to $\overline{WR0}$ in the R32C/118.

Table 4.17 Comparison Chart: Bus Control Pins (when $\overline{RD}$, $\overline{WR}$, $\overline{BC0}$, to $\overline{BC3}$ outputs are selected)

Bus Control Signal	Output Pins	
	M32C/87	R32C/118
$\overline{CS3}$	P4_4 (A20) (1)	P4_4 (A20) (1)
		P5_7 ($\overline{RDY}$) (1)
		P11_3 (1)
$\overline{CS2}$	P4_5 (A21) (1)	P4_5 (A21) (1)
		P5_6 (ALE) (1)
		P11_2
$\overline{CS1}$	P4_6 (A22) (1)	P4_6 (A22) (1)
		P5_4 ($\overline{HLDA}$) (1)
		P11_1
ALE	P5_6	P5_6 ($\overline{CS2}$) (1)
	P5_4 ($\overline{HLDA}$) (1)	
	P5_3 (BCLK) (1)	
$\overline{BC1}$/$\overline{BHE}$ (2)	P5_1	P5_1
$\overline{BC3}$	N/A	P11_4
$\overline{A23}$	P4_7 ($\overline{CS0}$) (1)	P4_7 (A23) ($\overline{CS0}$) (1)
$\overline{BC0}$/A0 (3)	P2_0	P2_0
$\overline{BC2}$/A1	N/A	P2_1

Notes:
1. A control pin in parentheses above shares an output pin with a corresponding bus control pin. Either of them should be selected for using.
2. $\overline{BHE}$ in the M32C/87 is changed to $\overline{BC1}$ in the R32C/118.
3. A0 in the M32C/87 is changed to $\overline{BC0}$ in the R32C/118.

Table 4.18 Comparison Chart: Bus-associated SFRs

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
DS	000Bh	N/A	-	Available only in the M32C/87	N/A
PM0	0004h	40044h	-	Address changed	
			5, 4	Multiplexed bus space select bits	Reserved
PM1	0005h	N/A	-	Available only in the M32C/87	N/A
EWCR0	0048h	N/A	-	Available only in the M32C/87	N/A
EWCR1	0049h	N/A	-	Available only in the M32C/87	N/A
EWCR2	004Ah	N/A	-	Available only in the M32C/87	N/A
EWCR3	004Bh	N/A	-	Available only in the M32C/87	N/A
CCR	N/A	0004h	-	N/A	Available only in the R32C/118
PBC	N/A	001Fh-001Eh	-	N/A	Available only in the R32C/118
CSOP0	N/A	40054h	-	N/A	Available only in the R32C/118
CSOP1	N/A	40055h	-	N/A	Available only in the R32C/118
CSOP2	N/A	40056h	-	N/A	Available only in the R32C/118
CB01	N/A	001Ah	-	N/A	Available only in the R32C/118
CB12	N/A	0016h	-	N/A	Available only in the R32C/118
CB23	N/A	0012h	-	N/A	Available only in the R32C/118
EBC0	N/A	001Dh-001Ch	-	N/A	Available only in the R32C/118
EBC1	N/A	0019h-0018h	-	N/A	Available only in the R32C/118
EBC2	N/A	0015h-0014h	-	N/A	Available only in the R32C/118
EBC3	N/A	0011h-0010h	-	N/A	Available only in the R32C/118

4.8 Protection

Table 4.19 lists the changes on SFRs associated with the protection.

Table 4.19 Comparison Chart: Protection-associated SFRs

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
PRCR	000Ah	4004Ah	-	Address changed	
			0	Protect bit 0: Write enable to registers CM0, CM1,CM2, MCD, PLC0, and PLC1	Protect bit 0: Write enable to registers CM0, CM1, CM2, and PM3
			1	Protect bit 1: Write enable to registers PM0, PM1, PM2, INVC0, and INVC1	Protect bit 1: Write enable to registers PM0, PM2, INVC0, INVC1, CSOP0, CSOP1, CSOP2, IOBC and I2CMR
			2	Protect bit 2: Write enable to registers PD9 and PS3	Protect bit 2: Write enable to registers PD9, P9_iS (i = 0 to 7), PLC0, and PLC1
			3	Protect bit 3: Write enable to registers VCR2 and D4INT	N/A
PRCR2	N/A	4405Fh	7	N/A	CM3 protect bit: Write enable to the CM3 register
PRCR3	N/A	4004Ch	1	N/A	Protect bit 31: Write enable to registers VRCR, LVDC, and DVCR
PRR	N/A	0007h	7 to 0	N/A	Write enable to registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0, EBC1, EBC2, EBC3, CB01, CB12, and CB23: AAh: write enabled other than AAh: write disabled

4.9 Interrupts

Table 4.20 and Table 4.22 respectively list the changes on interrupt and associated SFRs.
The relocatable vector tables and interrupt priority level select circuitry of each are different.

Table 4.20 Comparison Chart: Interrupts

Item	M32C/87	R32C/118
Address match interrupt	Settable up to 8 addresses	N/A

Table 4.21 Comparison Chart: Interrupt-associated SFRs (1/2)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
TB5IC	0069h	0061h	-	Address changed	
S2TIC	0089h	0081h	-	Address changed	
S3TIC	008Bh	0083h	-	Address changed	
S4TIC	008Dh	0085h	-	Address changed	
S5TIC	N/A	0062h	-	N/A	Available only in the R32C/118
S6TIC	N/A	0064h	-	N/A	Available only in the R32C/118
S7TIC	N/A	00DDh	-	N/A	Available only in the R32C/118
S8TIC	N/A	00DFh	-	N/A	Available only in the R32C/118
S2RIC	006Bh	0063h	-	Address changed	
S3RIC	006Dh	0065h	-	Address changed	
S4RIC	006Fh	0067h	-	Address changed	
S5RIC	N/A	0082h	-	N/A	Available only in the R32C/118
S6RIC	N/A	0084h	-	N/A	Available only in the R32C/118
S7RIC	N/A	00FDh	-	N/A	Available only in the R32C/118
S8RIC	N/A	00FFh	-	N/A	Available only in the R32C/118
BCN0IC/ BCN3IC	0071h	0069h	-	Address changed	
BCN1IC/ BCN4IC	0091h	0089h	-	Address changed	
BCN2IC	008Fh	0087h	-	Address changed	
BCN5IC/ BCN6IC	N/A	0066h	-	N/A	Available only in the R32C/118
AD0IC	0073h	006Bh	-	Address changed	
KUPIC	0093h	008Bh	-	Address changed	
INT6IC	N/A	00FEh	-	N/A	Available only in the R32C/118
INT7IC	N/A	00DEh	-	N/A	Available only in the R32C/118
INT8IC	N/A	00FCh	-	N/A	Available only in the R32C/118
IIO0IC	0075h	006Dh	-	Address changed	
IIO1IC	0095h	008Dh	-	Address changed	
IIO2IC	0077h	006Fh	-	Address changed	
IIO3IC	0097h	008Fh	-	Address changed	
IIO4IC	0079h	0071h	-	Address changed	
IIO5IC	0099h	0091h	-	Address changed	
IIO6IC	007Bh	0073h	-	Address changed	
IIO7IC	009Bh	0093h	-	Address changed	
IIO8IC	007Dh	0075h	-	Address changed	
IIO9IC	009Dh	0095h	-	Address changed	

Table 4.22 Comparison Chart: Interrupt-associated SFRs (2/2)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
IIO10IC	007Fh	0077h	-	Address changed	
IIO11IC	0081h	0097h	-	Address changed	
CAN0IC	009Dh	N/A	-	Available only in the M32C/87	N/A
CAN1IC	007Fh	N/A	-	Available only in the M32C/87	N/A
CAN2IC	0081h	N/A	-	Available only in the M32C/87	N/A
CAN3IC	0075h	N/A	-	Available only in the M32C/87	N/A
CAN4IC	0095h	N/A	-	Available only in the M32C/87	N/A
CAN5IC	0099h	N/A	-	Available only in the M32C/87	N/A
C0TIC	N/A	00C1h	-	N/A	Available only in the R32C/118
C1TIC	N/A	00E3h	-	N/A	Available only in the R32C/118
C0RIC	N/A	00E1h	-	N/A	Available only in the R32C/118
C1RIC	N/A	00C5h	-	N/A	Available only in the R32C/118
C0EIC	N/A	00C3h	-	N/A	Available only in the R32C/118
C1EIC	N/A	00E5h	-	N/A	Available only in the R32C/118
C0WIC	N/A	007Bh	-	N/A	Available only in the R32C/118
C1WIC	N/A	009Bh	-	N/A	Available only in the R32C/118
C0FTIC	N/A	00D0h	-	N/A	Available only in the R32C/118
C1FTIC	N/A	00D2h	-	N/A	Available only in the R32C/118
C0FRIC	N/A	00F0h	-	N/A	Available only in the R32C/118
C1FRIC	N/A	00F2h	-	N/A	Available only in the R32C/118
I2CLIC	N/A	0063h	-	N/A	Available only in the R32C/118
I2CIC	N/A	00F2h	-	N/A	Available only in the R32C/118
RLVL	009Fh	N/A	-	Available only in the M32C/87	N/A
RIPL1	N/A	4407Fh	-	N/A	Available only in the R32C/118
RIPL2	N/A	4407Dh	-	N/A	Available only in the R32C/118
IFSR	031Fh	N/A	-	Available only in the M32C/87	N/A
IFSR0	N/A	4406Fh	-	N/A	Available only in the R32C/118
IFSRA	031Eh	N/A	-	Available only in the M32C/87	N/A
IFSR1	N/A	4406Dh	-	N/A	Available only in the R32C/118
AIER	0009h	N/A		Available only in the M32C/87	N/A
RMAD0	0012h-0010h	N/A	-	Available only in the M32C/87	N/A
RMAD1	0016h-0014h	N/A	-	Available only in the M32C/87	N/A
RMAD2	001Ah-0018h	N/A	-	Available only in the M32C/87	N/A
RMAD3	001Eh-001Ch	N/A	-	Available only in the M32C/87	N/A
RMAD4	002Ah-0028h	N/A	-	Available only in the M32C/87	N/A
RMAD5	002Eh-002Ch	N/A	-	Available only in the M32C/87	N/A
RMAD6	003Ah-0038h	N/A	-	Available only in the M32C/87	N/A
RMAD7	003Eh-003Ch	N/A	-	Available only in the M32C/87	N/A
AIER	0009h	N/A	-	Available only in the M32C/87	N/A

4.10 Watchdog Timer

Table 4.23 and Table 4.24 respectively list the changes on watchdog timer and associated SFRs.

Table 4.23 Comparison Chart: Watchdog Timer

Item	M32C/87	R32C/118
Clock source for watchdog timer	• CPU clock divided by the MCD register (PLL clock, main clock, on-chip oscillator clock) • Sub clock • On-chip oscillator clock	Peripheral bus clock (PLL clock, sub clock, or on-chip oscillator clock respectively divided by CCR register setting)
Watchdog timer prescaler divide ratio	Divide-by-2 (when sub clock is selected), -16, or -128	Divide-by-16, or -128

Table 4.24 Comparison Chart: Watchdog Timer-associated SFRs

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
CM0	0006h	40046h	-	Address changed	
			7	CPU clock select bit 0	Reserved
WDC	000Fh	4404Fh	-	Address changed	
			5	Coldstart/warmstart determination bit	Reserved
WDTS	000Eh	4404Eh	-	Address changed	

4.11 DMAC

Table 4.25 to Table 4.27 respectively list the changes on DMAC characteristics, settings, and associated SFRs.

Table 4.25 Comparison Chart: DMAC

Item	M32C/87	R32C/118
Transfer memory space	From a given address in a 16-Mbyte space to a fixed address in the same space or from a fixed address in a 16-Mbyte space to a given address in the same space	From a given address in a 64-Mbyte space (00000000h to 01FFFFFFh and FE000000h to FFFFFFFFh) to another given address in the same space
Maximum transfer bytes	• 128 Kbytes (when a 16-bit data is transferred) • 64 Kbytes (when a 8-bit data is transferred)	• 64 Mbytes (when a 32-bit data is transferred) • 32 Mbytes (when a 16-bit data is transferred) • 16 Mbytes (when a 8-bit data is transferred)
Transfer unit	8 bits or 16 bits	8 bits, 16 bits, or 32 bits
Destination address	Fixed address: one specified address Forward address: address which is incremented by a transfer unit on each successive access. (Source address and destination address cannot be both fixed nor both icremented.)	Forward or fixed

Table 4.26 Comparison Chart: DMAC Settings

Item	M32C/87	R32C/118
DMA request sources	Selected by bits DSEL4 to DSEL0 in the DMiSL register (i = 0 to 3)	Selected by bits DSEL4 to DSEL0 in the DMiSL register (i = 0 to 3) or bits DSEL24 to DSEL20 in the DMiSL2 register (i = 0 to 3)
Source address	DSAi register (i = 0 to 3) when either source address or destination address is fixed, or DMAi register (i = 0 to 3) when either source address or destination address is forward address (reloaded value in repeat transfer mode is set to the DRAi register)	DSAi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DSRi register)
Destination address		DDAi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DDRi register)

Table 4.27 Comparison Chart: DMAC-associated SFRs

Symbol		Address		Bits	M32C/87	R32C/118
M32C/87	R32C/118	M32C/87	R32C/118			
DM0SL		0378h	44078h	-	Address changed	
				5	Software DMA request bit	N/A (3)
				7	DMA request bit	N/A
DM1SL		0379h	44079h	-	Address changed	
				5	Software DMA request bit	N/A (4)
				7	DMA request bit	N/A
DM2SL		037Ah	4407Ah	-	Address changed	
				5	Software DMA request bit	N/A (5)
				7	DMA request bit	N/A
DM3SL		037Bh	4407Bh	-	Address changed	
				5	Software DMA request bit	N/A (6)
				7	DMA request bit	N/A
DM0SL2		N/A	44070h	-	N/A	Available only in the R32C/118
DM1SL2		N/A	44071h	-	N/A	Available only in the R32C/118
DM2SL2		N/A	44072h	-	N/A	Available only in the R32C/118
DM3SL2		N/A	44073h	-	N/A	Available only in the R32C/118
DMD0		CPU internal register (1)	CPU internal register (1)	-	Setting for the registers DMA0 and DMA1	DMD0: DMA0 setting
DMD1				-	Setting for registers DMA2 and DMA3	DMD1: DMA1 setting
N/A	DMD2	N/A		-	N/A	DMD2: DMA2 setting
N/A	DMD3	N/A		-	N/A	DMD3: DMA3 setting
DCT0 to DCT3		CPU internal register (1, 2)		-	DCT0, DCT1, DCT2 (bank1: R0), and DCT3 (bank1: R1)	DCT0, DCT1, DCT2, and DCT3
DRC0 to DRC3	DCR0 to DCR3			-	DRC0, DRC1, DRC2 (bank1: R2), and DRC3 (bank1: R3)	DCR0, DCR1, DCR2, and DCR3
DMA0 to DMA3	DDA0 to DDA3			-	DMA0, DMA1, DMA2 (bank1: A0), and DMA3 (bank1: A1) (forward source address and forward destination address are set)	DDA0, DDA1, DDA2, and DDA3 (destination address is set)
DSA0 to DSA3				-	DSA0, DSA1, DSA2 (bank1: FB), and DSA3 (bank1: SB) (fixed source address and fixed destination address are set)	DSA0, DSA1, DSA2, and DSA3 (source address is set)
DRA0 to DRA3	DSR0 to DSR3			-	DRA0, DRA1, DRA2 (SVP), and DRA3 (VCT) (reloaded value of the DMAi register (i = 0 to 3) is set)	DSR0, DSR1, DSR2, and DSR3 (reloaded value of the DSAi register (i = 0 to 3) is set)
N/A	DDR0 to DDR3	N/A		-	N/A	DDR0, DDR1, DDSR2, and DDR3 (reloaded value of the DDAi register (i = 0 to 3) is set)

Notes:
1. The LDC instruction should be used to write to this register.
2. To use DMA2 and DMA3, the register bank 1 and fast interrupt register are used.
3. Software DMA request bit is moved to bit 5 of the DM0SL2 register in the R32C/118.
4. Software DMA request bit is moved to bit 5 of the DM1SL2 register in the R32C/118.
5. Software DMA request bit is moved to bit 5 of the DM2SL2 register in the R32C/118.
6. Software DMA request bit is moved to bit 5 of the DM3SL2 register in the R32C/118.

4.12 Three-phase Motor Control Timers

Table 4.28 and Table 4.29 respectively list the changes on three-phase motor control timers and associated SFR.

Table 4.28 Comparison Chart: Three-phase Motor Control Timers

Item	M32C/87	R32C/118
Output function	N/A	Switchable pin combination: U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ of ports P7 and P8 or those of port P3

Table 4.29 Comparison Chart: Three-phase Motor Control Timers-associated SFR

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
IOBC	N/A	40097h	7	N/A	Three-phase output buffer control register

4.13 Serial Interface

Table 4.30 to Table 4.35 respectively list the changes on serial interface, associated pins, and associated SFRs.

Table 4.30 Comparison Chart: Serial Interface

Item	M32C/87	R32C/118
Synchronous/asynchronous serial interface	7 channels (UART0 to UART6)	9 channels (UART0 to UART8)
I^2C bus	5 channels (UART0 to UART4)	7 channels (UART0 to UART6)
Special mode 2	5 channels (UART0 to UART4)	7 channels (UART0 to UART6)
GCI mode	5 channels (UART0 to UART4)	N/A
SIM mode	5 channels (UART0 to UART4)	N/A
IEBus mode (optional (1))	5 channels (UART0 to UART4)	7 channels (UART0 to UART6)
IrDA mode	1 channel (UART0)	N/A

Note:
1. Please contact a Renesas sales office to use the optional feature.

Table 4.31 Comparison Chart: Serial Interface-associated Pins (1/2)

Channel	Port	M32C/87	R32C/118
UART0	P6_0	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$
	P6_1	CLK0	CLK0
	P6_2	RXD0/SCL0/STXD0/IrDAIN	RXD0/SCL0/STXD0
	P6_3	TXD0/SDA0/SRXD0/IrDAOUT	TXD0/SDA0/SRXD0
UART1	P6_4	$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$
	P6_5	CLK1	CLK1
	P6_6	RXD1/SCL1/STXD1	RXD1/SCL1/STXD1
	P6_7	TXD1/SDA1/SRXD1	TXD1/SDA1/SRXD1
UART2	P7_0	TXD2/SDA2/SRXD2	TXD2/SDA2/SRXD2/MSDA
	P7_1	RXD2/SCL2/STXD2	RXD2/SCL2/STXD2/MSCL
	P7_2	CLK2	CLK2
	P7_3	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$
UART3	P9_0	CLK3	CLK3
	P9_1	RXD3/SCL3/STXD3	RXD3/SCL3/STXD3
	P9_2	TXD3/SDA3/SRXD3	TXD3/SDA3/SRXD3
	P9_3	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$
	P4_0	N/A	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$
	P4_1	N/A	CLK3
	P4_2	N/A	RXD3/SCL3/STXD3
	P4_3	N/A	TXD3/SDA3/SRXD3
UART4	P9_4	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$
	P9_5	CLK4	CLK4
	P9_6	TXD4/SDA4/SRXD4	TXD4/SDA4/SRXD4
	P9_7	RXD4/SCL4/STXD4	RXD4/SCL4/STXD4
UART5	P7_6	TXD5	TXD5/SDA5/SRXD5
	P7_7	CLK5	CLK5
	P8_0	RXD5	RXD5/SCL5/STXD5
	P8_1	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$
	P15_0	TXD5	N/A
	P15_1	CLK5	N/A
	P15_2	RXD5	N/A
	P15_3	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	N/A

Table 4.32 Comparison Chart: Serial Interface-associated Pins (2/2)

Channel	Port	M32C/87	R32C/118
UART6	P12_0	$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$	TXD6/SDA6/SRXD6
	P12_1	CLK6	CLK6
	P12_2	RXD6	RXD6/SCL6/STXD6
	P12_3	TXD6	$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$
	P15_4	TXD6	TXD6/SDA6/SRXD6
	P15_5	RXD6	RXD6/SCL6/STXD6
	P15_6	CLK6	CLK6
	P15_7	$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$	$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$
	P4_4	N/A	$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$
	P4_5	N/A	CLK6
	P4_6	N/A	RXD6/SCL6/STXD6
	P4_7	N/A	TXD6/SDA6/SRXD6
UART7	P5_4	N/A	TXD7
	P5_5	N/A	CLK7
	P5_6	N/A	RXD7
	P5_7	N/A	$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$
	P15_0	N/A	TXD7
	P15_1	N/A	CLK7
	P15_2	N/A	RXD7
	P15_3	N/A	$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$
UART8	P7_3	N/A	TXD8
	P7_4	N/A	CLK8
	P7_5	N/A	RXD8
	P7_6	N/A	$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$
	P11_0	N/A	TXD8
	P11_1	N/A	CLK8
	P11_2	N/A	RXD8
	P11_3	N/A	$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$

Table 4.33 Comparison Chart: Serial Interface-associated SFRs (1/3)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
U5MR	01C0h	01C8h	-	Address changed	
			7	Reserved	TXD, RXD I/O polarity switch bit
U6MR	01C8h	01D8h	-	Address changed	
			7	Reserved	TXD, RXD I/O polarity switch bit
U7MR	N/A	01E0h	-	N/A	Available only in the R32C/118
U8MR	N/A	01E8h	-	N/A	Available only in the R32C/118
U0C0	036Ch		2	CTS function select bit	Reserved
			5	Data output select bit	Reserved
U1C0	02ECh		2	CTS function select bit	Reserved
			5	Data output select bit	Reserved
U2C0	033Ch		2	CTS function select bit	Reserved
			5	Data output select bit	Reserved
U3C0	032Ch		2	CTS function select bit	Reserved
			5	Data output select bit	Reserved
U4C0	02FCh		2	CTS function select bit	Reserved
			5	Data output select bit	Reserved
U5C0	01C4h	01CCh	-	Address changed	
			2	CTS function select bit	Reserved
U6C0	01CCh	01DCh	-	Address changed	
			2	CTS function select bit	Reserved
U7C0	N/A	01E4h	-	N/A	Available only in the R32C/118
U8C0	N/A	01ECh	-	N/A	Available only in the R32C/118
U0C1	036Dh		7	Clock division synchronous stop bit (Special mode 3), Error signal output enable bit (Special mode 4)	Reserved
U1C1	02EDh		7	Clock division synchronous stop bit (Special mode 3), Error signal output enable bit (Special mode 4)	Reserved
U2C1	033Dh		7	Clock division synchronous stop bit (Special mode 3), Error signal output enable bit (Special mode 4)	Reserved
U3C1	032Dh		7	Clock division synchronous stop bit (Special mode 3), Error signal output enable bit (Special mode 4)	Reserved
U4C1	02FDh		7	Clock division synchronous stop bit (Special mode 3), Error signal output enable bit (Special mode 4)	Reserved

Table 4.34 Comparison Chart: Serial Interface-associated SFRs (2/3)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
U5C1	01C5h	01CDh	-	Address changed	
			4	N/A	UART5 transmit interrupt source select bit
			5	N/A	UART5 continuous receive mode enable bit
			6	N/A	Logical inversion select bit
			7	N/A	Reserved
U6C1	01CDh	01DDh	-	Address changed	
			4	N/A	UART6 transmit interrupt source select bit
			5	N/A	UART6 continuous receive mode enable bit
			6	N/A	Logical inversion select bit
			7	N/A	Reserved
U7C1	N/A	01E5h	-	N/A	Available only in the R32C/118
U8C1	N/A	01EDh	-	N/A	Available only in the R32C/118
U56CON	01D0h	N/A	-	Available only in the M32C/87	N/A
U78CON	N/A	01F0h	-	N/A	Available only in the R32C/118
U0SMR	0367h		7	Clock division synchronous bit	Reserved
U1SMR	02E7h		7	Clock division synchronous bit	Reserved
U2SMR	0337h		7	Clock division synchronous bit	Reserved
U3SMR	0327h		7	Clock division synchronous bit	Reserved
U4SMR	02F7h		7	Clock division synchronous bit	Reserved
U5SMR	N/A	01C7h	-	N/A	Available only in the R32C/118
U6SMR	N/A	01D7h	-	N/A	Available only in the R32C/118
U0SMR2	0366h		7	External clock synchronous enable bit	Reserved
U1SMR2	02E6h		7	External clock synchronous enable bit	Reserved
U2SMR2	0336h		7	External clock synchronous enable bit	Reserved
U3SMR2	0326h		7	External clock synchronous enable bit	Reserved
U4SMR2	02F6h		7	External clock synchronous enable bit	Reserved
U5SMR2	N/A	01C6h	-	N/A	Available only in the R32C/118
U6SMR2	N/A	01D6h	-	N/A	Available only in the R32C/118
U0SMR3	0365h		3	Clock output select bit	Reserved
U1SMR3	02F5h		3	Clock output select bit	Reserved
U2SMR3	0335h		3	Clock output select bit	Reserved
U3SMR3	0325h		3	Clock output select bit	Reserved
U4SMR3	02F5h		3	Clock output select bit	Reserved
U5SMR3	N/A	01C5h	-	N/A	Available only in the R32C/118
U6SMR3	N/A	01D5h	-	N/A	Available only in the R32C/118
U5SMR4	N/A	01C4h	-	N/A	Available only in the R32C/118

Table 4.35 Comparison Chart: Serial Interface-associated SFRs (3/3)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
U6SMR4	N/A	01D4h	-	N/A	Available only in the R32C/118
U5BRG	01C1h	01C9h	-	Address changed	
U6BRG	01C9h	01D9h	-	Address changed	
U7BRG	N/A	01E1h	-	N/A	Available only in the R32C/118
U8BRG	N/A	01E9h	-	N/A	Available only in the R32C/118
U5TB	01C3h-01C2h	01CBh-01CAh	-	Address changed	
U6TB	01CBh-01CAh	01DBh-01DAh	-	Address changed	
U7TB	N/A	01E3h-01E2h	-	N/A	Available only in the R32C/118
U8TB	N/A	01EBh-01EAh	-	N/A	Available only in the R32C/118
U5RB	01C7h-01C6h	01CFh-01CEh	-	Address changed	
			11	N/A	Arbitration lost detection flag
U6RB	01CFh-01CEh	01DFh-01DEh	-	Address changed	
			11	N/A	Arbitration lost detection flag
U7RB	N/A	01E7h-01E6h	-	N/A	Available only in the R32C/118
U8RB	N/A	01EFh-01EEh	-	N/A	Available only in the R32C/118
IRCON	0372h	N/A	-	Available only in the M32C/87	N/A
U56IS	01D1h	N/A	-	Available only in the M32C/87	N/A
IFSRA (IFSR0)	031Eh	4406Fh	-	Address changed	
IFSR1	N/A	4406Dh	-	N/A	Available only in the R32C/118

4.14 D/A Converter

Table 4.36 lists the change on SFR associated with the D/A converter.

Table 4.36 Comparison Chart: D/A Converter-associated SFR

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
DACON1	039Dh	N/A	-	Available only in the M32C/87	N/A

4.15 Intelligent I/O

Table 4.37 and Table 4.39 respectively list the changes on the configuration of intelligent I/O and associated SFRs.

Table 4.37 Comparison Chart: Intelligent I/O

Item	M32C/87	R32C/118
Base timer	• Group 0: No timer • Group 1: 1 timer (two-phase pulse processing provided) • Group 2: 1 timer (two-phase pulse processing not provided)	• Group 0: 1 timer (two-phase pulse processing provided) • Group 1: 1 timer (two-phase pulse processing provided) • Group 2: 1 timer (two-phase pulse processing not provided)
Time measurement	• Group 0: No channel • Group 1: 16 bits × 8 • Group 2: No channel	• Group 0: 16 bits × 8 • Group 1: 16 bits × 8 • Group 2: No channel
Waveform generation	• Group 0: No channel • Group 1: 16 bits × 8 • Group 2: 16 bits × 8	• Group 0: 16 bits × 8 • Group 1: 16 bits × 8 • Group 2: 16 bits × 8
Serial interface	• Group 0: 1 channel Synchronous serial I/O mode, HDLC data processing mode • Group 1: 1 channel Synchronous serial I/O mode, asynchronous serial I/O mode, HDLC data processing mode • Group 2: 1 channel Variable-length synchronous serial I/O mode, IEBus mode (optional (1))	• Group 0: No channel • Group 1: No channel • Group 2: 1 channel Variable-length synchronous serial I/O mode, IEBus mode (optional (1))

Note:
1. Please contact a Renesas sales office to use the optional feature.

Table 4.38 Comparison Chart: Intelligent I/O associated SFRs (1/2)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
G0BT	N/A	01A1h-01A0h	-	N/A	Available only in the R32C/118
G0BCR0	N/A	01A2h	-	N/A	Available only in the R32C/118
G0BCR1	N/A	01A3h	-	N/A	Available only in the R32C/118
G1BCR1	0123h		0	Reserved	Base timer reset source select bit 0
BTSR	0164h		0	Reserved	Group 0 base timer start bit
G0TMCR0	N/A	0198h	-	N/A	Available only in the R32C/118
G0TMCR1	N/A	0199h	-	N/A	Available only in the R32C/118
G0TMCR2	N/A	019Ah	-	N/A	Available only in the R32C/118
G0TMCR3	N/A	019Bh	-	N/A	Available only in the R32C/118
G0TMCR4	N/A	019Ch	-	N/A	Available only in the R32C/118
G0TMCR5	N/A	019Dh	-	N/A	Available only in the R32C/118
G0TMCR6	N/A	019Eh	-	N/A	Available only in the R32C/118
G0TMCR7	N/A	019Fh	-	N/A	Available only in the R32C/118
G0TPR6	N/A	01A4h	-	N/A	Available only in the R32C/118
G0TPR7	N/A	01A5h	-	N/A	Available only in the R32C/118
G0TM0/ G0PO0	N/A	0181h-0180h	-	N/A	Available only in the R32C/118
G0TM1/ G0PO1	N/A	0183h-0182h	-	N/A	Available only in the R32C/118
G0TM2/ G0PO2	N/A	0185h-0184h	-	N/A	Available only in the R32C/118
G0TM3/ G0PO3	N/A	0187h-0186h	-	N/A	Available only in the R32C/118
G0TM4/ G0PO4	N/A	0189h-0188h	-	N/A	Available only in the R32C/118
G0TM5/ G0PO5	N/A	018Bh-018Ah	-	N/A	Available only in the R32C/118
G0TM6/ G0PO6	N/A	018Dh-018Ch	-	N/A	Available only in the R32C/118
G0TM7/ G0PO7	N/A	018Fh-018Eh	-	N/A	Available only in the R32C/118
G0POCR0	N/A	0190h	-	N/A	Available only in the R32C/118
G0POCR1	N/A	0191h	-	N/A	Available only in the R32C/118
G0POCR2	N/A	0192h	-	N/A	Available only in the R32C/118
G0POCR3	N/A	0193h	-	N/A	Available only in the R32C/118
G0POCR4	N/A	0194h	-	N/A	Available only in the R32C/118
G0POCR5	N/A	0195h	-	N/A	Available only in the R32C/118
G0POCR6	N/A	0196h	-	N/A	Available only in the R32C/118
G0POCR7	N/A	0197h	-	N/A	Available only in the R32C/118
G0FS	N/A	01A7h	-	N/A	Available only in the R32C/118
G0FE	N/A	01A8h	-	N/A	Available only in the R32C/118
CCS	00F6h	-	-	Available only in the M32C/87	N/A

Table 4.39 Comparison Chart: Intelligent I/O associated SFRs (2/2)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
G0EMR	00FCh	-	-	Available only in the M32C/87	-
G1EMR	013Ch	-	-	Available only in the M32C/87	-
G0MR	00EDh	-	-	Available only in the M32C/87	-
G1MR	012Dh		-	Available only in the M32C/87	-
G0CR	00EFh		-	Available only in the M32C/87	-
G1CR	012Fh	-	-	Available only in the M32C/87	-
G0ETC	00FFh	-	-	Available only in the M32C/87	-
G1ETC	013Fh	-	-	Available only in the M32C/87	-
G0ERC	00FDh	-	-	Available only in the M32C/87	-
G1ERC	013Dh	-	-	Available only in the M32C/87	-
G0IRF	00FEh			Available only in the M32C/87	
G1IRF	013Eh	-	-	Available only in the M32C/87	-
G0CMP0	00F0h	-	-	Available only in the M32C/87	-
G0CMP1	00F1h	-	-	Available only in the M32C/87	-
G0CMP2	00F2h	-	-	Available only in the M32C/87	-
G0CMP3	00F3h	-	-	Available only in the M32C/87	-
G1CMP0	0130h	-	-	Available only in the M32C/87	-
G1CMP1	0131h	-	-	Available only in the M32C/87	-
G1CMP2	0132h	-	-	Available only in the M32C/87	-
G1CMP3	0133h	-	-	Available only in the M32C/87	-
G0MSK0	00F4h	-	-	Available only in the M32C/87	-
G0MSK1	00F5h	-	-	Available only in the M32C/87	-
G1MSK0	0134h	-	-	Available only in the M32C/87	-
G1MSK1	0135h	-	-	Available only in the M32C/87	-
G0TCRC	00FBh-00FAh	-	-	Available only in the M32C/87	-
G1TCRC	013Bh-013Ah	-	-	Available only in the M32C/87	-
G0RCRC	00F9h-00F8h	-	-	Available only in the M32C/87	-
G1RCRC	0139h-0138h	-	-	Available only in the M32C/87	-
G0TB/G0DR	00EAh	-	-	Available only in the M32C/87	-
G1TB/G1DR	012Ah	-	-	Available only in the M32C/87	-
G0RB	00E9h-00E8h	-	-	Available only in the M32C/87	-
G1RB	0129h-0128h	-	-	Available only in the M32C/87	-
G0RI	00ECh	-	-	Available only in the M32C/87	-
G1RI	012Ch	-	-	Available only in the M32C/87	-
G0T0	00EEh	-	-	Available only in the M32C/87	-
G1T0	012Eh	-	-	Available only in the M32C/87	-

4.16 CAN Module

Table 4.40 lists the changes in the CAN module.

Table 4.40 Comparison Chart: CAN Module

Item	M32C/87	R32C/118
Protocol	CAN Specification 2.0B	ISO11898-1 Specifications
Bit rate	Up to 1 Mbps	Up to 1 Mbps
Message boxes	16 slots	32 mailboxes
Time stamp function	Time stamp function using a 16-bit counter. Count source can be selected from the CAN bus bit clock divided by 1, 2, 3, or 4	Time stamp function using a 16-bit counter. The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.
Interrupt sources	6 types: • Message slot k (k = 0 to 15) transmit operation completed • Message slot k receive operation completed • Bus error detected • Error-passive state entered • Bus-off state entered • Wake-up	6 types: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error (bus-error, error-warning, error-passive, bus-off entry, bus-off recovery, overload frame transmit, and bus lock) • Wake-up
Software support units		3 software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Selectable peripheral function clock (f1) or main clock	Selectable peripheral bus clock or main clock
Test modes	• Listen-only mode • Self-test mode 1 (internal loop back)	• Listen-only mode • Self-test mode 0 (external loop back) • Self-test mode 1 (internal loop back)

There is no compatibility with the SFRs in the CAN module. Refer to the hardware manual for details.

4.17 Ports

4.17.1 Port Pi Registers and Port Pi Direction Registers

Table 4.41 to Table 4.42 list the the changes on port Pi register and port Pi direction register, respectively. Table 4.43 lists the changes on port Pi pull-up control register.

Table 4.41 Comparison Chart: Port Pi registers (i = 0 to 15)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
P0	03E0h	03C0h	-	Address changed	
P1	03E1h	03C1h	-	Address changed	
P2	03E4h	03C4h	-	Address changed	
P3	03E5h	03C5h	-	Address changed	
P4	03E8h	03C8h	-	Address changed	
P5	03E9h	03C9h	-	Address changed	
P6	03C0h	03CCh	-	Address changed	
P7	03C1h	03CDh	-	Address changed	
P8	03C4h	03D0h	-	Address changed	
P9	03C5h	03D1h	-	Address changed	
P10	03C8h	03D4h	-	Address changed	
P11	03C9h	03D5h	-	Address changed	
P12	03CCh	03D8h	-	Address changed	
P13	03CDh	03D9h	-	Address changed	
P14	03D0h	03DCh	-	Address changed	
			0	Port P14_0 bit	Reserved
			1	Port P14_1 bit	Port P14_1 bit input only
			2	Port P14_2 bit	Reserved
P15	03D1h	03DDh	-	Address changed	

Table 4.42 Comparison Chart: Port Pi Direction Registers (i = 0 to 15)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
PD0	03E2h	03C2h	-	Address changed	
PD1	03E3h	03C3h	-	Address changed	
PD2	03E6h	03C6h	-	Address changed	
PD3	03E7h	03C7h	-	Address changed	
PD4	03EAh	03CAh	-	Address changed	
PD5	03EBh	03CBh	-	Address changed	
PD6	03C2h	03CEh	-	Address changed	
PD7	03C3h	03CFh	-	Address changed	
PD8	03C6h	03D2h	-	Address changed	
PD9	03C7h	03D3h	-	Address changed	
PD10	03CAh	03D6h	-	Address changed	
PD11	03CBh	03D7h	-	Address changed	
PD12	03CEh	03DAh	-	Address changed	
PD13	03CFh	03DBh	-	Address changed	
PD14	03D2h	03DEh	-	Address changed	
			0	Port P14_0 direction bit	Reserved
			1	Port P14_1 direction bit	Reserved
			2	Port P14_2 direction bit	Reserved
PD15	03D3h	03DFh	-	Address changed	

Table 4.43 Comparison Chart: Port Pi Pull-up Control Registers (i = 0 to 15)

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
PUR1	03F1h		0	P4_0 to P4_3 pull-up	No register bit
			1	P4_4 to P4_7 pull-up	No register bit
			3	P5_4 to P5_7 pull-up	No register bit
PUR2	03DAh	03F2h	-	Address changed	
			0	P6_0 to P6_3 pull-up	No register bit
			1	P6_4 to P6_7 pull-up	No register bit
			2	P7_2 to P7_3 pull-up	No register bit
			3	P7_4 to P7_7 pull-up	No register bit
			4	P8_0 to P8_3 pull-up	No register bit
PUR3	03DBh	03F3h	-	Address changed	
PUR4	03DCh	03F4h	-	Address changed	
			0	P14_0 to P14_3 pull-up	P14_1, P14_3 pull-up control bit

4.17.2 Port I/O Function Selection

In the R32C/118, an output function of either the programmable I/O port or a peripheral function is selected by the port Pi_j function select registers (i = 0 to 10, j = 0 to 7). As for the input function, the R32C/118 has differently configured registers from those of the M32C/87 as shown in Table 4.44. Refer to the hardware manual for details.

Table 4.44 Comparison Chart: Port I/O Function Select Registers

Item	M32C/87	R32C/118
Output function	• Function select registers A (PSm register (m = 0 to 9) • Function select registers B (PSLn register (n = 0 to 3, 5 to 7, and 9) • Function select registers C (PSC, PSC2, PSC3, and PSC6) • Function select registers D (PSD1 and PSD2) • Function select registers E (PSE1 and PSE2)	Port Pi_j function select registers (Pi_js (i = 0 to 15, j = 0 to 7)
Input function	Input function select registers (IPS, IPSA, and IPSB)	Input function select registers (IFS0 to IFS3)

4.18 Flash Memory

4.18.1 Flash Memory

Table 4.45 to Table 4.47 respectively list the changes on flash memory, software commands, and associated registers.

Table 4.45 Comparison Chart: Flash Memory

Item	M32C/87	R32C/118
Unit to be programmed	2 bytes	8 bytes
Software commands	7	9

Table 4.46 Comparison Chart: Software Commands

Item	M32C/87				R32C/118			
	First command		Second command		First command		Second command	
	Address	Data	Address	Data	Address	Data	Address	Data
Read array mode shift	x	xxFFh	N/A	N/A	FFFFF800h	00FFh	N/A	N/A
Read status register mode shift (1)	x	xx70h	N/A	N/A	FFFFF800h	0070h	N/A	N/A
Clear status register	x	xx50h	N/A	N/A	FFFFF800h	0050h	N/A	N/A
Program (2, 3)	WA	xx40h	WA	WD	FFFFF800h	0043h	WA	WD
Block erase	x	xx20h	BA	xxD0h	FFFFF800h	0020h	BA	00D0h
Lock bit program	BA	xx77h	BA	xxD0h	FFFFF800h	0077h	BA	00D0h
Read lock bit status	x	xx71h	BA	xxD0h	FFFFF800h	0071h	BA	00D0h
Read lock bit status mode shift (4)	N/A	N/A	N/A	N/A	FFFFF800h	0071h	N/A	N/A
Protect bit program	N/A	N/A	N/A	N/A	FFFFF800h	0067h	PBA	00D0h
Read protect bit status mode shift (4)	N/A	N/A	N/A	N/A	FFFFF800h	0061h	N/A	N/A

WA: Even address to be written
WD: 16-bit write data
BA: Even address in specified block
PBA: Address of the protect bit
x: Any even address in the user ROM area
xx: Upper byte of command code (ignored)
N/A: Not applicable

Notes:
1. This command cannot be executed in EW1 mode.
2. In the M32C/87, a set of command consists of two words from the first command to the second. The program is performed in 16-bit (1-word) unit.
3. In the R32C/118, a set of command consists of five words from the first command to the fifth. The program is performed in 64-bit (4-word) unit. The higher 29 bits of the address WA should be fixed and the lower three bits of respective command from the second to fifth should be set to 000b, 010b, 100b, and 110b for the addresses 0h, 2h, 4h, and 6h, or 8h, Ah, Ch, and Eh.
4. This command should be executed in RAM.

Table 4.47 Comparison Chart: Flash Memory-associated SFRs

Symbol	Address		Bits	Differences	
	M32C/87	R32C/118		M32C/87	R32C/118
FMR0	0057h	40000h	7 to 0	Register configuration is completely different	
FMR1	0055h	40009h	7 to 0	Register configuration is completely different	
FMCR	N/A	0006h	-	N/A	Available only in the R32C/118
FEBC0	N/A	001Dh-001Ch	-	N/A	Available only in the R32C/118
FEBC3	N/A	0010h-0011h	-	N/A	Available only in the R32C/118
FPR0	N/A	40008h	-	N/A	Available only in the R32C/118
FMSR0	N/A	40001h	-	N/A	Available only in the R32C/118
FBPM0	N/A	4000Ah	-	N/A	Available only in the R32C/118
FBPM1	N/A	4000Bh	-	N/A	Available only in the R32C/118
FBPM2	N/A	40011h	-	N/A	Available only in the R32C/118

4.18.2 Flash Memory Block Configuration

The R32C/118 has the different block configuration of flash memory from that of the M32C/87. Refer to the yellow blocks in Figure 4.1 below.

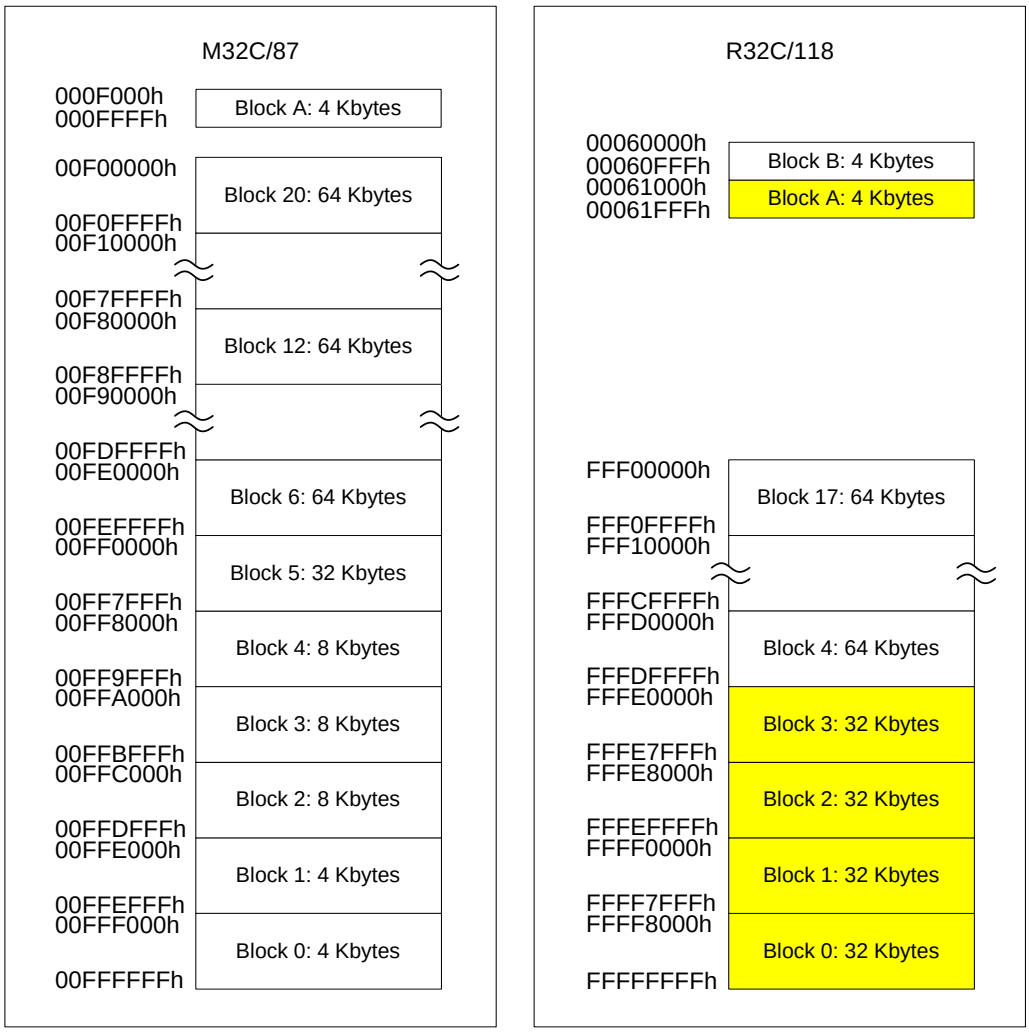

Figure 4.1 Comparison Diagram: Flash Memory Block Configuration

4.18.3 ID Code Protection

Figure 4.2 shows the stored ID code location of respective product.

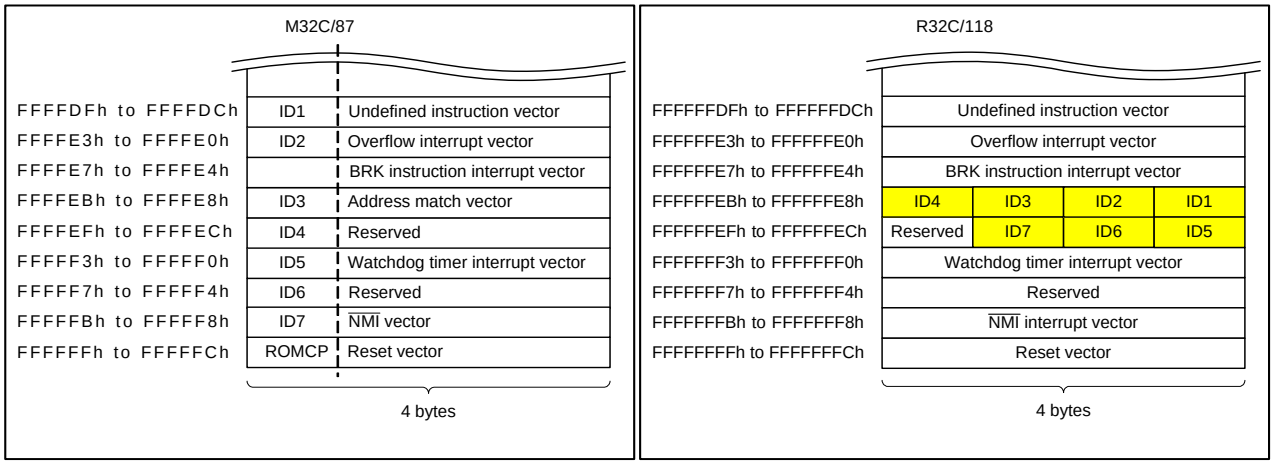

Figure 4.2 Comparison Diagram: Addresses for ID Code Stored

4.18.4 ROM Code Protection

Table 4.48 lists the change on ROM code protection-associated register.

Table 4.48 Comparison Chart: ROM Code Protection

Symbol	Address		Bits	M32C/87	R32C/118
	M32C/87	R32C/118			
ROMCP	FFFFFFh	N/A	7, 6	Available only in the M32C/87	N/A

In the R32C/118, each block has two protect bits. Table 4.49 lists the addresses of the protect bits. If any of these protect bits is set to 0 (protected), all areas are protected. Refer to the hardware manual for details.

Table 4.49 R32C/118 **Protect Bit Addresses**

Block	Protect bit 0	Protect bit 1
Block B	00060100h	00060300h
Block A	00061100h	00061300h
Block 17	FFF00100h	FFF00300h
Block 16	FFF10100h	FFF10300h
Block 15	FFF20100h	FFF20300h
Block 14	FFF30100h	FFF30300h
Block 13	FFF40100h	FFF40300h
Block 12	FFF50100h	FFF50300h
Block 11	FFF60100h	FFF60300h
Block 10	FFF70100h	FFF70300h
Block 9	FFF80100h	FFF80300h
Block 8	FFF90100h	FFF90300h
Block 7	FFFA0100h	FFFA0300h
Block 6	FFFB0100h	FFFB0300h
Block 5	FFFC0100h	FFFC0300h
Block 4	FFFD0100h	FFFD0300h
Block 3	FFFE0100h	FFFE0300h
Block 2	FFFE8100h	FFFE8300h
Block 1	FFFF0100h	FFFF0300h
Block 0	FFFF8100h	FFFF8300h

4.19 Differences in Development Tools

Table 4.50 lists the differences on development tools.

Table 4.50 Comparison Chart: Development Tools

Tools	For M32C/87	For R32C/118
C compiler (including simulator debugger)	M3T-NC308WA	C compiler package for R32C Series
Real-time OS	M3T-MR308/4	M3T-MR100/4
Emulator debugger	PC7501	E30A
Emulation probe	M30870T-EPB	N/A
Compact emulator	M30870T2-CPE	N/A
Renesas Stater Kits	R0K330879S001BE	R0K564189S000BE

5. Reference Documents

- Hardware Manuals
  M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual (Rev.1.51) issued on Jul.31, 2008
  R32C/118 Group Hardware Manual (Rev.1.00) issued on Nov.24, 2009.
  The latest version can be downloaded from the Renesas Electronics website.

- Technical News/Technical Update
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REVISION HISTORY	M32C/87 Group, R32C/118 Group Differences between M32C/87 and R32C/118

Rev.	Date	Description	
		Page	Summary
1.00	Apr 01, 2010	—	First Edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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