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4513 Group, 4518 Group

Differences between 4513 Group and 4518 Group

1. Differences between 4513 Group and 4518 Group

Parameter			4513 Group	4518 Group
CPU	TABP instruction	*1	Low-order 8 bits of 10 bits data in ROM can be referred. (Register A,B)	All 10 bits data in ROM can be referred. (Register A,B,D)
	Minimum instruction execution time		0.75 μ s(f(XIN)=4.0 MHz)	0.5 μ s(f(XIN)=6.0 MHz)
I/O port	D	*2	N-channel open-drain output Input voltage : Vss to 12 V	N-channel open-drain output / CMOS output selectable Input voltage : Vss to VDD
	P0		N-channel open-drain output	N-channel open-drain output / CMOS output selectable
	P1		N-channel open-drain output	N-channel open-drain output / CMOS output selectable
	P2		Input port	I/O port
	P6		-	P6 can be also used as analog input pins.
	P0, P1 pull-up transistor control		2-port unit	1 port unit
	Input control of INT0 and INT1	*3	-	Available
Timer	Prescaler		Prescaler(divided by 4/divided by 16)	8-bit programmable timer
	Timer 1	Count source	ORCLK	INSTCK, ORCLK, XIN, CNTR0
		Timer 1 count auto-stop circuit	-	Available
		Period measurement and pulse width measurement function	-	Available
	Timer 2	Count source	*4 T1UDF, ORCLK, CNTR0, WDTUDF	T1UDF, ORCLK, STCK, PWMOUT
	Timer 3	Count source	T2UDF, ORCLK	T2UDF, ORCLK, CNTR1, PWMOUT
		Timer 3 count auto-stop circuit	-	Available
		PWM output function	-	Available
	Timer 4	Count source	*5 T3UDF, ORCLK, CNTR1	ORCLK/2, XIN
		Reload register	*6 1 (R4)	2(R4L, R4H)
		PWM output function	-	Available
	CNTR0 input		Timer 2 count source (Rising edge)	Timer 1 count source (Rising edge / falling edge selectable)
	CNTR0 output		T1UDF/2 AND signal of T1UDF/2 and T2UDF/2	T1UDF/2 T2UDF/2
	CNTR1 input		Timer 4 count source (Rising edge)	Timer 3 count source (Rising edge / falling edge selectable)
	CNTR1 output		T3UDF/2 AND signal of T3UDF/2 and T4UDF/2	PWM output (Timer 4)

Parameter			4513 Group	4518 Group
Timer	Watchdog timer	At reset *7	Invalid at reset. Watchdog timer becomes valid when WRST instruction is executed.	Valid at reset. Watchdog timer becomes invalid when DWDT and WRST instructions are executed continuously.
		WRST instruction *7	(WDF1) <- 0 (WEF) <- 1	(WDF1) = 1? After skipping, (WDF1) <- 0
		WRST instruction execution period	Executed until 32766 machine cycles	Executed until 65534 machine cycles
		RAM back-up	Invalid after system returns from RAM back-up mode	Valid after system returns from RAM back-up mode
A/D converter	Supply voltage *8		3.0 V to 5.5 V	2.0 V to 5.5 V (MASK ROM) , 3.0 V to 5.5 V (One Time PROM)
	A/D conversion clock (ADCK)		INSTCK/6	INSTCK/6 , INSTCK/12 , INSTCK/24 , INSTCK/48 f(RING)/6 , f(RING)/12 , f(RING)/24 , f(RING)/48
	Pin function	A _{IN0} to A _{IN3} *9	Analog input-only pin (A _{IN0} /CMP0- to A _{IN3} /CMP1+)	Pin function is switched to analog input or port input/output. (P6 ₀ /A _{IN0} to P6 ₃ /A _{IN3})
	A/D conversion time		62 machine cycles	2 machine cycles+10/f(ADCK)
	Comparator comparison time		8 machine cycles	2 machine cycles+1/f(ADCK)
	Voltage comparator		Available	-
Serial I/O	Synchronous clock		External , INSTCK/8 , INSTCK/4	External , INSTCK/8, INSTCK/4, INSTCK/2
	Port function selected		Selected from 2 patterns.	Selected from 4 patterns.
Reset	Reset release timing		System is released from reset after f(X _{IN}) counts 16892 to 16895 times.	System is released from reset after f(RING) counts 120 to 144 times.
	Built-in power-on reset circuit		-	Available
	SRST instruction *10		-	Available
	Pull-up transistor in RESET pin		-	Available
Voltage drop detection circuit	Operation state	VDCE pin = "L"	Stop	Stop
		VDCE pin = "H"	At CPU operating : operation At RAM back-up : stop	At CPU operating : operation At RAM back-up : operation
	Detection voltage hysteresis		-	Available (typ. 0.2V)
RAM back-up mode	External wakeup signal	P0 *11	falling edge	H leve/L level and Rising edge / falling edge selectable
	valid waveform	P1 *11	falling edge	L level
		INT0, INT1 *11	H/L level	H leve/L level and Rising edge / falling edge selectable
	*12 INT0, INT1 wakeup function		Always valid	Valid/invalid selcstable

Parameter		4513 Group	4518 Group
Clock control	On-chip oscillator	-	Available
	Main clock	Ceramic resonator	Ceramic resonator/RC oscillation / quartz-crystal oscillation
	System clock	High-speed mode: $f(X_{IN})$ Middle-speed mode: $f(X_{IN})/2$	Through mode : $f(X_{IN})$, $f(RING)$ Frequency divided by 2 mode : $f(X_{IN})/2$, $f(RING)/2$ Frequency divided by 4 mode : $f(X_{IN})/4$, $f(RING)/4$ Frequency divided by 8 mode : $f(X_{IN})/8$, $f(RING)/8$
Electrical characteristics	Supply voltage	2.0 V to 5.5 V(MASK ROM) Depends on operating mode.	1.8 V to 5.5 V(MASK ROM) Depends on operating mode.
	RAM back-up voltage	1.8 V(MASK ROM), 2.0 V(One Time PROM)	1.6 V(MASK ROM), 2.0V(One Time PROM)

- * 1. Register D is changed.
2. The maximum value of input voltage is VDD.
3. According to the difference of I/O pin structure, the setting of unused pins may be different.
4. In the 4518 Group, CNTR0 input is a timer 1 count source, and there is no underflow count function of a watchdog timer.
5. In the 4518 Group, CNTR1 input is a timer 3 count source.
6. T4AB instruction becomes storing in R4L, not in timer 4
7. At reset, a watchdog function becomes valid and the function of a WRST instruction differs from the 4513 Group.
8. The supply voltage value is guaranteed accurately under the -20°C to 85°C condition .
9. The pin set as the analog input does not function as a port.
10. The cold start by program is possible.
11. The valid waveform of a wakeup signal can be selected.
12. State transition has changed by difference of an oscillation circuit.
Moreover, super low consumption current operation is possible by operating system by the on-chip oscillator or quartz-crystal oscillation (32kHz).
13. RAM of M34518M2-XXXSP/FP is 256 words. (RAM of M34513M2-XXXSP/FP is 128 words.)
14. The One Time PROM version is M34518E8SP/FP only. (E4 version is not existed.)

The above table shows difference, some specifications and standards, not for all.

Moreover, fundamentally, the specification of each function is strengthened and register ability also differs.

Be sure to refer to the data sheet as for the latest detailed specification and an electrical characteristics.

2. Reference Document

Data Sheet

4518 Group Datasheet

4513/4514 Group Datasheet

(Use the most recent version of the document on the Renesas Technology Web site.)

User's Manual

4513/4514 Group User's Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical News/Technical Update

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Revision History

Rev.	Date	Description	
		Page	Summary
1.01	Jul 14.2004	—	Issue as reference selection.
1.02	Mar 18.2005	—	Change to application note format and issue
2.00	May 18,2007	2	Add parameter of Voltage drop detection circuit

Notes regarding these materials

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