Debugging IDT S-RIO Gen2 Switches Using RapidFET JTAG™

Application Note

Formal Status

March 29, 2012

About this Document

This document discusses common problems that are encountered when debugging with a board that contains S-RIO Gen2 switches using RapidFET (Fabric Embedded Tools) JTAG. Examples are provided and possible solutions are explained.

Topics discussed include the following:

- Getting Started
- Connecting RapidFET JTAG to the Target Device
- Checking the S-RIO Links
- Signal Integrity Issues
- Error Status
- Datapath Testing
- Loading Serial EEPROMs

Getting Started

Installing RapidFET JTAG Software

This document does not discuss software installation. It is assumed that software is properly installed and licensing is valid.

Loading IDT Device-Specific Libraries

The base software installation does not include device-specific register definitions. Therefore it is necessary to download the RapidFET JTAG modules for the targeted S-RIO switches. The modules can be downloaded from the IDT secure website. Download the files and run setup.exe.

RapidFET FET JTAG Options

RapidFET JTAG is offered in two versions: Standard and Enhanced. Throughout this document, features that are specific to RapidFET Enhanced are marked as (Enhanced Version Only).

RapidFET JTAG Pod Pinout

The RapidFET JTAG pod interface connects to the board under test on a 5 x 2 (0.1 inch pin pitch) header. The pin assignment is displayed in Figure 1.

Figure 1: 10-pin Header Pin Location

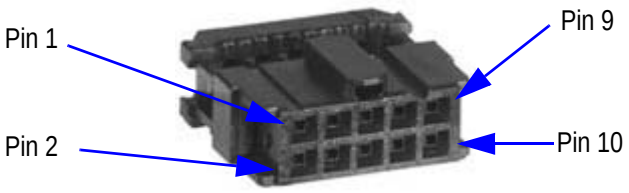


Table 1: JTAG Header Signal Description

Pin Number	Description
1	TRST#
2	GND
3	TDI
4	GND
5	TDO
6	GND
7	TMS
8	GND
9	TCK
10	GND

The RapidFET pod I2C interface connects to the board under test on a 5 x 2 (0.1 inch pin pitch) header. The pin assignment is provided below.

Table 2: I2C Header Signal Description

Pin Number	Description
1	SCL
2	GND
3	SDA
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	GND

Fabric Embedded Tools also provides a flying lead header breakout adapter to be used when connecting to custom equipment.

Connecting RapidFET JTAG to the Target Device

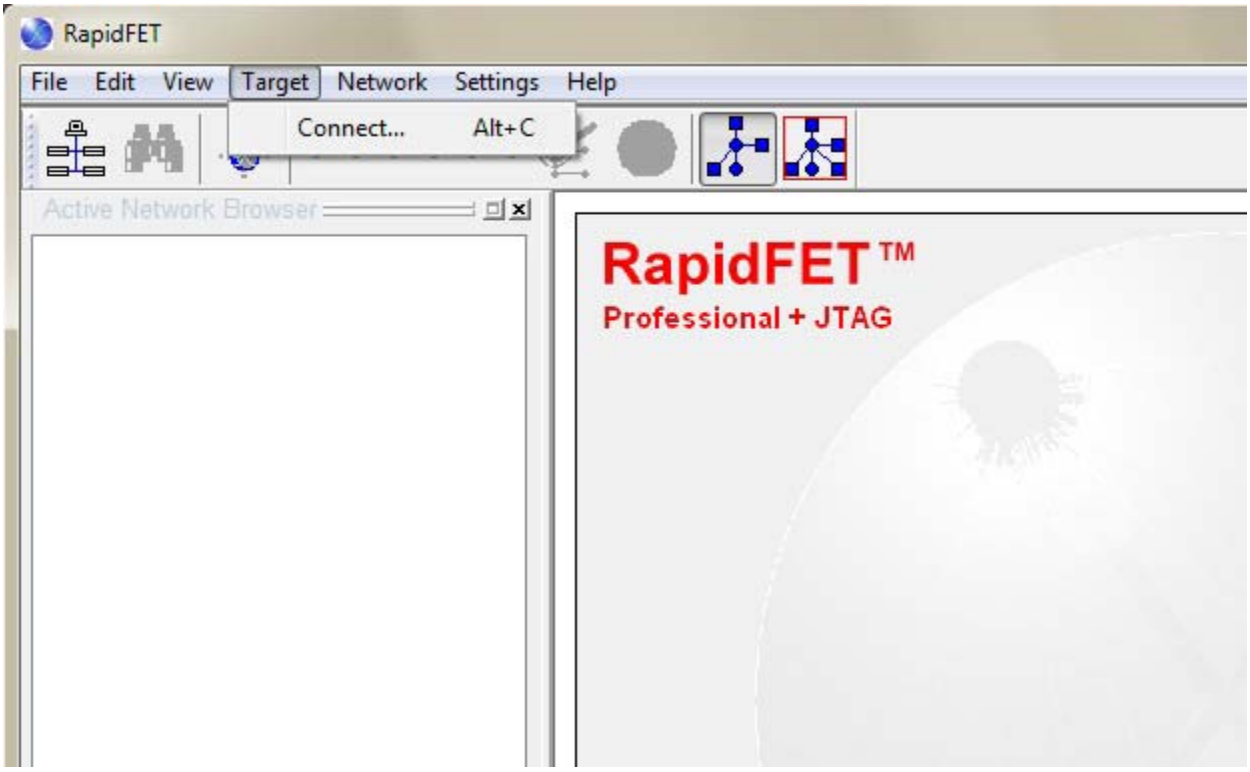
In order to establish a connection to the target device, several aspects of the system *must* be functional:

- RapidFET JTAG software and device drivers must be installed properly on a host PC.
- The JTAG chain or the I2C bus on the target board must be properly connected.
- The target device must be properly powered up, have a valid clock, and be out of reset.

When the items above are completed, proceed as follows:

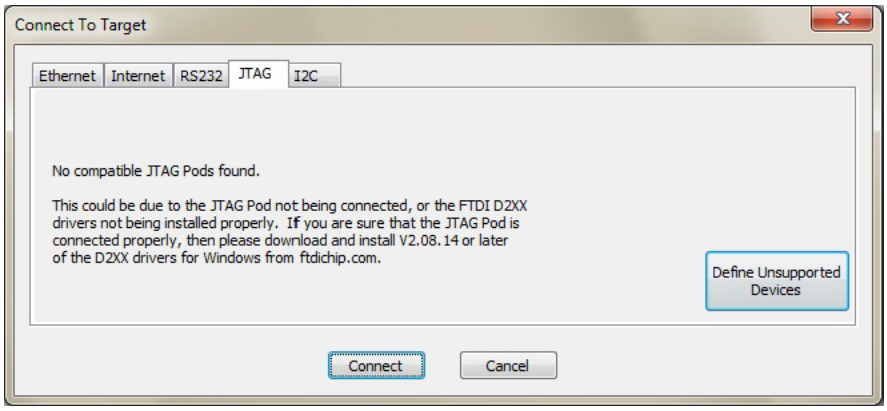
1. Connect the RapidFET JTAG pod to the target board.
2. Connect the RapidFET JTAG pod to the USB port on the host PC.
3. Launch RapidFET JTAG by selecting Target > Connect.

Figure 2: RapidFET JTAG Connect



The following error message may appear at this time. This is not an indication that the target board is faulty. The problem is most likely the result of how Windows handles the USB to JTAG/I2C converter device drivers.

Figure 3: No Pod Found

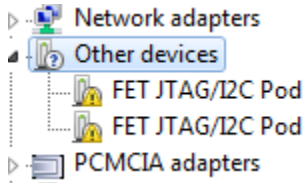


If the pod is connected but not found, check the following:

1. Another RapidFET JTAG window is already active. There can be only one application window per pod.
2. Windows seems to remember which location the USB cable for pod was connected the first time. It appears that the drivers will work only when the pod is connected in that specific location. Close RapidFET JTAG, re-connect the pod in the USB port where it was originally connected, and then re-launch RapidFET JTAG.
3. Check if the USB drivers are functional.
   a. In Windows, open Control Panel > System > Device Manager > Universal Serial Bus controllers.
   b. In the list of devices, check for the FET JTAG/I2C Pod Designation with an exclamation mark in “Other Devices,” as displayed in Figure 4.

   This indicates Windows is unable to load the drivers. If this is the case, download the D2XX drivers for your operating system from ftdichip.com and manually update the FET JTAG/I2C Pod driver with this download.

Figure 4: RapidFET JTAG Pod Driver Problems

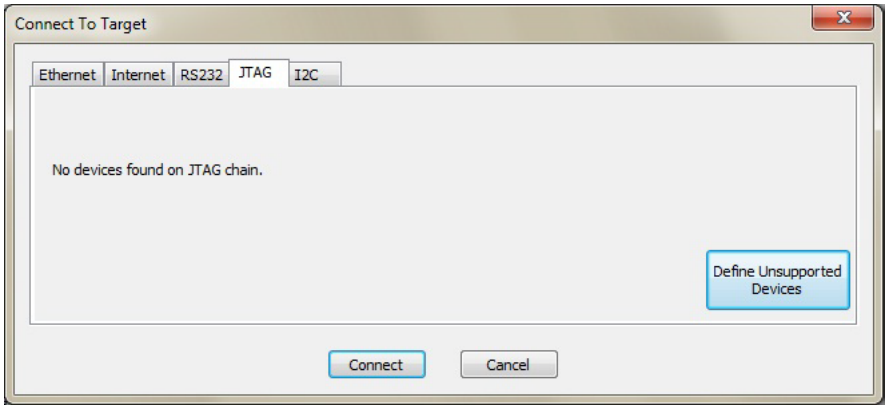


Connecting via JTAG

No device found on JTAG chain indicates there is a problem with the device, or the JTAG connection (see Figure 5). When this problem arises, check the following:

- The JTAG TRST pin on the S-RIO switch must not be connected directly to ground. The RapidFET JTAG Pod drives this pin high.
- The S-RIO switch must not be held in reset
- The RapidFET JTAG pod contains a signature recognized by software. A pod with a different signature will not work with RapidFET JTAG.

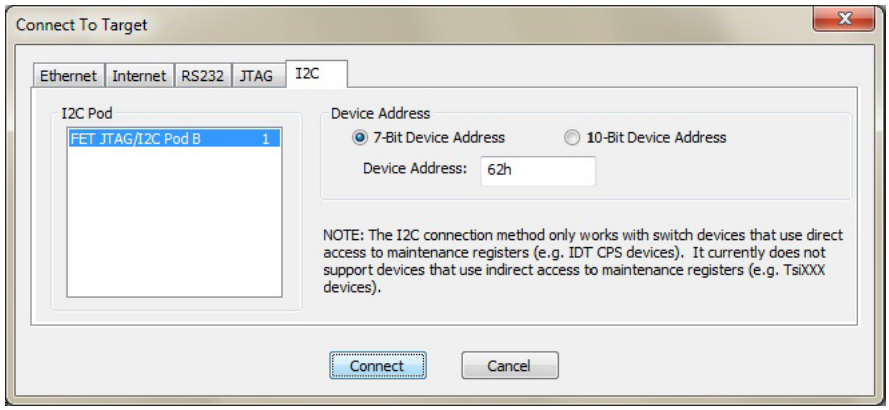
Figure 5: No Device Found



Connecting via I2C

- Ensure the FET JTAG/I2C Pod B appears in the I2C Pod window.
- Select the Device Address as it is configured on the AD[9:0] pins of the S-RIO switch.

Figure 6: I2C



If RapidFET JTAG cannot properly recognize the S-RIO switch, check the following:

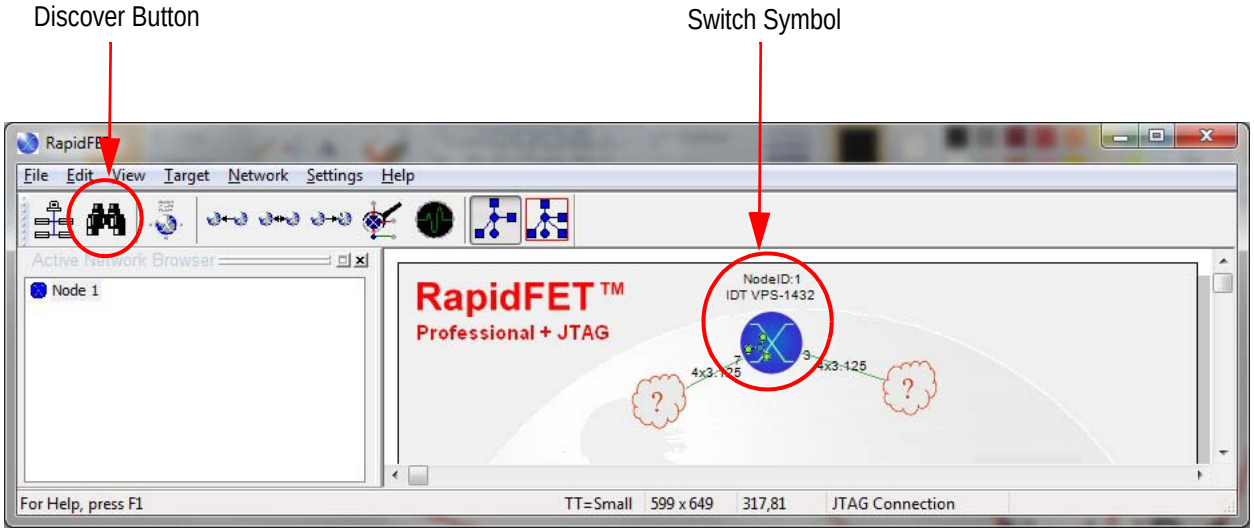
- Are there pull-ups on the I2C bus?
- Is there another master on the I2C bus driving concurrently?
- Is there more than one device with the same address on the bus?
- Is Address 0 configured on AD[9:0] (Address 0 is not a valid address)?

Checking the S-RIO Links

Once RapidFET JTAG establishes a connection to the S-RIO switch, a switch symbol and link status appears in the network map window (see Figure 7). The active links appear green and the endpoints (or other switches) appear as clouds. To remove unused links from the view, select View from the pull-down menu and click Hide Nulls.

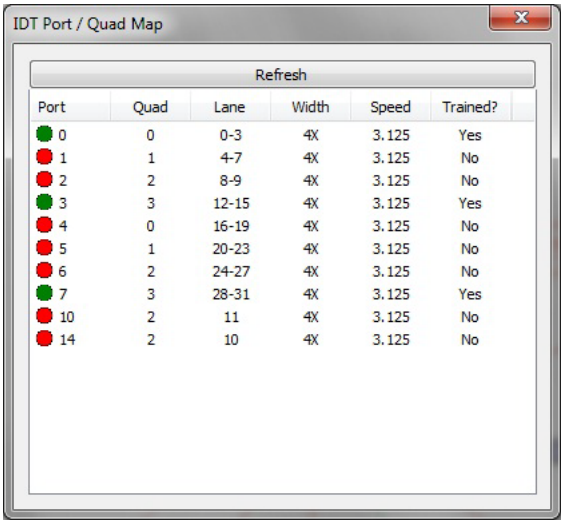
The Link status in the map window does not refresh until the discover button at the top left of the application is clicked. Adding or removing connections will not appear in the network map window unless the widow is refreshed.

Figure 7: RapidFET Menu



To display a concise link status window, right-click on the switch symbol in the map window and select Port/Quad Map (see Figure 8). To refresh the link status window, click on the large button on top of the window.

Figure 8: Port/Quad Map Window



Port	Quad	Lane	Width	Speed	Trained?
0	0	0-3	4X	3.125	Yes
1	1	4-7	4X	3.125	No
2	2	8-9	4X	3.125	No
3	3	12-15	4X	3.125	Yes
4	0	16-19	4X	3.125	No
5	1	20-23	4X	3.125	No
6	2	24-27	4X	3.125	No
7	3	28-31	4X	3.125	Yes
10	2	11	4X	3.125	No
14	2	10	4X	3.125	No

If one or more links are expected to be trained but do not show as trained in the status window, then check the following parameters.

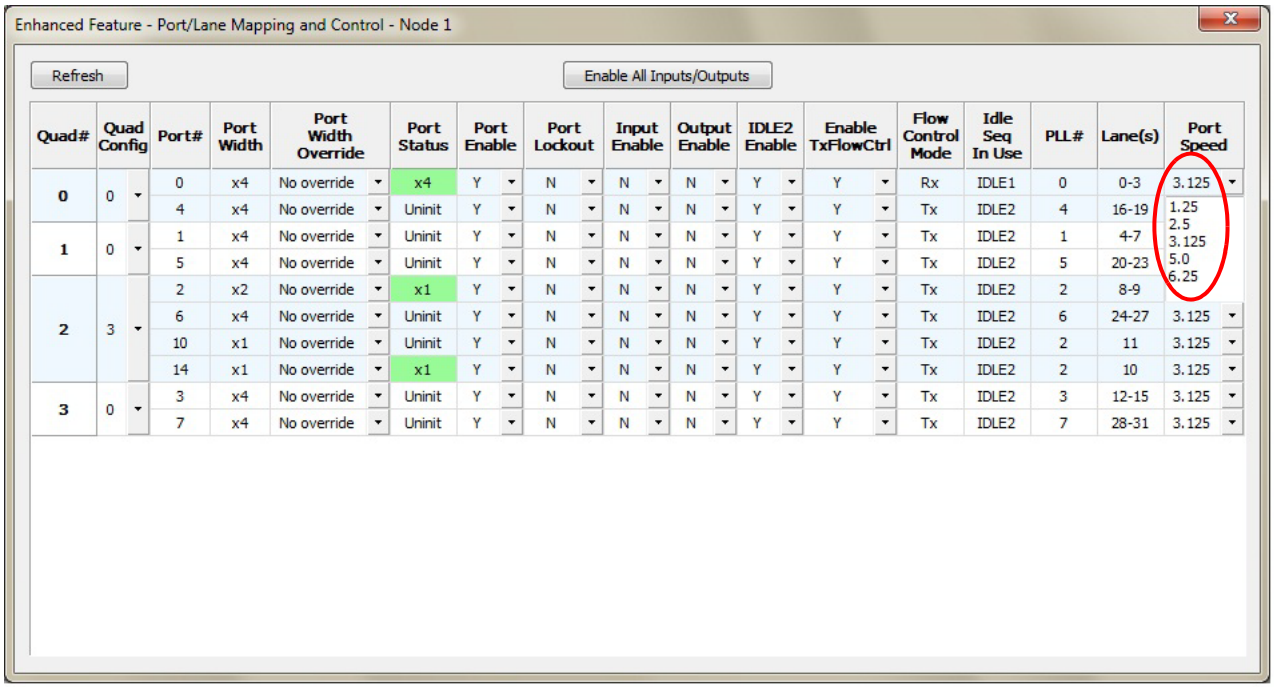
Link Speed

The speed (baud rate) of the link between the switch and the endpoint must be set to the same rate. RapidIO endpoints do not auto-negotiate link speed. Link speed must be set manually on both ends of the link. Link speed on the switch can be set globally with SPD[2:0] pins on the device, or on a port basis through register programming.

- Changing port link speed:

  When using RapidFET JTAG *Enhanced*, a link speed dialog can be brought up: right-click on the switch symbol in the map window and select Port/Lane Mapping and Control (see Figure 9). Change the Port speed from the column on the right.

Figure 9: Port/Lane Mapping and Control (Enhanced Version Only)



When using RapidFET JTAG *Standard*, the port speed must be changed through registers. The procedure for changing the port speed is described in the relevant Gen2 Switch User Manual. The following is an example using the registers editor feature of RapidFET JTAG.

Example – Changing the Link Speed on Port 0

1. Expand the register tree as in Figure 10.
2. In Port Specific LP-Serial Extended Features Register, select the port for which the speed is going to be modified.
3. Select the Port_n_CTL_1 register and set PORT_DIS (bit 8) to 1. (Figure 10, Register Editor)
4. Select the LANE_n _CTL register in Lane Specific - Lane Control Registers and change the lane speed to the desired value in the TX_RATE and RX_RATE fields for each lane of the port (see Figure 11).
5. Set the bit corresponding to the port affected by the speed change in the PORT_SEL field of the Device Reset Control Register, 0xF20300 (see Figure 12). Set DO_RESET in the same register to 1.
6. Re-enable the port in the LP-Serial Extended Features Register by setting PORT_DIS (bit 8) in the Port_n_CTL_1 register to 0.
7. Refresh the Port/Quad Map window to confirm that the port speed has changed (see Figure 8).

Figure 10: Register Editor – Disable Port

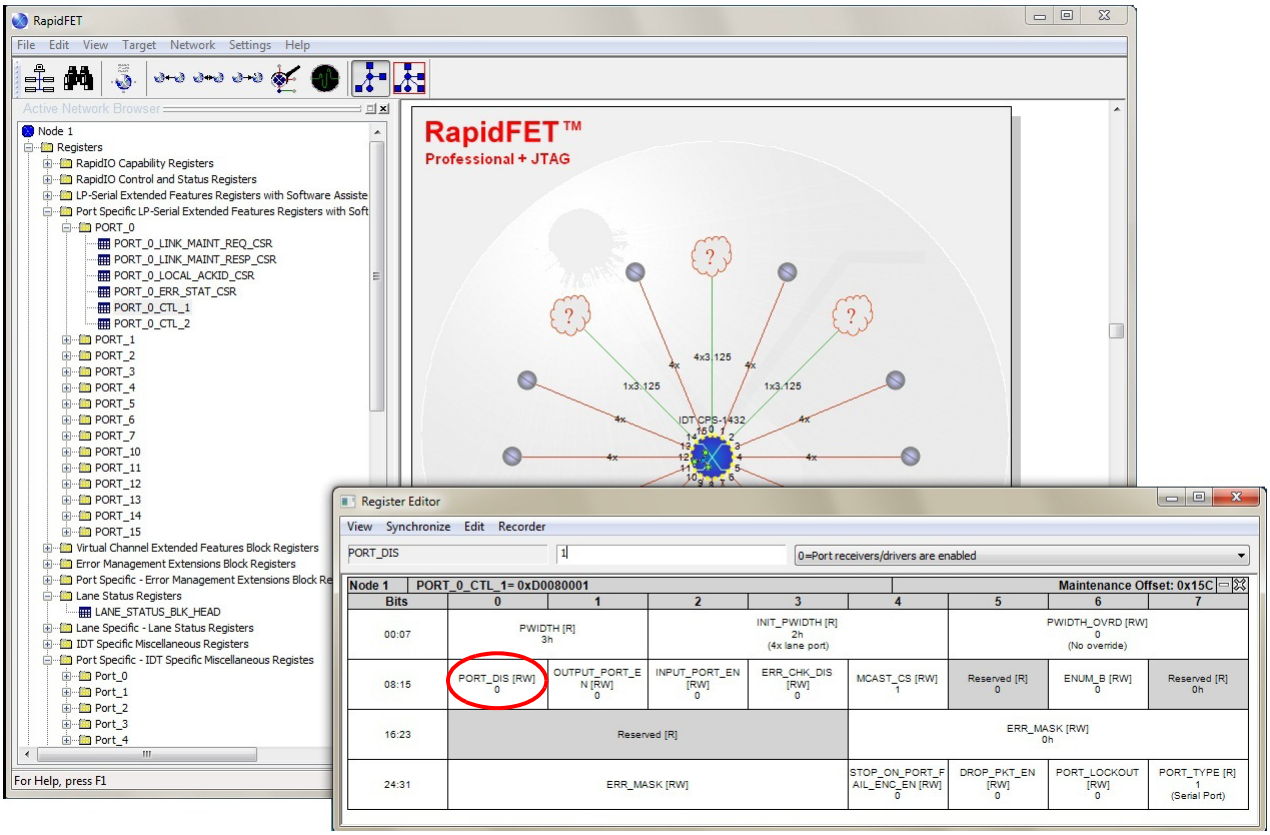


Figure 11: LANE_n_CTL Register

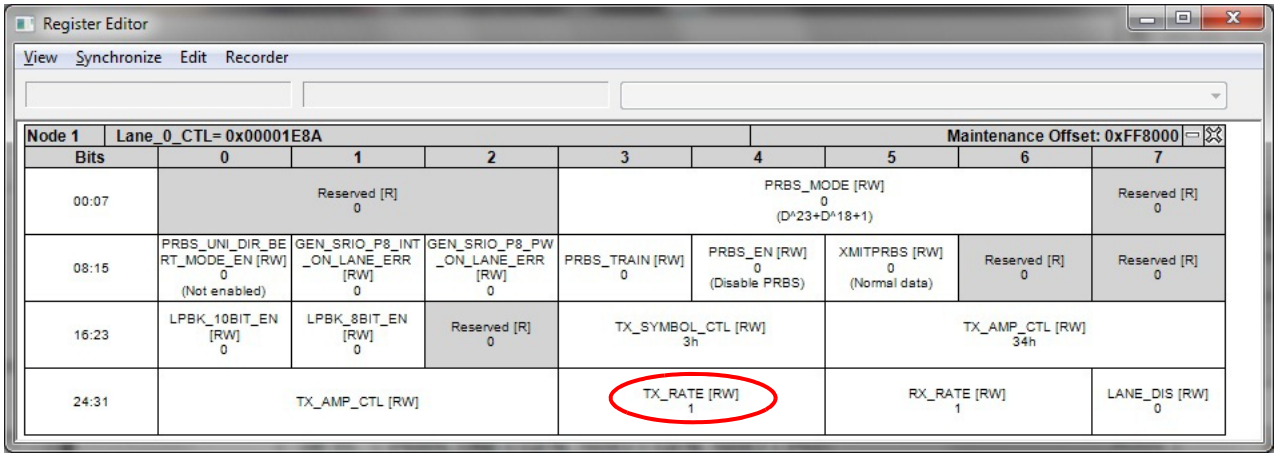
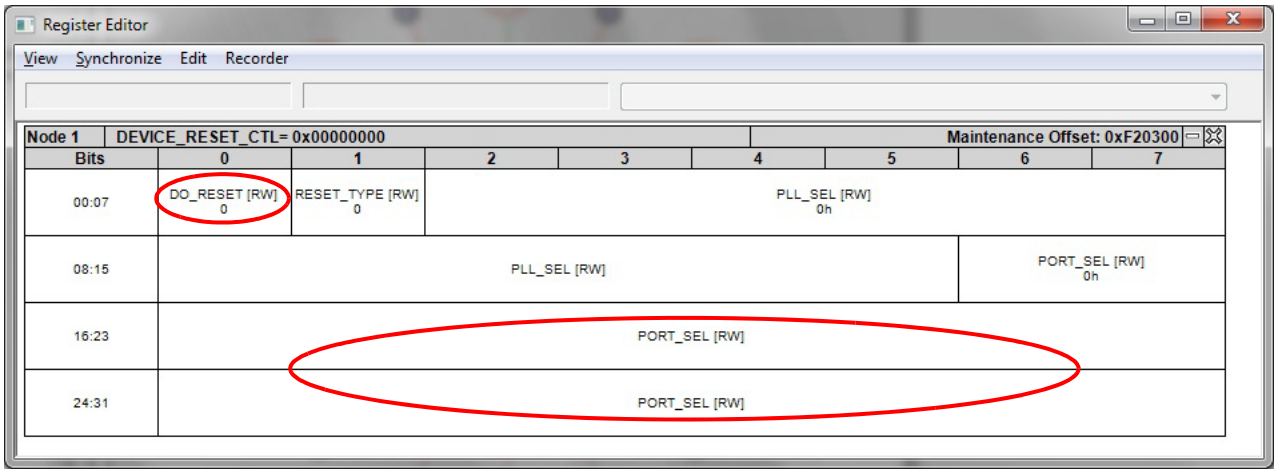


Figure 12: DEVICE_RESET_CTL Register



Lane Reversal

S-RIO switches only support lane reversal with Gen2 devices that support the IDLE2 control sequence. Connections with reversed lanes to other non S-RIO Gen2 switches will most likely not function.

If your system has reversed lane connections, the ports may not be operational. If this is the case, the only option is to configure one endpoint (if possible) in 1x mode and continue to use the other endpoint configured in 4x mode, but force it to operate in 1x mode.

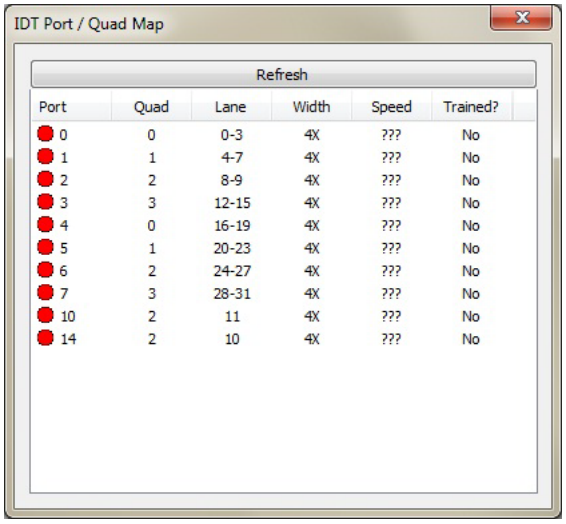
Lane Reversal in 4x Ports (Not supported without IDLE2)	Lane Reversal Patch, 4x to 1x
Lane A – Lane D	Lane A – Lane D (1x)
Lane B – Lane C	Lane B – Powered down
Lane C – Lane B	Lane C – Powered down
Lane D – Lane A	Lane D – Powered down

S-RIO switches can be forced to downgrade the link to 1x mode (only one lane is active; other three lanes are not used) by setting the Port Width override field (PWIDTH_OVRD) in the PORT_{0..17}_CTL_1_CSR register to 0b010 (single-lane port).

Illegal Port Speed Configuration

Strapping pins, SPD[2:0], set the initial link speed at power up. For example, SPD[2:0] = 1,0,0 will result in non-functional links between the switch and its endpoints. In RapidFET JTAG these will appear as "???" in the Speed column, as displayed in Figure 13.

Figure 13: Illegal Port Speed



Illegal Port Width Configuration

Strapping pins, CFG[7:0], set the initial port width at power up. There are port width configurations on CFG[1:0] and CFG[3:2] that are undefined. If these configuration are inadvertently set up, the port will not achieve Port OK status, and will appear as 4x in the width column in the Port/Quad Map window.

Signal Integrity Issues

Signal integrity issues can prevent S-RIO links from achieving Port OK status, or loose Port OK status due to bit errors. RapidFET JTAG can help troubleshoot signal integrity issues and make SerDes adjustments to help compensate for poor signal integrity.

Signal integrity issues are common in large systems where the S-RIO links are subjected to long traces on FR4 based PCBs, and transitions through one or several pairs of connectors. In these conditions, the default SerDes configuration may not be adequate to achieve a stable S-RIO link. RapidFET JTAG Enhanced provides utilities to test the links and adjust SerDes.

Reduce Link Speed

The first step in troubleshooting signal integrity issues is to verify that the links work at lower-than-desired speeds. Therefore, set the link speed as low as the switch and endpoint will support. Link speed setting is described in Figure 9.

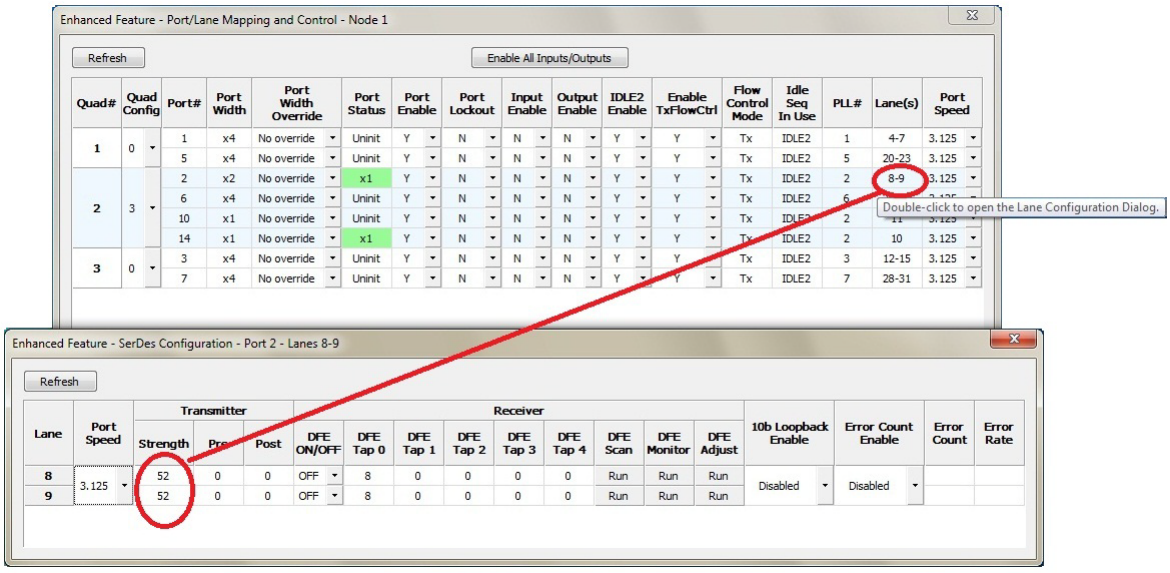
If the links still do not achieve Port OK status at baud rates lower than 3.125 Gbps, the problem is probably not due to signal integrity. It is more likely a connectivity issue as described in previous sections.

If the links are trained and Port OK status is achieved at lower-than-desired baud rates, then adjustments to the SerDes drive strength and pre/post emphasis parameters may make the links work at higher speeds. To adjust SerDes parameters, follow the steps below in the order given.

Increase Tx Amplitude

1. Bring up the Port/Lane Mapping and Control Dialog as described for Figure 9.
2. Double-click on the lane to be adjusted in the lane column.
3. In the SerDes Configuration Window, set the strength to the maximum value (63) for all lanes in the port.
4. Go back to the Port/Lane Mapping and Control window and click on Refresh.
5. The port may now be trained. If not, the other endpoint may not be driving the SerDes with enough amplitude. If the Other endpoint is also a S-RIO Gen2 switch, move RapidFET JTAG to the other endpoint and increase the SerDes drive strength.

Figure 14: SerDes Configuration Dialog



Increase Post-emphasis Setting

The transmitter field labeled “Post” in the SerDes Configuration window programs the post-emphasis parameter of the SerDes (see Figure 14). Post-emphasis is a feature of the SerDes analog circuit that modifies the electrical waveform of the bit stream based on the content of the bitstream itself. Post-emphasis is most effective when the physical link between the switch and the endpoint is long and uniform.

Ensure that Strength is high (52 or greater). Increase the Post value gradually from 0 to 63. Refresh at each increment. Verify if the link achieves Port OK. Note that if the other endpoint is also a S-RIO Gen2 switch, the other end of the link should also be set with the same parameters.

Increase Pre-emphasis Setting

The transmitter field labeled “Pre” in SerDes Configuration window programs the pre-emphasis parameter of the SerDes (see Figure 14). Pre-emphasis has a similar effect as post-emphasis, but is less effective. This field varies from 0 to 31. As a last resort, when the Strength and Post are set to their maximum value but the links still do not achieve Port OK, set Pre to 31.

DFE (Receiver Decision Feedback Equalization)

When the SerDes of the endpoint connected to the switch cannot compensate for signal quality loss through the PCB and connectors, the switch SerDes' receiver can compensate for some of the signal loss. This feature can be enabled and adjusted in the SerDes Configuration window (see Figure 14). For more information on DFE configuration, see the *S-RIO Gen2 Switch Signal Quality Optimization Application Note*.

Error Status

The following sections describe how to check for errors with RapidFET JTAG. S-RIO switches have several error status registers that can be accessed through the register editor. The following sections discuss a subset of the error status registers that can help identify the cause of malfunctions. For more information on error report and management, see the relevant Gen2 Switch User Manual.

When Port OK is Not Achieved

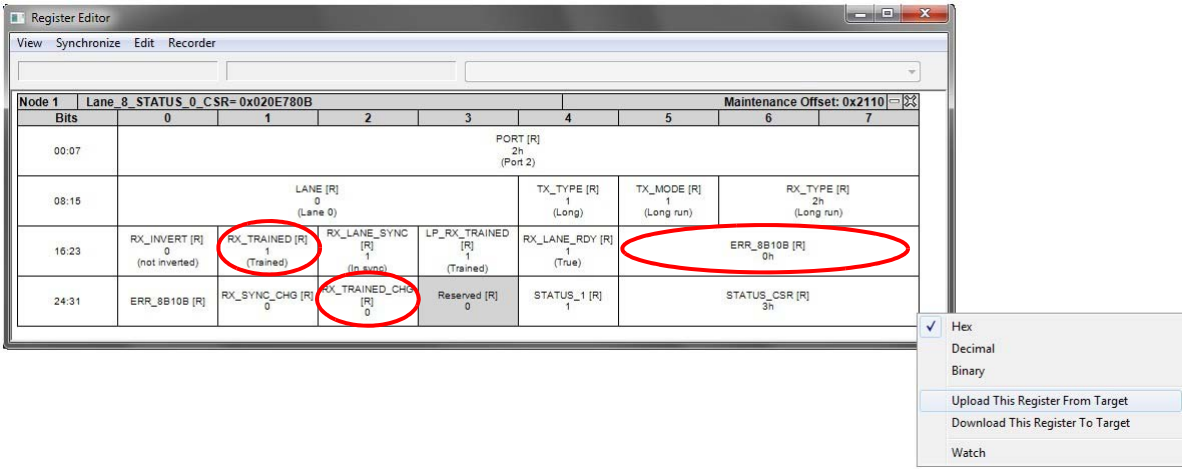
Errors are expected when two endpoints become active upon power up. Power-up errors should be ignored and cleared, while subsequent errors should be analyzed.

If a port is composed of several lanes (either 2x or 4x lanes), all lanes must be properly trained with its endpoint before Port OK status is achieved. If one or several lanes are not training properly, the port may not achieve Port OK status, or may train with a less-than-expected number of lanes.

If Port OK status is not detected, the LANE_{0..47}_STATUS_0_CSR [Register Offset: 0x002010 + (0x20 * lane_num)] can help identify which lane is at fault:

1. In the RapidFET JTAG Register tree, select Lane Specific - Lane Status Registers.
2. Select the lanes specific to the port under observation.
3. In the Register Editor Window, right-click and select Upload This Register From Target. This will clear all status bits.
4. Check the status bits for RX_TRAINED and RX_TRAINED_CHG. These bits indicate if the lane is trained with the endpoint and whether the trained status is changing.
5. Check the ERR_8B10B field, and upload the register several times to see if the error count is increasing (or bring up a RapidFET JTAG Watch window). 8B10B errors indicate that the link is not connected, or the link has very poor signal quality. 8B10B errors may also indicate that the two endpoints have a baud rate mismatch, either from mismatching baud rate, or from reference clock frequency mismatch.

Figure 15: Lane_n_STATUS_0_CSR Register



6. Check whether the PORT_DIS bit is set in the Port_n_CTL_1 register (see Figure 16). If set, the port cannot receive and transmit any packets or control symbols.

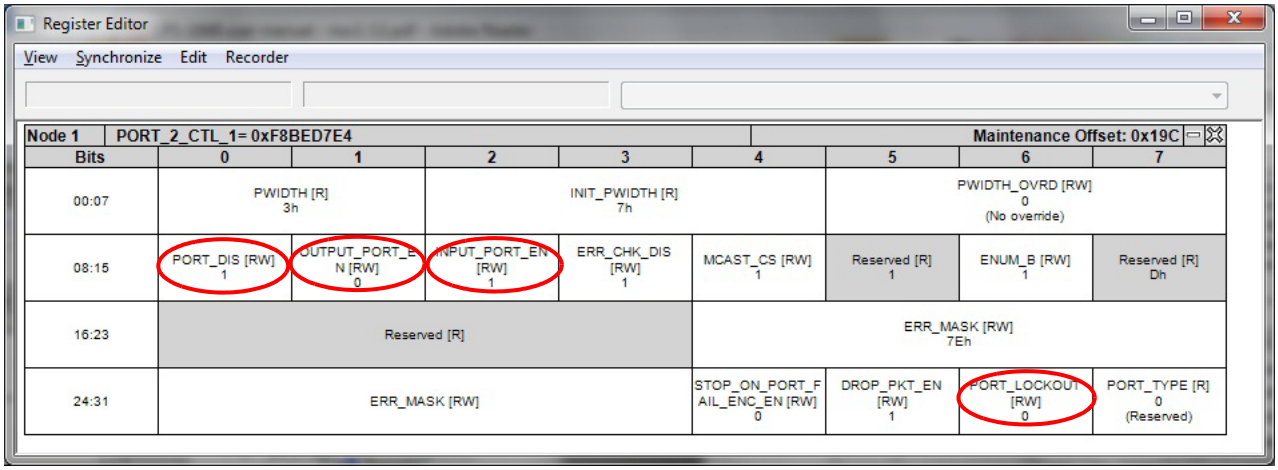
When Port OK is Achieved

Port OK status is an indication that two S-RIO endpoints can exchange control characters. Port OK status, however, does not guarantee that the link is stable and error free. Even if Port OK status is set, it may not be possible to exchange maintenance and data packets on the link because of setup or error conditions.

If Port OK status is achieved, the Port_n_CTL_1 Register can help identify the reasons for the setup or error conditions (see Figure 16):

- Check the PORT_LOCKOUT bit in the Port_n_CTL_1 register. If PORT_LOCKOUT is set the port is stopped and it cannot issue or receive any packets.
- OUTPUT_PORT_EN and INPUT_PORT_EN in the Port_n_CTL_1 register must be set to enable receiving and transmitting data packets.

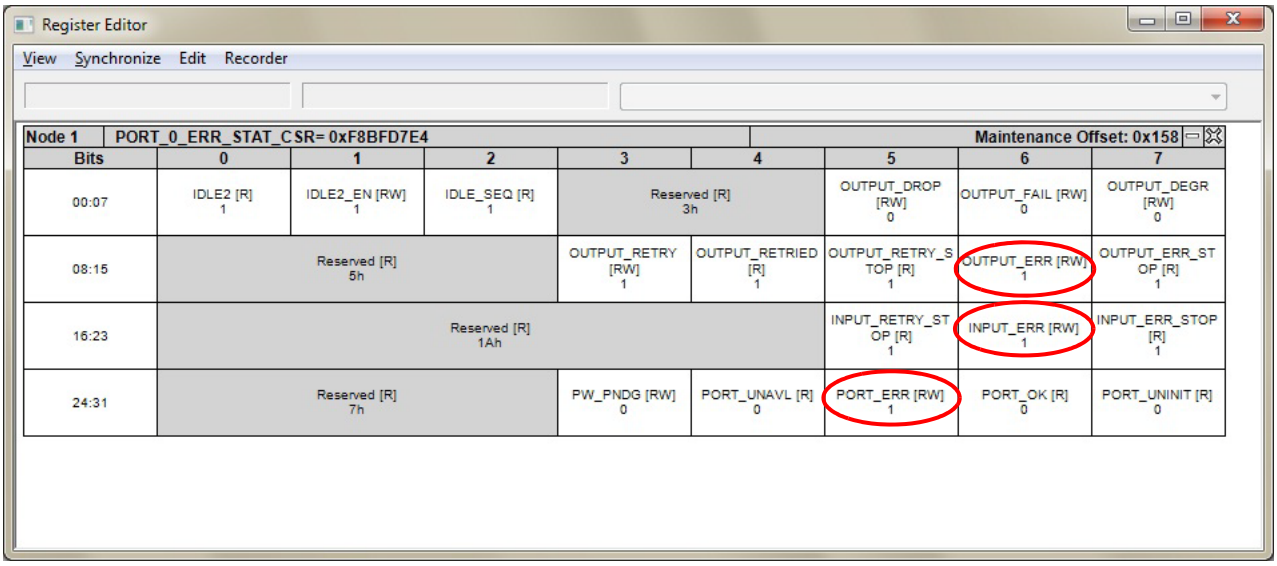
Figure 16: Port_n_CTL_1 Register



The Port_n_ERR_STAT_CSR register, which is located in the Port Specific LP-Serial Extended Features Registers with Software Assisted Error Recovery register group, contains important error status bits (see Figure 17):

- Check OUTPUT_ERR and INPUT_ERR. These bits must be cleared (write 1 to clear). If either bit is set to 1 it does not indicate that the port has stopped transmitting and receiving packets. However if the bits are set immediately after clearing, this is an indication that the port is processing repeated errors.
- If the PORT_ERR bit is set then the port will drop all packets, including maintenance packet responses. For information on how to clear PORT_ERR, see the relevant Gen2 Switch User Manual.

Figure 17: Port_n_ERR_STAT_CSR Register



The Port_n_ERR_DET register (see Figure 18), which is located in the Port Specific - Error Management Extensions Block Registers register group and the Port_n_IMPL_SPEC_ERR_DET register (see Figure 19), which is located in the Port Function Registers register group, can be used to pinpoint reasons for errors flagged in the PORT_n_ERR_STAT_CSR register (see Figure 17). Descriptions of the error bits associated with these registers are located in the relevant Gen2 Switch User Manual. These errors are port specific, not lane or link specific.

Figure 18: Port_n_ERR_DET Register

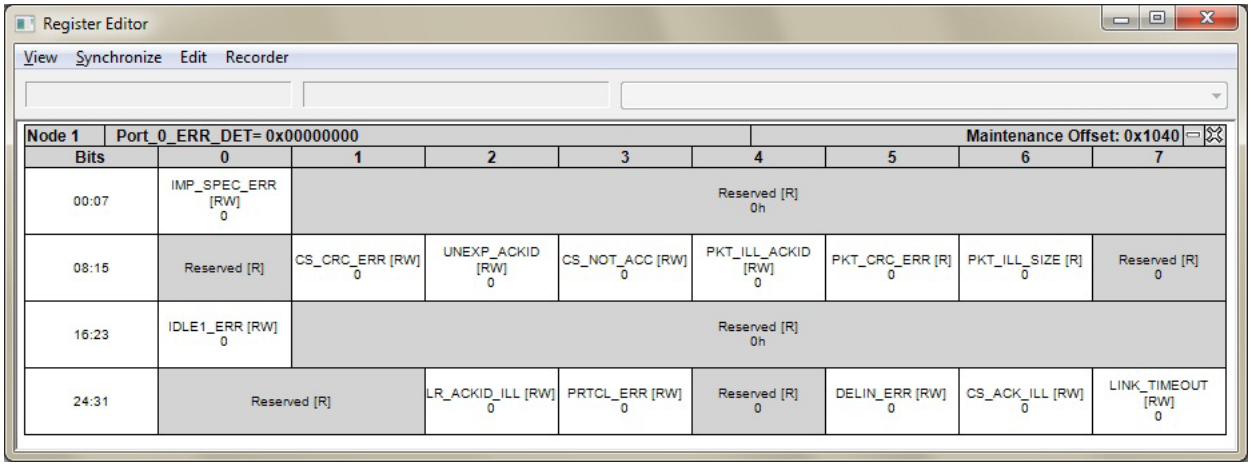
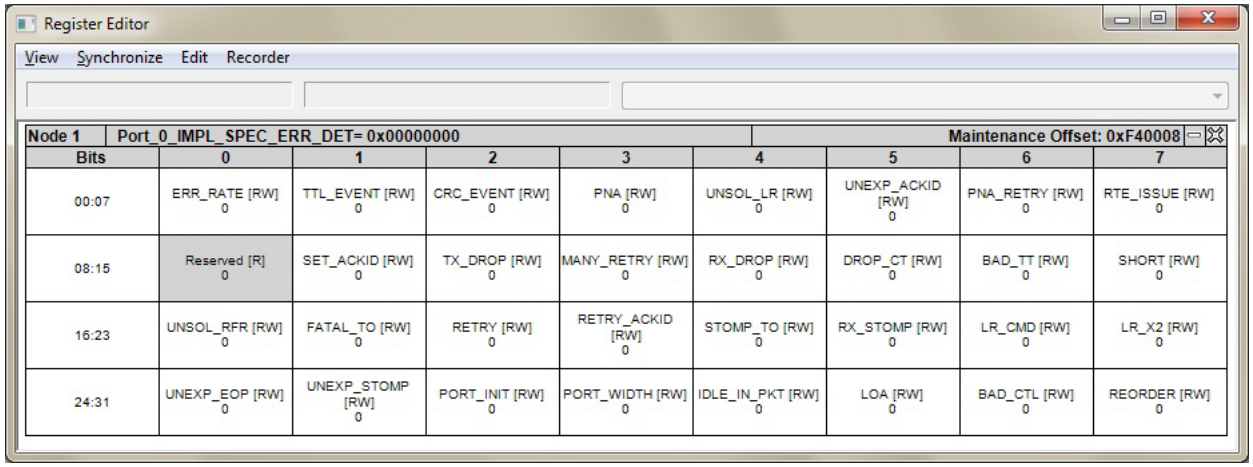


Figure 19: Port_n_IMPL_SPEC_ERR_DET Register

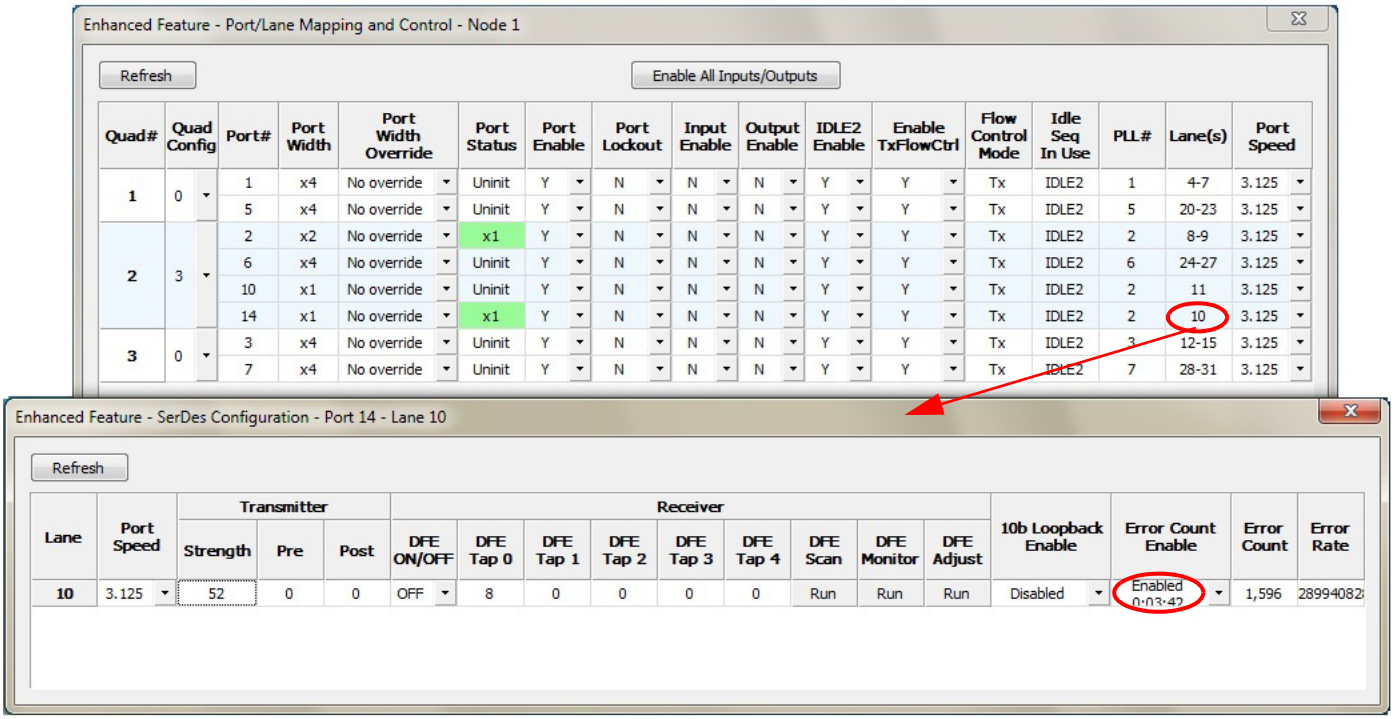


Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE [RW] 0	TTL_EVENT [RW] 0	CRC_EVENT [RW] 0	PNA [RW] 0	UNSOL_LR [RW] 0	UNEXP_ACKID [RW] 0	PNA_RETRY [RW] 0	RTE_ISSUE [RW] 0
08:15	Reserved [R] 0	SET_ACKID [RW] 0	TX_DROP [RW] 0	MANY_RETRY [RW] 0	RX_DROP [RW] 0	DROP_CT [RW] 0	BAD_TT [RW] 0	SHORT [RW] 0
16:23	UNSOL_RFR [RW] 0	FATAL_TO [RW] 0	RETRY [RW] 0	RETRY_ACKID [RW] 0	STOMP_TO [RW] 0	RX_STOMP [RW] 0	LR_CMD [RW] 0	LR_X2 [RW] 0
24:31	UNEXP_EOP [RW] 0	UNEXP_STOMP [RW] 0	PORT_INIT [RW] 0	PORT_WIDTH [RW] 0	IDLE_IN_PKT [RW] 0	LOA [RW] 0	BAD_CTL [RW] 0	REORDER [RW] 0

Error Counters (Enhanced Version Only)

RapidFET JTAG Enhanced implements a bit error rate counter as part of the Port/Lane Mapping and Control Dialog. To bring up the SerDes Configuration Window, double click on the Lane(s) Field. In the Error Count Enable field, click on Enable (see Figure 20). 8B10B errors are counted.

Figure 20: Error Counter



Quad#	Quad Config	Port#	Port Width	Port Width Override	Port Status	Port Enable	Port Lockout	Input Enable	Output Enable	IDLE2 Enable	Enable TxFlowCtrl	Flow Control Mode	Idle Seq In Use	PLL#	Lane(s)	Port Speed
1	0	1	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	1	4-7	3.125
		5	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	5	20-23	3.125
2	3	2	x2	No override	x1	Y	N	N	N	Y	Y	Tx	IDLE2	2	8-9	3.125
		6	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	6	24-27	3.125
		10	x1	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	2	11	3.125
		14	x1	No override	x1	Y	N	N	N	Y	Y	Tx	IDLE2	2	10	3.125
3	0	3	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	3	12-15	3.125
		7	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	7	28-31	3.125

Lane	Port Speed	Transmitter			Receiver									10b Loopback Enable	Error Count Enable	Error Count	Error Rate
		Strength	Pre	Post	DFE ON/OFF	DFE Tap 0	DFE Tap 1	DFE Tap 2	DFE Tap 3	DFE Tap 4	DFE Scan	DFE Monitor	DFE Adjust				
10	3.125	52	0	0	OFF	8	0	0	0	0	Run	Run	Run	Disabled	Enabled	1,596	28994082

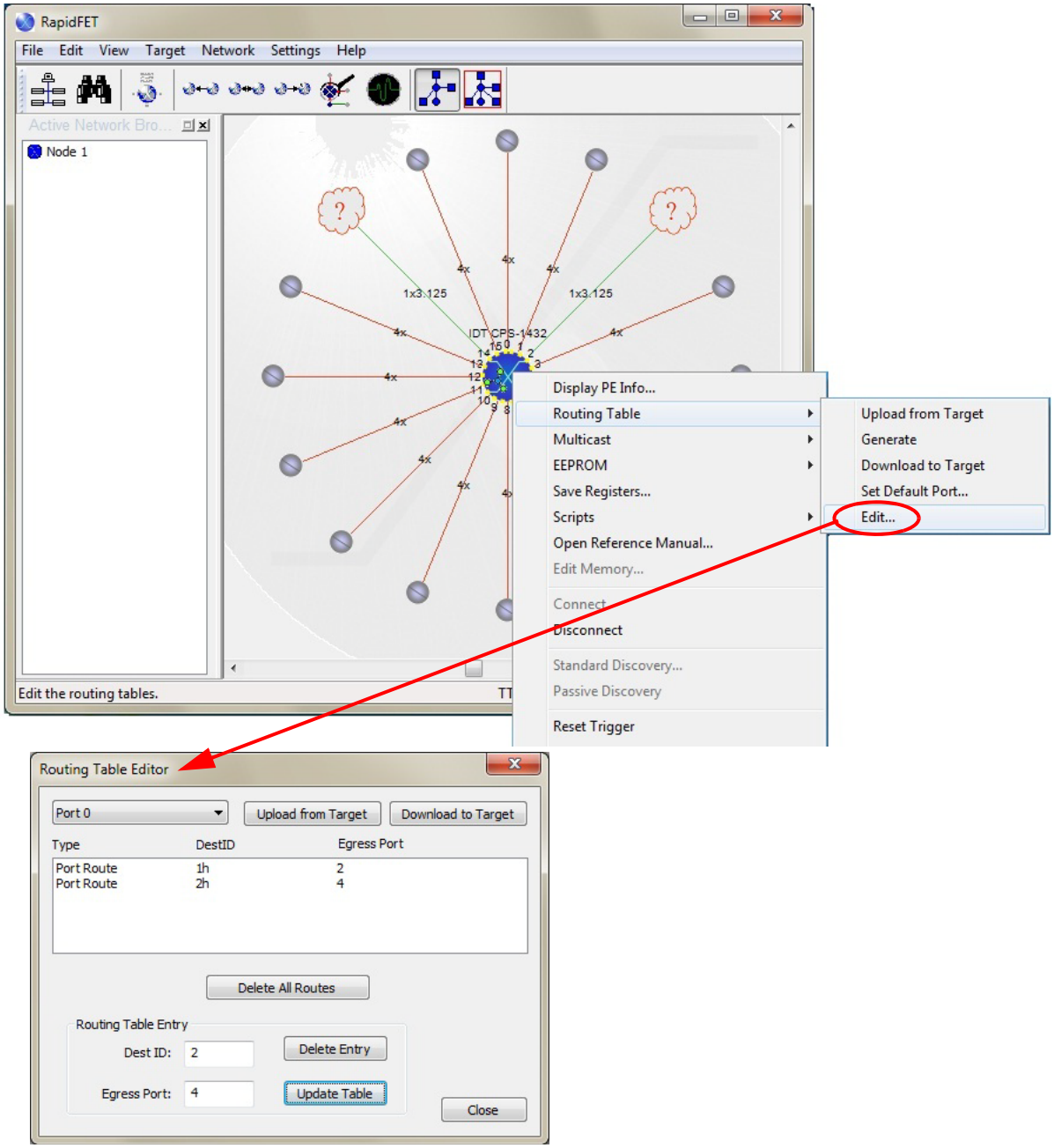
Datapath Testing

RapidFET JTAG allows datapath testing with GUIs for packet generation and routing table creation. S-RIO switches also have packet counters that can monitor traffic through the device. The following examples show how to use the Routing Table and Packet Counter dialogs.The packet generator editor is beyond the scope of this document. For instructions on how to use the packet generator, refer to the RapidFET Help Menu and the relevant Gen2 Switch User Manual.

Routing Table Editor

The routing table editor can be used to edit routing tables or to verify if programming was done properly. In the switch map view, right-click on the device and select Routing Table > Edit (see Figure 21). In the Routing Table editor, select the ingress port to be edited and click on Upload from Target. Verify that the entries listed are as expected.

Figure 21: Routing Table Menu



Packet Counters

S-RIO switches have Rx and Tx packets counters. The counters can be monitored in a watch window and used to verify traffic through the switch. The steps to enable counter are described below.

1. Verify and set the Input and Output Enable bits in the Port_n_CTL_1 register (see Figure 16). This can also be done in the Port/Lane Mapping and Control Dialog in RapidFET JTAG Enhanced.
2. In the Port Function Register, set the CNTRS_EN bit to 1 (Figure 22).
3. From the Port Function Registers, add Portn_VC0_PTK_TX_CNTR and Portn_VC0_PTK_RX_CNTR to a Watch window (see Figure 23).
4. In the Watch window, enable the watch function.

Figure 22: Counters Enable Bit

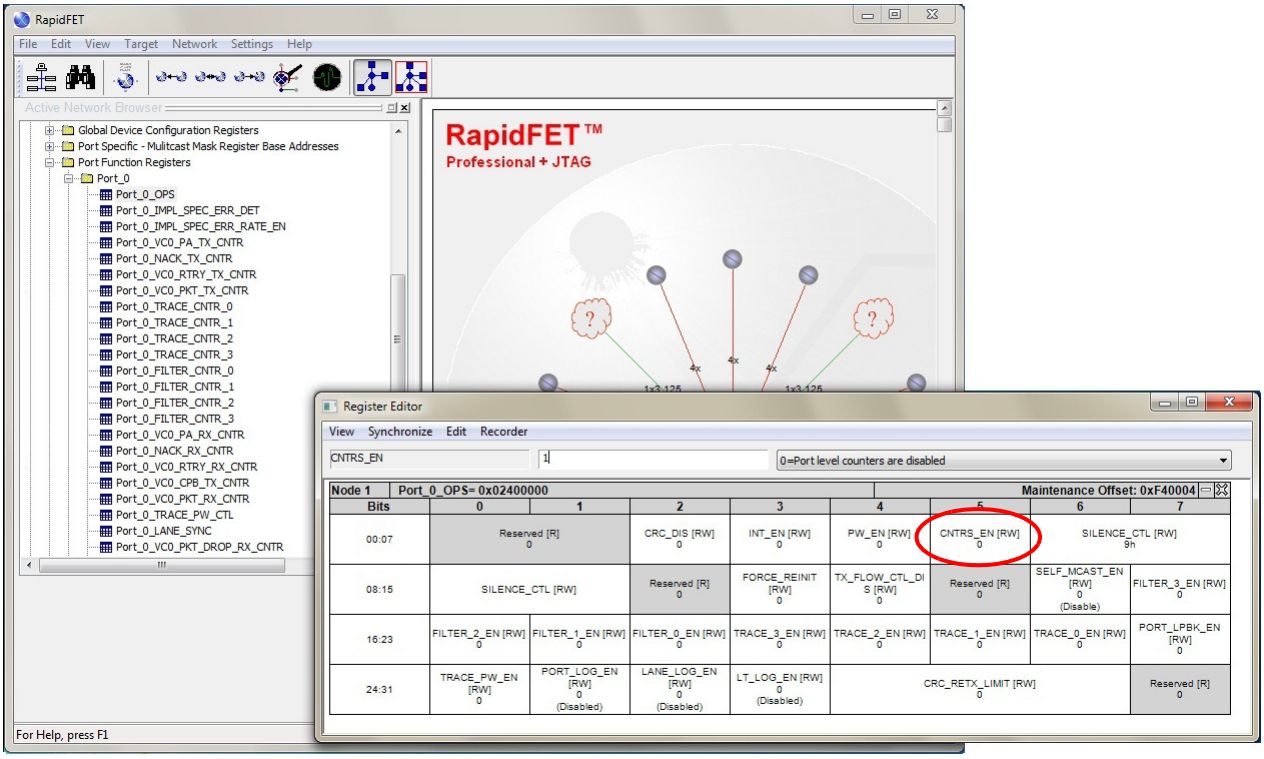


Figure 23: Watch Window

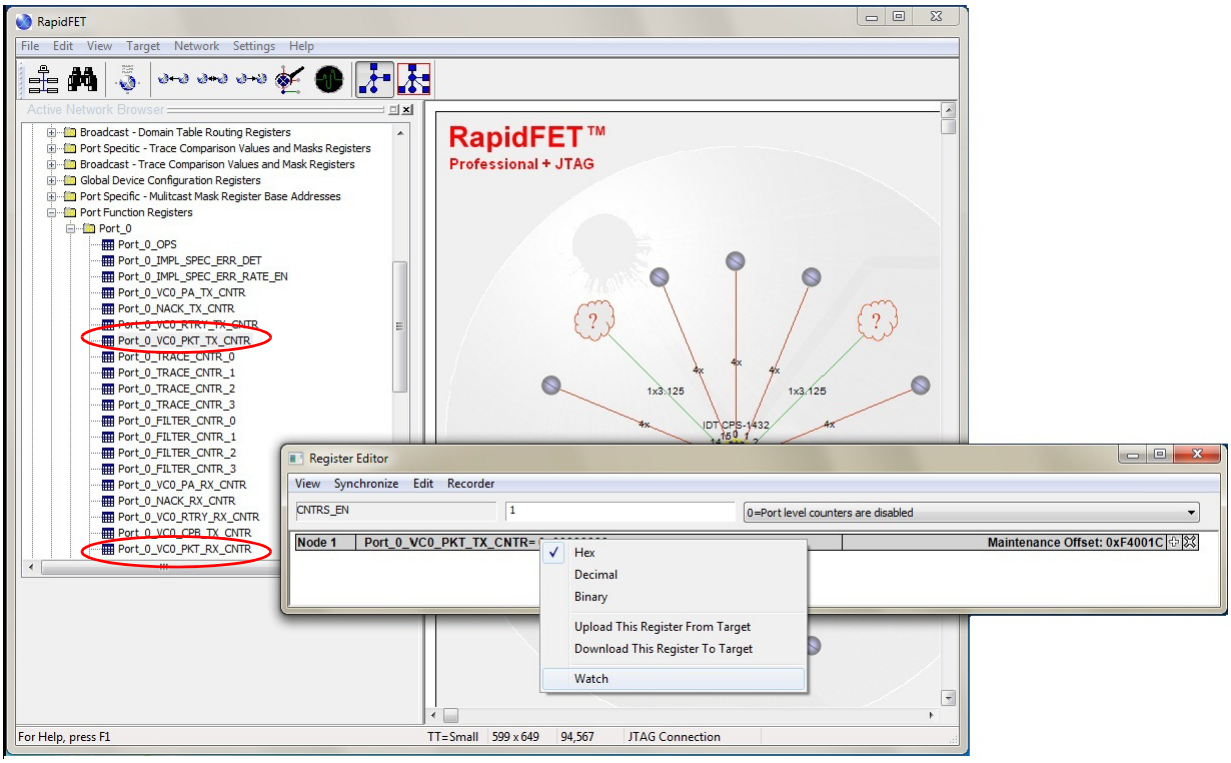
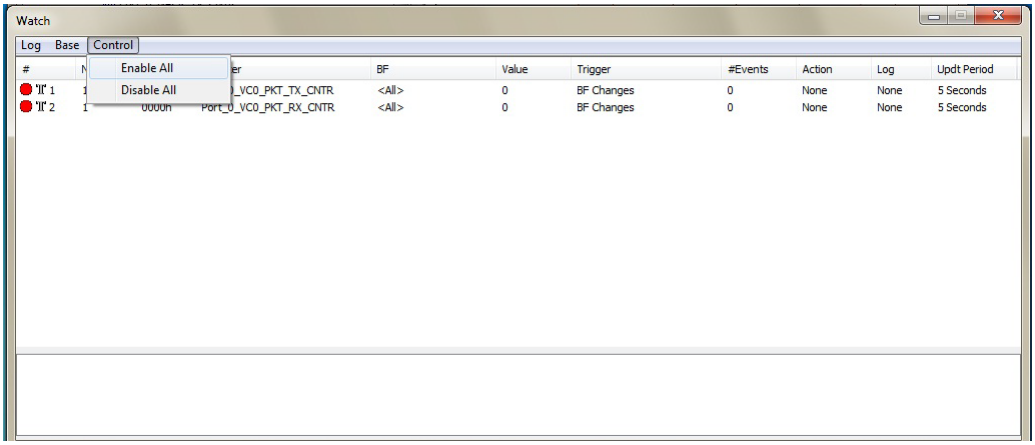


Figure 24: Enable Counters



Performance Monitor (Enhanced Version Only)

RapidFET JTAG provides a graphical view of Port Function Registers data through the Performance Monitor function. To enable performance monitors, right-click on the switch symbol in the network map window then select Performance Monitor.

In the dialog view, select the port to monitor, and in the pull-down menu select the parameter to watch. Click on Enable to start the graphic trace.

Figure 25: Performance Monitor (Enhanced Version Only)

Loading Serial EEPROMs

The RapidFET JTAG pod can be used to program serial EEPROMs on the I2C bus. Note that the pod has a separate I2C header to be connected to the board's I2C bus. For pinout information, see Table 2.

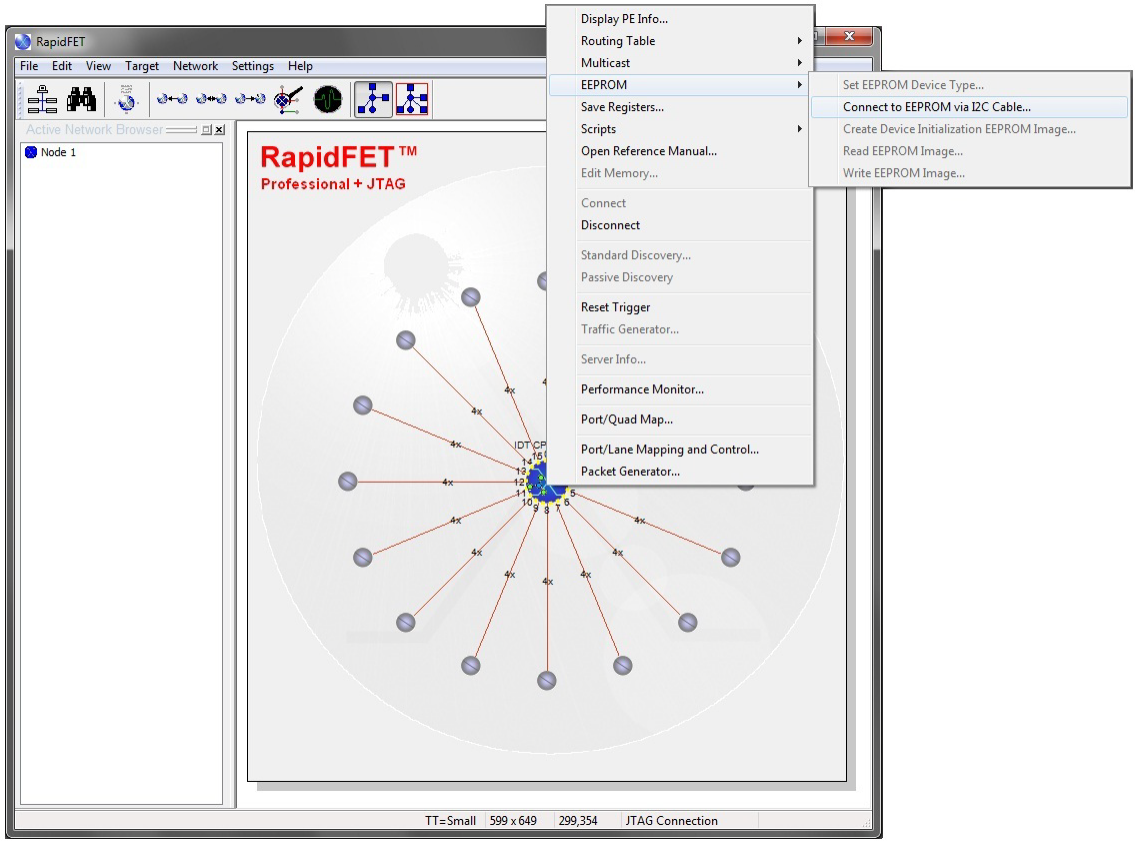
RapidFET JTAG needs a binary file to write content to the serial EEPROM. This file can be generated manually with a third-party binary file editor, created with IDT's script2bin utility, or created with the RapidFET EEPROM Image utility.

Downloading a Binary File

To program a serial EEPROM, follow these steps:

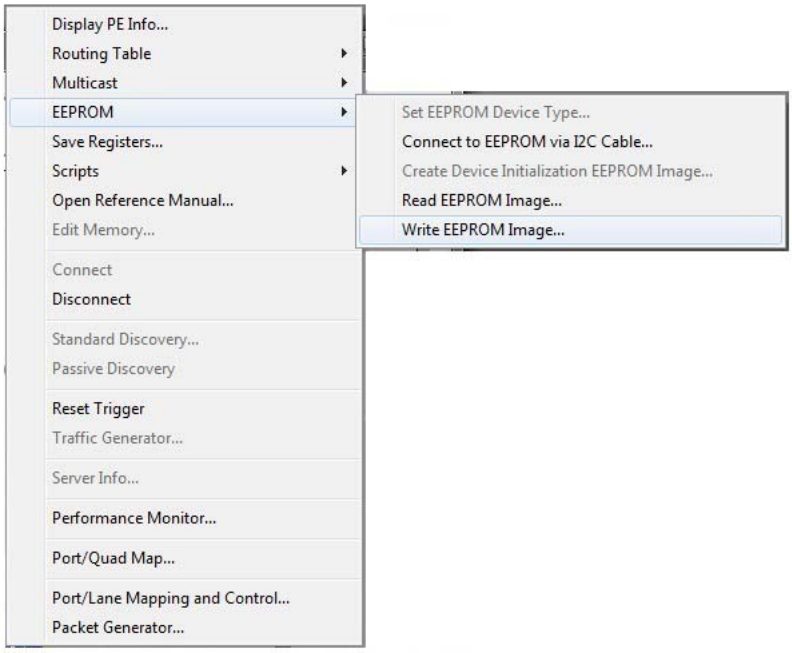
1. Right-click on the device in the network map window, select EEPROM > Connect to EEPROM via I2C Cable (see Figure 26).
2. Select the Serial EEPROM in the device list.
3. Select the I2C address of the EEPROM attached to the S-RIO switch, and then click Connect.

Figure 26: EEPROM Menu



4. Click again on the device in the network map window, and then re-select EEPROM > Write EEPROM Image (see Figure 27).
5. Select the .bin file to program and click Open. The file gets downloaded to the serial EEPROM.

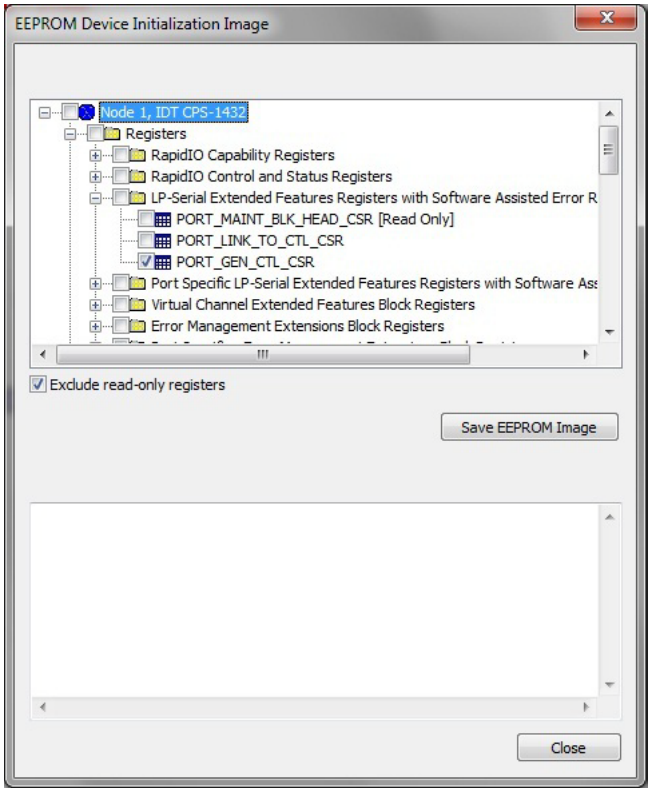
Figure 27: EEPROM Write Command



RapidFET JTAG can also directly create a serial EEPROM file using the device's current register content. To do so, complete the following:

1. In the EEPROM menu, select Create Device Initialization EEPROM Image.
2. In the Register selection list, select the registers to be downloaded in the Serial EEPROM (see Figure 28).
3. Click Save EEPROM Image.

Figure 28: Device Initialization Image



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