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SH7211 Group

Data Transfer to On-chip Peripheral Modules with DMAC

Introduction

This application note provides an example of transferring data to on-chip peripheral modules with the direct memory access controller (DMAC) of the SH7211.

Target Device

SH7211

Contents

1. Introduction

1.1 Specification

- DMAC channel 1 is used to transfer data from external memory to the transmit FIFO data register (SCFTDR) in the serial communication interface with FIFO (SCIF channel 1) in order to transmit character string data.
- SCIF transmit FIFO data empty transfer requests (on-chip peripheral module request) are used to request DMA transfer.

1.2 Used Modules

- Direct memory access controller (DMAC channel 1)
- Serial communication interface with FIFO (SCIF channel1)

1.3 Applicable Conditions

- Microcontroller: SH7211
- Operating Frequency: Internal clock 160 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
- C Compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01, manufactured by Renesas Technology
- Compile Option: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gb r= auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo

1.4 Related Application Note

- The sample program of this application note has been evaluated in the initial settings described in SH7211 Initialization Application Note. Refer to it for details.

2. Description of Sample Application

In this sample application, the DMAC and on-chip peripheral module requests are used to transfer data from external memory to the SCIF.

2.1 Operational Overview of Used Module

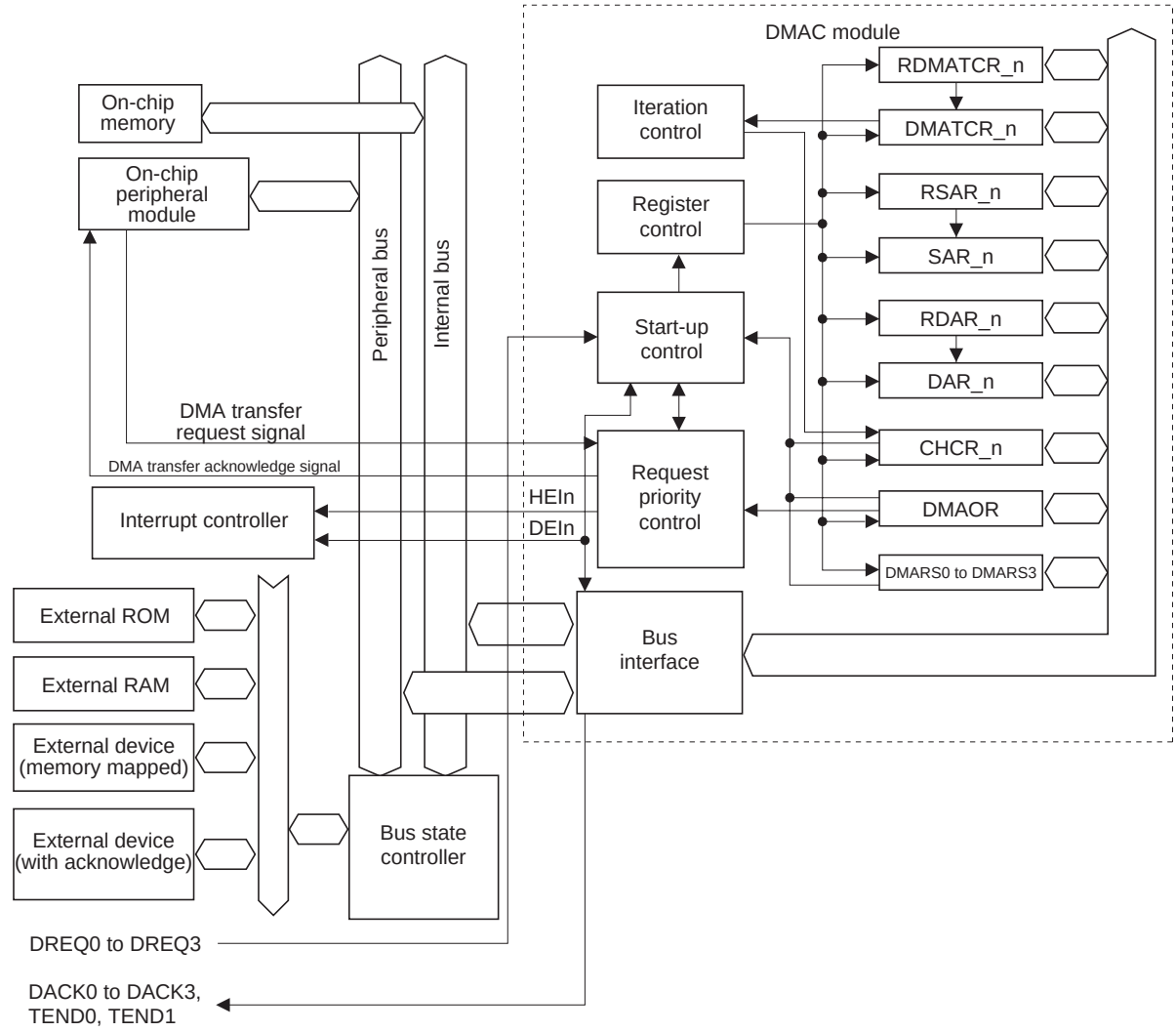
When a DMA transfer request is made, the DMAC starts to transfer data in accordance with the priority order of channels, and continues the transfer operation until the transfer end condition is met. Transfer requests for the DMAC are of three kinds: auto requests, external requests, and on-chip peripheral module requests. The bus mode is selectable as burst mode or cycle-stealing mode.

An overview of the DMAC is given in table 1. Also, a block diagram of the DMAC is shown in figure 1.

Table 1 Overview of DMAC

Item	Description
Number of channels	8 (CH0 to CH7) Only 4 (CH0 to CH3) can receive external requests.
Address space	4 Gbytes
Length of transfer data	Byte, word (2 bytes), longword (4 bytes), and 16 bytes (longword × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address mode	Single address mode and dual address mode
Transfer request	Auto request, external request, and on-chip peripheral module request (SCIF: 8 sources, IIC3: 2 sources, ADC: 1 source, MTU2: 5 sources, CMT: 2 sources)
Bus mode	Cycle-stealing mode and burst mode
Priority level	Channel priority fixed mode and round-robin mode
Interrupt request	An interrupt request to the CPU is made when half or all of a transfer process is completed.
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and TEND can be set independently

Note: For details on the DMAC, refer to the section on the direct memory access controller in the SH7211 Group Hardware Manual.



[Legend]

RDMATCR:	DMA reload transfer count register	CHCR:	DMA channel control register
DMATCR:	DMA transfer count register	DMAOR:	DMA operation register
RSAR:	DMA reload source address register	DMARS0 to DMARS3:	DMA extension resource selectors 0 to 3
SAR:	DMA source address register	HEIn:	DMA transfer half-end interrupt request to the CPU
RDAR:	DMA reload destination address register	DEIn:	DMA transfer end interrupt request to the CPU
DAR:	DMA destination address register	n:	0, 1, 2, 3, 4, 5, 6, 7

Figure 1 Block Diagram of DMAC

2.2 Procedure for Setting Used Modules

This section describes the procedure for making initial settings when the DMAC is to be used to transfer data from memory to on-chip peripheral modules. On-chip peripheral module requests are used for transfer requests. A flowchart of DMAC initialization is shown in figure 2. For details on registers, refer to the SH7211 Group Hardware Manual.

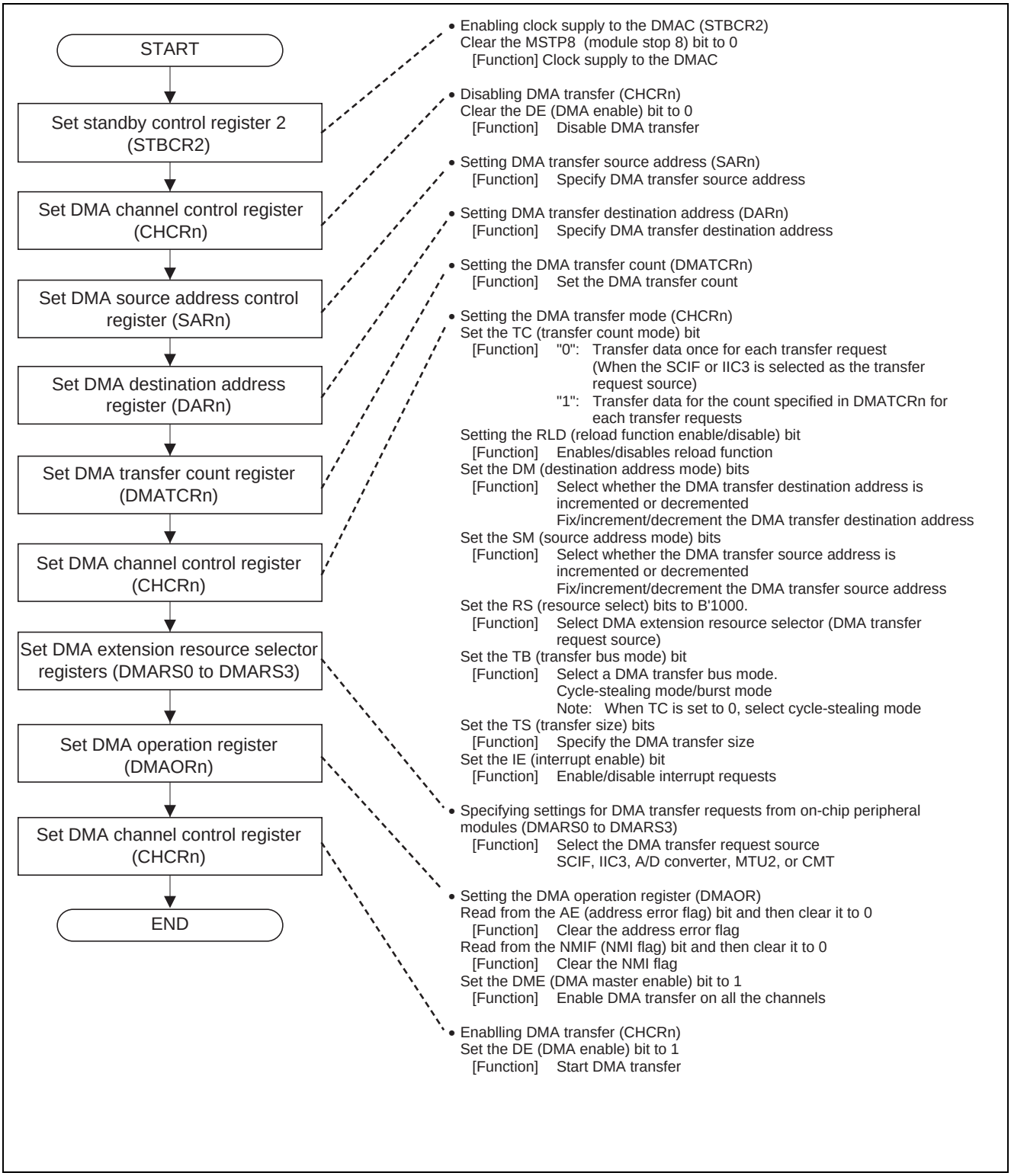


Figure 2 Flowchart of Initializing DMAC

2.3 Operation of Sample Program

In this sample program, SCIF transmit FIFO data empty transfer requests are made to activate DMAC channel 1, and to transfer data from external memory to the transmit FIFO data register (SCFTDR) on SCIF channel 1. The data written to SCFTDR on SCIF channel are transmitted in UART mode. An operation timing of the sample program is shown in figure 3.

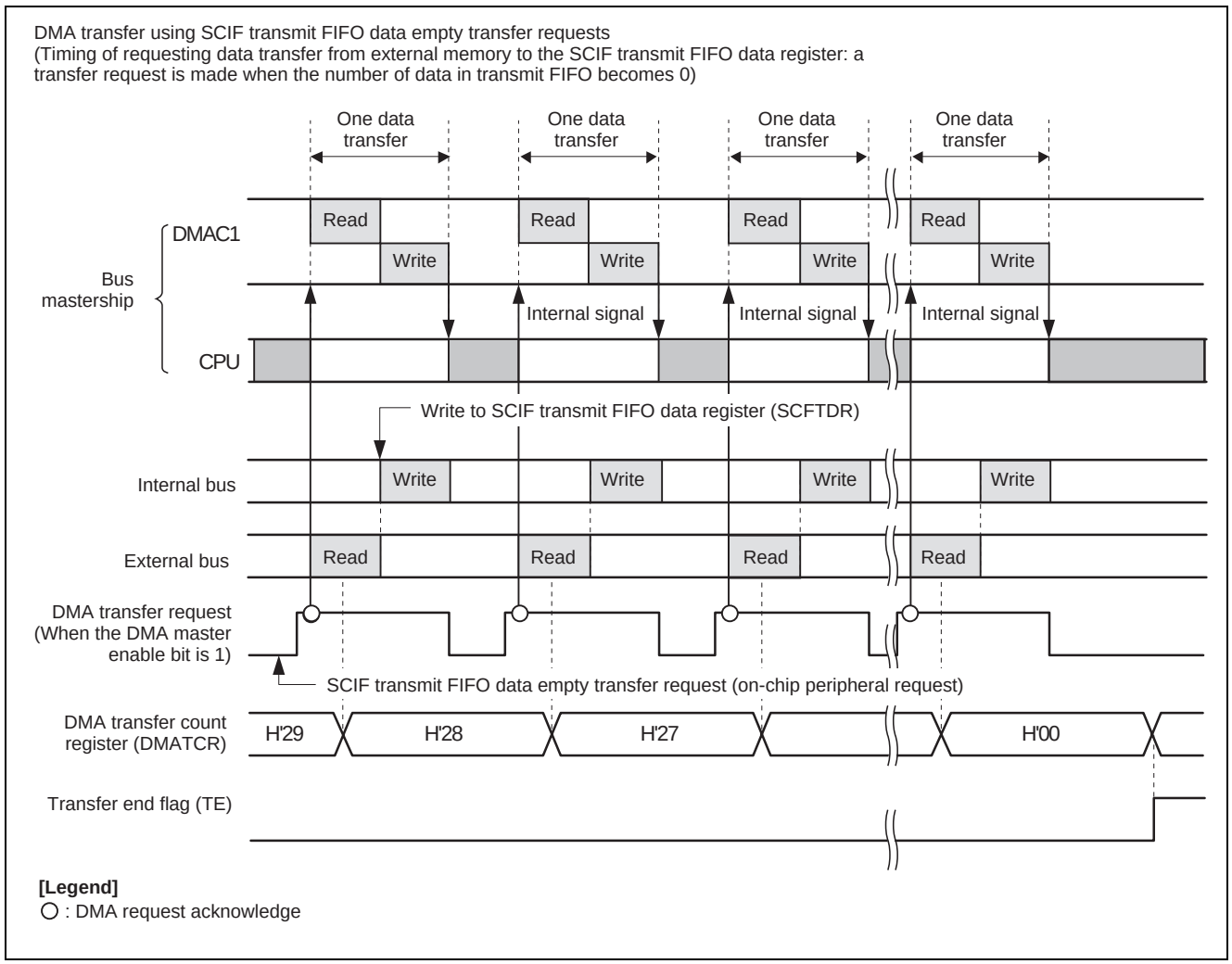


Figure 3 Operation Timing of Sample Application

2.4 Processing Procedure of Sample Program

In this sample program, character string data stored in external memory are transferred by DMA to the transmit FIFO data register (SCFTDR) on SCIF channel 1, and then are transmitted in UART mode.

The register settings for the sample program are listed in table 2. The macro definitions used in this sample program are also listed in table 3. A flowchart of the sample program is illustrated in figure 4.

Table 2 Register Settings for Sample Program

Register Name	Address	Setting Value	Description
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP8="0": DMAC operates
DMA channel control register 1 (CHCR1)	H'FFFE 101C	H'0000 0000	DE="0": Disables DMA transfer
		H'0000 1800	TC = "0": Transfers data once for each DMA transfer request RLD = "0": Disable reload function DM = "B'00": Fixes destination address SM = "B'01": Increments source address RS = "B'1000": Extension resource selector TB = "0": Cycle-stealing mode TS = "B'00": Byte transfer IE = "0": Disables interrupt request
		H'0000 1801	DE = "1": Enables DMA transfer
DMA source address register_1 (SAR1)	H'FFFE 1010	Address where character string data are stored	Start address of transfer source: Start address of character string stored in external memory
DMA destination address register_1 (DAR1)	H'FFFE 1014	H'FFFE 800C	Start address of transfer destination: Address of the SCIF transmit FIFO data register_1 (SCFTDR_1)
DMA transfer count register_1 (DMATCR1)	H'FFFE 1014	Number of character string data	Transfer count: the number of character string data
DMA operation register (DMAOR)	H'FFFE 1200	H'0001	DME = "1": Enables DMA transfer on all the channels
DMA extension resource selector (DMARS0)	H'FFFE 1300	H'8500	MID = "B'100001" RID = "B'01" Set to SCIF_1 transmit FIFO data empty transfer request

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
DMA_SIZE_BYTE	H'0000	Byte transfer
DMA_SIZE_WORD	H'0001	Word transfer
DMA_SIZE_LONG	H'0002	Longword transfer
DMA_SIZE_LONGx4	H'0003	16-byte transfer
DMA_INT_DISABLE	H'0000	DMA transfer end interrupt disabled
DMA_INT_ENABLE	H'0010	DMA transfer end interrupt enabled

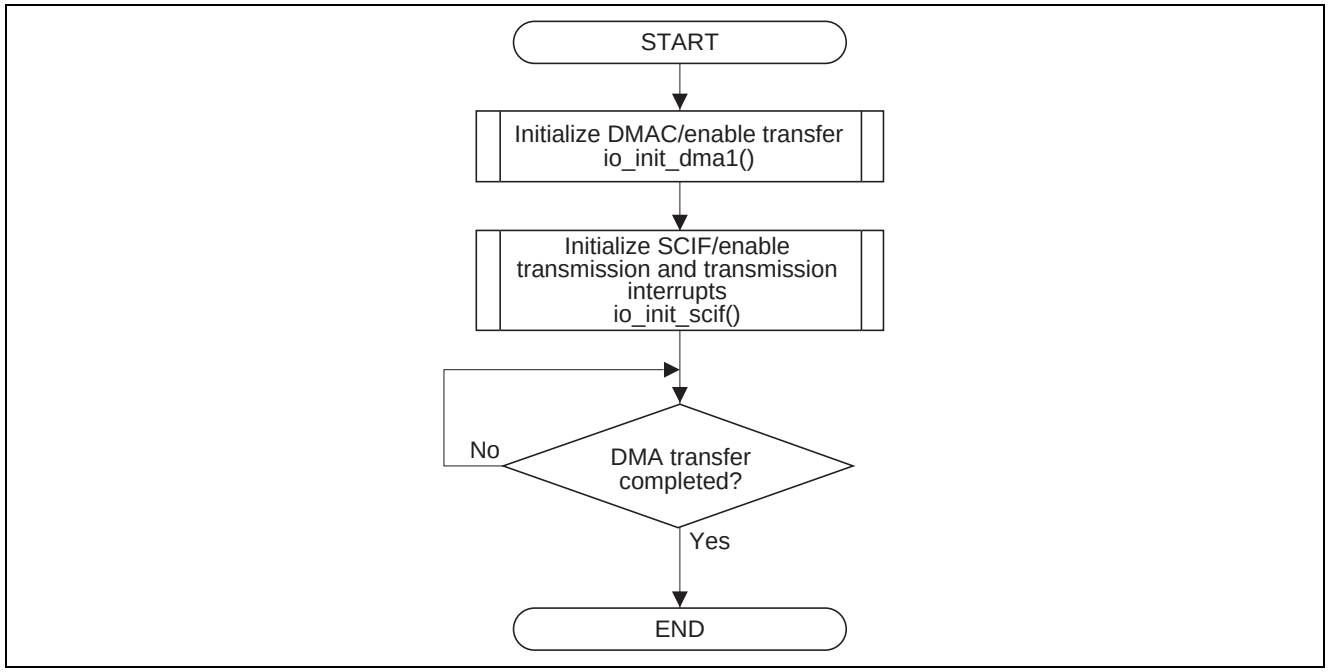


Figure 4 Flowchart of Sample Program

3. Sample Program

1. Sample Program Listing "main.c" (1)

```
1       /*""FILE COMMENT""*****************************************************************
2       *
3       *       System Name : SH7211 Sample Program
4       *       File Name   : main.c
5       *       Contents    : Data transfer to on-chip peripheral module with DMAC
6       *       Version     : 1.00.00
7       *       Model       : M3A-HS11
8       *       CPU         : SH7211
9       *       Compiler    : SHC9.1.1.0
10      *       note        : Data transfer to the SCIF is performed using the DMAC
11      *
12      *       The information described here may contain technical inaccuracies or
13      *       typographical errors. Renesas Technology Corporation and Renesas Solutions
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16      *s
17      *       Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
18      *       AND Renesas Solutions Corp. All Rights Reserved
19      *
20      *       history   : 2007.12.27 ver.1.00.00
21      *""FILE COMMENT END""*************************************************/
22      #include <string.h>
23      #include "iodefine.h"       /* SH7211 iodefine  */
24
25      /* ==== symbol definition ==== */s
26      /* ==== DMAC Settings ==== */
27      #define DMA_SIZE_BYTE 0x0000u
28      #define DMA_SIZE_WORD 0x0001u
29      #define DMA_SIZE_LONG 0x0002u
30      #define DMA_SIZE_LONGx4 0x0003u
31      #define DMA_INT_DISABLE 0x0000u
32      #define DMA_INT_ENABLE 0x0010u
33      #define DMA_INT (DMA_INT_ENABLE >> 4u)
34
35      /* ==== prototype declaration ==== */
36      void main(void);
37      void io_init_dma1(void *src, void *dst, size_t size, unsigned int mode);
38      void io_dma1_stop(void);
39      void io_init_scif(int);
40
41      /* ==== RAM allocation variable declaration ==== */
42      typedef struct {
43          unsigned char scbrr;
44          unsigned short scsmr;
45      } SH_BAUD_SET;
46
47      /* ---- baud rate ---- */
48      enum{
49          CBR_1200,
50          CBR_2400,
51          CBR_4800,
52          CBR_9600,
53          CBR_19200,
54          CBR_31250,
55          CBR_38400,
56          CBR_57600,
57          CBR_115200
58      };
```

2. Sample Program Listing "main.c" (2)

```
59      static SH_BAUD_SET sci_baud[] = {
60          { 64, 2}, /* 1200bps  */
61          {129, 1}, /* 2400bps  */
62          { 64, 1}, /* 4800bps  */
63          {129, 0}, /* 9600bps  */
64          { 64, 0}, /* 19200bps */
65          { 39, 0}, /* 31250bps */
66          { 32, 0}, /* 38400bps */
67          { 21, 0}, /* 57600bps */
68          { 10, 0}  /*115200bps */
69      };
70
71      /* Transmission character string */
72      signed char data[] = "SCIF request DMAC Sample Software.\r\n";
73
74
75      /*""FUNC COMMENT""*****************************************************
76       * Outline     : Sample Program Main
77       *---------------------------------------------------------------------
78       * Include     : #include "iodefine.h"
79       *             : #include <machine.h>
80       *---------------------------------------------------------------------
81       * Declaration : void main(void);
82       *---------------------------------------------------------------------
83       * Function    : Sample Program Main
84       *---------------------------------------------------------------------
85       * Argument    : void
86       *---------------------------------------------------------------------
87       * Return Value: void
88       *---------------------------------------------------------------------
89       * Notice      :
90       *""FUNC COMMENT END""************************************************/
91      void main(void)
92      {
93          /* ==== Setting of DMAC ==== */
94          io_init_dma1(data, (void *)&SCIF1.SCFTDR ,sizeof(data),
95                                  DMA_SIZE_BYTE | DMA_INT_DISABLE);
96              /* Transfer requests : SCIF1 transmitter */
97              /* RAM -> SCIF transmitter               */
98
99          /* ==== Setting of SCIF ==== */
100         io_init_scif(CBR_9600);
101             /* UART mode            */
102             /* bit rate : 9600bps */
103
104         /* ==== DMA start ==== */
105         DMAC1.CHCR.BIT.DE = 1ul;        /* DMA enable */
106
107         /* ==== DMA stop ==== */
108         io_dma1_stop();
109
110         while(1){
111             /* Program end */
112         }
113     }
114
```

3. Sample Program Listing "main.c" (3)

```
/*""FUNC COMMENT""*****************************************************
 * Outline     : Initialization for DATA transfer between memory areas with DMAC
 *---------------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *---------------------------------------------------------------------
 * Declaration : void io_init_dma(void *src, void *dst, size_t size, unsigned int mode);
 *---------------------------------------------------------------------
 * Function    : The DMAC transfers the amount of data specified by "size".
 *             : from the source address "src" to the destination address "dst."
 *             : Transfer is performed using requests from the SCIF1.
 *             : "mode" is specified for transfer size and interrupt used/not used.
 *---------------------------------------------------------------------
 * Argument    : void *src  : Source address
 *             : void *dst  : Destination address
 *             : size_t size: Transfer size (byte)
 *             : unsigned int mode: Transfer mode, specifies the following with logical OR.
 *             :     DMA_SIZE_BYTE  (0x0000) Byte transfer
 *             :     DMA_SIZE_WORD  (0x0001) Word transfer
 *             :     DMA_SIZE_LONG  (0x0002) Longword transfer
 *             :     DMA_SIZE_LONGx4(0x0003) 16-byte transfer
 *             :     DMA_INT_DISABLE(0x0000) DMA transfer end interrupt disabled
 *             :     DMA_INT_ENABLE (0x0010) DMA transfer end interrupt enabled
 *---------------------------------------------------------------------
 * Return Value: void
 *---------------------------------------------------------------------
 * Notice      : Operation is not guaranteed when the alignment of the source/destination.
 *             : address is inconsistent.
 *             : When interrupts are used, interrupt routines must be registered.
 *""FUNC COMMENT END""*************************************************/
void io_init_dma(void *src, void *dst, size_t size, unsigned int mode)
{
    unsigned int ts;
    unsigned long ie;

    ts = mode & 0x3u;
    ie = (mode & 0x00f0u ) >> 4u;

    /* ==== Setting of power down mode ==== */
    STB.CR2.BIT._DMAC = 0x0;        /* Release of the DMAC module standby mode */

    /* ==== Setting of DMAC ==== */
    /* ---- DMA Channel Control Register(CHCR) ---- */
    DMAC1.CHCR.BIT.DE = 0ul;        /* DMA disable */

    /* ---- DMA Source Address Register(SAR) ---- */
    DMAC1.SAR = (void *)src;

    /* ---- DMA Destination Address Register(DAR) ---- */
    DMAC1.DAR = (void *)dst;

```

4. Sample Program Listing "main.c" (4)

```
165         /* ---- DMA Transfer Count Register(DMATCR) ---- */
166     switch(ts){
167     case DMA_SIZE_BYTE:
168          DMAC0.DMATCR = size;             /* Specify transfer count (1/1) */
169          DMAC0.RDMATCR = size;
170          break;
171     case DMA_SIZE_WORD:
172          DMAC0.DMATCR = size >> 1u;       /* Specify transfer count (1/2) */
173          DMAC0.RDMATCR = size >> 1u;
174          break;
175     case DMA_SIZE_LONG:
176          DMAC0.DMATCR = size >> 2u;       /* Specify transfer count (1/4) */
177          DMAC0.RDMATCR = size >> 2u;
178          break;
179     case DMA_SIZE_LONGx4:
180          DMAC0.DMATCR = size >> 4u;       /* Specify transfer count (1/16) */
181          DMAC0.RDMATCR = size >> 4u;
182          break;
183     default:
184          break;
185     }
186
187         /* ---- DMA Channel Control Register(CHCR) ---- */
188         DMAC1.CHCR.LONG = 0x00001800ul | (ts << 3u) | (ie << 2u) ;
189                           /* Fixed destination address       */
190                           /* Source address is incremented   */
191                           /* DMA extension resource selector */
192                           /* Cycle steal mode                */
193                           /* Transfer Size : Byte unit       */
194
195         /* ---- DMA Extension Resource Selector 0(DMARS0) ---- */
196         DMAC.DMARS0.BIT.C1MID = 0x21;   /* Transfer requests : SCIF1 transmitter */
197         DMAC.DMARS0.BIT.C1RID = 0x1;
198
199         /* ---- DMA Operation Register(DMAOR) ---- */
200         DMAC.DMAOR.WORD &= 0xfff9u;     /* AE,NMIF clear */
201
202         if(DMAC.DMAOR.BIT.DME == 0ul){  /* DMA Master Enable */
203             DMAC.DMAOR.BIT.DME = 1ul;
204         }
205     }
206
207     /*""FUNC COMMENT""*****************************************************
208      * Outline     : DMAC stop
209      *-------------------------------------------------------------------
210      * Include     : #include "iodefine.h"
211      *-------------------------------------------------------------------
212      * Declaration : void io_dma1_stop(void);
213      *-------------------------------------------------------------------
214      * Function    : Stop DMA transfer
215      *-------------------------------------------------------------------
216      * Argument    : void
217      *-------------------------------------------------------------------
218      * Return Value: void
219      *-------------------------------------------------------------------
220      * Notice      :
221      *""FUNC COMMENT END""*************************************************/
222     void io_dma1_stop(void)
223     {
224         /* Transmission end detection */;
225         while(DMAC1.CHCR.BIT.TE == 0ul){
226             /* wait for TE bit to be set */
227         }
228
229         /* ---- DMA end ---- */
230         DMAC1.CHCR.BIT.DE = 0ul;    /* DMA disable */
231     }
232
```

5. Sample Program Listing "main.c" (5)

```
233     /*""FUNC COMMENT""*****************************************************
234      * Outline     : Setting of SCIF
235      *-------------------------------------------------------------------------
236      * Include     : #include "iodefine.h"
237      *-------------------------------------------------------------------------
238      * Declaration : void io_init_scif(void);
239      *-------------------------------------------------------------------------
240      * Function    : Settings for the serial communication interface with FIFO.
241      *-------------------------------------------------------------------------
242      * Argument    : int bps : Specified baud rate
243      *-------------------------------------------------------------------------
244      * Return Value: void
245      *-------------------------------------------------------------------------
246      * Notice      :
247      *""FUNC COMMENT END""*************************************************/
248     void io_init_scif(int bps)
249     {
250         int i;
251
252         /* ==== Setting of power down mode ==== */
253         STB.CR4.BIT._SCIF1 = 0;     /* Release of the SCIF1 module standby mode */
254
255         /* ==== Setting of SCIF ==== */
256         /* ---- Serial Control Register(SCSCR) ---- */
257         SCIF1.SCSCR.WORD = 0x00;   /* Transmitter/Receiver disabled */
258         SCIF1.SCSCR.BIT.CKE = 0x0;  /* Internal clock */
259
260         /* ---- Serial Mode Register(SCSMR) ---- */
261         SCIF1.SCSMR.WORD = sci_baud[bps].scsmr;
262                                     /* Asynchronous mode               */
263                                     /* 8-bit data                      */
264                                     /* Parity bit not added or checked */
265                                     /* One stop bit                    */
266
267         /* ---- Bit Rate Register(SCBRR) ---- */
268         SCIF1.SCBRR = sci_baud[bps].scbrr;
269
270         /* ==== Setting of PFC ==== */
271         /* ---- Port A Control Register H3 (PACRH3) ---- */
272         PFC.PACRH3.BIT.PA25MD = 5;  /* Set TxD1 */
273
274         /* ---- Serial Control Register(SCSCR) ---- */
275         SCIF1.SCSCR.BIT.TIE = 1;    /* Transmit interrupt enabled */
276         SCIF1.SCSCR.BIT.TE = 1;     /* Transmitter enabled */
277     }
278
279     /* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7211 Group Hardware Manual
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