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SH7211 Group

Data Transfer between Memory Areas with DMAC

Introduction

This application note provides an example of transferring data between memory areas with the direct memory access controller (DMAC) of the SH7211.

Target Device

SH7211

Contents

1. Introduction

1.1 Specification

- DMAC channel 0 is used to transfer data from the on-chip RAM to external memory. Data are transferred in cycle-stealing mode.
- Auto-request mode (software transfer request) is used for requesting DMA transfer.

1.2 Used Module

- Direct memory access controller (DMAC channel 0)

1.3 Applicable Conditions

- Microcontroller: SH7211
- Operating Frequency: Internal clock 160 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
- C Compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01, manufactured by Renesas Technology
- Compile Option: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gb r= auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo

1.4 Related Application Note

The sample program of this application note has been evaluated in the initial settings described in SH7211 Initialization Application Note. Refer to it for details.

2. Description of Sample Application

In this sample application, the direct memory access controller (DMAC) is used to transfer data from the on-chip RAM to external memory.

2.1 Operational Overview of Used Module

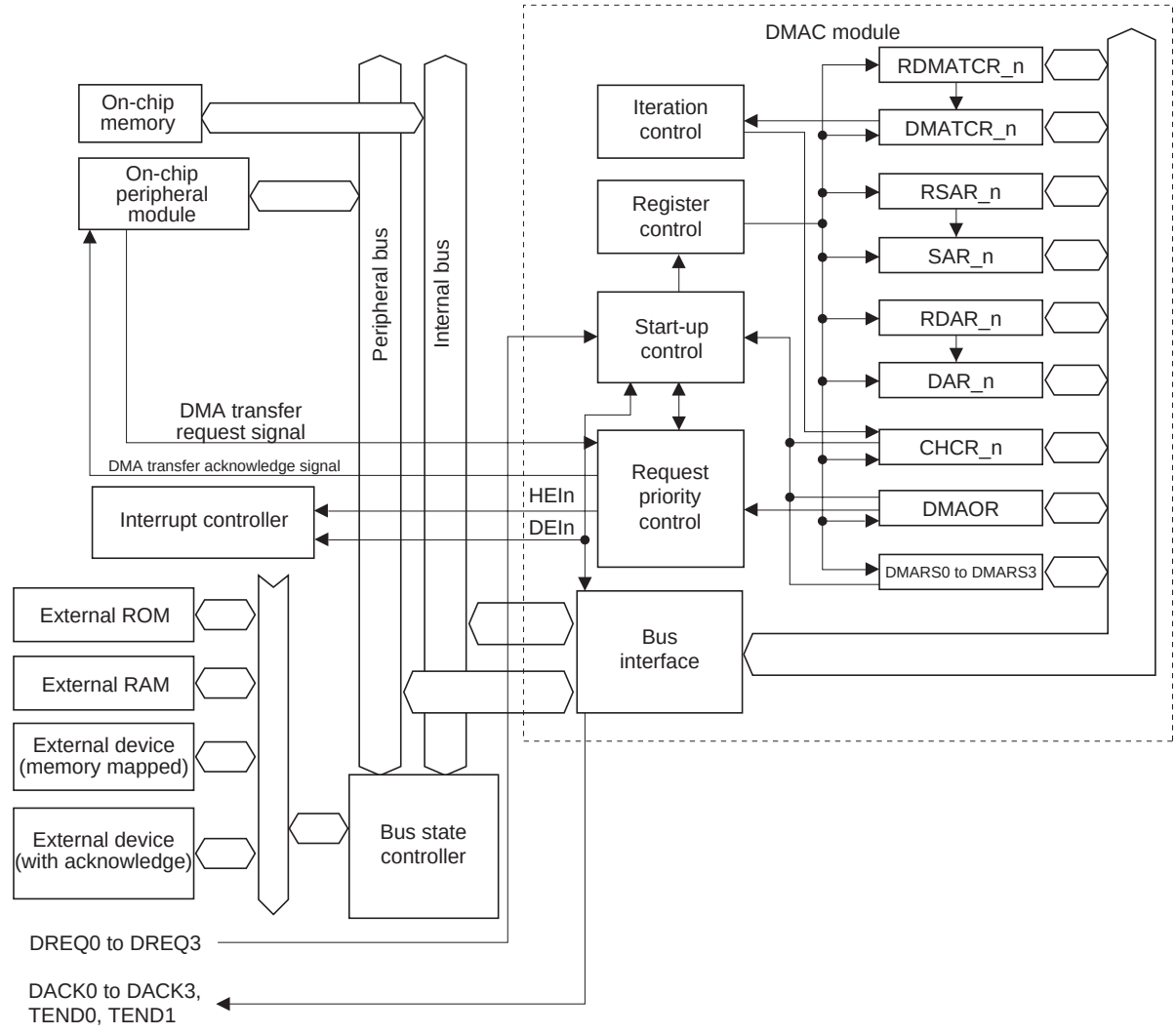
When a DMA transfer request is made, the DMAC starts to transfer data in order of priority of channels. Then, it continues the transfer operation until transfer end condition is met. It has three transfer request modes: auto request, external request, and on-chip peripheral module request. The bus mode is selectable from burst mode and cycle-stealing mode.

An overview of the DMAC is provided in table 1. Also, a block diagram of the DMAC is shown in figure 1.

Table 1 Overview of DMAC

Item	Description
Number of channels	8 channels (CH0 to CH7) Only 4 channels (CH0 to CH3) can receive external requests.
Address space	4 Gbytes
Length of transfer data	Byte, word (2 bytes), longword (4 bytes), and 16 bytes (longword × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address mode	Single address mode and dual address mode
Transfer request	Auto request, external request, and on-chip peripheral module request (SCIF: 8 sources, IIC3: 2 sources, ADC: 1 source, MTU2: 5 sources, CMT: 2 sources)
Bus mode	Cycle-stealing mode and burst mode
Priority level	Channel priority fixed mode and round-robin mode
Interrupt request	An interrupt request to the CPU is made when half or all of a transfer process is completed.
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and TEND can be set independently

Note: For details on the DMAC, refer to the section on the direct memory access controller in the SH7211 Group Hardware Manual.



[Legend]

RDMATCR:	DMA reload transfer count register	CHCR:	DMA channel control register
DMATCR:	DMA transfer count register	DMAOR:	DMA operation register
RSAR:	DMA reload source address register	DMARS0 to DMARS3:	DMA extension resource selectors 0 to 3
SAR:	DMA source address register	HEIn:	DMA transfer half-end interrupt request to the CPU
RDAR:	DMA reload destination address register	DEIn:	DMA transfer end interrupt request to the CPU
DAR:	DMA destination address register	n:	0, 1, 2, 3, 4, 5, 6, 7

Figure 1 Block Diagram of DMAC

2.2 Procedure for Setting Used Module

This section describes the procedure for specifying initial settings for transferring data between memory areas with the DMAC. Auto request mode is used for transfer requests. A flowchart of initializing the DMAC is shown in figure 2. For details on registers, refer to the SH7211 Group Hardware Manual.

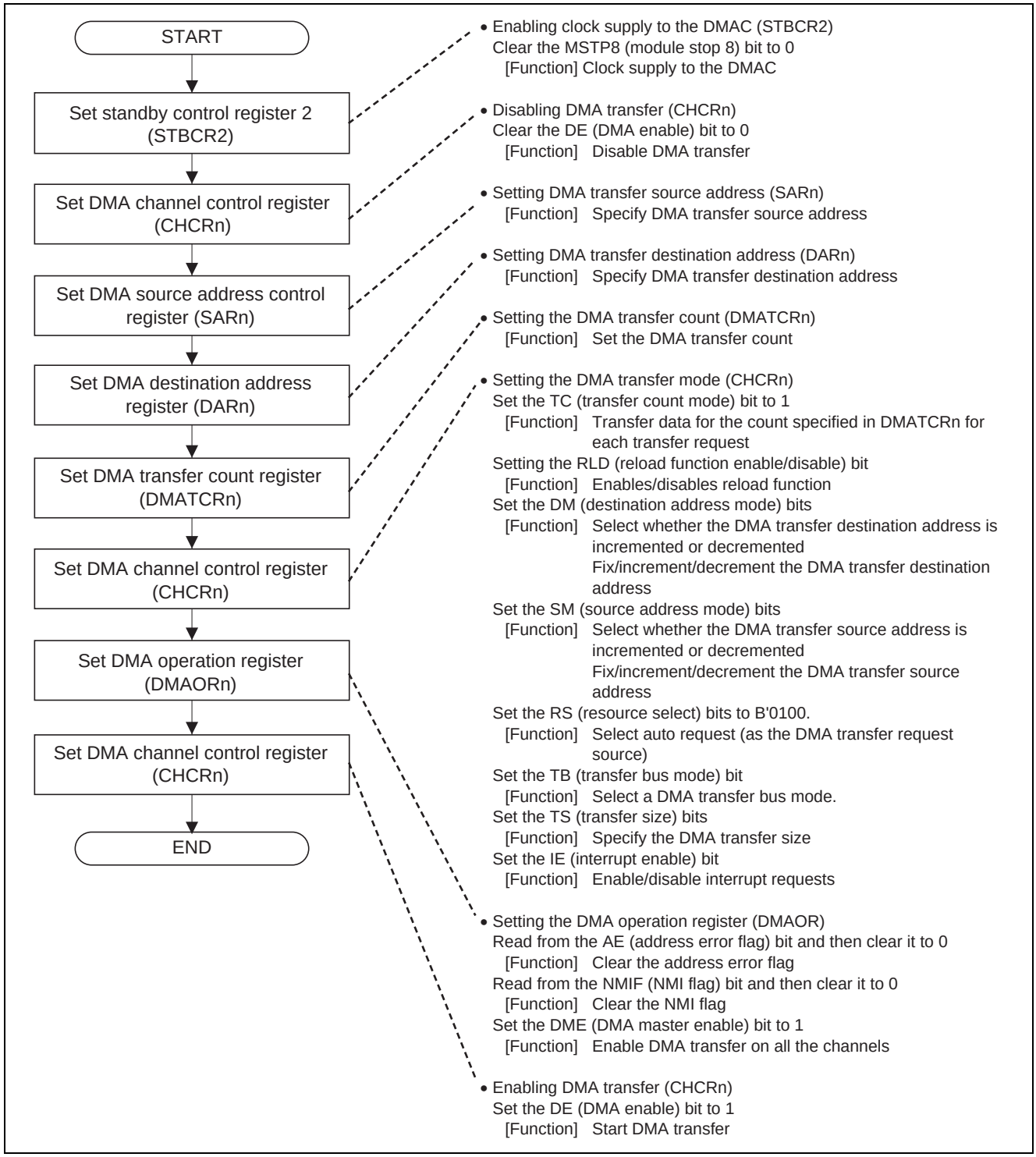


Figure 2 Flowchart of Initializing DMAC

2.3 Operation of Sample Program

In this sample program, DMAC channel 0 is activated by auto request, and data are transferred from the on-chip RAM to external memory in cycle-stealing mode. In cycle-stealing transfer operation, the DMAC gives the bus mastership to the CPU after each round of transferring a single unit of data. An operation timing of the sample application is shown in figure 3.

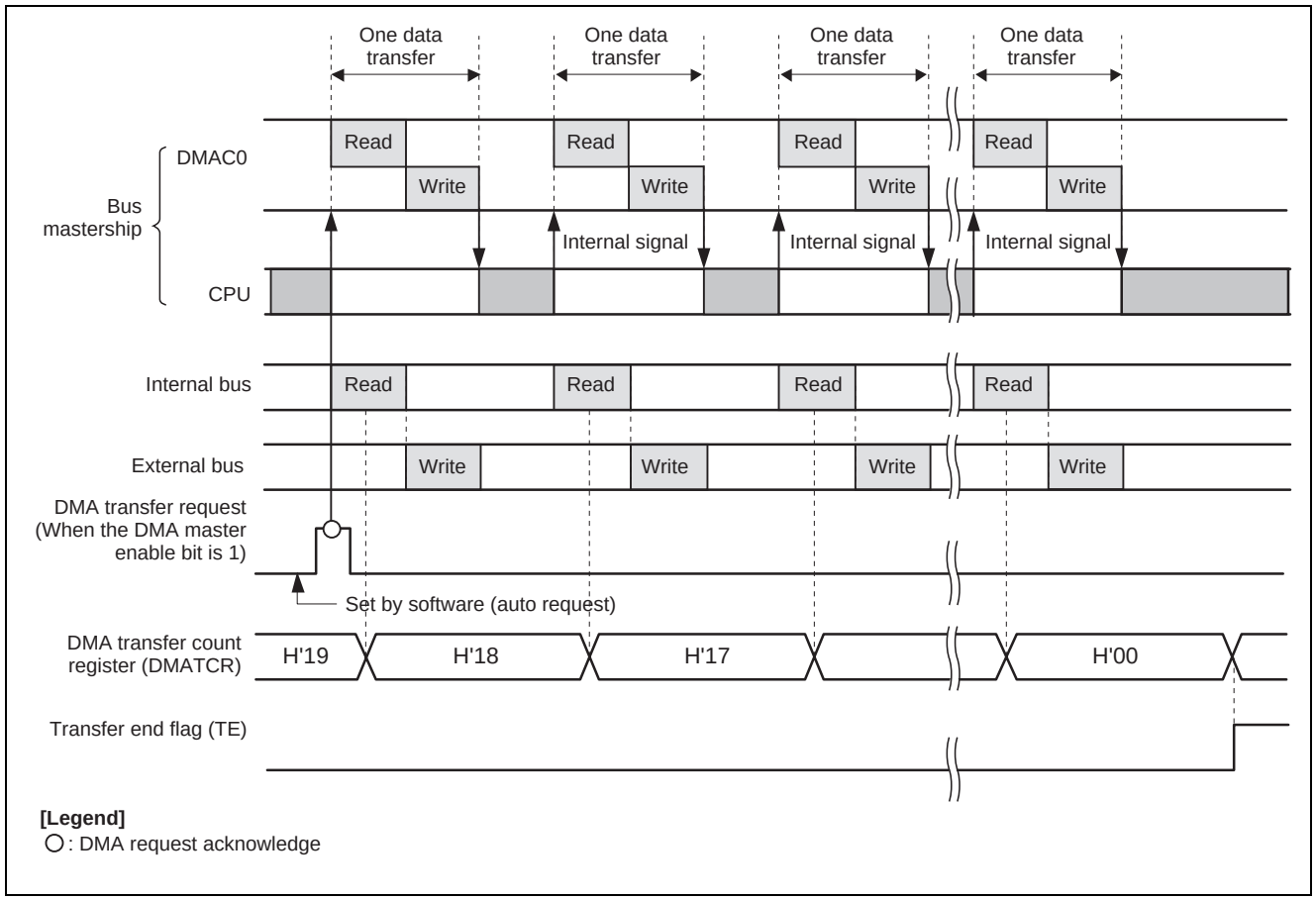


Figure 3 Operation Timing of Sample Application

2.4 Usage Notes on Sample Program

In the reference program, the addresses where the source and destination areas of the transfer start are assigned as absolute addresses for clarity. Ensure that sections used by the user program do not overlap with the source and destination regions that start from the absolute addresses.

2.5 Processing Procedure of Sample Program

In this sample program 100-byte data stored in the on-chip RAM are transferred to external memory by DMA transfer. The transfer end flag (TE bit) is used to check whether DMA transfer is completed.

The register settings for the sample program are listed in table 2. The macro definitions used in this sample program are also listed in table 3. A flowchart of the sample program is illustrated in figure 4.

Table 2 Register Settings for Sample Program

Register Name	Address	Setting Value	Description
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP8="0": DMAC operates
DMA channel control register 0 (CHCR0)	H'FFFE 100C	H'0000 0000	DE="0": Disables DMA transfer
		H'8000 5410	TC = "1" Transfers data for the count specified in DMATCR0 for each DMA transfer request RLD = "0": Disable reload function DM = "B'01": Increments destination address SM = "B'01": Increments source address RS = "B'0100": Auto request TB = "0": Cycle-stealing mode TS = "B'10": Longword transfer IE = "0": Disables interrupt request
		H'8000 5411	DE = "1": Enables DMA transfer
DMA source address register 0 (SAR0)	H'FFFE 1000	H'FFF8 4000	Set start address of transfer source in an on-chip RAM area
DMA destination address register 0 (DAR0)	H'FFFE 1004	H'0C00 0000	Set start address of transfer destination in an external memory area*
DMA transfer count register 0 (DMATCR0)	H'FFFE 1008	H'64	Transfer count: 100 transfers (H'64)
DMA operation register (DMAOR)	H'FFFE 1200	H'0001	DME = "1": Enables DMA transfer on all the channels
DMA extension resource selector 0 (DMARS0)	H'FFFE 1300	H'0000	Not used for auto request

Note: * The address of external memory varies depending on the target board to be used.

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
SDRAM_DST_ADR	H'0C00 0000	• Start address of SDRAM
SRAM_SRC_ADR	H'FFF8 4000	• Start address of on-chip RAM
SIZE	H'64	• Transfer count
DMA_SIZE_BYTE	H'0000	• Byte transfer
DMA_SIZE_WORD	H'0001	• Word transfer
DMA_SIZE_LONG	H'0002	• Longword transfer
DMA_SIZE_LONGx4	H'0003	• 16-byte transfer
DMA_INT_DISABLE	H'0000	• DMA transfer end interrupt disabled
DMA_INT_ENABLE	H'0010	• DMA transfer end interrupt enabled

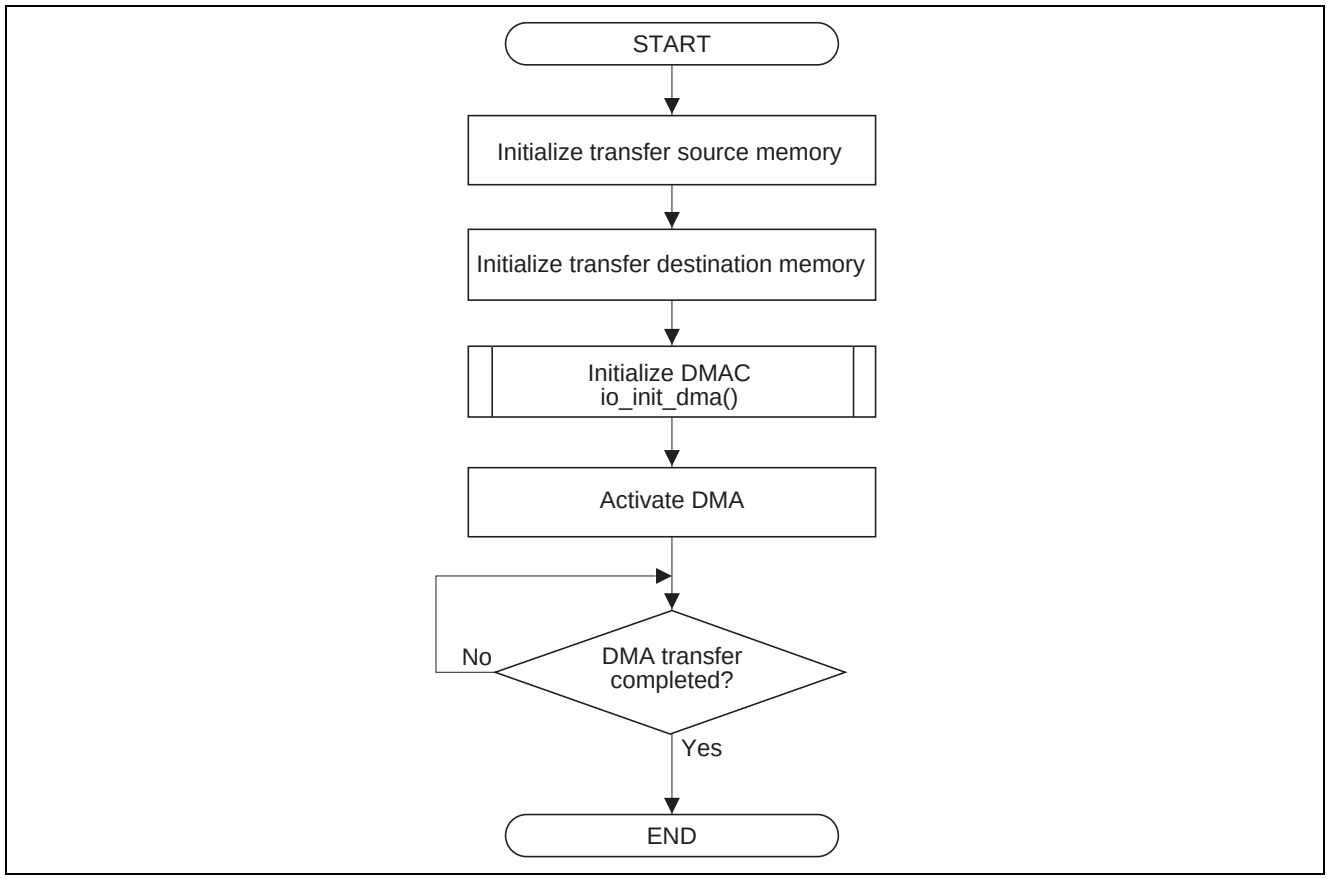


Figure 4 Flowchart of Sample Program

3. Sample Program

1. Sample Program Listing "main.c" (1)

```
1     /*""FILE COMMENT""*****************************************************************
2     *
3     *       System Name : SH7211 Sample Program
4     *       File Name   : main.c
5     *       Contents    : Sample program of DMAC memory-to-memory transfer
6     *       Version     : 1.00.00
7     *       Model       : M3A-HS11
8     *       CPU         : SH7211
9     *       Compiler    : SHC9.1.1.0
10    *       note        : A sample program for transferring data with the DMAC.
11    *                     Using software triggers transfers 100-byte data from the on-chip RAM to
12                          external memory.
13    *
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21    *
22    *       history   : 2007.12.27 ver.1.00.00
23    *""FILE COMMENT END""*************************************************************/
24    #include <machine.h>
25    #include <stdio.h>
26    #include "iodefine.h"       /* SH7211 iodefine  */
27
28    /* ==== symbol definition ==== */
29    #define SDRAM_DST_ADR ((void *)0x0c000000)  /* External SDRAM top address */
30    #define SRAM_SRC_ADR ((void *)0xfff84000)   /* Internal SRAM address  */
31    #define SIZE 100                            /* Transmission bytes         */
32    #define DMA_SIZE_BYTE 0x0000u
33    #define DMA_SIZE_WORD 0x0001u
34    #define DMA_SIZE_LONG 0x0002u
35    #define DMA_SIZE_LONGx4 0x0003u
36    #define DMA_INT_DISABLE 0x0000u
37    #define DMA_INT_ENABLE 0x0010u
38    #define DMA_INT (DMA_INT_ENABLE >> 4u)
39
40    /* ==== prototype declaration ==== */
41    void main(void);
42    void io_init_dma(void *src, void *dst, size_t size, unsigned int mode);
43    void io_dma_enable(void);
44    void io_dma_stop(void);
45
```

2. Sample Program Listing "main.c" (2)

```
46    /*""FUNC COMMENT""*****************************************************
47     * Outline     : Sample Program Main
48     *-------------------------------------------------------------------------
49     * Include     : #include "iodefine.h"
50     *             : #include <machine.h>
51     *-------------------------------------------------------------------------
52     * Declaration : void main(void);
53     *-------------------------------------------------------------------------
54     * Function    : Sample program main
55     *-------------------------------------------------------------------------
56     * Argument    : void
57     *-------------------------------------------------------------------------
58     * Return Value: void
59     *-------------------------------------------------------------------------
60     * Notice      :
61     *""FUNC COMMENT END""*************************************************/
62    void main(void)
63    {
64        int i;
65        volatile unsigned char *ptr;
66
67
68        /* ==== Initialize source memory ==== */
69        ptr = SRAM_SRC_ADR;
70        for(i=0; i < SIZE; i++){
71            *ptr++ = 0x55;
72        }
73
74        /* ==== Initialize destination memory ==== */
75        ptr = SDRAM_DST_ADR;
76        for(i=0; i < SIZE; i++){
77            *ptr++ = 0;
78        }
79
80        /* ==== Setting of DMAC ==== */
81        io_init_dma(SRAM_SRC_ADR, SDRAM_DST_ADR, SIZE , DMA_SIZE_LONG | DMA_INT_DISABLE);
82
83        /* ---- DMA start ---- */
84        io_dma_enable();
85
86        /* ---- DMA stop ---- */
87        io_dma_stop();
88
89        while(1){
90            /* Program end */
91        }
92    }
93
```

3. Sample Program Listing "main.c" (3)

```
93     /*""FUNC COMMENT""*****************************************************
94      * Outline     : Initialization for DATA transfer between memory areas with DMAC
95      *-------------------------------------------------------------------------
96      * Include     : #include "iodefine.h"
97      *-------------------------------------------------------------------------
98      * Declaration : void io_init_dma(void *src, void *dst, size_t size, unsigned int mode);
99      *-------------------------------------------------------------------------
100     * Function    : The DMAC transfers the amount of data specified by "size".
101     *             : from the source address "src" to the destination address "dst."
102     *             : Auto request mode is used to transfer data.
103     *             : "mode" is specified for transfer size and interrupt used/not used
104     *-------------------------------------------------------------------------
105     * Argument    : void *src  : Source address
106     *             : void *dst  : Destination address
107     *             : size_t size: Transfer size (byte)
108     *             : unsigned int mode: Transfer mode, specifies the following with logical OR.
109     *             :     DMA_SIZE_BYTE  (0x0000) Byte transfer
110     *             :     DMA_SIZE_WORD  (0x0001) Word transfer
111     *             :     DMA_SIZE_LONG  (0x0002) Longword transfer
112     *             :     DMA_SIZE_LONGx4(0x0003) 16-byte transfer
113     *             :     DMA_INT_DISABLE(0x0000) DMA transfer end interrupt disabled
114     *             :     DMA_INT_ENABLE (0x0010) DMA transfer end interrupt enabled
115     *-------------------------------------------------------------------------
116     * Return Value: void
117     *-------------------------------------------------------------------------
118     * Notice      : Operation is not guaranteed when the alignment of the source/destination
119     *             : address is inconsistent.
120     *             : When interrupts are used, interrupt routines must be registered.
121     *""FUNC COMMENT END""*************************************************/
122    void io_init_dma(void *src, void *dst, size_t size, unsigned int mode)
123    {
124        unsigned int ts;
125        unsigned long ie;
126
127
128        ts = mode & 0x3u;
129        ie = (mode & 0x00f0u ) >> 4u;
130
131        /* ==== Setting of power down mode ==== */
132        STB.CR2.BIT._DMAC = 0x0;        /* Release of the DMAC module standby mode */
133
134        /* ==== Setting of DMAC ==== */
135        /* ---- DMA Channel Control Register(CHCR) ---- */
136        DMAC0.CHCR.BIT.DE = 0ul;        /* DMA disable */
137
138        /* ---- DMA Source Address Register(SAR) ---- */
139        DMAC0.SAR = (void *)src;
140
141        /* ---- DMA Destination Address Register(DAR) ---- */
142        DMAC0.DAR = (void *)dst;
143
```

4. Sample Program Listing "main.c" (4)

```
144       /* ---- DMA Transfer Count Register(DMATCR) ---- */
145   switch(ts){
146   case DMA_SIZE_BYTE:
147     DMAC0.DMATCR = size;        /* Specify transfer count (1/1) */
148     DMAC0.RDMATCR = size;
149     break;
150   case DMA_SIZE_WORD:
151     DMAC0.DMATCR = size >> 1u;      /* Specify transfer count (1/2) */
152     DMAC0.RDMATCR = size >> 1u;
153     break;
154   case DMA_SIZE_LONG:
155     DMAC0.DMATCR = size >> 2u;      /* Specify transfer count (1/4) */
156     DMAC0.RDMATCR = size >> 2u;
157     break;
158   case DMA_SIZE_LONGx4:
159     DMAC0.DMATCR = size >> 4u;      /* Specify transfer count (1/16) */
160     DMAC0.RDMATCR = size >> 4u;
161     break;
162   default:
163     break;
164   }
165
166       /* ---- DMA Channel Control Register(CHCR) ---- */
167       DMAC0.CHCR.LONG = 0x00005400ul | (ts << 3u) | (ie << 2u) ;
168                           /* Destination address is incremented */
169                           /* Source address is incremented      */
170                           /* Auto request                       */
171                           /* Cycle-stealing mode                   */
172                           /* Transfer Size : Longword unit      */
173
174       /* ---- DMA Operation Register(DMAOR) ---- */
175       DMAC.DMAOR.WORD &= 0xfff9u;     /* AE,NMIF clear */
176
177       if(DMAC.DMAOR.BIT.DME == 0){    /* DMA Master Enable */
178           DMAC.DMAOR.BIT.DME = 1;
179       }
180   }
181
```

5. Sample Program Listing "main.c" (5)

```
/*""FUNC COMMENT""************************************************
 * Outline     : DMAC Actibation
 *-----------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-----------------------------------------------------------------
 * Declaration : void io_dma_enable(void);
 *-----------------------------------------------------------------
 * Function    : Performs DMA transfer
 *-----------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------
 * Return Value: void
 *-----------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*******************************************/
void io_dma_enable(void)
{
    /* ---- DMA start ---- */
    DMAC0.CHCR.BIT.DE = 1ul;    /* DMA enable */
}

/*""FUNC COMMENT""************************************************
 * Outline     : DMAC Stop
 *-----------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-----------------------------------------------------------------
 * Declaration : void io_dma_stop(void);
 *-----------------------------------------------------------------
 * Function    : Checks whether the transfer is completed and stops the DMA transfer.
 *-----------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------
 * Return Value: void
 *-----------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*******************************************/
void io_dma_stop(void)
{
    /* Transmission end detection */;
    while(DMAC0.CHCR.BIT.TE == 0ul){
        /* wait for TE bit to be set */
    }

    /* ---- DMA stop ---- */
    DMAC0.CHCR.BIT.DE = 0ul;    /* DMA disable */ }

/* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
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1.01	Dec.17.08	9 to 13	Source file is updated

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