# Application Note

## DA9213 Standard Variants Overview

### AN-PM-121


### Abstract

*This application note describes the default register settings of the DA9213 standard variants.*

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# 1 Terms and Definitions

| | |
|---|---|
| CPU | Central Processing Unit |
| GPIO | General Purpose Input/Output |
| GPU | Graphic Processing Unit |
| OTP | One Time Programmable (Memory) |
| PMU | Power Management Unit |
| PWM | Pulse-Width Modulation |

# 2 References

[1] DA9213, Datasheet, Dialog Semiconductor.

 

# 3 Introduction

The DA9213 is a PMU optimized for the supply of CPUs, GPUs, and DDR memory rails in smartphones, tablets and other portable applications. The fast transient response and load regulation are optimized for the latest generation of multi-core application processors. The DA9213 operates as a single four-phase buck converter delivering up to 20 A output current.

This application note intended to help a hardware designer understand the configurations of the DA9213 standard variants.

## 3.1 System Diagram

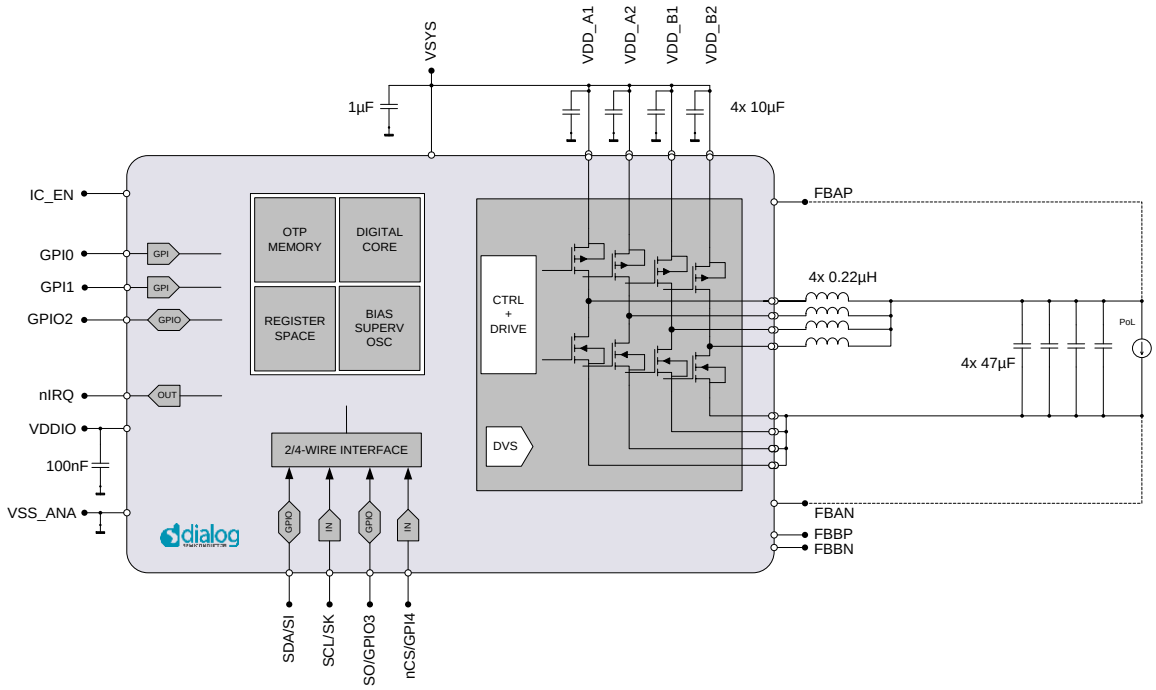


**Figure 1: DA9213 System Diagram**

## 3.2 Variant Table and Ordering Information

**Table 1: Ordering Information**

| Part Number | Package | Shipment Form | Pack Quantity |
|---|---|---|---|
| DA9213-xxUP2 | 66 WL-CSP | Tape and Reel | 4500pcs |
| DA9213-xxUP6 | 66 WL-CSP | Waffle | |
| DA9213-JEUP2 | 66 WL-CSP | Tape and Reel | 4500pcs |
| DA9213-JEUP6 | 66 WL-CSP | Tray | |
| DA9213-88UP2 | 66 WL-CSP | Tape and Reel | 4500pcs |
| DA9213-88UP2 | 66 WL-CSP | Waffle | |

# 4 DA9213-JEUP Detailed Description

Key settings:

- Default output voltage is set to 1.0 V.
- Buck is set to operate in SYNC (forced PWM) mode.
- Maximum allowed output voltage is set to 1.57 V.
- GPI0, GPI1, GPIO2, GPIO3 and GPI4 are assigned as active-high digital input.

**Table 2: DA9213-JEUP Register Settings**

| Register Address | Function | Default Value | Description |
|---|---|---|---|
| 0x054 | MASK_A | 0x5F | nIRQ interrupt at GPI0 to GPI4 and UVLO_IO caused nIRQ are masked. |
| 0x055 | MASK_B | 0x3F | PWRGOOD Buck A and Buck B, TEMP_WARN, TEMP_CRIT, OV_CURR Buck A and OV_CURR Buck B caused event are masked. |
| 0x056 | CONTROL_A | 0x53 | GPIO debounce time = 10 ms<br>DVC slew rate A = 10 mV/µs<br>DVC slew rate B = 10 mV/µs<br>V_LOCK = 0: Allows host writes into registers 0xD0 to 0x14F. |
| 0x058 | GPI0-1 | 0x44 | GPI0: input, active high, debouncing off.<br>GPI1: input, active high, debouncing off. |
| 0x059 | GPIO2-3 | 0x44 | GPIO2: input, active high, debouncing off.<br>GPIO3: input, active high, debouncing off. |
| 0x05A | GPI4 | 0x04 | GPI4: input, active high, debouncing off. |
| 0x05D | BUCKA_CONT | 0x00 | Buck is default OFF.<br>Pull down resistor is enabled.<br>Buck output voltage is selected from VBUCK_A. |
| 0x0D0 | BUCK_ILIM | 0x99 | Current limit per phase BUCKA_ILIM = 5800 mA<br>(peak inductor current) |
| 0x0D1 | BUCKA_CONF | 0x92 | Operation mode is set to SYNC (forced PWM) mode.<br>Start-up control = 20 mV/µs<br>Down control = 20 mV/µs |
| 0x0D3 | VBUCK_CONF | 0x1F | Maximum 4-phase is selected. Phase-shedding is enabled. |
| 0x0D5 | VBUCKA_MAX | 0x7F | Max output voltage VBUCKA_MAX = 1.57 V |
| 0x0D7 | VBUCKA_A | 0x46 | Output voltage VBUCKA_A = 1.00 V |
| 0x0D8 | VBUCKA_B | 0x46 | Output voltage VBUCKA_B = 1.00 V |
| 0x105 | INTERFACE | 0xD9 | Primary 2-wire interface slave address = 0xD0 |
| 0x106 | INTERFACE2 | 0x80 | Communication interface is 2-wire, standard speed, PM_IF_V=VDDCORE. |
| 0x143 | CONFIG_A | 0x12 | Enabled automatic reset of 2-WIRE interface in case of clock stays low for >35 ms.<br>nIRQ output port is open drain, active low.<br>GPIs are supplied from VDDCORE. |
| 0x144 | CONFIG_B | 0xE0 | UVLO_IO is disabled.<br>Power good signal masked during DVC transitions (keep previous status).<br>Reload function is disabled. |

## DA9213 Standard Variants Overview

| Register Address | Function | Default Value | Description |
|---|---|---|---|
| 0x145 | CONFIG_C | 0x00 | GPI0, GPI1, GPIO2, GPIO3 and GPI4 pull-down resistors are disabled. |
| 0x146 | CONFIG_D | 0x00 | Buck Power Good (PG) and READY are not assigned to any GPIOs. |
| 0x147 | CONFIG_E | 0x80 | DA9213 is set as standalone device.<br>No tune of oscillator frequency. |
| 0x148 | CONFIG_F | 0xD0 | Secondary 2-wire interface slave address = 0xD0 |

# 5 DA9213-88UP Detailed Description

Key settings:

- Default output voltage is set to 0.85 V.
- Secondary voltage is set to 0.90 V and can be triggered via GPIO1.
- Buck is set to operate in AUTO mode.
- Maximum allowed output voltage is set to 1.57 V.
- GPI0 is assigned as active-high digital input and serves as buck enable/disable pin.
- GPI1 is assigned as active- high digital input and serves as buck output voltage switch pin.
- GPIO2 is assigned active-high open-drain output and serves as a ready signal output pin.
- GPIO3 is assigned as active-high open-drain output and serves as a power good signal output pin
- GPI4 is not used.

**Table 3: DA9213-88UP Register Settings**

| Register Address | Function | Default Value | Description |
|---|---|---|---|
| 0x054 | MASK_A | 0x5F | nIRQ interrupt at GPI0 to GPI4 and UVLO_IO caused nIRQ are masked. |
| 0x055 | MASK_B | 0x3F | PWRGOOD Buck A and Buck B, TEMP_WARN, TEMP_CRIT, OV_CURR Buck A and OV_CURR Buck B caused event are masked. |
| 0x056 | CONTROL_A | 0x51 | GPIO debounce time = 0.1 ms<br>DVC slew rate A = 10 mV/µs<br>DVC slew rate B = 10 mV/µs<br>V_LOCK = 0: Allows host writes into registers 0xD0 to 0x14F. |
| 0x058 | GPI0-1 | 0x44 | GPI0: input, active high, debouncing off.<br>GPI1: input, active high, debouncing off. |
| 0x059 | GPIO2-3 | 0xEE | GPIO2: output open-drain, active high, debouncing on.<br>GPIO3: output open-drain, active high, debouncing on. |
| 0x05A | GPI4 | 0x0C | GPI4: input, active high, debouncing on. |
| 0x05D | BUCKA_CONT | 0x22 | Buck is default OFF.<br>Pull down resistor is enabled.<br>Buck is controlled by GPI0 (enable on passive to active, disable on active to passive).<br>VBUCK is controlled by GPI1 (VBUCK_A on active to passive, VBUCK_B on passive to active). |
| 0x0D0 | BUCK_ILIM | 0xFF | Current limit per phase BUCKA_ILIM = 7000 mA.<br>(peak inductor current) |
| 0x0D1 | BUCKA_CONF | 0x0F | Operation mode is set to AUTO mode.<br>Start-up control = 10 mV/µs<br>Down control = 1.25 mV/µs |
| 0x0D3 | VBUCK_CONF | 0x1F | Maximum 4-phase is selected. Phase-shedding is enabled. |
| 0x0D5 | VBUCKA_MAX | 0x7F | Max output voltage VBUCKA_MAX = 1.57 V |
| 0x0D7 | VBUCKA_A | 0x37 | Output voltage VBUCKA_A = 0.85 V |
| 0x0D8 | VBUCKA_B | 0x3C | Output voltage VBUCKA_B = 0.9 V |
| 0x105 | INTERFACE | 0xD9 | Primary 2-wire interface slave address = 0xD0 |
| 0x106 | INTERFACE2 | 0x90 | Communication interface is 2-wire, standard speed, |

## DA9213 Standard Variants Overview

| Register Address | Function | Default Value | Description |
|---|---|---|---|
| | | | PM_IF_V=VDDIO. |
| 0x143 | CONFIG_A | 0x1A | Enabled automatic reset of 2-WIRE interface in case of clock stays low for > 35 ms.<br>nIRQ output port is open drain, active low.<br>GPIs are supplied from VDDIO. |
| 0x144 | CONFIG_B | 0xE0 | UVLO_IO is disabled.<br>Power good signal masked during DVC transitions (keep previous status).<br>Reload function is disabled. |
| 0x145 | CONFIG_C | 0x1F | GPI0, GPI1, and GPI4 pull-down resistors are enabled.<br>GPO2 and GPO3 pull-up resistors are enabled. |
| 0x146 | CONFIG_D | 0x21 | GPO3 is assigned as Power Good (PG), GPO2 is assigned as READY. |
| 0x147 | CONFIG_E | 0x80 | DA9213 is set as standalone device.<br>No tune of oscillator frequency. |
| 0x148 | CONFIG_F | 0xD0 | Secondary 2-wire interface slave address = 0xD0 |

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**Table 4: DA9213 Standard Variants Overview**

| Register Address | Function | Standard Variant DA9213- | | | | | |
|---|---|---|---|---|---|---|---|
| | | JEUP | 88UP | | | | |
| 0x054 | MASK_A | 0x5F | 0x5F | | | | |
| 0x055 | MASK_B | 0x3F | 0x3F | | | | |
| 0x056 | CONTROL_A | 0x53 | 0x51 | | | | |
| 0x058 | GPI0-1 | 0x44 | 0x44 | | | | |
| 0x059 | GPIO2-3 | 0x44 | 0xEE | | | | |
| 0x05A | GPI4 | 0x04 | 0x0C | | | | |
| 0x05D | BUCKA_CONT | 0x00 | 0x22 | | | | |
| 0x0D0 | BUCK_ILIM | 0x99 | 0xFF | | | | |
| 0x0D1 | BUCKA_CONF | 0x92 | 0x0F | | | | |
| 0x0D3 | VBUCK_CONF | 0x1F | 0x1F | | | | |
| 0x0D5 | VBUCKA_MAX | 0x7F | 0x7F | | | | |
| 0x0D7 | VBUCKA_A | 0x46 | 0x37 | | | | |
| 0x0D8 | VBUCKA_B | 0x46 | 0x3C | | | | |
| 0x105 | INTERFACE | 0xD9 | 0xD9 | | | | |
| 0x106 | INTERFACE2 | 0x80 | 0x90 | | | | |
| 0x143 | CONFIG_A | 0x12 | 0x1A | | | | |
| 0x144 | CONFIG_B | 0xE0 | 0xE0 | | | | |
| 0x145 | CONFIG_C | 0x00 | 0x1F | | | | |
| 0x146 | CONFIG_D | 0x00 | 0x21 | | | | |
| 0x147 | CONFIG_E | 0x80 | 0x80 | | | | |
| 0x148 | CONFIG_F | 0xD0 | 0xD0 | | | | |

# 7 Conclusions

Understanding the configuration of the OTP described in this document can help minimize system issues such as incorrect hardware configuration. For further information please refer to the datasheets [1], on the Dialog website (https://www.dialog-semiconductor.com/pmics) or contact Dialog via either your sales representative or the support forum (https://support.dialog-semiconductor.com/forums/pmic-audio).

# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 06-Aug-2018 | Initial version. |
| 1.1 | 24-Feb-2022 | File was rebranded with new logo, copyright and disclaimer |

# DA9213 Standard Variants Overview

## Status Definitions

| Status | Definition |
|---|---|
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| APPROVED or unmarked | The content of this document has been approved for publication. |

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