Application Note

DA9063-A Power Management for Renesas R-Car M3 Platform

AN-PM-097

Abstract

The R-Car M3 System-on-Chip (SoC)-based platform from Renesas is part of a family of platforms (R-Car series) for automotive infotainment systems. The M3 is aimed at the mid-level segment, and is optimized for automotive Human Machine Interface (HMI), infotainment and integrated dashboards.

The platform features the Dialog DA9063-A as system PMIC (Power Management IC) and the Dialog DA9224-A multi-phase sub-PMIC step-down buck converter to power and supervise the complete system.

Through a description of the general system configuration, power capabilities and requirements and an overview of the component interconnections, it will be shown that the combination of DA9063-A and DA9224-A are highly suited as the R-Car power management system solution for M3 platforms.

DA9063-A Power Management for Renesas R-Car M3 Platform

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1 Terms and Definitions

PMIC	Power Management Integrated Circuit
MRM	Memory Retention Mode

2 References

[1] DA9063-A, Datasheet, Dialog Semiconductor.

[2] DA9224-A, Datasheet, Dialog Semiconductor.

[3] AN-SW-127, DA9063_and_DA9224_Integration_for_R-Car_M3_1v0, Application Note, Dialog Semiconductor.

3 Introduction

This document describes how to interconnect the DA9063-A Power Management IC (PMIC) and the DA9224-A sub-PMIC to the Renesas R-Car M3 System on a Chip (SoC). The DA9063-A is a highly integrated chip that supports Dynamic Voltage Control (DVC) technology, enabling significant power saving: this feature supports the Dynamic Voltage and Frequency Scaling (DVFS) technology that is used by many processors.

As a result of their highly integrated features, the DA9063-A PMIC, and DA9224-A sub-PMIC significantly reduce the overall system cost and size compared to a discrete solution. This application note addresses only the power supply related features: discussion of other features of the optimized PMIC is beyond the scope of this document.

For further information on the DA9063-A, and DA9224-A please refer to the datasheets available via your local Dialog sales office.

For information about Renesas R-Car M3 SoC, please refer to Renesas website:

https://www.renesas.com/en-us/solutions/automotive/products/rcar-m3.html

4 Renesas R-Car M3 SoC Description

Renesas R-Car M3 is a platform for automotive infotainment with an SoC containing eight cores (ARM®Cortex®-A57 Quad Core, ARM Cortex-A53 Quad, ARM Cortex-R7 Dual lock-step) and PowerVR GX6650 GPU.

Figure 1 shows a typical system block diagram of the R-Car M3 SoC application. The embedded cores require suitable power management that is readily achieved using the Dialog DA9063-A, and DA9224-A.

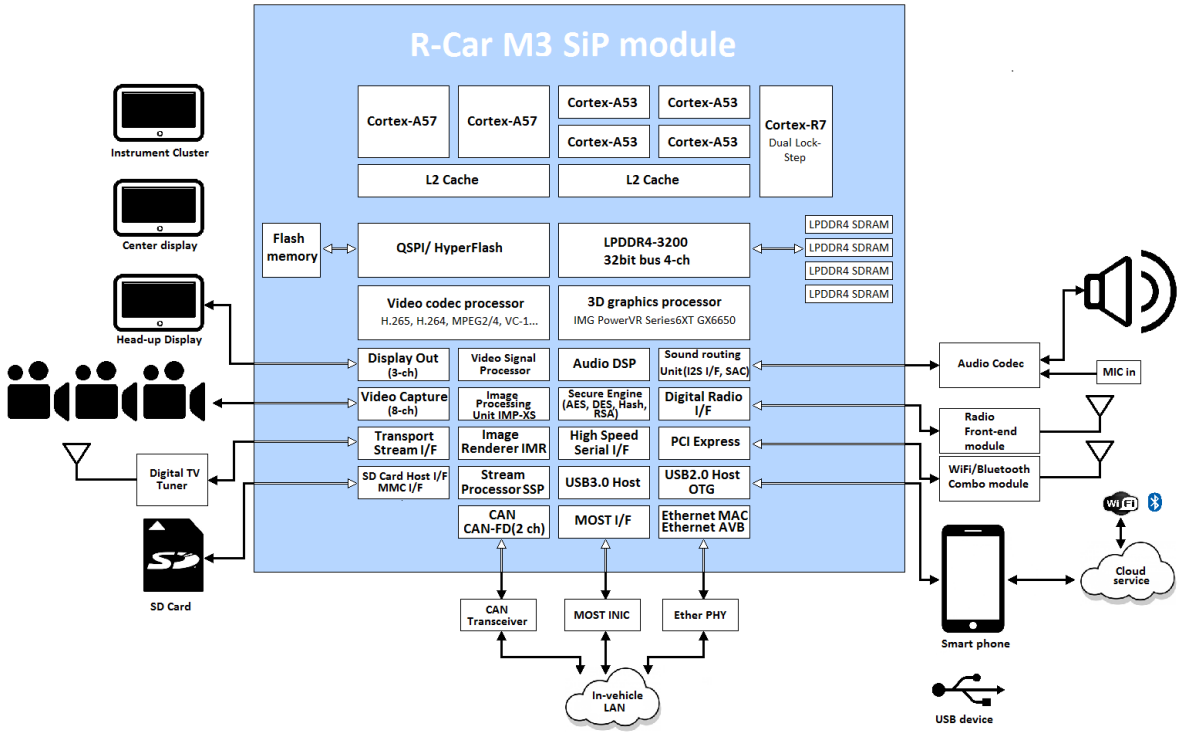

Figure 1: R-Car M3 System Block Diagram

5 DA9063-A and DA9224-A Description

The DA9063-A (Figure 2) is a high-current system PMIC suitable for dual- and quad-core processors that require up to 5 A core processor supply. The DA9063-A contains:

- Six DC-DC buck converters designed to use small external 1 µH inductors, capable of supplying in total up to 12 A continuous output current (0.3 V to 3.3 V). The buck converters do not require external Schottky diodes; they dynamically optimize their efficiency depending on the load-current using an Automatic Sleep Mode (ASM) and incorporate pin and software controlled Dynamic Voltage Control (DVC) to support processor load adaptive adjustment of the supply voltage. In addition BuckPro includes the facility to implement VTT memory bus termination if required.
- 11 SmartMirror™ programmable low-dropout (LDO) regulators rated up to 300 mA. All support remote capacitor placement and can operate from low 1.5 V/1.8 V input supplies. This allows these LDOs to be cascaded with (in other words: supplied by) a suitable buck supply to improve overall system efficiency.

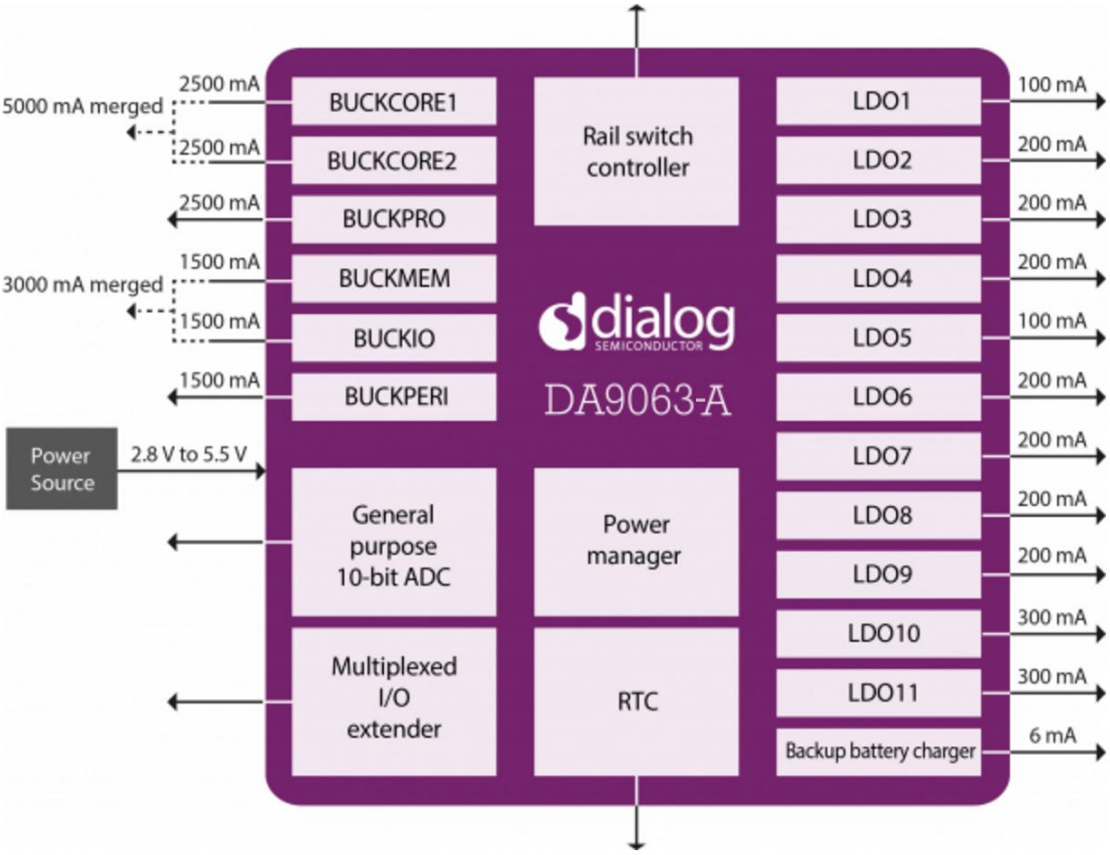

Figure 2: DA9063-A System Block Diagram

DA9063-A Power Management for Renesas R-Car M3 Platform

The DA9224-A (Figure 3) provides two, dual-phase synchronous step-down converters suitable for supplying CPUs that require high currents. The converter operates using a small external 0.22 µH inductor on each phase. It produces an output voltage in the range of 0.3 V to 1.57 V. The input voltage range of 2.8 V to 5.5 V makes it suited to a wide variety of low-voltage systems.

To guarantee the highest accuracy and support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented on each DA9224-A output.

Each DA9224-A buck operates with two phases and is capable of delivering up to 10 A continuous output current per buck.

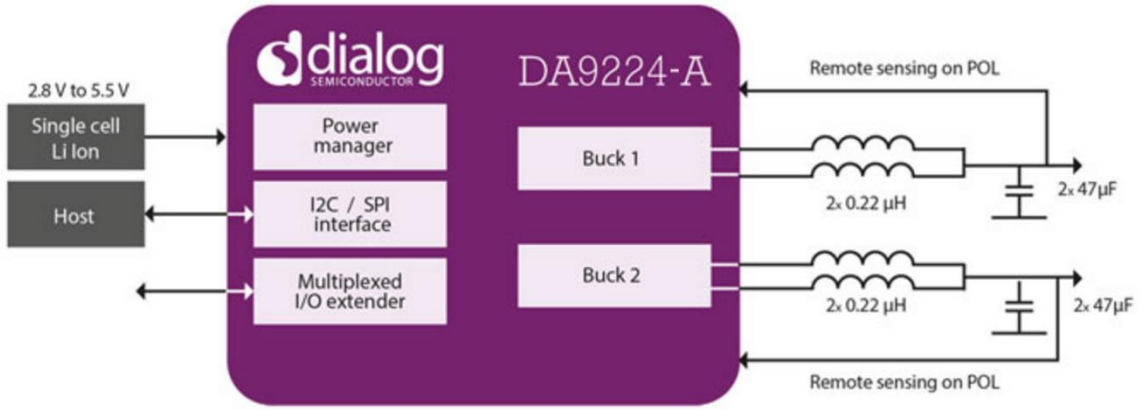

Figure 3: DA9224-A System Block Diagram

6 R-Car M3 SoC Power Requirements

Several power domains in the R-Car M3 SoC platform require precise voltage management for reliable system operation. The primary power domains are:

- VDD_DFVS
- VDD_08V
- DDR_1.1V
- DDR_1.8V

Other supplies will be required for peripherals, I/O interfaces, SD cards, and such. Additionally, the system power management must comply with the specific power-up and power-down sequence guidelines for the R-Car SoC (shown in Figure 4).

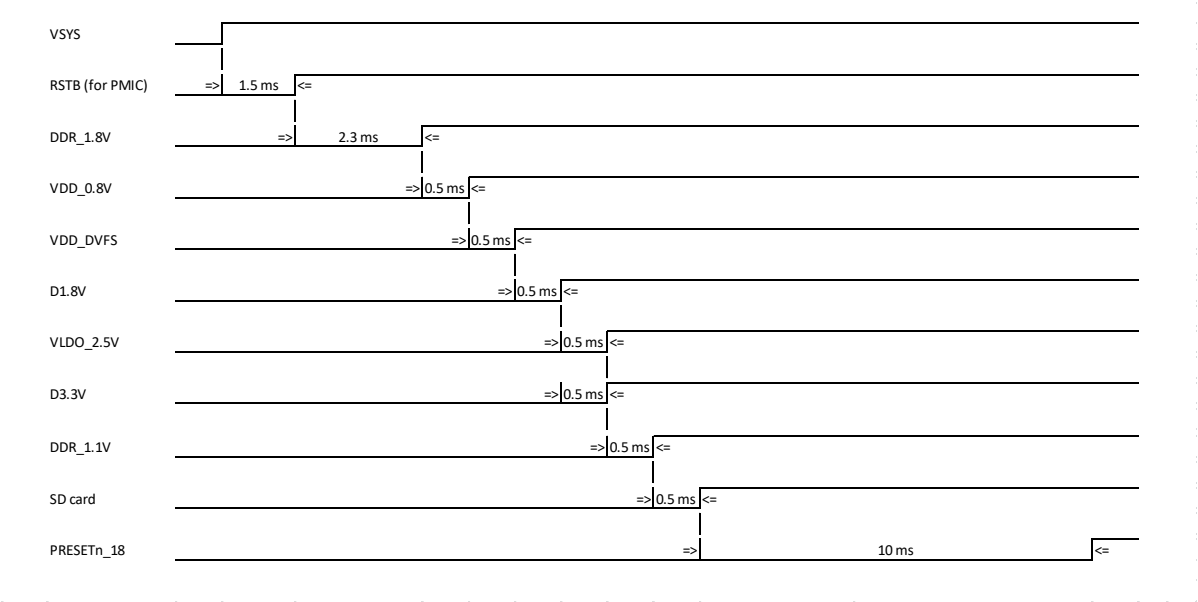

Figure 4: Start-Up Sequence (Timing is Not to Scale)

Figure 5 shows the PMIC interconnections that satisfies this requirement.

7 R-Car M3 SoC Power Tree System Diagram

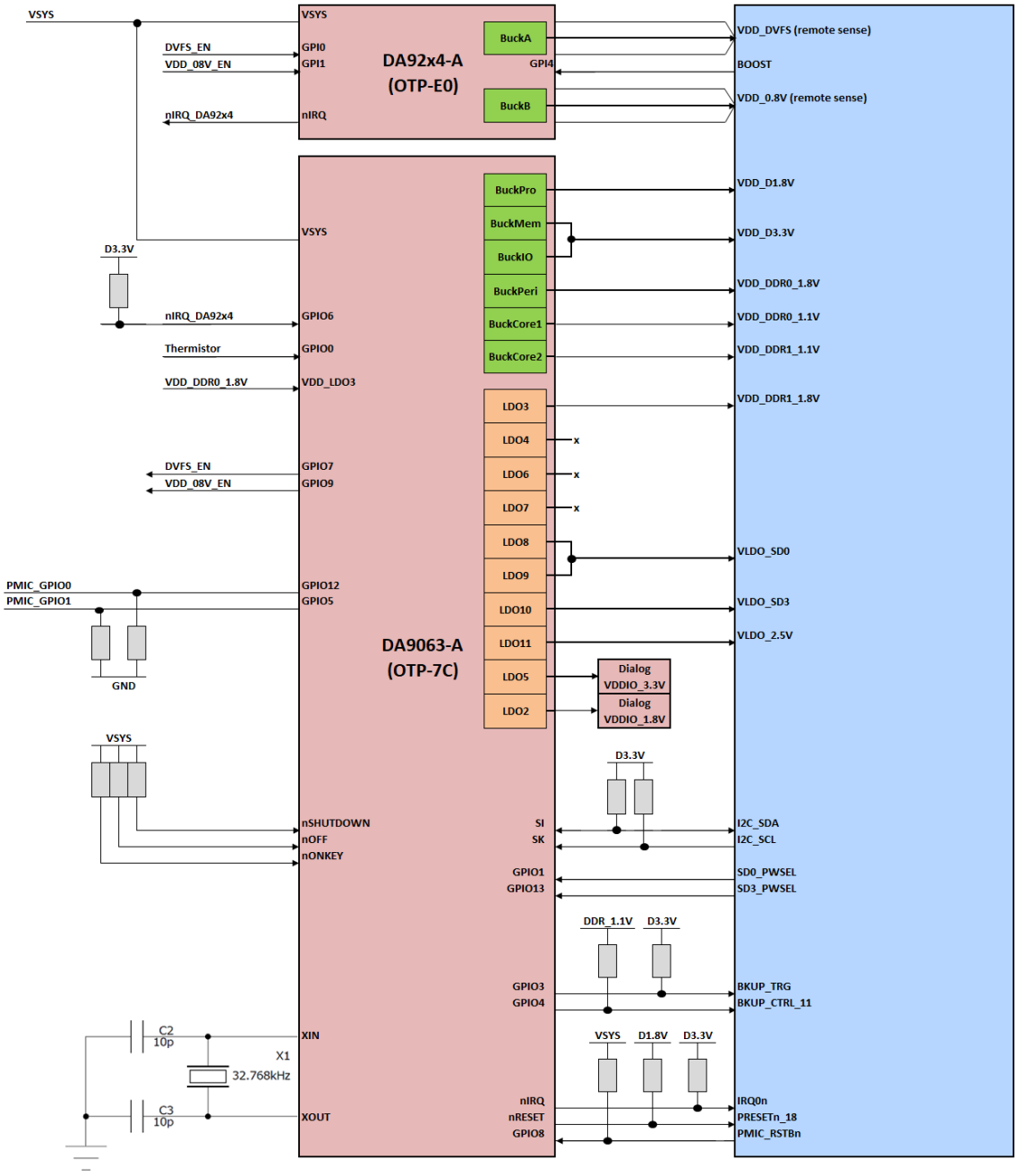

Figure 5: R-Car M3 and PMIC Interconnections

8 Cold Boot Sequence for R-Car M3

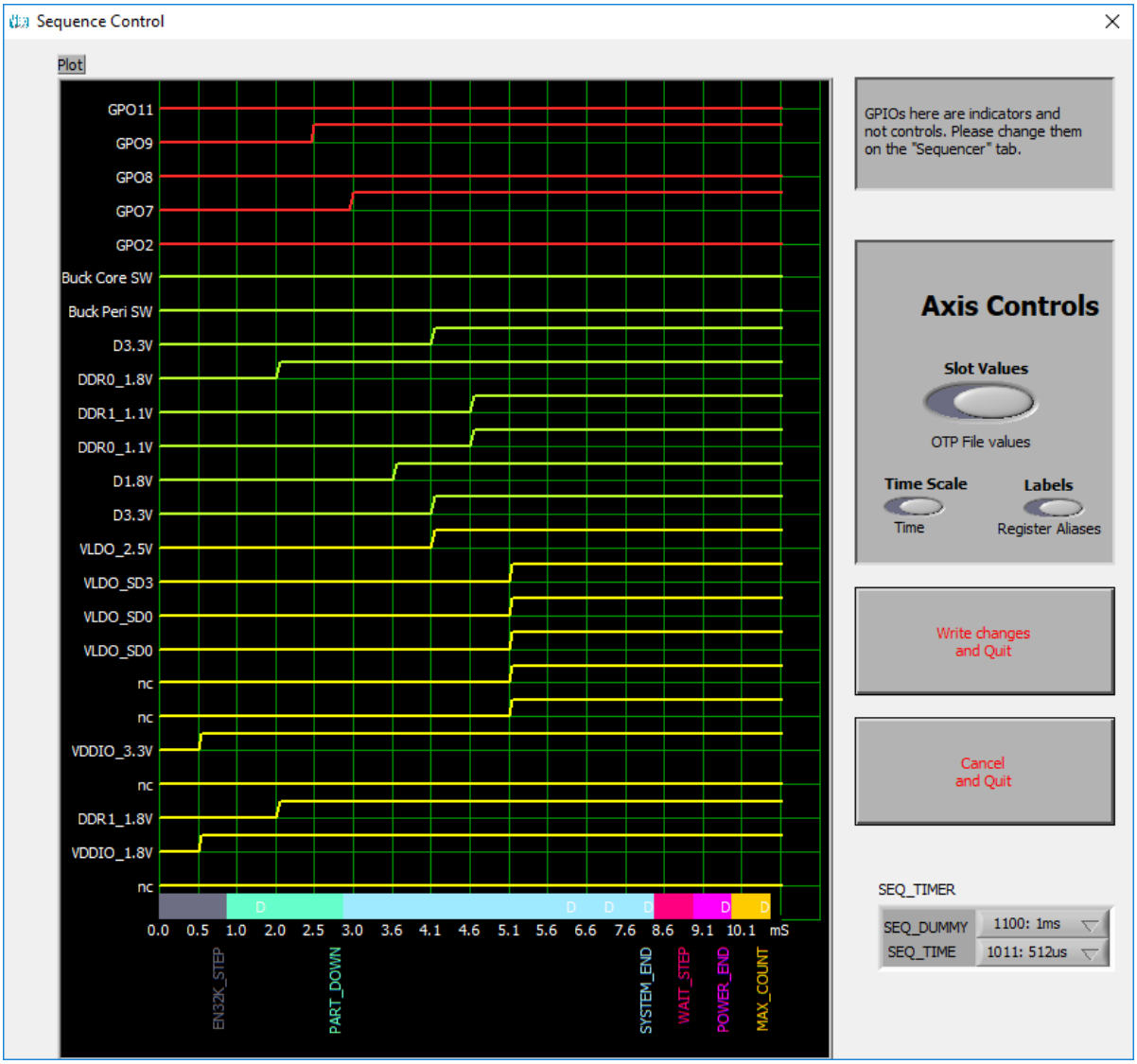

Figure 6: DA9063-7C-HO2-A Power-Up Sequence

Please contact your local Dialog representative for the recommended OTPs.

9 Operation

When 5 V is applied to the V_{SYS} supply the DA9063-A system PMIC starts up automatically. It follows the start-up sequence programmed in the OTP, enabling output power rails in the order specified. GPIO7 and 9 are configured to control the enabling of the two sub-PMIC bucks and are also part of the power sequencer timing. In this way the start-up timing of the sub-PMIC buck outputs are controlled.

Once the sequencer has completed the start-up sequence the nRESET signal from the DA9063-A is released to allow the SoC to start operation.

The outputs of LDO8 and LDO9 are combined to power SD0 card supply. LDO10 is a 300 mA LDO and can supply the SD3 card individually. If fewer SD cards are used in a customer end application or lower current SD cards are used then unused LDOs may be reused elsewhere in the end application.

GPIO1 and 13 provide the ability for the SoC to select respectively the SD0 and SD3 card output voltages by controlling the logic level applied to the GPIO input. A logic low from the SoC produces an SD card voltage of 1.8 V output on the respective output; a logic high produces an output of 3.3 V.

LDO5 is used to generate the internal power supplies for the Dialog system and sub-PMICs.

9.1 DVFS and AVS

The DVFS voltage is set in OTP to be the default start-up voltage that is guaranteed to ensure the system powers up and runs. Deviations in the manufacturing process result in some processors that are capable of operating from lower voltages than the nominal. AVS allows for adjustments to the DVFS voltage to cater for these processors.

The SoC can adjust the DVFS set voltage by an I^2C write to the DA9224-A, VBUCKA_CTRL_A register (address 0xD7). The output voltage can be adjusted in 10 mV steps.

The DVFS power rail can also be switched to a higher voltage for a short period of time. The higher voltage, BOOST mode is selected when the SoC takes the BOOST pin high.

The BOOST voltage is set in OTP to be the default boost voltage and can be adjusted by an I^2C write to the DA9224-A, VBUCKA_CTRL_B register (address 0xD8). The output voltage can be adjusted in 10 mV steps.

9.2 Memory Retention Mode (Sleep Mode)

PMIC_RSTBn from the SoC is used to enter and exit memory retention mode. When PMIC_RSTBn is taken to a logic low the system PMIC performs a power-down sequence. The SoC configures the bucks and LDO3 to remain on in memory retention mode.

Under normal ACTIVE mode conditions all bucks are programmed to operate in PWM mode to produce predictable noise performance. Efficiency is reduced at low load currents when operating in this mode so when entering memory retention mode the bucks supplying DDR1.1V and DDR1.8V are automatically changed to operate in Pulse-Frequency Modulation (PFM) mode. In doing this the quiescent current from the 5 V input is reduced to less than 1 mA.

When PMIC_RSTBn is taken to a logic high once more or a wake event occurs the DDR1.1V and DDR1.8V bucks are automatically re-configured to operate in Pulse-Width Modulation (PWM) mode before the system returns fully to ACTIVE mode by following the start-up sequence.

9.2.1 Warm Boot vs Cold Boot

Figure 8 shows the procedure for exiting from memory retention mode. Memory retention mode exit is triggered by a wake-up event. A wake-up event can be triggered from a wake-up enabled GPIO edge, nONKEY going low, the SYS_EN pin rising or an RTC alarm being triggered. The wake-up event causes the PMIC to move up the sequencer and then release nRESET to start the SoC. At this point the SoC will begin the software boot-up procedure.

During system boot-up the SoC checks the state of BKUP_TRG to determine if the start-up requires a cold or warm boot process. BKUP_TRG is programmed in OTP to be low during a system power-up to indicate a cold boot is required. Before entering memory retention mode the SoC sets BKUP_TRG to be high to indicate a warm boot is required when the system is next started. If all power is lost BKUP_TRG reverts to the OTP setting which results in a cold boot.

If the SoC GPIO, GP1-08, is connected to BKUP_TRG output pin on DA9063-A the SoC can directly determine the BKUP_TRG status by reading GP1-08.

If GP1-08 is not connected to BKUP_TRG the SoC can determine if a warm or cold boot is required by either reading BKUP_TRG status via an I^2C read of the DA9063-A.

Please refer to application note AN-PM-127 [3] for examples of the software implementation.

9.2.2 BKUP_CTRL

BKUP_CTRL is connected to DA9063 GPIO4. The SoC sets BKUP_CTRL when entering memory retention mode and clears it when exiting. Please refer to application note AN-PM-127 [3] for examples of the software implementation.

9.2.3 Sleep Timer

Taking PMIC_RSTBn high will result in a system wake-up event, with the PMIC following the power-up sequence.

An alternative approach is to use a sleep timer to wake the system after a predetermined time in memory retention mode.

This can be implemented on the Dialog power management solution by use of the RTC clock and RTC alarm function.

As before the SoC sets BKUP_TRG to be a logic high to indicate a warm boot when exiting sleep. Before entering sleep mode the SoC reads the RTC time within the DA9063-A. The SoC adds the required sleep interval to the RTC time and sets the DA9063-A alarm time to this new value. The SoC then sets the alarm to be active. Finally the SoC clears all interrupts before entering memory retention mode.

After the set time has elapsed the RTC alarm is triggered causing a wake-up event to be triggered within the DA9063-A. This causes the PMIC to move from memory retention mode to active waking up the SoC in the process.

The SoC checks BKUP_ TRG state and determines the wake-up event is a warm boot.

Figure 7 shows the process by which the SoC enters memory retention mode if required. Firstly the SoC determines whether the system is shutting down to off or memory retention mode. If memory retention mode is required the following sequence is followed:

- The SoC performs an I^2C write of 0xBB to PMIC register address 0x94.
- The SoC performs an I^2C write to set PMIC GPIO3 = 1
  - An alternative option is the SoC performs an I^2C write to set GP_ID_1 = 0x01
- If a wake from memory retention mode after a predetermined time is required the SoC performs an I^2C read of the RTC time, adds on the required sleep time and writes back an RTC ALARM time into the PMIC before setting the RTC ALARM_ON bit.
- The SoC sets the DDR into self-refresh mode before performing an I^2C write of 0x02 to register address 0x0E, thus clearing the SYSTEM_EN bit.

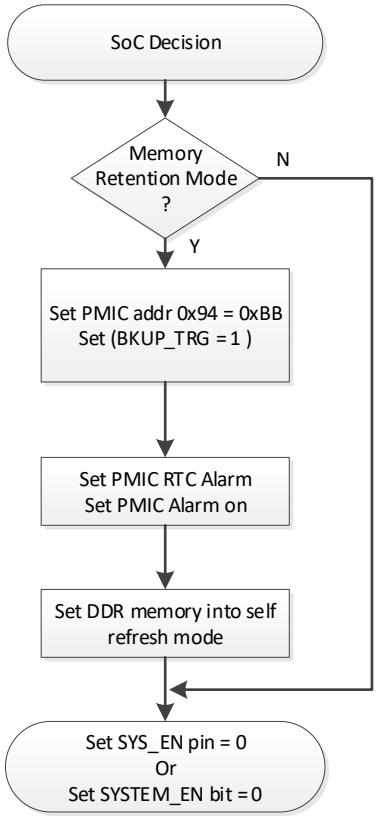

Figure 7: SoC Sequence for Memory Retention Entry

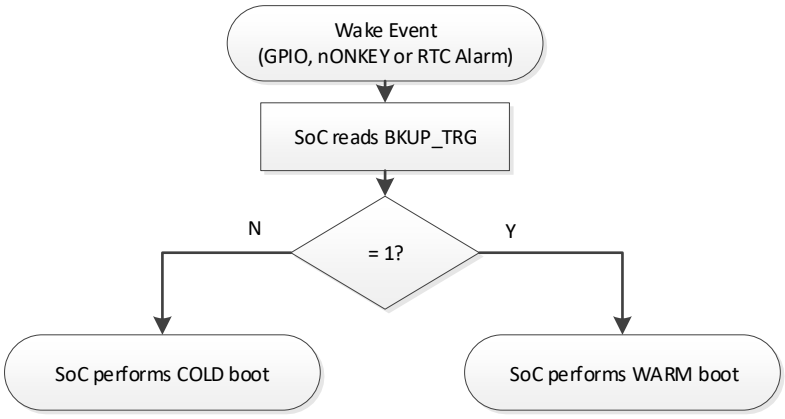

Figure 8: SoC Sequence for Memory Retention Exit

Please refer to application note AN-PM-127 [3] for examples of the software implementation.

9.3 Measurement Results

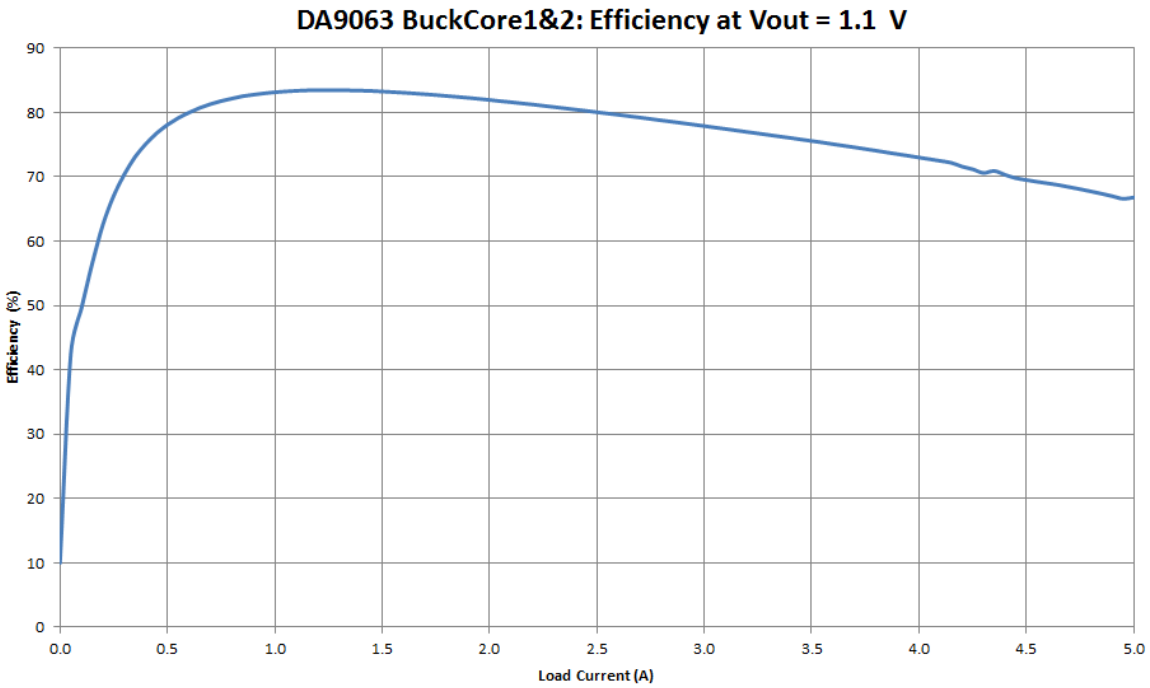

Figure 9: DDR_1.1V Efficiency

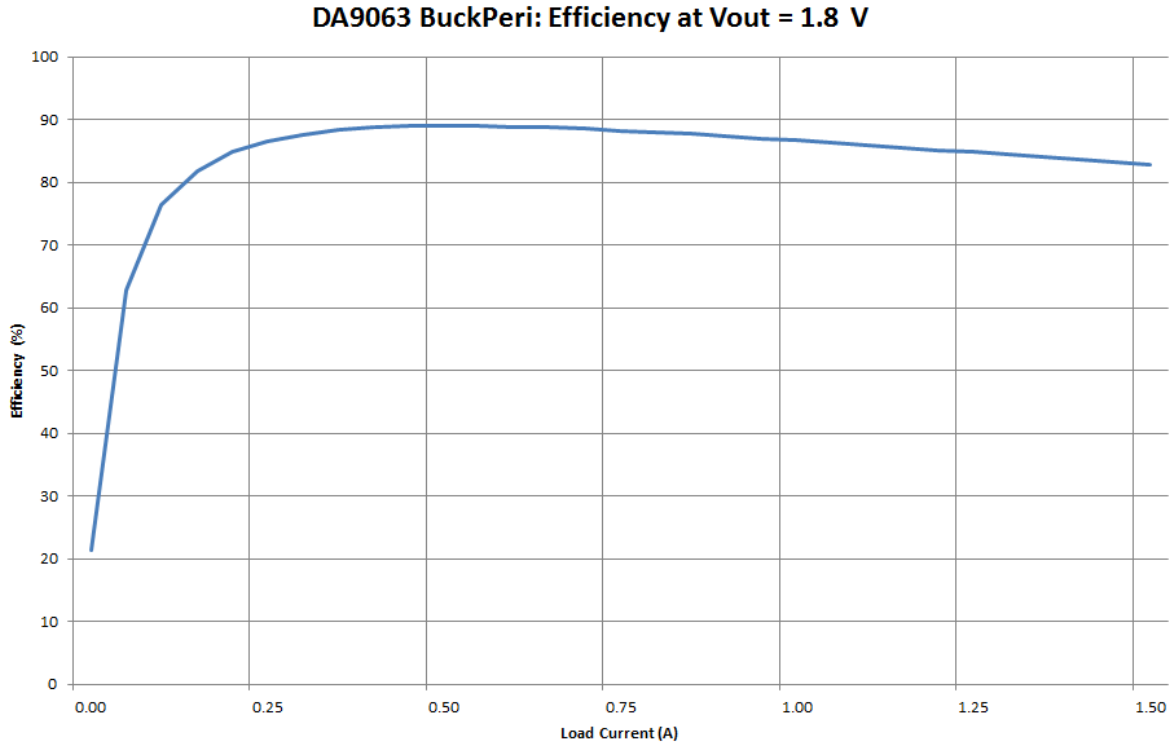

Figure 10: DDR_1.8V Efficiency

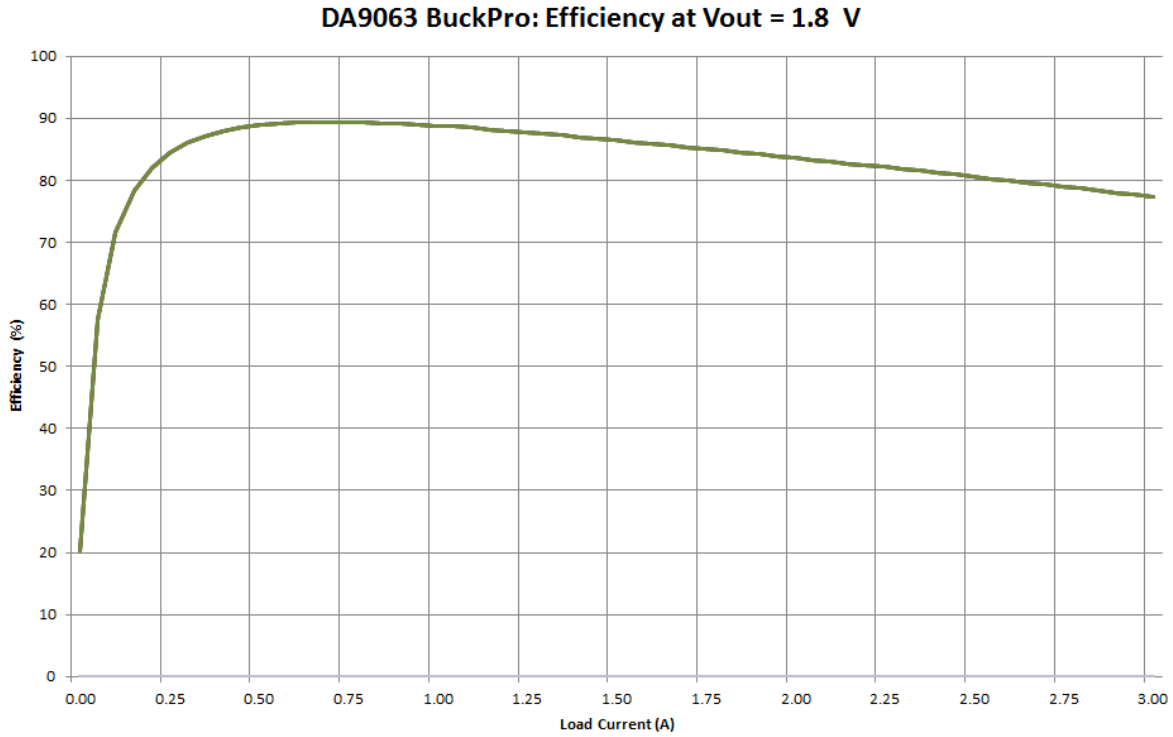

Figure 11: D1.8V Efficiency

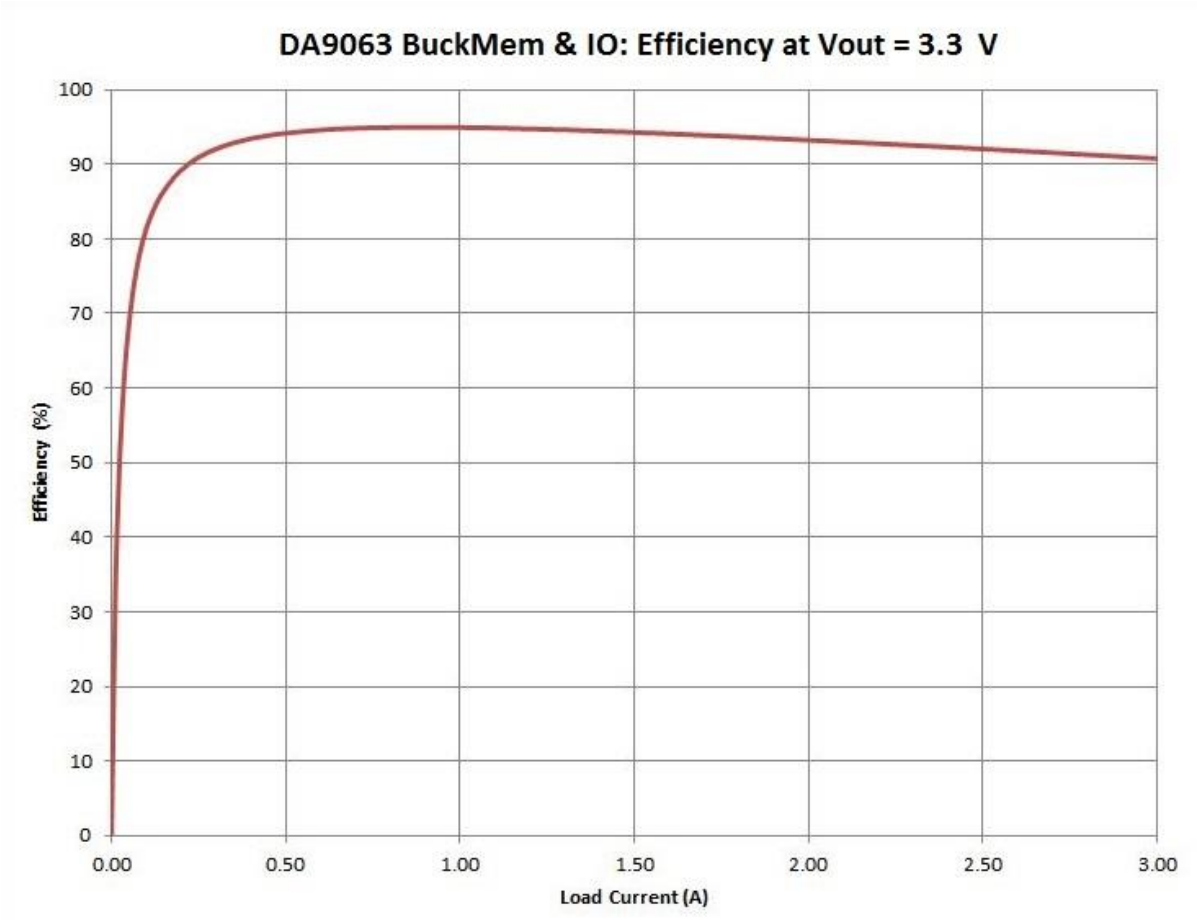

Figure 12: D3.3V Efficiency

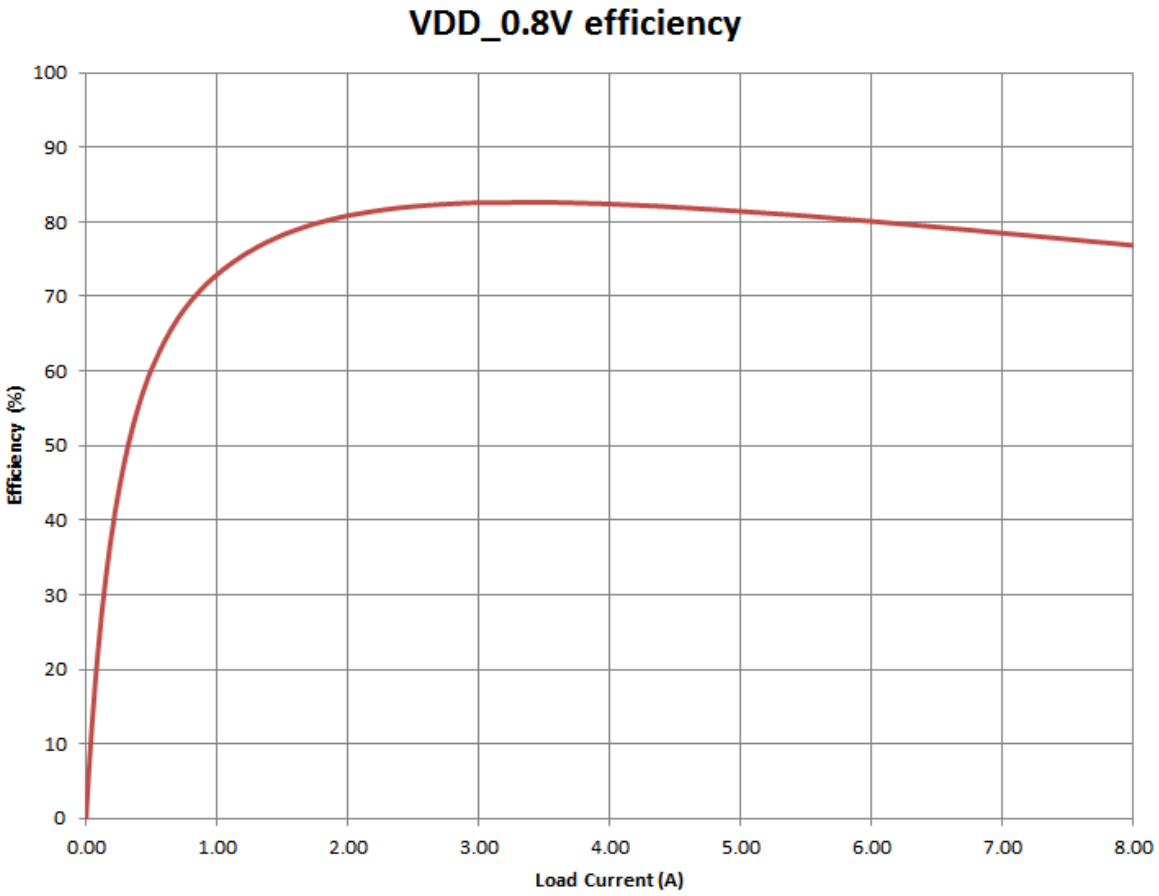

Figure 13: VDD_08 Efficiency

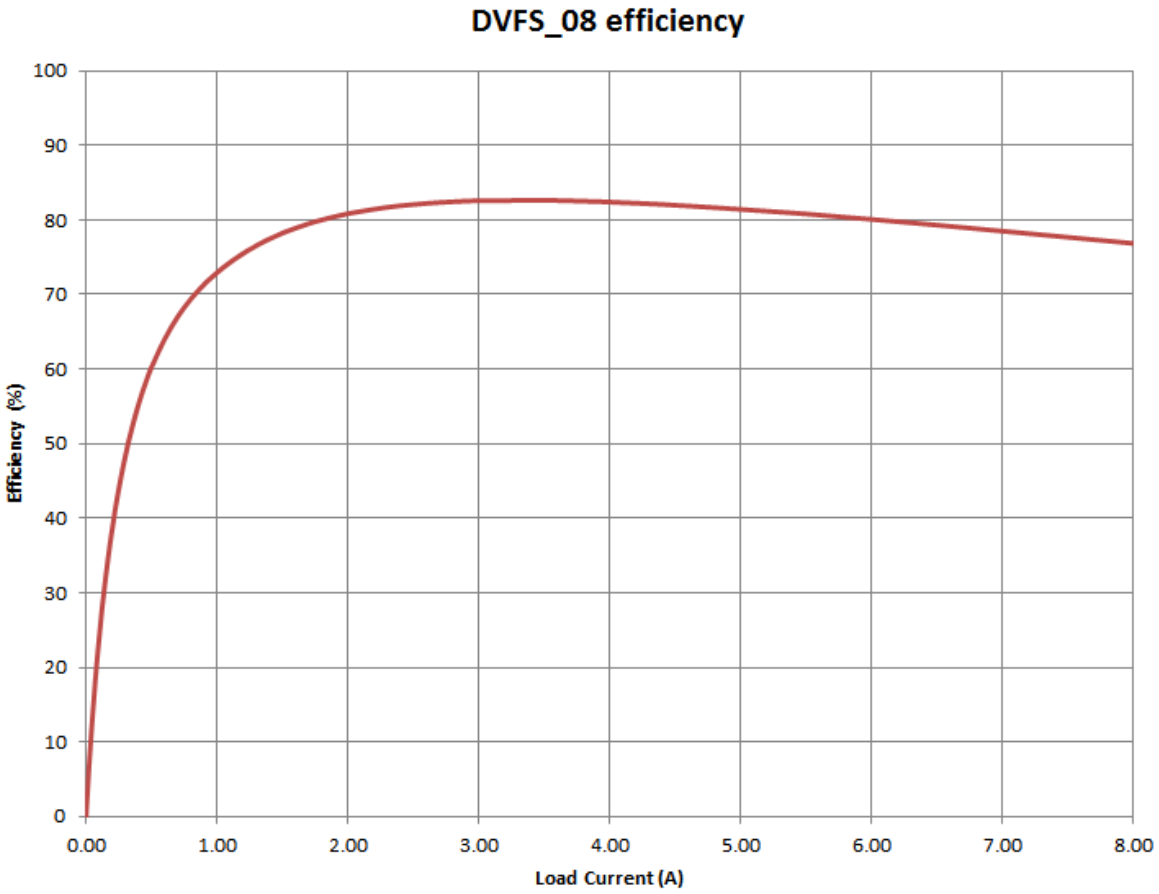

Figure 14: DVFS_08 Efficiency

Appendix A DA9063-7C-HO2-A Detailed Register Description

Key Settings

- Normal start-up
- Voltage monitor
- Buck Core1 and Buck Core2 dual phase mode.
- Buck Mem and Buck IO merged mode
- 2-wire control interface, standard speed
- RTC enabled
- LDO 4, 6, 7, 8, 9 and 10 are GPIO controlled by host for 1.8 V or 3.3 V SD card supply select

Table 1: DA9063-7C-HO2-A Register Settings

Register Address	Function	Register Value	Register Description
0x00A	IRQ_MASK_A	0x00	nONKEY, RTC, and some status IRQ masks
0x00B	IRQ_MASK_B	0x10	Charger wakeup and temperature, current, or voltage IRQ masks
0x00C	IRQ_MASK_C	0x00	GPI7 to 0 and ADCIN1-3 IRQ masks
0x00D	IRQ_MASK_D	0x00	GPI15 to 8 and external control signal IRQ masks
0x00E	CONTROL_A	0x07	PSM target status, companion charger control
0x00F	CONTROL_B	0x09	Power-down / -up signaling
0x010	CONTROL_C	0x5B	Debounce, boot, DVC, and DEF_SUPPLY control
0x011	CONTROL_D	0x68	Watchdog and LED blink control
0x012	CONTROL_E	0x04	RTC, feedback pins, V_LOCK
0x013	CONTROL_F	0x00	Watchdog reset, shutdown, and wakeup
0x014	PD_DIS	0x40	Disable / pause blocks when below the PSS sequencer PD_DIS slot
0x015	GPIO_0_1	0xDE	GPIO0 and 1 control
0x016	GPIO_2_3	0xED	GPIO2 and 3 control
0x017	GPIO_4_5	0xEE	GPIO4 and 5 control
0x018	GPIO_6_7	0xE9	GPIO6 and 7 control
0x019	GPIO_8_9	0xE4	GPIO8 and 9 control
0x01A	GPIO_10_11	0xCE	GPIO10 and 11 control
0x01B	GPIO_12_13	0xDF	GPIO12 and 13 control
0x01C	GPIO_14_15	0xEE	GPIO14 and 15 control registers
0x01D	GPIO_MODE0_7	0x80	GPIO0 to 7 mode control
0x01E	GPIO_MODE8_15	0x02	GPIO8 to 15 mode control
0x01F	SWITCH_CONT	0xB0	Rail switches
0x020	BCORE2_CONT	0x00	BUCKCORE2 control
0x021	BCORE1_CONT	0x00	BUCKCORE1 control
0x022	BPRO_CONT	0x00	BUCKPRO control
0x023	BMEM_CONT	0x00	BUCKMEM control
0x024	BIO_CONT	0x00	BUCKIO control
0x025	BPERI_CONT	0x00	BUCKPERI control

Register Address	Function	Register Value	Register Description
0x026	LDO1_CONT	0x00	LDO1 control
0x027	LDO2_CONT	0x80	LDO2 control
0x028	LDO3_CONT	0x00	LDO3 control
0x029	LDO4_CONT	0x00	LDO4 control
0x02A	LDO5_CONT	0x80	LDO5 control
0x02B	LDO6_CONT	0x00	LDO6 control
0x02C	LDO7_CONT	0x00	LDO7 control
0x02D	LDO8_CONT	0x20	LDO8 control
0x02E	LDO9_CONT	0x20	LDO9 control
0x02F	LDO10_CONT	0x60	LDO10 control
0x030	LDO11_CONT	0x00	LDO11 control
0x031	SUPPLIES	0x00	Vibrator output level
0x032	DVC_1	0x00	Dynamic voltage control
0x033	DVC_2	0x00	Dynamic voltage control
0x034	ADC_MAN	0x00	ADC manual and automatic measurement control
0x035	ADC_CONT	0x00	ADC automatic measurement control
0x036	VSYS_MON	0xAA	
0x083	ID_2_1	0x10	PSS sequence control
0x084	ID_4_3	0x03	PSS sequence control
0x085	ID_6_5	0x91	PSS sequence control
0x086	ID_8_7	0x99	PSS sequence control
0x087	ID_10_9	0x99	PSS sequence control
0x088	ID_12_11	0x07	PSS sequence control
0x089	ID_14_13	0x88	PSS sequence control
0x08A	ID_16_15	0x76	PSS sequence control
0x08B	ID_18_17	0x37	PSS sequence control
0x08C	ID_20_19	0x00	PSS sequence control
0x08D	ID_22_21	0x00	PSS sequence control
0x08E	ID_24_23	0x05	PSS sequence control
0x08F	ID_26_25	0x00	PSS sequence control
0x090	ID_28_27	0x04	PSS sequence control
0x091	ID_30_29	0x00	PSS sequence control
0x092	ID_32_31	0x10	PSS sequence control
0x095	SEQ_A	0xEA	PSS sequencer slot end points
0x096	SEQ_B	0x4F	PSS sequencer slot end points
0x097	WAIT	0x10	Power sequencer wait cycle
0x098	EN_32K	0xEA	RTC clocking control
0x099	RESET	0x88	Reset timer control

Register Address	Function	Register Value	Register Description
0x09A	BUCK_ILIM_A	0xFF	Buck current limit
0x09B	BUCK_ILIM_B	0xFF	Buck current limit
0x09C	BUCK_ILIM_C	0xFF	Buck current limit
0x09D	BCORE2_CFG	0x81	BUCKCORE2 control
0x09E	BCORE1_CFG	0x81	BUCKCORE1 control
0x09F	BPRO_CFG	0x81	BUCKPRO control
0x0A0	BIO_CFG	0x81	BUCKPRO control
0x0A1	BMEM_CFG	0x81	BUCKMEM control
0x0A2	BPERI_CFG	0x81	BUCKPERI control
0x0A3	VBCORE2_A	0x50	BUCKCORE2 voltage A
0x0A4	VBCORE1_A	0x50	BUCKCORE1 voltage A
0x0A5	VBPRO_A	0x7F	BUCKPRO voltage A
0x0A6	VBMEM_A	0x7D	BUCKMEM voltage A
0x0A7	VBIO_A	0x7D	BUCKIO voltage A
0x0A8	VBPERI_A	0x32	BUCKPERI voltage A
0x0A9	VLDO1_A	0x3C	LDO1 voltage A
0x0AA	VLDO2_A	0x3C	LDO2 voltage A
0x0AB	VLDO3_A	0x2D	LDO3 voltage A
0x0AC	VLDO4_A	0x78	LDO4 voltage A
0x0AD	VLDO5_A	0x32	LDO5 voltage A
0x0AE	VLDO6_A	0x32	LDO6 voltage A
0x0AF	VLDO7_A	0x32	LDO7 voltage A
0x0B0	VLDO8_A	0x32	LDO8 voltage A
0x0B1	VLDO9_A	0x32	LDO9 voltage A
0x0B2	VLDO10_A	0x32	LDO10 voltage A
0x0B3	VLDO11_A	0x22	LDO11 voltage A
0x0B4	VBCORE2_B	0x50	BUCKCORE2 voltage B
0x0B5	VBCORE1_B	0x50	BUCKCORE1 voltage B
0x0B6	VBPRO_B	0x7F	BUCKPRO voltage B
0x0B7	VBMEM_B	0x7D	BUCKMEM voltage B
0x0B8	VBIO_B	0x7D	BUCKIO voltage B
0x0B9	VBPERI_B	0x32	BUCKPERI voltage B
0x0BA	VLDO1_B	0x3C	LDO1 voltage B
0x0BB	VLDO2_B	0x3C	LDO2 voltage B
0x0BC	VLDO3_B	0x2D	LDO3 voltage B
0x0BD	VLDO4_B	0x2D	LDO4 voltage B
0x0BE	VLDO5_B	0x32	LDO5 voltage B
0x0BF	VLDO6_B	0x14	LDO6 voltage B

Register Address	Function	Register Value	Register Description
0x0C0	VLDO7_B	0x14	LDO7 voltage B
0x0C1	VLDO8_B	0x14	LDO8 voltage B
0x0C2	VLDO9_B	0x14	LDO9 voltage B
0x0C3	VLDO10_B	0x14	LDO10 voltage B
0x0C4	VLDO11_B	0x22	LDO11 voltage B
0x0C5	BBAT_CONT	0x00	Backup battery charger
0x0C6	GPO11_LED	0x00	High power GPO PWM
0x0C7	GPO14_LED	0x00	High power GPO PWM
0x0C8	GPO15_LED	0x00	High power GPO PWM
0x0C9	ADC_CFG	0x00	ADC automatic measurement control
0x0CA	AUTO1_HIGH	0x00	ADC measurement thresholds
0x0CB	AUTO1_LOW	0x00	ADC measurement thresholds
0x0CC	AUTO2_HIGH	0x00	ADC measurement thresholds
0x0CD	AUTO2_LOW	0x00	ADC measurement thresholds
0x0CE	AUTO3_HIGH	0x00	ADC measurement thresholds
0x0CF	AUTO3_LOW	0x00	ADC measurement thresholds
0x105	INTERFACE	0xB9	Host interfaces
0x106	CONFIG_A	0x84	Host interfaces and other IOs
0x107	CONFIG_B	0x7F	VDD_FAULT comparator
0x108	CONFIG_C	0x50	Buck duty cycle and clock polarity
0x109	CONFIG_D	0x00	
0x10A	CONFIG_E	0Xff	BUCK and rail switch default settings
0x10B	CONFIG_F	0x07	LDO default and bypass mode settings
0x10C	CONFIG_G	0xFF	LDO default settings
0x10D	CONFIG_H	0xF0	
0x10E	CONFIG_I	0x04	
0x10F	CONFIG_J	0xE3	
0x110	CONFIG_K	0x02	GPIO pull resistors
0x111	CONFIG_L	0x20	GPIO pull resistors
0x112	CONFIG_M	0x00	
0x113	CONFIG_N	0x00	
0x114	MON_REG_1	0x88	
0x115	MON_REG_2	0x00	
0x116	MON_REG_3	0x00	
0x117	MON_REG_4	0x00	
0x121	GP_ID_0	0x03	
0x122	GP_ID_1	0x00	
0x123	GP_ID_2	0x00	

Register Address	Function	Register Value	Register Description
0x124	GP_ID_3	0x00	
0x125	GP_ID_4	0x00	
0x126	GP_ID_5	0x00	
0x127	GP_ID_6	0x00	
0x128	GP_ID_7	0x00	
0x129	GP_ID_8	0x00	
0x12A	GP_ID_9	0x00	
0x12B	GP_ID_10	0x00	
0x12C	GP_ID_11	0x00	
0x12D	GP_ID_12	0x00	
0x12E	GP_ID_13	0x00	
0x12F	GP_ID_14	0x00	
0x130	GP_ID_15	0x00	
0x131	GP_ID_16	0x00	
0x132	GP_ID_17	0x00	
0x133	GP_ID_18	0x00	
0x134	GP_ID_19	0x00	
0x183	CUSTOMER_ID	0x02	Chip ID
0x184	CONFIG_ID	0x7C	Customer ID

Revision History

Revision	Date	Description
1.0	25-Oct-2017	Initial version.
2.0	19-Jan-2018	Update to memory retention mode
3.0	12-Feb-2018	Software implementation of memory retention mode
4.0	17-Jan-2019	Update to memory retention mode
5.0	25-Feb-2022	File was rebranded with new logo, copyright and disclaimer

DA9063-A Power Management for Renesas R-Car M3 Platform

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Status	Definition
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