Application Note

DA9063 / i.MX 6Dual/Quad/Quad+ Power Connections

AN-PM-027

Abstract

This document outlines the required connectivity between the DA9063 Power Management Integrated Circuit (PMIC) and the NXP i.MX 6Dual, Quad or Quad+ system application processors.

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1 Terms and Definitions

ASM	Automatic Sleep Mode
BSP	Board Support Package
BOM	Bill of Materials
GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
DVC	Dynamic Voltage Control
POR	Power on Reset
HW	Hardware
SoC	System on (a) chip
SW	Software

2 References

[1] NXP i.MX 6Dual/Quad Automotive and Infotainment Application Processors, Datasheet

[2] NXP i.MX 6Dual/Quad Power Consumption Measurement, AN4509

[3] NXP i.MX 6Dual/Quad Application Processor Reference Manual, I.MX 6DQRM

[4] NXP i.MX 6DQ6SDLHDG Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors

[5] AN4509 i.MX 6Dual/6Quad Power Consumption Measurement

[6] DA9063 Datasheet, https://support.diasemi.com/

[7] SABRE Board for Smart Devices Based on the NXP i.MX 6 Series (schematic SCH-27516 PDF: SPF-27516)

[8] NXP i.MX 6Q to DA9063 Interconnections ver. C, Schematic

[9] NXP i.MX 6Q to DA9063 Interconnection, BOM

[10] Performance DB Separate Bucks 44-179-176-07-A, Schematic

[11] DA9063 Motherboard 44-179-176-05-A.sch, Schematic

[12] DA9063_FSL_MCIMX6Q-SDB_Android_IMX6_R13.41_1r0

3 Introduction

The NXP i.MX 6 series multimedia processor family is based on an ARM®Cortex™-A9 architecture, with dual and quad core, that requires a dedicated power management solution for a stable and reliable system platform.

The power requirements can vary dependent not only on the processor type (for example, dual or quad core) but also on the user application and use cases.

This application note analyzes the power requirements for each of the following:

- Quad core
- Dual core

The DA9063 PMIC is a highly integrated chip that supports the Dynamic Voltage Control (DVC) technology, enabling significant power savings by intelligently managing voltage changes similar to the technology used in many processors. As a result of its highly integrated features, the DA9063 PMIC reduces overall system cost and size significantly when compared to an equivalent discrete solution. This document addresses only the power supply related features; addressing all of the features and functions of the optimized PMIC is beyond the scope of this document.

For further information about Dialog PMIC solutions for NXP SoCs, please refer to:

https://www.dialog-semiconductor.com/power-solutions-nxpr-imx-application-processor-family

NOTE
Since this document was created Freescale™ has been acquired by NXP™. All references to Freescale™ now apply to NXP™

3.1 Purpose

This document describes:

- the DA9063 PMIC and its power capabilities
- the NXP i.MX 6Dual/Quad power requirements
- the interconnections between the DA9063 PMIC and the NXP i.MX 6Dual/Quad application processor
- recommended components

4 DA9063 Description

DA9063 is a high current system PMIC suitable for dual and quad core processors used in smartphones, tablets, ultra-books, embedded and other handheld applications that require up to 5 A core processor supply current.

DA9063 contains 6 DC-DC buck converters designed for small external 1 µH inductors capable of supplying in total up to 12 A continuous output current (0.3 V to 3.3 V). The buck converters do not require external Schottky diodes, dynamically optimize their efficiency depending on the load current using an Automatic Sleep Mode (ASM) and incorporate Dynamic Voltage Control (DVC) to support processor load adaptive adjustment of the supply voltage.

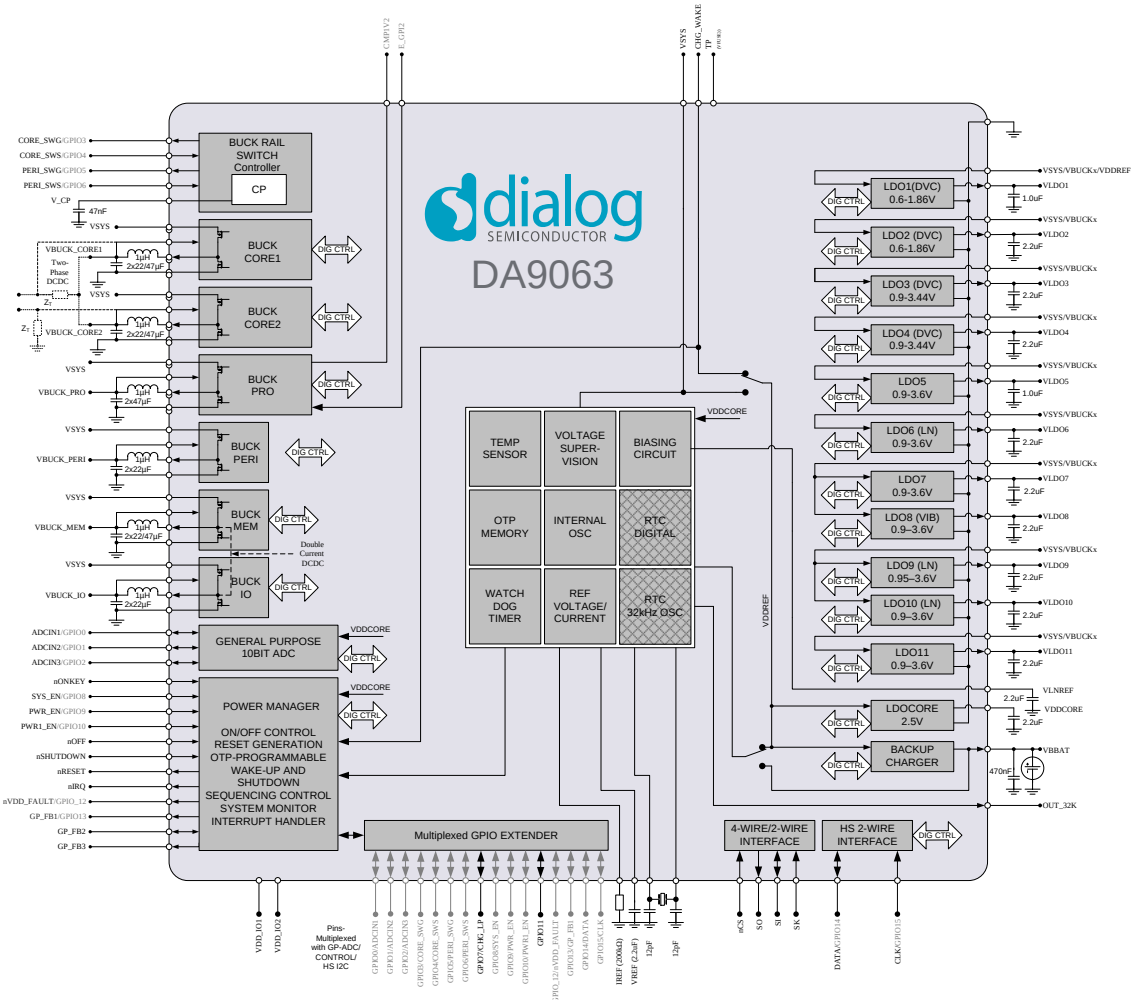

Figure 1: DA9063 System Block Diagram

5 NXP i.MX 6Dual/Quad Application Processor Family Description

The NXP i.MX 6Dual/Quad application processor is an advanced, highly integrated platform for multimedia-centric devices.

Figure 2 (courtesy of NXP [3].) shows a system block diagram of an i.MX 6Dual/Quad processor system and the internal functional modules.

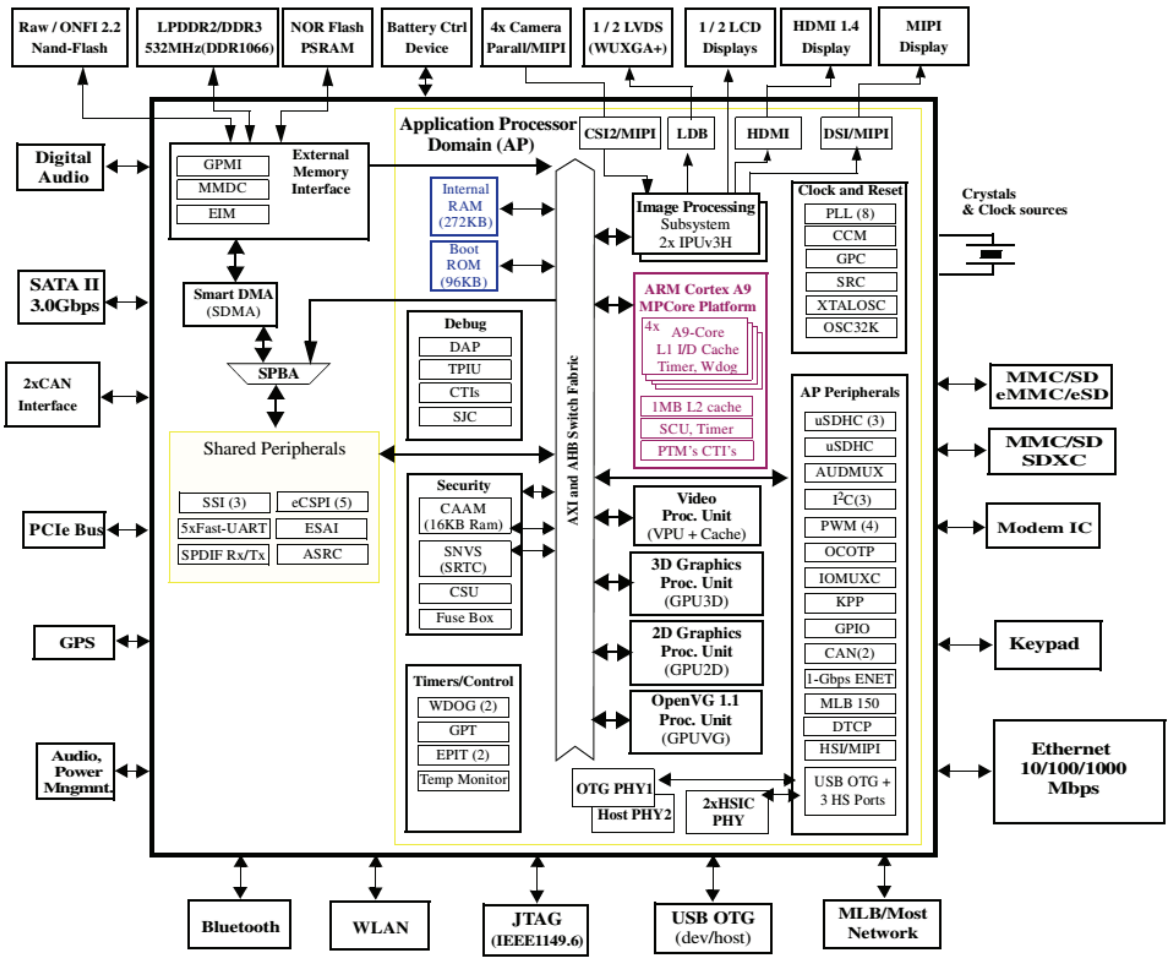

Figure 2: NXP i.MX 6Dual/Quad System Block Diagram

6 NXP i.MX 6 Family Power Requirements

Several power domains can be identified on an i.MX 6 processor all requiring precise power management for reliable system operation.

The solution for a quad core based system can be scaled down for use with other devices in the i.MX 6 family that contain fewer cores.

The primary power domains required for the i.MX 6Quad core device are as follows:

VDDARM_IN: supplies the internal ARM cores

VDDSOC_IN: supplies the internal peripherals

VDDHIGH_IN: supplies PLLs, DDR pre-drivers, PHYs and miscellaneous circuitry

VDD_SNVS_IN: supplies the SNVS regulator for the RTC and SNVS (Secure Non Volatile Storage)

Additional supplies may be required for DDR3 memory, peripherals, I/O interfaces, USB, etc.

The overall power management system must comply with the specific power up and power down sequence guidelines. In particular the following restrictions need to be considered for the power up and power down sequences with regards the correct programming of a PMIC.

6.1 POWER-UP Sequence

VDD_SNVS_IN:

Always on (for example, from a coin cell) or must be turned on before any other supply.

VDDSOC_IN, VDDARM_IN

Enable both at the same time or if generated from independent supplies, apply first VDDSOC_IN and then VDDARM_IN with a delay no longer than 1 ms.

POR_B

Reset from the PMIC to the i.MX 6. This is to be asserted immediately at power up and released after the last supply reaches its stable voltage level.

USB_OTG_VBUS, USB_H1_VBUS

USB specific supplies which are not required to be included in the power up sequence control.

6.2 POWER-DOWN Sequence

No specific requirements.

Other specific restrictions for other supplies can be found in detail in [1].

6.3 Typical Use Case Current Consumption

In general, current consumption levels are very dependent on the use cases. In this application note, it assumes a typical current consumption requirement specific for the NXP SABRE board running Linux/Android.

Table 1 lists typical current values extracted from the table in the NXP SABRE schematic [7].

Table 1: Primary Supply Requirements (RUN mode)

Power Supply Rail	Operating Voltage (V)	Typical Current (mA)
VDDCORE	1.38	2155
VDDSOC	1.38	1590
VDDHIGH_IN	2.78	75
DDR_1V5	1.50	1500
AUX_3V15	3.15	200
GEN_3V3	3.30	653

Other rail current requirements will also depend on the system hardware architecture and use cases.

For other modes of operation and use cases, please refer to the NXP Application Note [5].

7 NXP i.MX 6Dual/Quad Power Supply Rails

Table 2 summarizes the supply rails of the NXP i.MX 6Dual/Quad processor and the corresponding regulator outputs from the DA9063 device to connect to. Sequencer slots are defined relatively to each other.

Table 2: NXP i.MX 6Quad/Dual Power Supply Rails/ DA9063 PMIC

I.MX 6Q/D Power Supply Rail	i.MX 6Q/D Voltage Range (V)	DA9063	Sequencer Slot	DA9063 Nominal Output Voltage (Note 1) (V)	DA9063 Max Current (mA)	i.MX 6 Current (Note 2) Requirement (mA)	Notes
Run mode: LDO enabled VDDARM_IN Run mode: LDO enabled VDDARM23_IN	1.05 V to 1.5 V (LDO Output Set Point (VDDARM_CAP Note 4) of 0.925 V minimum for operating up to 396 MHz) 1.25 V to 1.5 V (LDO output Set Point (VDDARM_CAP Note 3) of 1.125 V minimum for operating up to 792 MHz) 1.35 V to 1.5 V (LDO Output Set Point (VDDARM_CAP Note 3) of 1.225 V minimum for operating up to 852 MHz or 996 MHz)	BUCKCORE1	1	1.38	1250/ 2500 (OD mode)	2155	QUAD core operation: short together DUAL operation: Connect power to VDDARM_IN. Connect VDDARM23_IN to GND
Run mode: LDO enabled VDDSOC_IN Note 5	1.275 V Note 6 to 1.5 V (VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) require 1.15 V minimum.) 1.350 V Note 5 to 1.5 V (264 MHz < VPU < 352 MHz; VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) require 1.225 V minimum.)	BUCKCORE2	1	1.38	1250/ 2500 (OD mode)	1590	
VDDHIGH_IN Note 7, Note 8	2.8 V to 3.3 V	LDO11	11	2.8	300	75	
VDD_SNVS_IN Note 6	2.8 V to 3.3 V	VBBAT	0	2.8	6		

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I.MX 6Q/D Power Supply Rail	i.MX 6Q/D Voltage Range (V)	DA9063	Sequencer Slot	DA9063 Nominal Output Voltage (Note 1) (V)	DA9063 Max Current (mA)	i.MX 6 Current (Note 2) Requirement (mA)	Notes
NVCC_DRAM	1.14 V to 1.30 V (LPDDR2, DDR3U) 1.425 V to 1.575 V (DDR3) 1.283 V to 1.45 V (DDR3L)	BUCKPRO	3	1.5	1250/ 2500 (OD Mode)	1500	Set to 1.5 as DDR3 are used.
NVCC_RGMII	1.65 V to 3.6 V						
NVCC_LCD, NVCC_NANDF, NVCC_SD2, NVCC_SD310	1.65 V to 3.6 V	BUCKPERI	5	3.3	1500	653	Depends on system architecture. These rails may require different supplies. Refer to [1] for details.
NVCC_ENET10	1.65 V to 3.6 V						
NVCC_EIM0, NVCC_EIM1, NVCC_EIM210	1.65 V to 3.6 V						
NVCC_SCI, NVCC_SD110	1.65 V to 3.6 V						
NVCC_GPIO, NVCC_JTAG10	1.65 V to 3.6 V						

Note 1 Supply values are defined as Vmin + 3% accuracy.

Note 2 Current values based on Table 1.

Note 3 VDDARM_IN and VDDSOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

Note 4 VDDARM_CAP must not exceed VDD_CACHE_CAP by more than 50 mV. VDD_CACHE_CAP must not exceed VDDARM_CAP by more than 200 mV.

Note 5 VDDSOC_CAP and VDDPU_CAP must be equal.

Note 6 VDDSOC and VDDPU output voltages must be set according to this rule: VDDARM - VDDSOC/PU < 50 mV.

Note 7 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (I.MX 6DQ6SDLHDG).

Note 8 Must match the range of voltages that the rechargeable backup battery supports.

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Several i.MX 6Q/D supply interfaces are generated by internal regulators as described in Table 3.

Table 3: External Interface Supplies

Power Supply Rail	Operating Voltage (V)	i.MX 6Q/D	Sequencer Slot	Nominal Output Voltage Note 1 (V)	Notes
NVCC_LVDS2P5 Note 2 , NVCC_MIPI	2.25 V to 2.75 V	VDDHIGH_CAP1/2	NA	2.5	
HDMI_VP	0.99 V to 1.3 V	VDDSOC_CAP1...7	NA	1.1	
HDMI_VPH	2.25 V to 2.75 V	VDDHIGH_CAP1/2	NA	2.5	
PCIE_VP	1.023 V to 1.3 V	VDDSOC_CAP1...7	NA	1.1	
PCIE_VPH	2.325 V to 2.75 V	VDDHIGH_CAP1/2	NA	2.5	
PCIE_VPTX	1.023 V to 1.3 V	VDDSOC_CAP1...7	NA	1.1	
SATA_VP	0.99 V to 1.3 V	VDDSOC_CAP1...7	NA	1.1	
SATA_VPH	2.25 V to 2.75 V	VDDHIGH_CAP1/2	NA	2.5	

Note 1 Supply values are defined as Vmin + 3 % accuracy.

Note 2 This supply also powers the pre-drivers of the DDR I/O pins; therefore, it must always be provided, even when LVDS is not used.

Other supplies used within the SABRE boards for various on board interfaces are shown in Table 4.

Table 4: SABRE Board Interface Supplies

Power Supply Rail	Operating Voltage (V)	DA9063	Sequencer Slot	DA9063 Nominal Output Voltage Note 1 (V)	DA9063 Max Supplied Current (mA)	Typ. Current Requirement (mA)	Notes
VGEN1_1V5	1.5	LDO6	11	1.5	200	100	
VGEN2_1V5	1.5	LDO8	12	1.5	200	250	
VGEN3_2V5	2.8	LDO5	13	2.8	100	70	
VGEN4_1V8	1.8	LDO10	9	1.8	300	310	
VGEN6_3V3	3.3	LDO7	10	3.3	200	160	

Note 1 Supply values are defined as Vmin + 3 % accuracy.

8 Application

To demonstrate the correct operation of the i.MX 6Quad processor with the DA9063, a NXP SABRE Development Platform (MCIMX6Q-SDB) with touchscreen was modified. The original NXP PF0100 PMIC was removed and replaced with the Dialog DA9063, connecting each of the power rails as described later in this document.

Figure 3 shows the interconnection used to implement a working system in conjunction with the DA9063 BSP patch release for the Android: NXP i.MX 6Q MCI.MX 6Q-SDB Board [12].

Schematic references for this application are:

- [7] MCIMX6Q-Smart Device Board (Source:SCH-27516 PDF:SPF-27516)
- [10] DA9063 Performance DB Separate Bucks 44-179-176-07-A
- [11] DA9063 motherboard 44-179-176-05-A.sch
- [8] NXP i.MX 6Q to DA9063 interconnection ver. C, schematic

For clarity, Figure 3 and the schematic [8] use the same net names as the NXP schematic [7]. Care must be taken not to confuse different nets that have the same net name VDDCORE in the schematic [7] and the DA9063: The DA9063 VDDCORE is the name of the internal LDOCORE output and its power net is called PMIC_VDDCORE; in the NXP schematic [7] VDDCORE is a power net name and connects to DA9063 BUCKCORE1, see Figure 4.

To achieve a working platform environment, the DA9063 must be configured with the proper power up sequence to comply with the i.MX 6Q/D processor requirements as described in Section 6.1.

This power up sequence has been implemented in the DA9063-82 and -83 OTP variants only. For further information, please contact your local Dialog Sales Office.

For further information please refer to [7], [10], and [11].

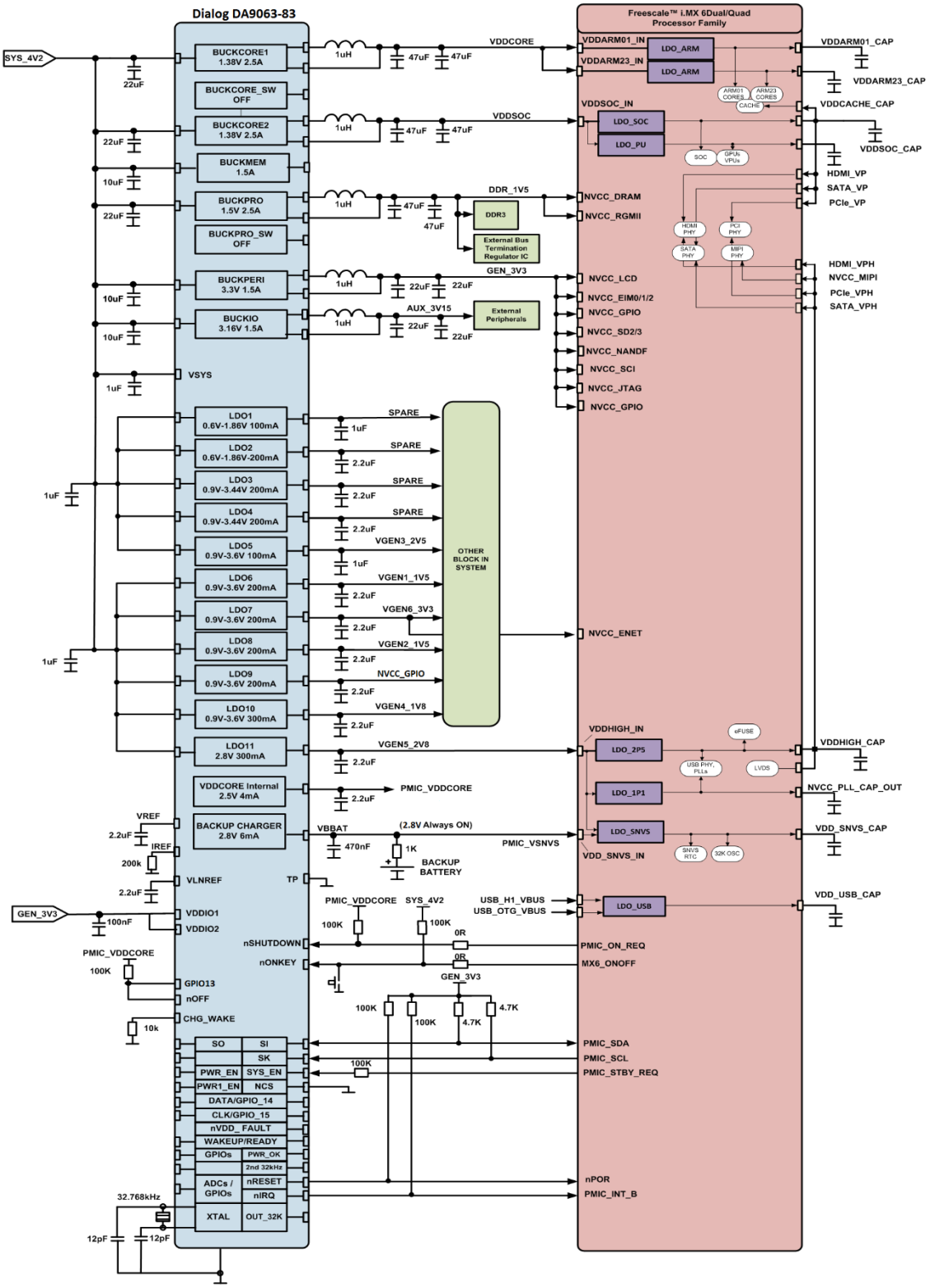

Figure 3: Application Diagram Example

DA9063 / i.MX 6Dual/Quad/Quad+ Power Connections

8.1 Input Source Supply

The input supply to the system is +5 V supplied from an external mains adapter (5V_DC_JACK) from which all the other supplies are derived:

- 5V_IN
- SYS_4V2
- PMIC_5V
- AUX_5V

The AUX_5 V supply on the SABRE board is generated via a boost converter from the SYS_4V2. This supply is not required when using a DA9063 PMIC. In fact, while the nominal main chip supply of the PF0100 is 4.5 V, the DA9063 can operate at +5 V and requires no pre-regulation. This allows a cost reduction due to a reduced overall Bill of Materials.

8.2 Core and SOC Power Supplies

BUCKCORE1 and BUCKCORE2 are used to supply the VDDARM_IN and VDDSOC_IN power rails (Figure 4).

The current demand on these rails is highly dependent on the CPU load (application use case dependent). To allow the max output current up to 2.5 A both bucks are used in overdrive mode.

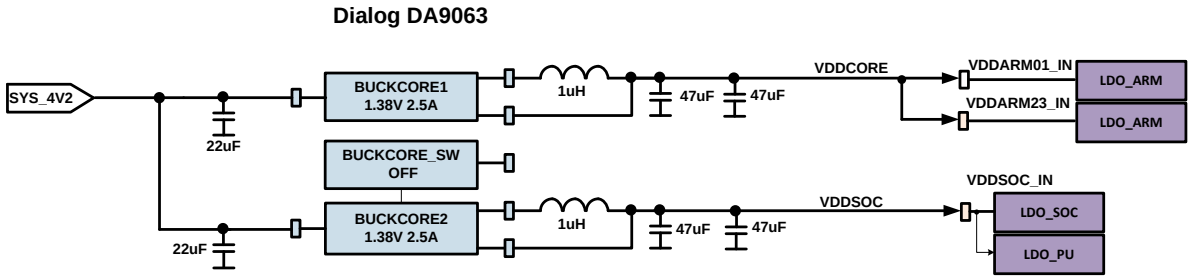

Figure 4: VDDARM_IN and VDDSOC_IN Rail Supplies

8.3 Digital IO and External Peripheral Supplies

BUCKPERI is used to supply some of the digital IO of i.MX 6 device (NVCC_xxxx), which are grouped and connected to the GEN_3V3 rail, (Figure 5).

BUCKIO is used to supply the AUX_3V15 rail for the external peripherals.

NOTE
The digital I/O supply (NVCC_xxxx) grouping is application dependent and should be analyzed case by case.

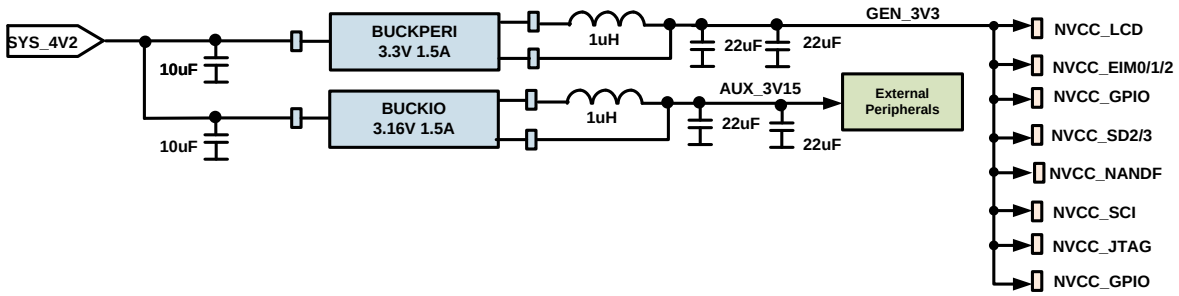

Figure 5: Digital IO and External Supplies

8.4 DDR Supply and Reference Circuit

BuckPRO is capable of 2.5 A in overdrive mode and is used to supply the external DDR3 memories (Figure 6). The BuckPro output voltage is selectable between 1.35 V and 1.5 V dependent on the logic level of GPIO13. See section 8.11 for details.

The DDR3 reference voltage DRAM_VREF can be generated from the DDR3 supply rail though a 2:1 potential divider, generating a tracking voltage of ½ DDR3 supply rail.

The value of the potential divider resistors depends on the maximum Vref input current of the DRAM in use and on the number of chips. See Table 1-15 of reference [4] for more details and recommended values.

Alternatively, connecting the DDR3 supply to the VDDQ pin on DA9063 results in the ½ DDR3 supply tracking voltage being generated at the VTTR pin of DA9063. The output from VTTR can be used to drive DRAM_VREF.

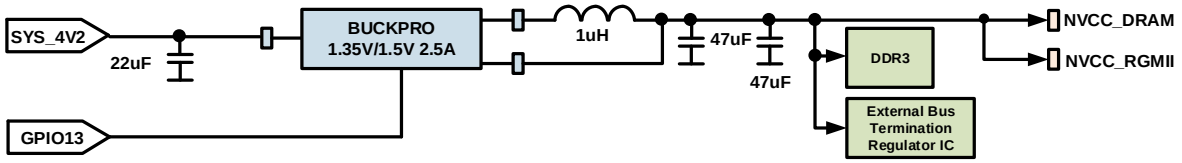

Figure 6: DDR3 Supply

8.5 Gigabit Ethernet Interface

VLDO7 is used to generate the 3.3 V NVCC_ENET rail supply voltage.

8.6 Primary Supplies to the Internal i.MX 6 LDOs

VLDO11 is used as a 2.8 V primary supply for the internal i.MX 6 LDOs (LDO_2P5, LDO_1P1), feeding the VDDHIGH_IN rail.

8.7 SD Card Interface and CMOS Camera IO Interface

VLDO10 is used to generate a 1.8 V supply for SD card interface (NVCC_SD1) and CSI CMOS camera interface NVCC_CSI. The LDO feeds the GEN_1V8 rail.

VLDO8 is used to generate the additional 1.5 V supply for the MIPI camera interface.

8.8 GPS and MiniPCI

VLDO6 is used to generate the supply for the GPS receiver and miniPCI interfaces.

8.9 Other Unused Supplies

Several supplies are not used for the NXP SABRE board and can be used for other purposes within the system: BUCKMEM, VLDO1, VLDO2, and VLDO3.

BUCKMEM is configured to have its output voltage selected by the logic level on GPIO2. Connecting GPIO2 to VDDIO produces an output voltage on BUCKMEM equivalent to the voltage set in the VBMEM_A register. Connecting GPIO2 to 0 V produces the alternate voltage set in the VBMEM_B register.

In OTP-83 VBMEM_A is preset to 1.8 V and VBMEM_B is preset to 3.3 V. These values are changeable by I^2C writes by the customer.

8.10 I^2C Interface

An I^2C interface connection between the i.MX 6 and the DA9063 PMIC device is used to allow the software application and Kernel to access the internal PMIC registers for control and monitoring.

The slave address to access the DA9063 PMIC is 0xB0.

8.11 DDR Memory Voltage Selection with GPIO13

In standard variant OTP-83, GPIO13 is used to select the output voltage of BUCKPRO. Connecting GPIO13 to 0 V produces a DDR memory voltage of 1.35 V. Connecting GPIO13 to VDDIO produces the alternate DDR memory voltage of 1.5 V.

9 Software/ Hardware Interaction

The overall system power management is handled by configuring the DA9063 PMIC OTP Note 1 memory.

A customized BSP (Board Support Package) has been developed by Dialog Semiconductor to support the DA9063 as explained in this application note.

The current BSP 1r0 release [12] implements a number of functions which are detailed in the release note [12]. In particular, the ONKEY button can perform the functions described in Table 5.

Note that the BSP can work correctly with DA9063 device with specific VARIANT_ ID: 0x6x. For more details refer to Section 13.

Table 5: Software / Hardware Interaction

Function	ONKEY Press Event Type	ONKEY Press Event Duration	Condition	Event Detection/Action
Power ON: OTP controlled	SHORT	> debouncing time	nONKEY rising edge before KEY_DELAY	DA9063 wakes-up (Android still not running)
Suspend to RAM (DSM Note 2)	SHORT	> debouncing time	nONKEY rising edge before KEY_DELAY	IRQ-handler in i.MX 6 detects DA9063 interrupt. PMIC_STBY_REQ asserted
Resume	SHORT	> debouncing time	nONKEY rising edge before KEY_DELAY	Wake-up interrupt controller in i.MX 6 wake-up internal cores DA9063 wakes up and BuckCore1/2 output voltage set to default values
Soft Power OFF	LONG	> KEY_DELAY	nONKEY rising edge before SHUT_DELAY	Awaiting user input from GUI for shutdown
Power ON after Soft Power OFF	SHORT	> debouncing time	nONKEY rising edge before KEY_DELAY	DA9063 wake-up event (Android still not running)
HW Power OFF	LONG	> KEY_DELAY+ SHUT_DELAY	nONKEY rising edge	DA9063 (HW)
RTC event from Suspend state	NA	NA	Real time clock expiration	DA9063 wake-up event
RTC event from OFF state	NA	NA	Real time clock expiration	DA9063 wake-up event

Note 1 The DA9063 device features an internal OTP (One Time Program) memory which can be programmed to define the start-up power sequence and first initialization of the device.

Note 2 DSM = Deep Sleep Mode

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Figure 7 shows a top level block diagram of the system application and the main signal and blocks involved for some of the above events.

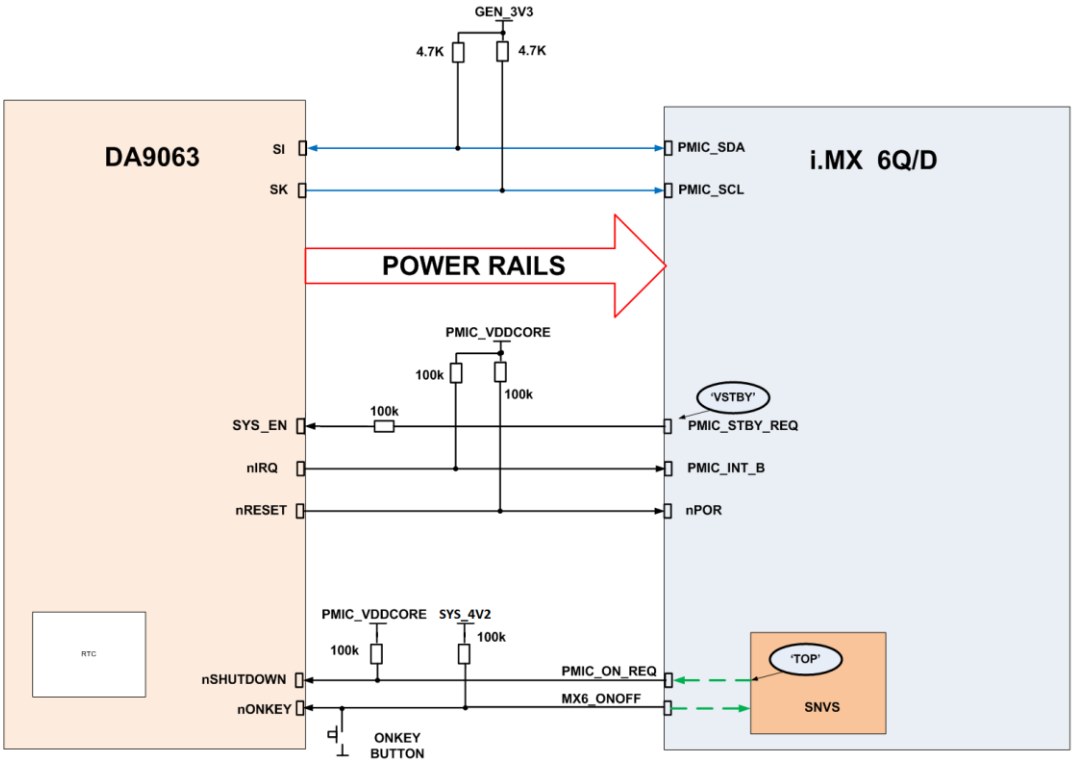

Figure 7: System Application Block Diagram

BSP version 0.5 and earlier are no longer supported and not recommended.

For BSP after version 0.5 the SW power off function is achieved by an I^2C command to the DA9063 device.

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9.1 System State Diagram

The operation of the whole system can be represented in 4 different states as depicted in Figure 8, along with the different conditions to enter or exit from each state:

- System ON
- System OFF after a POR (Power-On Reset)
- System OFF after an event from System ON state
- System SUSPENDED

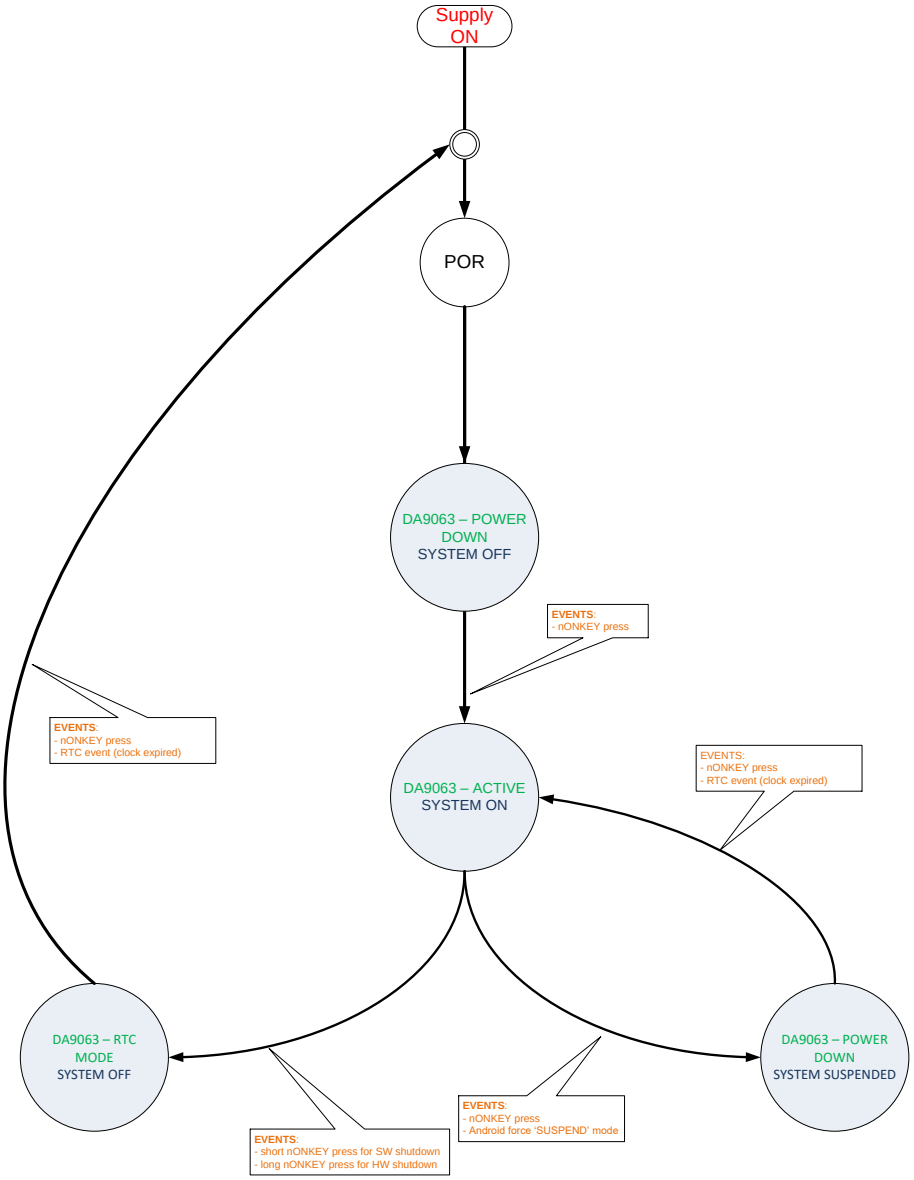

Figure 8: System State Diagram

Table 6 shows the average current (I_SYS) consumption values measured on the input supply rail (SYS_4V2) for each state condition. Suspend and ON conditions are achieved by running the BSP version 0.5. These values are to be considered only as guidance as they are very dependent on several factors such as board configuration, applications running, temperature, and more.

Table 6: Current Consumption

System State	DA9063 State	System Current (I_SYS)
OFF	Power down	800 µA
ON	Active	800 mA
SUSPEND (DSM)	Power down	17 mA
OFF	RTC shutdown	56 µA

9.2 Initial Start-Up

It is assumed that the DA9063 has already performed its internal Power-On-Reset after applying +5 V to SYS_4V2.

The internal OTP is then read and the internal registers of DA9063 initialized. The device then enters POWRDOWN state waiting for an un-masked wake-up event, see Figure 8.

9.3 Power On

When the ONKEY button is pressed a wake up interrupt/event is generated and the DA9063 PMIC executes its power on start-up sequence implemented in OTP, see Figure 12.

9.4 Suspend to RAM

If the ONKEY button is pressed for a time less than the programmed KEY_DELAY duration then a suspend request event is issued. The sequence of events 1, 2, 3 is depicted in Figure 9.

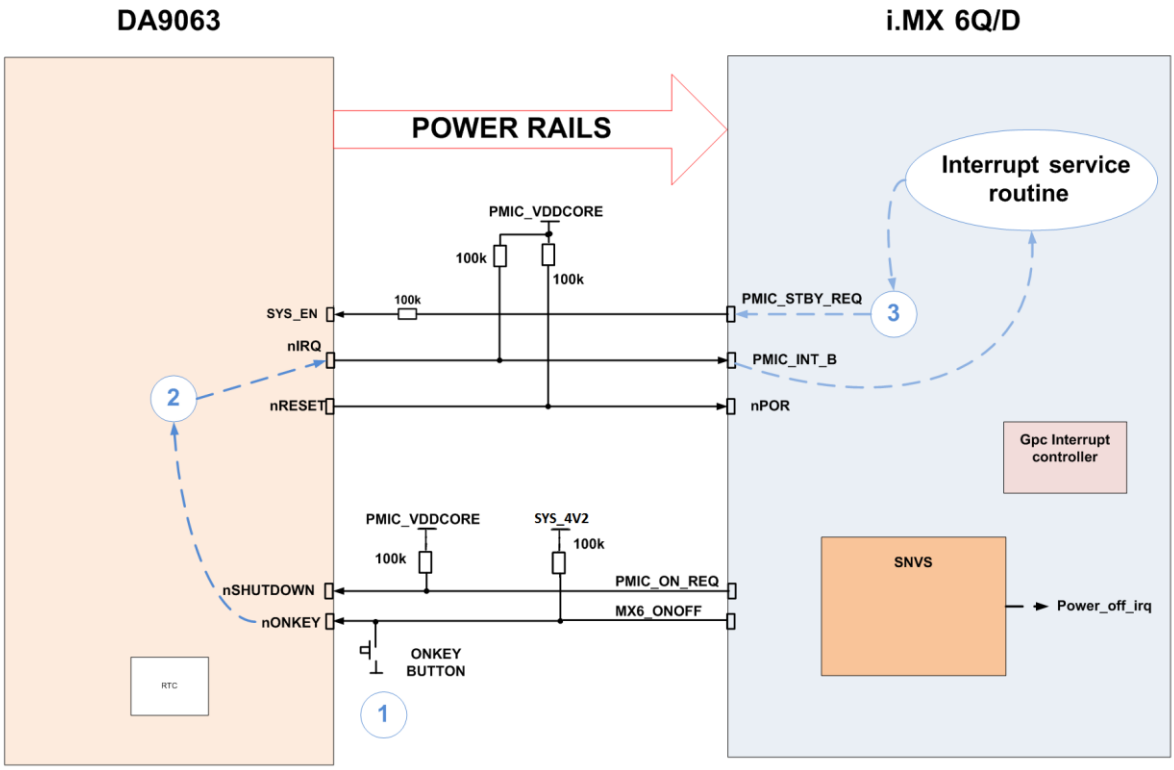

Figure 9: Suspend to Ram Event (DSM) Sequence

The interrupt request (nIRQ from PMIC to i.MX 6) is asserted at the release of the ONKEY button. The i.MX 6 processor responds by asserting PMIC_STBY_REQ (SYSEN in PMIC). The assertion of PMIC_STBY_REQ is controlled by software which may delay the immediate assertion. The PMIC then acknowledges this request by switching the VDDCORE and VDDSOC supply rails to the retention voltage level (0.92 V) which allows the system to be resumed following the press of the ONKEY button (Resume event). The DDR_1V5 and DDR_VREF supply voltages are maintained at the nominal values in order to retain the system status variables that Android saves before entering the Suspend state.

An actual scope screenshot showing the timing of signal waveforms involved are shown in Figure 14 (events A1, A2, A3 and A4).

If a platform is configured to use SUSPEND and RESUME via PMIC_STBY_REQ and SYS_4V2 is removed a significant current can flow via i.MX 6 out of the backup battery into SYS_EN causing premature loss of RTC information. The series resistor between i.MX 6 output pin PMIC_STBY_REQ and SYS_EN input pin on DA9063 in Figure 9 is included to limit the current in this scenario.

If the current out of the backup battery must be minimized in this state then SYS_EN should be disconnected from PMIC_STBY_REQ by not fitting the series resistor. This change requires the SYS_EN function that controls power up and power down to be handled by software I^2C writes.

If SUSPEND and RESUME is not required then the series resistor should not be fitted.

9.5 Resume Event

A resume from suspend state event is triggered by pressing the ONKEY button. The sequence of events 1, 2, 3 is depicted in Figure 10.

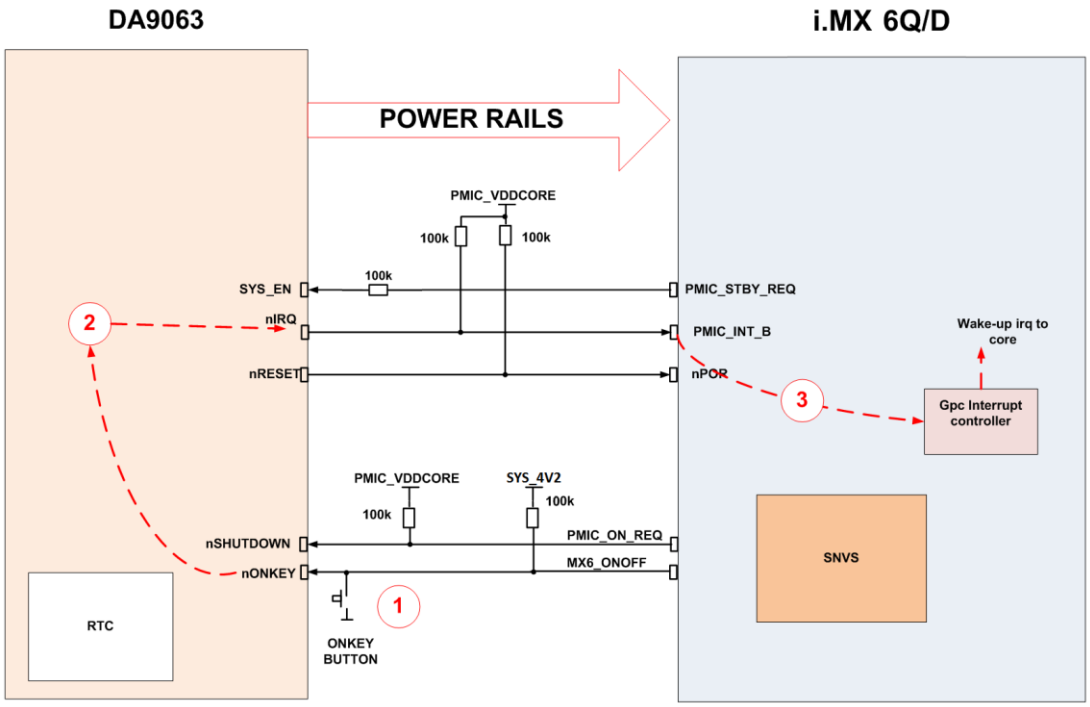

Figure 10: Resume Event Sequence from DSM

An interrupt request (nIRQ from PMIC to i.MX 6) is asserted at the release of the ONKEY button. The interrupt is handled by the wake-up interrupt controller within the i.MX 6 device. The registration of the nIRQ interrupt with the wake-up interrupt controller is the responsibility of the SW.

A scope screenshot showing the timing of signal waveforms involved are shown in Figure 12.

9.6 Soft Power Off

When the ONKEY button is pressed for a time longer than KEY_DELAY, an interrupt is asserted at time KEY_DELAY. An interrupt handler serves this interrupt by polling the nONKEY line in order to identify if a soft power off has been requested or if a direct I^2C write to trigger a PMIC shutdown is required.

If the ONKEY button is released before the SHUT_DELAY timer expires then Android displays a choice to the user to cancel/OK a power OFF option. On pressing the **OK** option, Android asserts a power off sequence (Figure 14 events B1, B2) after the SHUT_DELAY has expired and performs a shutdown.

The software power off is implemented as follows:

In BSP version 0.5 and onwards, by an I^2C write to the DA9063 registers SYSTEM_EN and RTC_MODE_PD, set as:

CONTROL_A (0x00Eh)	SYSTEM_EN	= ‘0’
CONTROL_E (0x012h)	RTC_MODE_PD	= ‘1’

9.7 Power On after Soft Power Off

After a soft power off, if the ONKEY button is pressed the system can power back on (Figure 13).

9.8 HW Power Off

If the ONKEY button is pressed for a time longer than (KEY_DELAY + SHUT_DELAY + 1 sec) then the PMIC forces a HW shutdown. The sequence of events 1, 2, 3 is depicted in Figure 11.

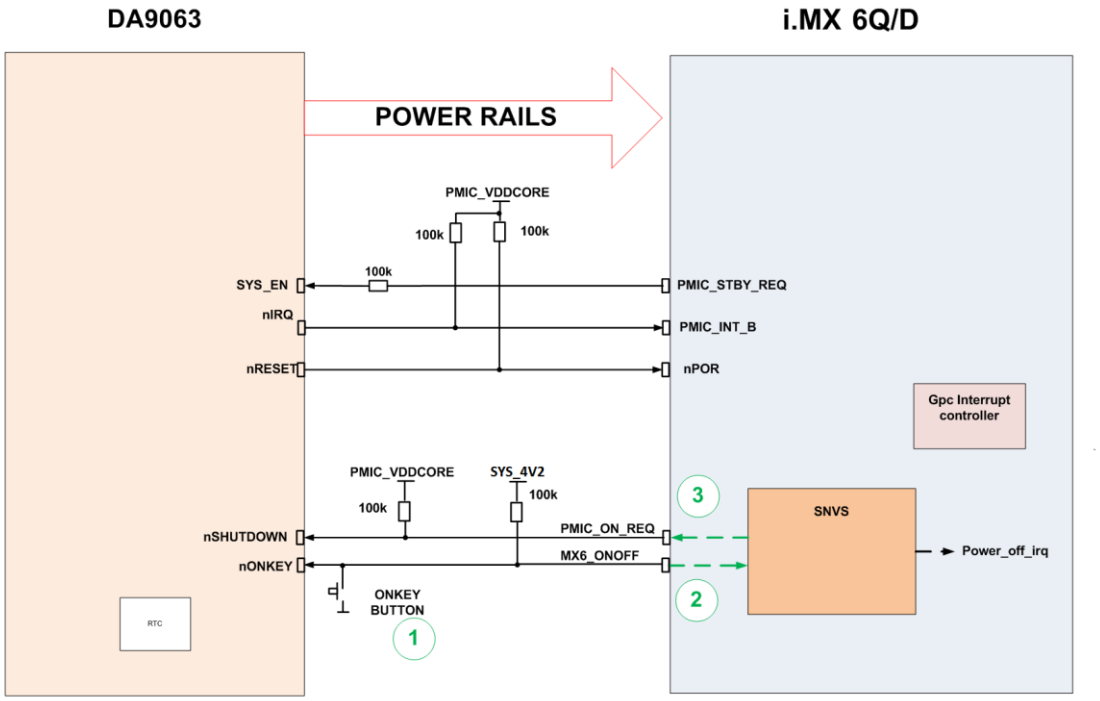

Figure 11: HW Power Off Event Sequence

9.9 DA9063 RTC Alarms

The system can handle RTC alarms from SUSPEND state (DSM) and RTC state.

If an RTC alarm has been set for a time in the future (before the system is set for power off or SUSPEND state), then a wake-up event is triggered and the PMIC exits the RTC state.

The wake-up mechanism is handled in one of two ways, depending on the state of the system:

In SUSPEND state the i.MX 6 processor is in DSM and the DA9063 is in POWERDOWN state (digital core still active). In this instance when the clock event occurs, it generates an interrupt request (DA9063 PMIC nIRQ to i.MX 6) to the wake-up interrupt controller. This event resumes the system operation.

Alternatively, when the system is in power off state (for example, after a SW power off or HW power off request), the DA9063 device powers back on if an RTC alarm occurs.

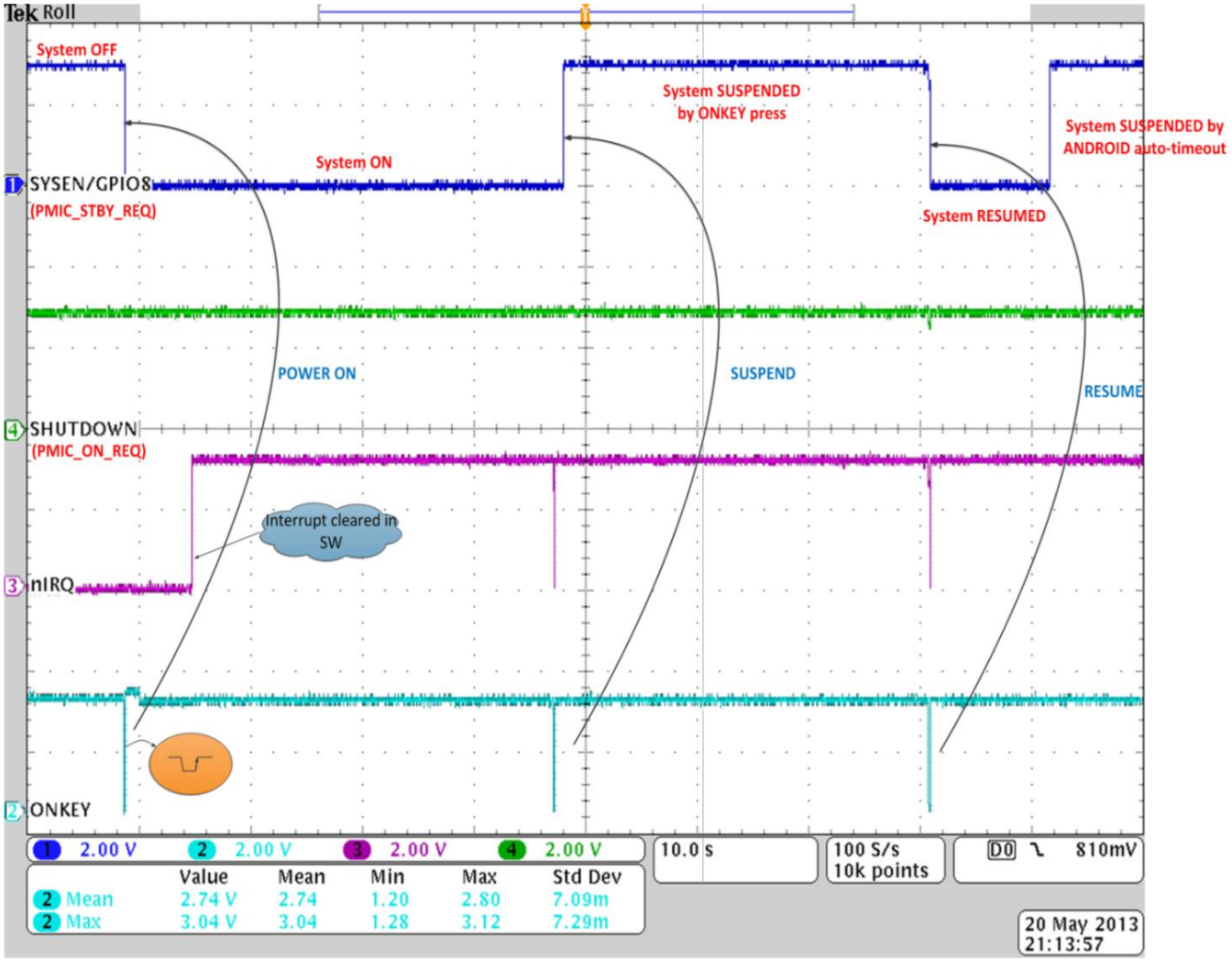

Figure 12: Power On and Sequence of SUSPEND/RESUME Events

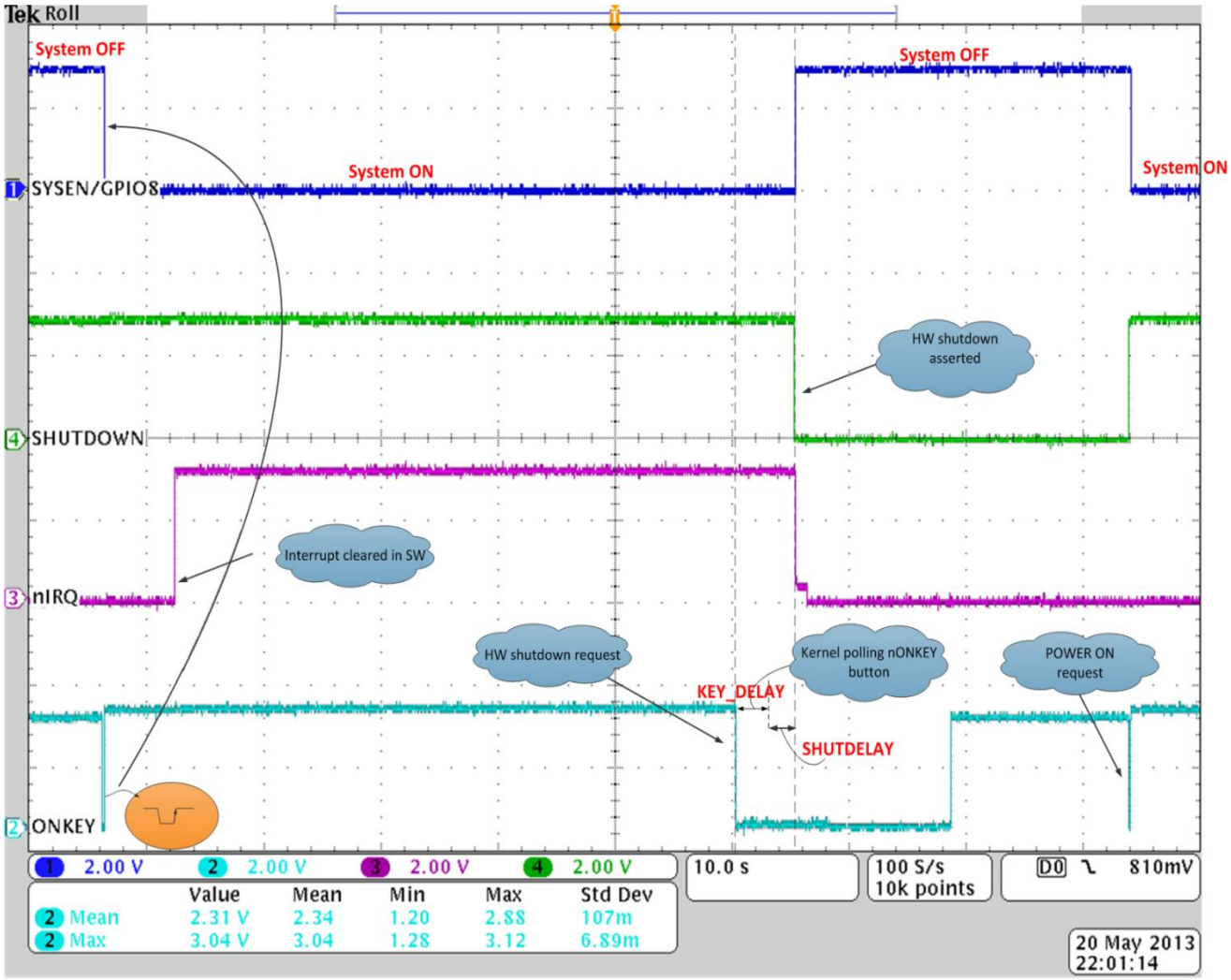

Figure 13: Power On and HW Shutdown Sequence

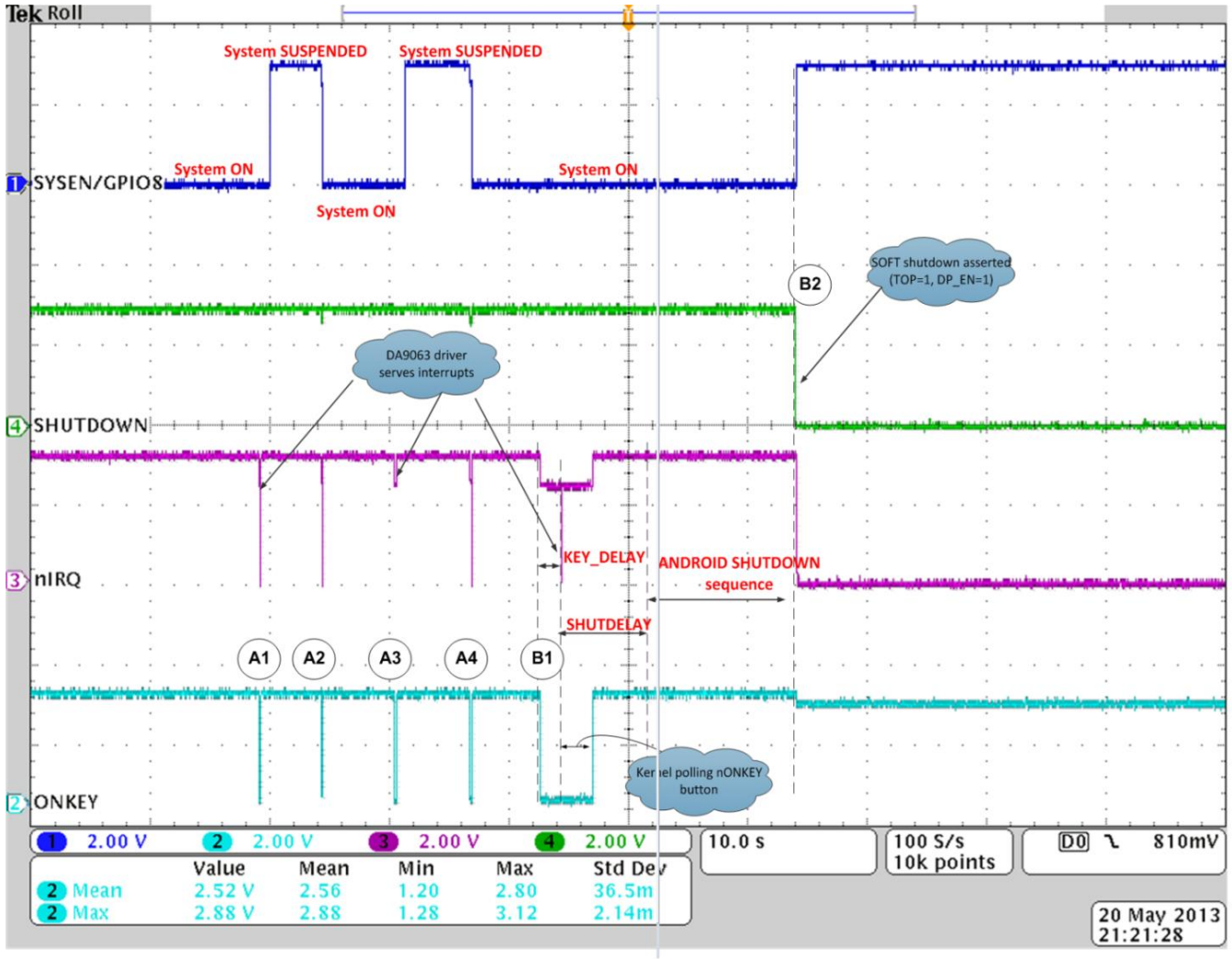

Figure 14: Sequence of SUSPEND/RESUME Events and Final Soft Shutdown

10 Power Up Sequence

Figure 15 shows the power up sequence generated by the DA9063 (-83 variant), which meets the NXP i.MX 6 start-up requirements.

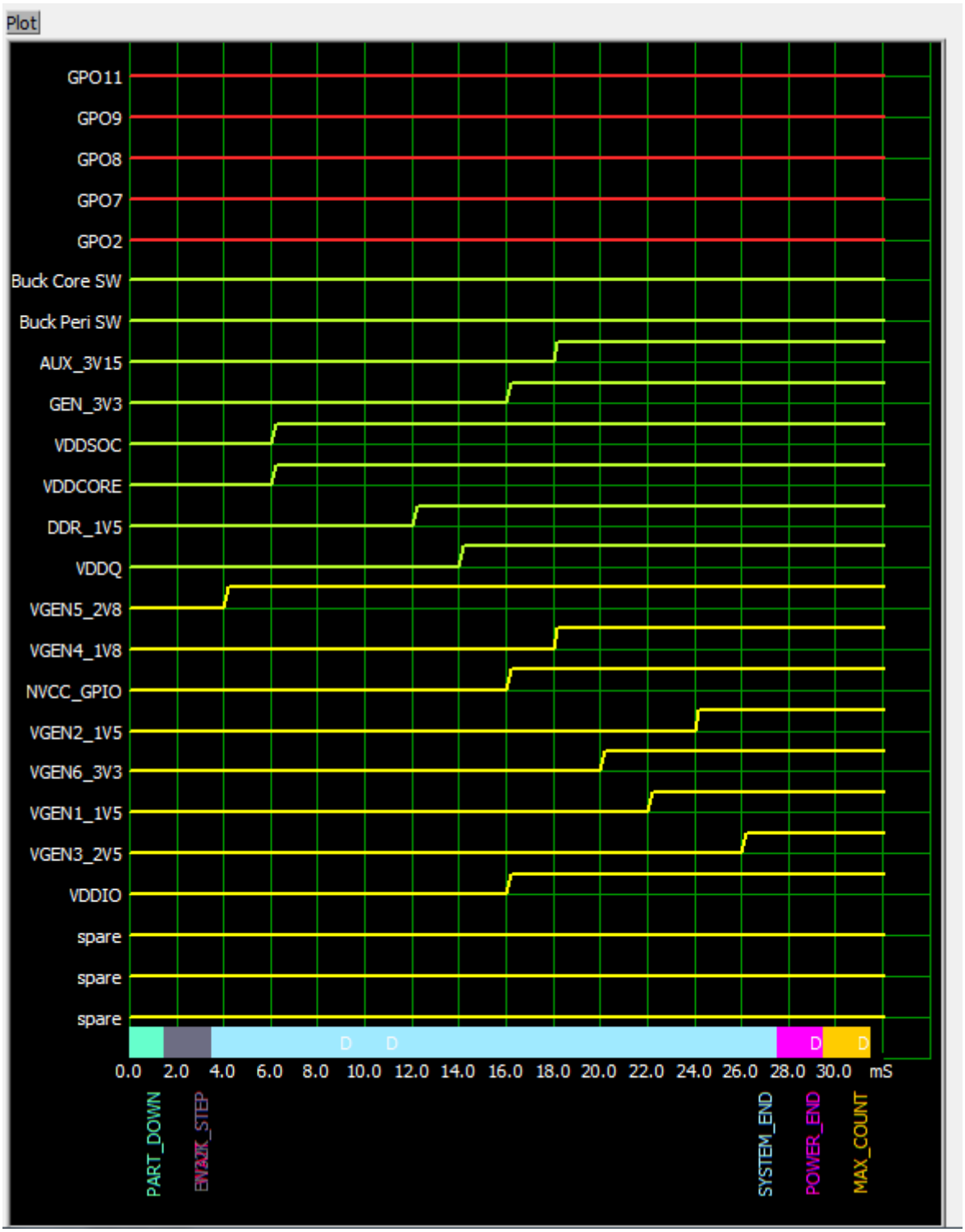

Figure 15: Power Up Sequence

11 Recommended External Components

For a list of recommended external components, please refer to the schematic [8] and its BOM [9].

Note that it is paramount to use the recommended values of inductors and capacitors at the output of all bucks and LDOs to guarantee the closed-loop stability and optimum efficiency of the supplies.

12 Power Commander Initialization File for NXP i.MX 6Q Application Processor Family

A useful and powerful SW tool is available from Dialog Semiconductor that assists in testing and evaluating the DA9063 PMIC.

The tool, namely Power Commander features a user-friendly GUI and can be run on any PC operating Windows 2000/XP/Vista/Windows 7 TM. The tool requires the use of a specific DA9063 motherboard in conjunction with a socket daughter board available from Dialog Semiconductor.

An example Power Commander initialization file is available on request from your local Dialog Sales Office. This file defines the DA9063 power up sequence and default configuration to power the NXP i.MX 6Q application processor family as shown in Figure 15.

Current DA9063 variant files available:

DA9063B_82_v01_BDF0. OTP with RTC and auto-boot support. This supersedes OTP-3F for new designs.

DA9063B_83_v01_1B3F. OTP with RTC support but not auto-boot. This supersedes OTP-3E for new designs.

12.1 Changes from OTP-3E to OTP-83

The following changes were made when updating the OTP-3E standard variant ini file to OTP-83. The same changes apply between OTP-3F and OTP-82, the only difference being the variant number stored in the ini file and whether AUTOBOOT bit is set or cleared.

Table 7: OTP Changes between OTP-3E and OTP-83

Register	OTP-3E	OTP-83	Change Description
R22	DC	DD	GPIO2 changed from ADCIN3 to GPI
R23	AC	AD	GPIO4 changed from CORE_SW_S to GPI
R24	D8	DD	GPIO6 changed from PERI_SW_S active low to GPI, active high
R25	C0	D0	GPIO9 changed from GPI_PWR_EN to GPI
R26	DC	DD	GPIO10 changed from GPI_PWR1_EN to GPI
R27	5C	DC	GPIO13 changed from wake-up to no wake-up
R29	80	00	GPIO7_MODE changed from debounce to instant
R30	0F	00	GPIO8-11_MODE changed from debounce to instant
R34	08	68	VBPRO_GPI changed from none to GPIO13
R35	00	40	VBMEM_GPI changed from none to GPIO2
R49	3F	00	VIBRATOR changed from 2.999 V to off
R132	00	80	LDO4_STEP changed from slot 0 to 8
R136	0E	02	LDO11_STEP changed from slot 14 to 2
R159	C9	09	BPRO_CFG MODE changed from Auto to Vsel
R166	23	32	VBMEM_A voltage changed from 1.5 V to 1.8 V

Register	OTP-3E	OTP-83	Change Description
R173	28	22	VLDO5_A voltage changed from 2.8 V to 2.5 V
R182	61	52	VBPRO_B voltage changed from 1.5 V to 1.35 V
R183	1C	7D	VBMEM_B voltage changed from 1.36 V to 3.3 V
R190	28	22	VLDO5_B voltage changed from 2.8 V to 2.5 V
R197	FE	FC	BCHG_VSET changed from 3.0 V to 2.8 V
R262	A0	A4	PM_O_TYPE changed from push-pull to open drain
R271	CE	EE	RESET_DUR changed from 22 ms to 500 ms
R272	00	02	GPIO1_PUPD changed from disabled to enabled
R289	09	01	GP_ID_0 changed from 09 to 01
R386	50	63	VARIANT_ID changed from 50 to 63
R388	3E	83	CONFIG_ID changed from 3E to 83
R426	CC	F7	TRIM update
R456	C1	C5	TRIM update

13 DA9063 Device Identification

To ensure the correct functionality of the BSP 1r0, it is important to use DA9063 devices with VARIANT_ID 0x6x.

The VARIANT_ID can be easily read by using the Power Commander software. If the device is already soldered into a system, a method of reading back the VARIANT_ID is by using U-boot. A simple example is given in release note [12].

If a custom variant is required, then please contact your local Dialog Sales Office.

Revision History

Revision	Date	Description
0.1	14/03/2013	First draft
0.2	24/05/2013	Updated after feedback comments. Aligned with BSP v0.2
0.3	11/06/2013	Updated application block diagram. Aligned with BSP v0.3
0.4	30/07/2013	Document aligned with BSP v0.4. Added RTC function from suspend mode only. Software System Power off is handled in HW via the two control signals PMIC_ON_REQ and MX6_ONOFF, and therefore a hardware connection is required between i.MX 6 and DA9063.
0.5	13/08/2013	The major change compared to the previous v0.4 is a change the software System Power off which now is achieved by an I^2C write. Therefore, it is not required the use of the two control signals PMIC_ON_REQ and MX6_ONOFF as in previous version. This is also reflected in the new BSP v0.5. Added RTC function from power off mode and system state diagram.
1.0	24/10/2013	Included chip ID and reference to new BSP1r0
1.1	09/12/2013	Added DDR3/LPDR2 support reference design.
2.0	14/01/2016	Updated to revised corporate template
2.1	01/03/2017	Correction to VSNVS_IN supply requirement
3.0	01/03/2018	Updated standard variants, documented changes and typo corrections
4.0	05/06/2018	Coverage of i.MX 6Quad+ added
5.0	18/10/2021	Clarification on BuckPro voltage selection via GPIO13
6.0	28/02/2022	File was rebranded with new logo, copyright and disclaimer

DA9063 / i.MX 6Dual/Quad/Quad+ Power Connections

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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