ClockMatrix™

Coordinating Timing Cards in Larger Systems

This document explains the ClockMatrix features for coordinating between two timing cards in active (working) and backup (protection) roles, and it shows an example GUI configuration for implementing this arrangement.

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Related Information

For more information, visit ClockMatrix™ Timing Solutions.

1. Introduction

For a system with two redundant Synchronous Ethernet (SyncE) timing cards, there is a need to switch between them because of a software command or card failure. The ClockMatrix devices have a set of features to implement this behavior. This application note shows an example system with dual timing cards and explains the desired behavior, and it details two DPLL configurations for coordinating two timing cards by using register writes and a separate implementation that uses a GPIO on each card.

2. Desired System Behavior

In this section, the example system includes two timing cards. The system gets its reference frequency from an external reference. (They could also use line timing from the incoming signal to the line card, but the diagram does not show this for clarity.) The active timing card has a low bandwidth per the SyncE specification for the external reference. The protection (or redundant) timing card has a high bandwidth to closely follow the frequency of the active timing card through the timing card to timing card signal (shown as the thick line in the diagram). The bandwidth associated with the normal and card-to-card input signals are set through the predefined configurations. The line cards always follow the frequency of the active timing card (shown as dashed lines).

The advantage of this approach is that both cards are always frequency-aligned allowing the other card to lock immediately after a switch. After a disruption, the high bandwidth of the protection card allows it to frequency lock quickly to be ready for a switch.

2.1 Sequence of Events During Switching

Prior to the switch, Timing Card A locks to the external reference with a low (SyncE) bandwidth. Timing Card B locks to Timing Card A with a high bandwidth. The line cards lock to Timing Card A. Figure 1 shows the diagram before the switch (with Timing Card A active).

In a switch from Timing Card A to Timing Card B:

1. Timing Card B changes from high to SyncE (low) bandwidth and starts locking to the external references. (It no longer follows the timing card to timing card signal.)
2. The line cards change their references to lock to Timing Card B.
3. Timing Card A stops following the external reference, changes to a high bandwidth, and starts following the frequency of Timing Card A.

After the switch, Timing Card B locks to the external reference with a low (SyncE) bandwidth. Timing Card A locks to Timing Card B. The line cards lock to Timing Card B. Figure 2 shows the diagram after the switch (with Timing Card B active).

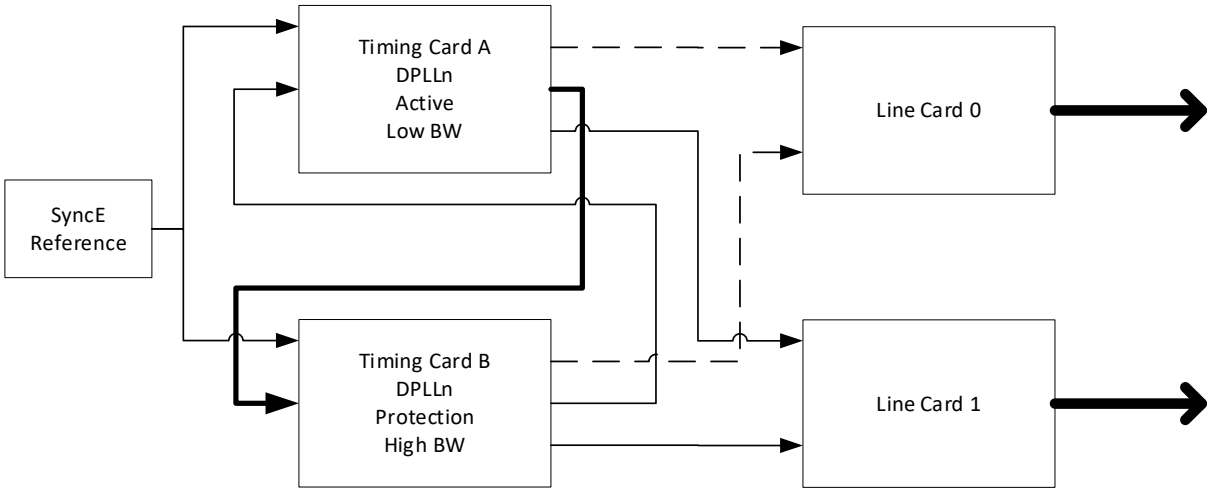

Figure 1. Diagram with Timing Card "A" Active

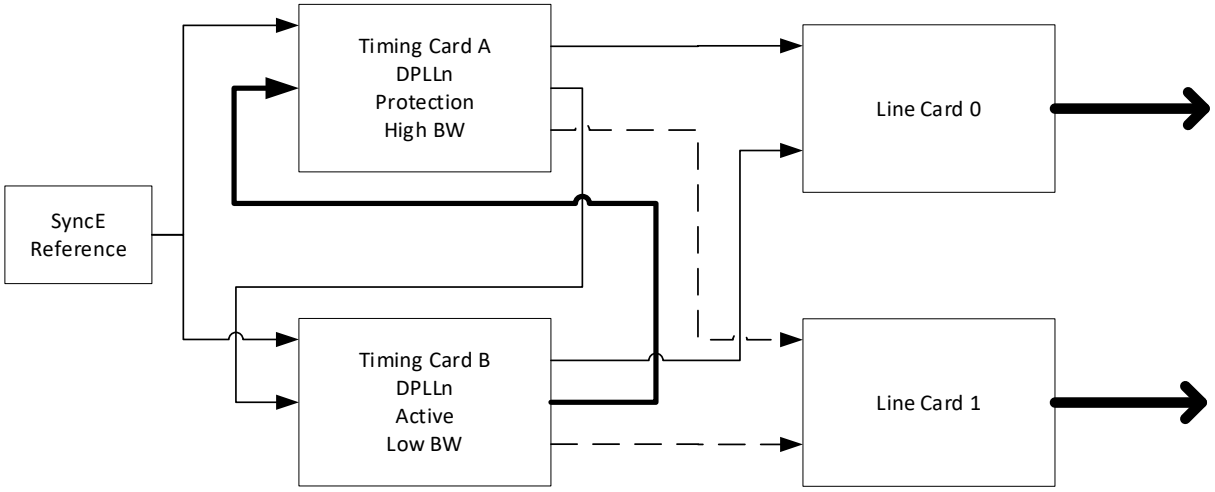

Figure 2. Diagram with Timing Card "B" Active

The reference of a DPLL in ClockMatrix can be switched using a GPIO or through changing the reference mode. To use registers select "Slave" DPLL reference mode for the protection card and select Automatic or Manual mode for the active card. To use a GPIO as shown in Figure 3, select GPIO_SLAVE DPLL reference mode and configure the GPIO to "master/slave signal (in)". The inverter in the figure ensures that only one card at a time is the master. Use Register GPIO_0.GPIO_SLAVE.GPIO_SLAVE_LEVEL to set the polarity of the GPIO input (for example, switch to slave mode when GPIO is low or switch to slave mode when GPIO is high). Using a GPIO ensures that the switch happens on both timing cards at the same time.

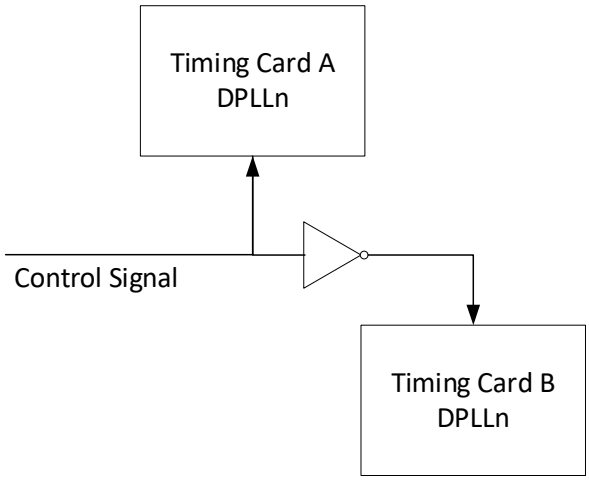

Figure 3. Use of GPIO for Timing Card Switching

When in slave mode, the register DPLL_n.DPLL_SLAVE_REF_CFG.SLAVE_REFERENCE sets the card-to-card timing signal and overrides any other reference selection.

2.2 Firmware Dependent Behavior

For firmware 4.8.7 and earlier, the DPLL uses the hitless switching setting when entering or leaving the slave or GPIO_slave reference modes. The user needs to write tie reset manually after the device has entered the slave or GPIO_slave mode. This is done by writing a 1 to the DPLL_CTRL_n.DPLL_HS_TIE_RESET.TIE_RESET bit. (This is a self-clearing bit.)

For future firmware versions, the DPLL always has hitless switching disabled (ignoring the DPLL setting) when entering slave or GPIO_slave mode. This setting (with the large DPLL bandwidth) allows the DPLL to stabilize as fast as possible. When leaving the slave or GPIO_slave mode, the DPLL would perform hitless switching based on the setting.

3. Configuring Timing Card Switching in GUI

The GUI can select the slave or GPIO_slave reference modes as displayed in Figure 4. This example has the SyncE DPLL on channel 0 with an external reference on clk0 and the timing card to timing card signal on clk1. For this application, the DPLL should use hitless switching mode. (The hitless switching mode setting only applies when the DPLL is not in slave or GPIO_slave modes.)

Figure 4 shows the digital loop filter configuration including the use of predefined configurations to switch the bandwidth for the different input clocks.

The reference configurations are in Figure 5 and Figure 6. Figure 7 shows the select of the card-to-card input reference. Figure 8 shows the GPIO configuration to use the GPIO_slave reference mode.

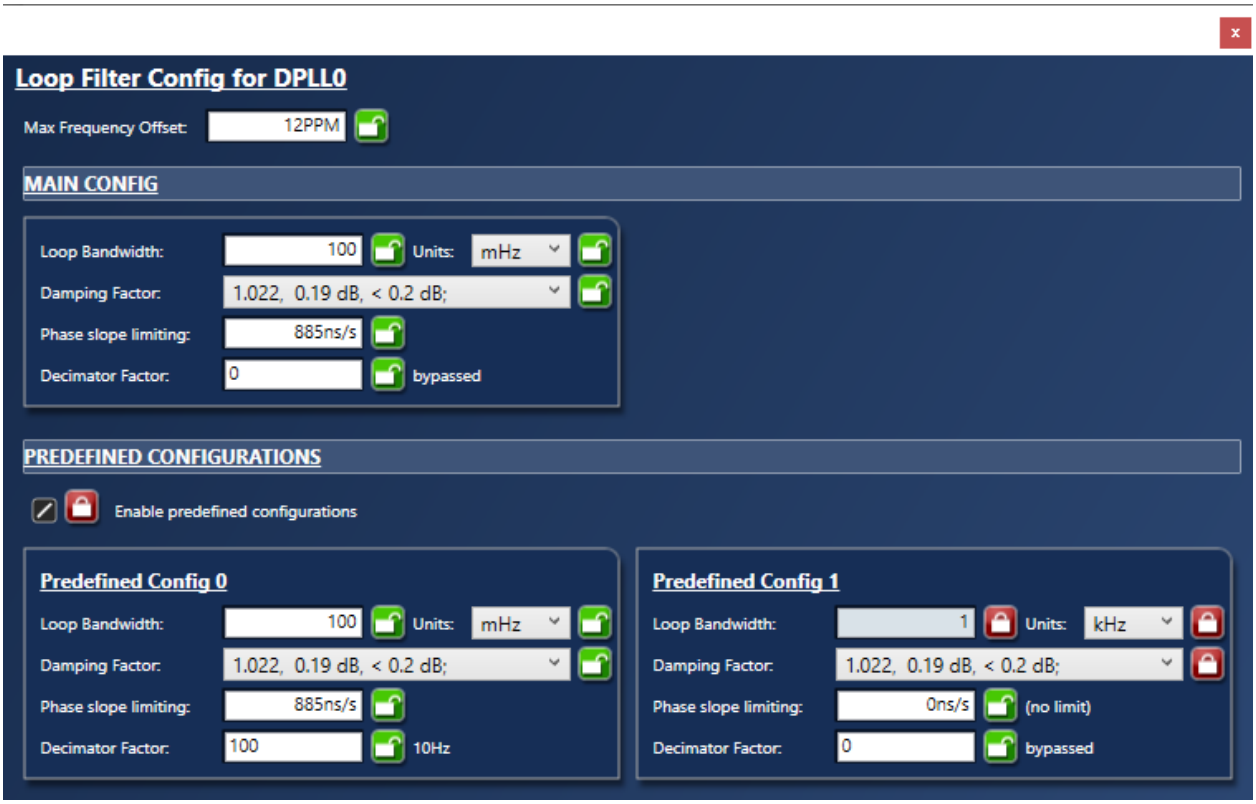

Figure 4. Digital Loop Filter Configuration

Note: In Figure 4, the “main config” settings are ignored when predefined configuration are enabled.

Figure 5. External Reference Configuration (clk0)

Figure 6. Card-to-Card Reference Configuration (clk1)

Figure 7 shows the selection of the slave (card-to-card) reference as shown by the heavy arrow in Figure 5 and Figure 6.

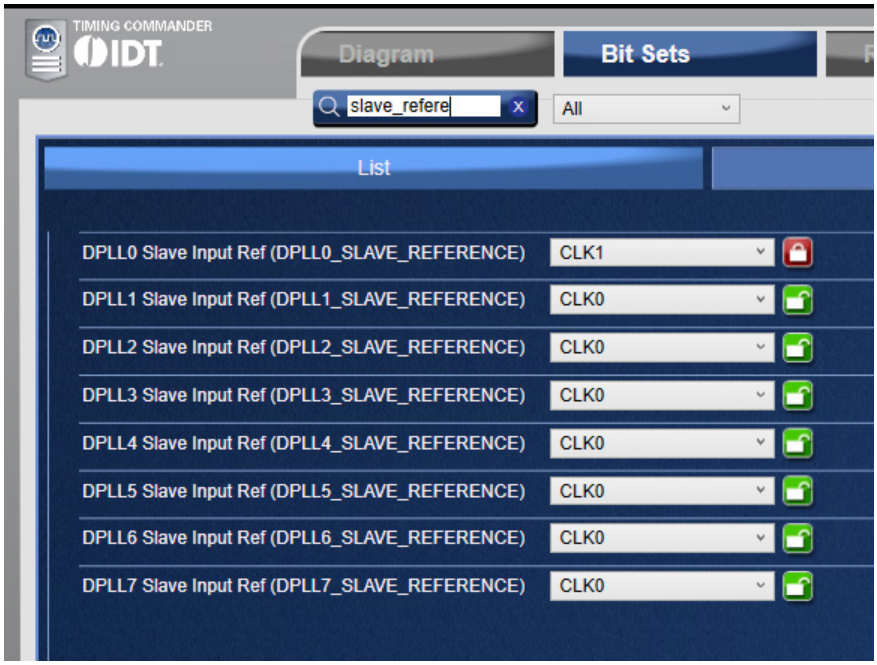

Figure 7. "Bit Sets" (Register) View Selection of Slave Reference

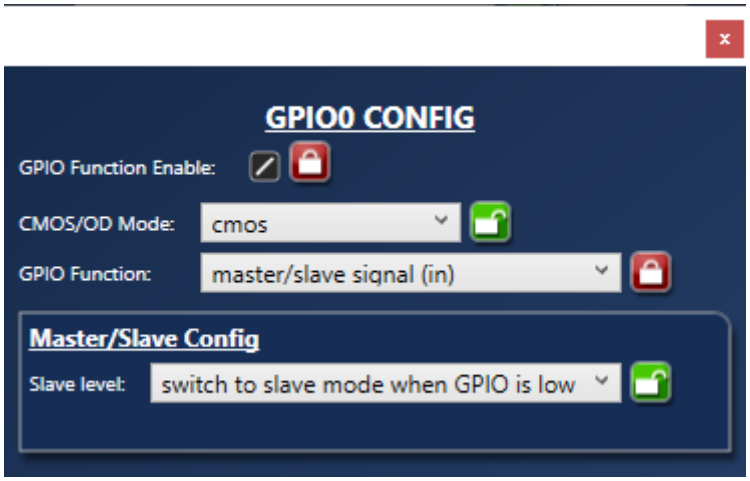

Figure 8. GPIO Configuration for Use with "GPIO_slave" Reference Mode

Note: To use the GPIO method, the user needs to configure the GPIO function for "master/slave signal (in)" and the input reference mode to "GPIO_slave".

4. Revision History

Revision	Date	Description
1.0	Mar 4, 2020	Initial release.

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