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Renesas Electronics Corporation

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H8/300L Super Low power Series

Conversion from Signed 32-Bit Binary to Single-Precision Floating-Point (KFTR)

Introduction

The software KFTR converts a signed 32-bit binary number, which is placed in general-purpose registers, to a single-precision floating-point number.

Target Device

H8/38024

Contents

1. Arguments

Description		Memory area	Data length (bytes)
Input	Signed 32-bit binary number	R0, R1	4
Output	Single-precision floating-point number	R0, R1	4

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6	R7
○	○	—	—	×	×	—	—

I	U	H	U	N	Z	V	C
—	—	×	—	×	×	×	×

Legend

—:	No change
×:	Undefined
○:	Result

3. Specifications

Program memory (bytes)
98
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
346
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Notes

The clock cycle count (346) in the specifications is for the example shown in figure 1.

For the format of floating-point numbers, see "About Single-Precision Floating-Point Numbers <Reference>."

5. Description

5.1 Details of functions

1. The following arguments are used with the software KFTR:
   a. Input arguments:
      R0: Sets the upper 2 bytes of a signed 32-bit binary number.
      R1: Sets the lower 2 bytes of a signed 32-bit binary number.
   b. Output arguments:
      R0: The upper 2 bytes of the single-precision floating-point number are placed here.
      R1: The lower 2 bytes of the single-precision floating-point number are placed here.
2. The following figure illustrates the execution of the software KFTR. When the input arguments are set as shown in (1), the result of conversion is placed in R0 and R1 as shown in (2).

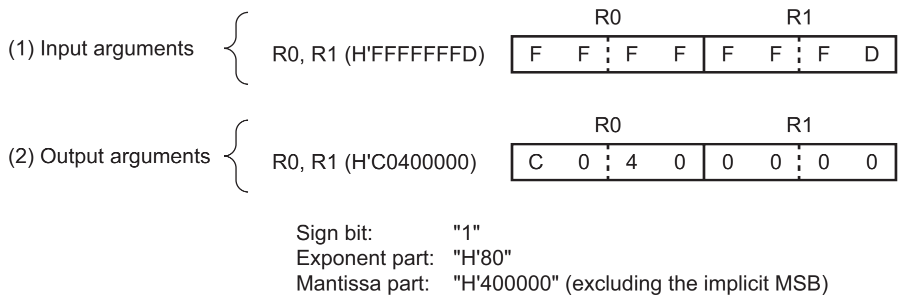


Figure 1 Example of Software KFTR Execution

5.2 Note on usage

After execution of the software KFTR, the signed 32-bit binary number is lost because the result of conversion is placed in R0 and R1. When the signed 32-bit binary number is still needed after software KFTR execution, save it in memory in advance.

5.3 Description of data memory

The software KFTR does not use data memory.

5.4 Example of usage

Set a signed 32-bit binary number in the general-purpose registers and call the software KFTR as a subroutine.

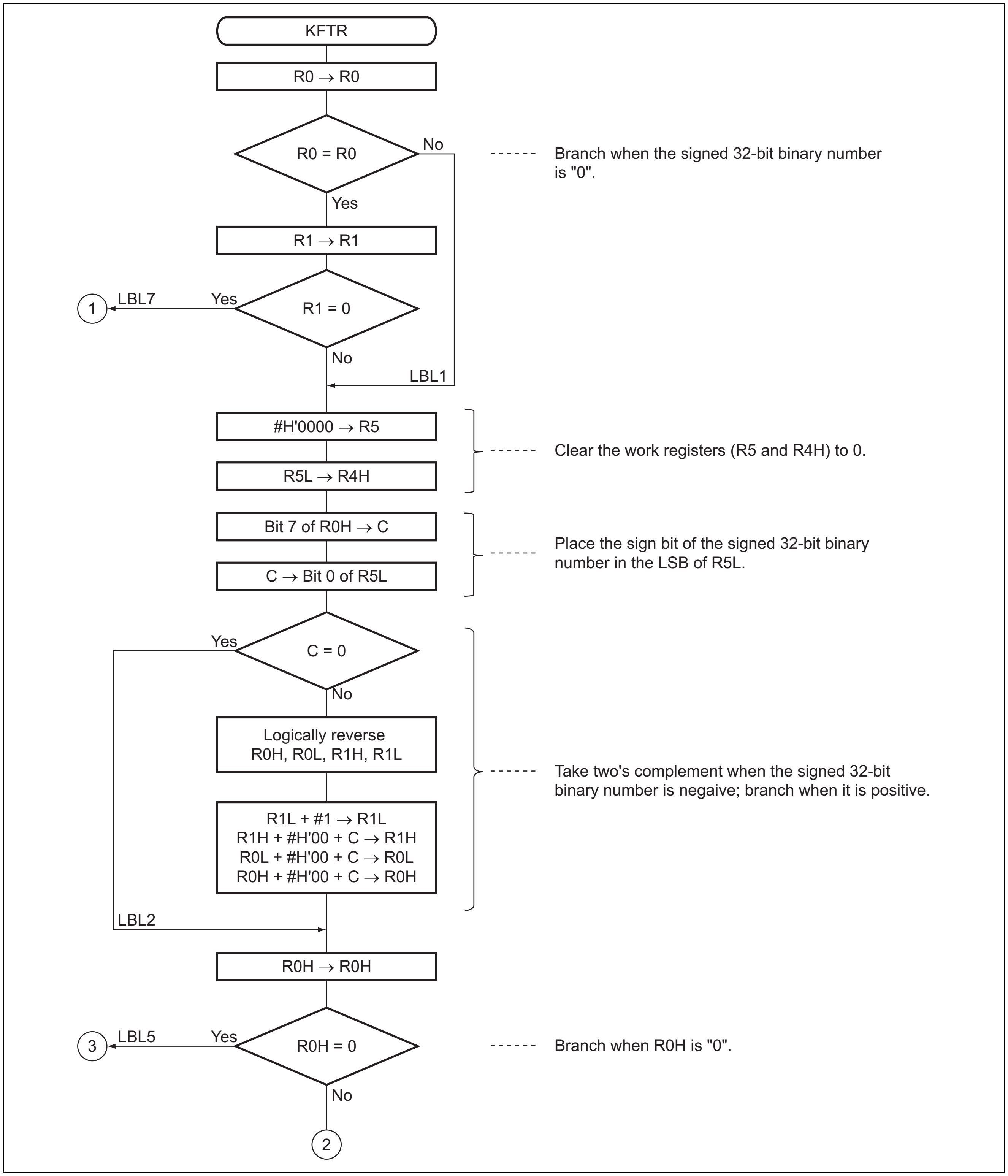
```
WORK1      . DATA. W      2, 0 ---------- Reserve a data memory area in which the user program places
                                          a signed 32-bit binary number.

WORK1      . DATA. W      2, 0 ---------- Reserve a data memory area in which the user program places
                 .                        a short floating-point number.
                 .
                 .
           MOV. W         @WORK1, R0   }------ Place the signed 32-bit binary number set by the user
           MOV. W         @WORK1+2, R1 }       program in R0 and R1 .

         | JSR            @KFTR      |   ------- Call the software KFTR as a subroutine.

           MOV. W         R0, @WORK2   }------ Place the short floating-point number set in the output
           MOV. W         R1, @WORK2+2 }       argument in R0 and R1 .
                 .
                 .
                 .
```

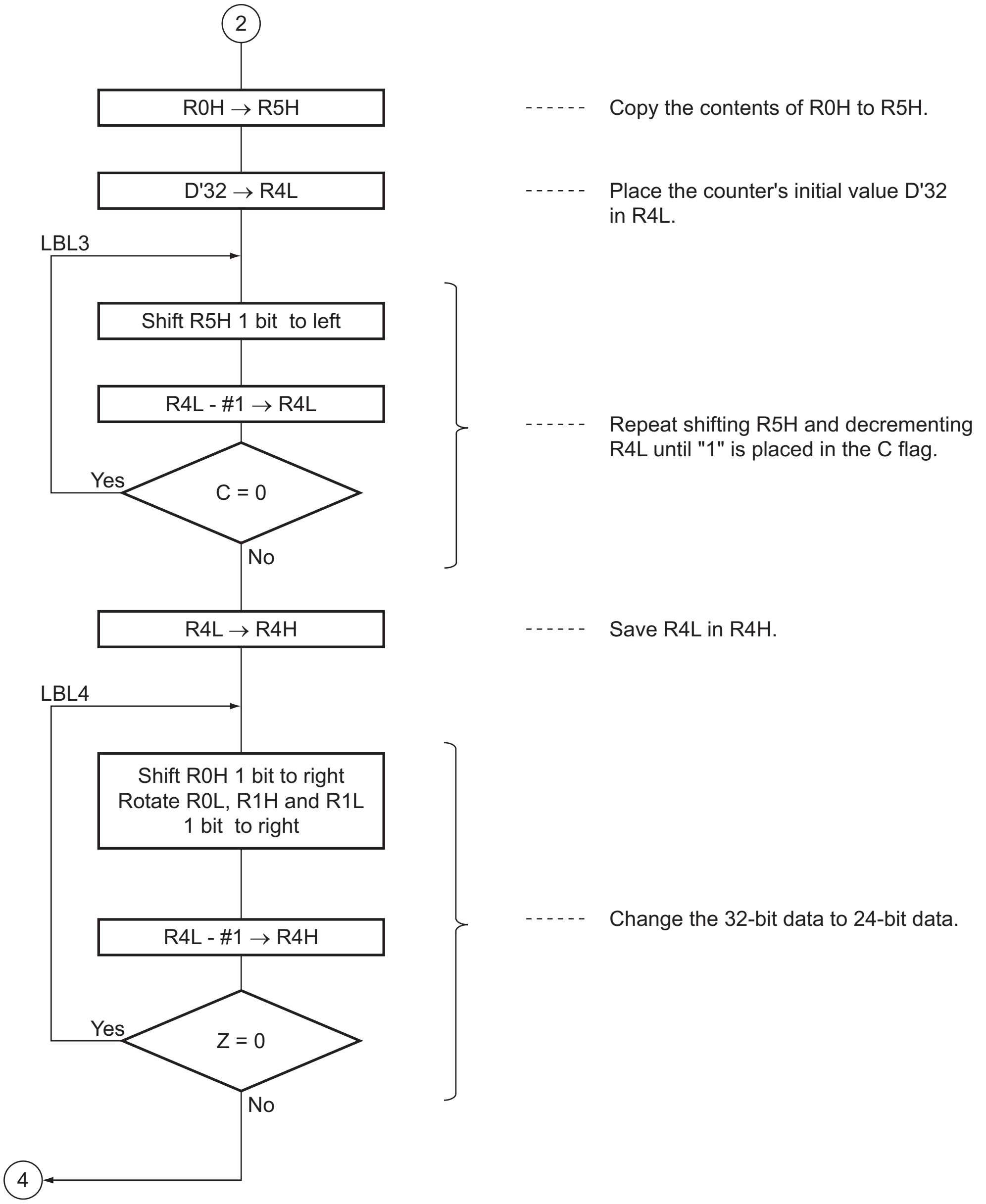
5.5 Operation

1. The software KFTR first checks whether the signed 32-bit binary number is positive or negative; when it is negative, the software takes two's complement of it. Next, the software performs either of the following operations depending on whether the upper 8 bits are "H'00" or not.
   a. When the upper 8 bits are not "H'00", the exponent is calculated and shifted to right to produce a 24-bit binary number.
   b. When the upper 8 bits are "H'00", the exponent is calculated and shifted to left to place "1" in the MSB of the lower 24 bits.

   Finally, "H'7F" is added to the exponent to convert into the floating-point format.

6. Flowchart


KFTR
R0 → R0
R0 = R0
No
Yes
R1 → R1
1
LBL7
Yes
R1 = 0
No
LBL1
#H'0000 → R5
R5L → R4H
Bit 7 of R0H → C
C → Bit 0 of R5L
Yes
C = 0
No
Logically reverse
R0H, R0L, R1H, R1L
R1L + #1 → R1L
R1H + #H'00 + C → R1H
R0L + #H'00 + C → R0L
R0H + #H'00 + C → R0H
LBL2
R0H → R0H
3
LBL5
Yes
R0H = 0
No
2
Branch when the signed 32-bit binary number is "0".
Clear the work registers (R5 and R4H) to 0.
Place the sign bit of the signed 32-bit binary number in the LSB of R5L.
Take two's complement when the signed 32-bit binary number is negaive; branch when it is positive.
Branch when R0H is "0".



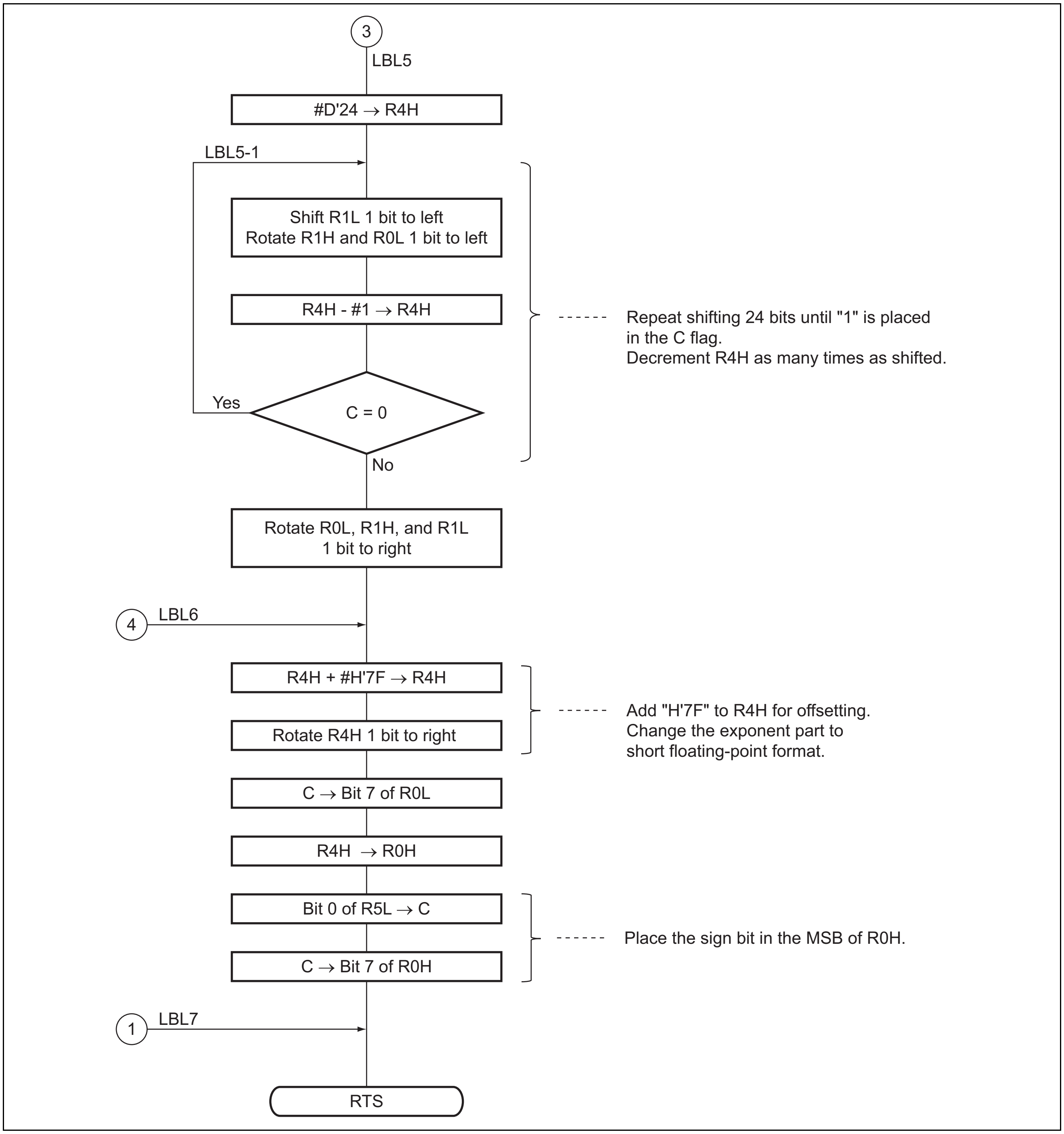
------ Copy the contents of R0H to R5H.

------ Place the counter's initial value D'32 in R4L.

------ Repeat shifting R5H and decrementing R4L until "1" is placed in the C flag.

------ Save R4L in R4H.

------ Change the 32-bit data to 24-bit data.



Repeat shifting 24 bits until "1" is placed in the C flag.
Decrement R4H as many times as shifted.

Add "H'7F" to R4H for offsetting.
Change the exponent part to short floating-point format.

Place the sign bit in the MSB of R0H.

7. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 09:39:38
PROGRAM NAME =
 1                                ;****************************************************************
 2                                ;*
 3                                ;*     00 - NAME    :CHANGE 32 BIT BINARY TO FLOATING POINT
 4                                ;*                   (KFTR)
 5                                ;*
 6                                ;****************************************************************
 7                                ;*
 8                                ;*     ENTRY        :R0 (UPPER WORD OF 32 BIT BINARY)
 9                                ;*                   R1 (LOWER WORD OF 32 BIT BINARY)
10                                ;*
11                                ;*     RETURNS      :R0 (UPPER WORD OF FLOATING POINT)
12                                ;*                   R1 (LOWER WORD OF FLOATING POINT)
13                                ;*
14                                ;****************************************************************
15                                ;
16  KFTR_cod C    0000                   .SECTION              KFTR_code,CODE,ALIGN=2
17                                       .EXPORT               KFTR
18                                ;
19  KFTR_cod C          00000000   KFTR   .EQU $                ;Entry point
20  KFTR_cod C    0000  0D00              MOV.W    R0,R0
21  KFTR_cod C    0002  4604              BNE      LBL1
22  KFTR_cod C    0004  0D11              MOV.W    R1,R1
23  KFTR_cod C    0006  4758              BEQ      LBL7         ;Branch if R0=R1=0
24  KFTR_cod C    0008             LBL1
25  KFTR_cod C    0008  79050000          MOV.W    #H'0000,R5   ;Clear R5
26  KFTR_cod C    000C  0CD4              MOV.B    R5L,R4H      ;Clear R4H
27  KFTR_cod C    000E  7770              BLD      #7,R0H
28  KFTR_cod C    0010  670D              BST      #0,R5L       ;Set sign bit to bit 0 of R5L
29  KFTR_cod C    0012  4410              BCC      LBL2         ;Branch if 32 bit binary is minus
30  KFTR_cod C    0014  1700              NOT      R0H          ;2's complement 32 bit binary
31  KFTR_cod C    0016  1708              NOT      R0L
32  KFTR_cod C    0018  1701              NOT      R1H
33  KFTR_cod C    001A  1709              NOT      R1L
34  KFTR_cod C    001C  8901              ADD.B    #H'01,R1L
35  KFTR_cod C    001E  9100              ADDX.B   #H'00,R1H
36  KFTR_cod C    0020  9800              ADDX.B   #H'00,R0L
37  KFTR_cod C    0022  9000              ADDX.B   #H'00,R0H
38  KFTR_cod C    0024             LBL2
39  KFTR_cod C    0024  0C00              MOV.B    R0H,R0H
40  KFTR_cod C    0026  471A              BEQ      LBL5         ;Branch if R0H=0
41  KFTR_cod C    0028  0C05              MOV.B    R0H,R5H
42  KFTR_cod C    002A  FC20              MOV.B    #D'32,R4L    ;Set bit counter1
43  KFTR_cod C    002C             LBL3
44  KFTR_cod C    002C  1005              SHLL.B   R5H          ;Shift R5H 1 bit left
45  KFTR_cod C    002E  1A0C              DEC.B    R4L          ;Decrement R4L
46  KFTR_cod C    0030  44FA              BCC      LBL3         ;Branch if C = 0
47  KFTR_cod C    0032  0CC4              MOV.B    R4L,R4H      ;Push R4L to R4H
```

```
48  KFTR_cod C    0034            LBL4
49  KFTR_cod C    0034  1100             SHLR.B   R0H          ;Change 32 bit binary to mantissa
50  KFTR_cod C    0036  1308             ROTXR.B  R0L
51  KFTR_cod C    0038  1301             ROTXR.B  R1H
52  KFTR_cod C    003A  1309             ROTXR.B  R1L
53  KFTR_cod C    003C  1A0C             DEC.B    R4L          ;Decrement bit counter1
54  KFTR_cod C    003E  46F4             BNE      LBL4         ;Branch if Z=0
55  KFTR_cod C    0040  4012             BRA      LBL6         ;Branch always
56                                ;
57  KFTR_cod C    0042            LBL5
58  KFTR_cod C    0042  F418             MOV.B    #D'24,R4H    ;Set bit counter2
59  KFTR_cod C    0044            LBL5_1
60  KFTR_cod C    0044  1009             SHLL.B   R1L          ;Change 32 bit binary to mantissa
61  KFTR_cod C    0046  1201             ROTXL.B  R1H
62  KFTR_cod C    0048  1208             ROTXL.B  R0L
63  KFTR_cod C    004A  1A04             DEC.B    R4H          ;Decrement bit counter2
64  KFTR_cod C    004C  44F6             BCC      LBL5_1
65  KFTR_cod C    004E  1308             ROTXR.B  R0L          ;Rotate mantissa 1 bit right
66  KFTR_cod C    0050  1301             ROTXR.B  R1H
67  KFTR_cod C    0052  1309             ROTXR.B  R1L
68  KFTR_cod C    0054            LBL6
69  KFTR_cod C    0054  847F             ADD.B    #H'7F,R4H    ;Biased exponent
70  KFTR_cod C    0056  1104             SHLR.B   R4H          ;Change floating point format
71  KFTR_cod C    0058  6778             BST      #7,R0L
72  KFTR_cod C    005A  0C40             MOV.B    R4H,R0H
73  KFTR_cod C    005C  770D             BLD      #0,R5L
74  KFTR_cod C    005E  6770             BST      #7,R0H
75  KFTR_cod C    0060            LBL7
76  KFTR_cod C    0060  5470             RTS
77                                ;
78                                       .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

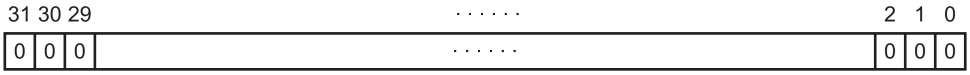
About Single-Precision Floating-Point Numbers <Reference>

Single-Precision Floating-Point Formats:

1. Internal representation of single-precision floating-point numbers

   In this Application Note, the following formats are applied to single-precision floating-point numbers depending on their values (R = real number):

   A. Internal representation for R = 0



All of the 32 bits are 0's.

   B. Normalized format

α is an exponent whose field is 8 bits long. β is a mantissa whose field is 23 bits long. The value of R can be represented by the following equation (on conditions that 1 ≤ α ≤ 254) :

$$R = 2^{S} \times 2^{\alpha-127} \times (1 + 2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \ldots\ldots + 2^{-23} \times \beta_{0})$$

where βi is the value of the i-th bit ($0 \leq i \leq 22$) and S is the sign bit.

   C. Denormalized format

where β is a mantissa whose field is 23 bits long. This format is used to represent a real number too small to be represented in the normal format. In this format, R can be represented by the following equation:

$$R = 2^{S} \times 2^{-126} \times (2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \ldots\ldots + 2^{-23} \times \beta_{0})$$

   D. Infinity

where β is a mantissa whose field is 23 bits long. In this Application Note, however, the following rules apply if all exponents are 1's;

Positive infinity when S = 0

$R = +\infty$

Negative infinity when S = 1

$R = -\infty$

2. Example of internal representation

If S = B'0 (binary)

α = B'10000011 (binary)

β = B'1011100……0 (binary)

Then the corresponding real number is as follows:

$R = 2^{0} \times 2^{131-127} \times (1 + 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5})$

$= 16 + 8 + 2 + 1 + 0.5 = 27.5$

A. Maximum and minimum values

The maximum value (R_{MAX}) and minimum value (R_{MIN}), in terms of the absolute value, are as follows:

$RMAX = 2^{254 - 127} \times (1 + 2^{-1} + 2^{-2} + 2^{-3} \ldots\ldots + 2^{-23})$

$= 3.37 \times 10^{38}$

$RMIN = 2^{-126} \times 2^{-23} = 2^{-140} = 1.40 \times 10^{-45}$

The absolute values within the above range can be represented.

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