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SH7262/SH7264 Group

Controller Area Network, Configuration to Transmit Data Frames

Summary

This application note describes the configuration example of the SH7264 microcomputers (MCUs) to transmit data frames using the Controller Area Network.

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

Contents

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2.	Applications	3
3.	Sample Program Listing	10
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1. Introduction

1.1 Specifications

• Uses the Controller Area Network channel 0

Transmission speed: 1 MbpsTransmit mailbox: Mailbox 1

Transmits the data frame with following specifications
 Identifier: 0; standard data frame; DLC: 2; Data: H'C1C2

1.2 Modules Used

• Controller Area Network (CAN) module

1.3 Applicable Conditions

MCU SH7262/SH7264

Internal clock: 144 MHz

Operating Frequencies Bus clock: 72 MHz

Peripheral clock: 36 MHz

Integrated Development Re

Renesas Technology Corp.

Environment

High-performance Embedded Workshop Ver.4.07.00 Renesas Technology SuperH RISC engine Family

C Compiler C/C++ Compiler Package Ver.9.03 Release 00

Default setting in the High-performance Embedded Workshop

Compiler Options (-cpu=sh2afpu -fpu=single -object="\$(CONFIGDIR)\\$(FILELEAF).obj"

-debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all

-infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7262/SH7264 Group Controller Area Network, Configuration to Receive Data Frames
- SH7262/SH7264 Group Controller Area Network, Configuration to Transmit Remote Frames
- SH7262/SH7264 Group Controller Area Network, Configuration to Receive Remote Frames



2. Applications

This application note uses the CAN module to transmit a standard data frame with identifier 0, DLC 2, and H'C1C2 data.

2.1 CAN Overview

The SH7264 includes two channels of a CAN module which is compliant with the CAN protocol, version 2.0B active, and ISO 11898.

The CAN module has 31 programmable mailboxes for transmission/reception, one mailbox for reception, and a programmable receive filtering mask to provide flexible communication procedure. Figure 1 shows the CAN block diagram. For more details, refer to Controller Area Network chapter in the SH7262 Group, SH7264 Group Hardware Manual.

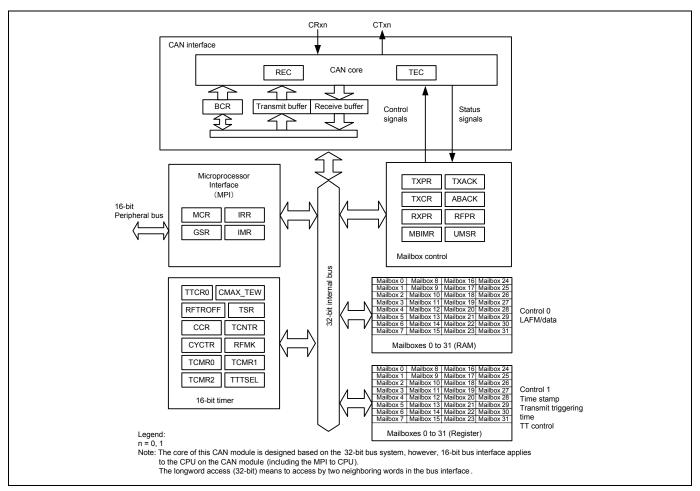


Figure 1 CAN Block Diagram (For One Channel)



2.2 Configuration Procedure

This section describes how to configure the SH7264 MCU to transmit data frames using the CAN module channel 0.

Configure the CAN module in reset mode (configuration mode). After configuration is complete, clear the reset mode to join the CAN bus activity. The sample program sets two mailboxes in SH7264 - one transmit mailbox and one receive mailbox. Figure 2 and Figure 3 show the flow charts for configuring the CAN module. For details on register settings, refer to the Controller Area Network chapter in the SH7262 Group, SH7264 Group Hardware Manual.

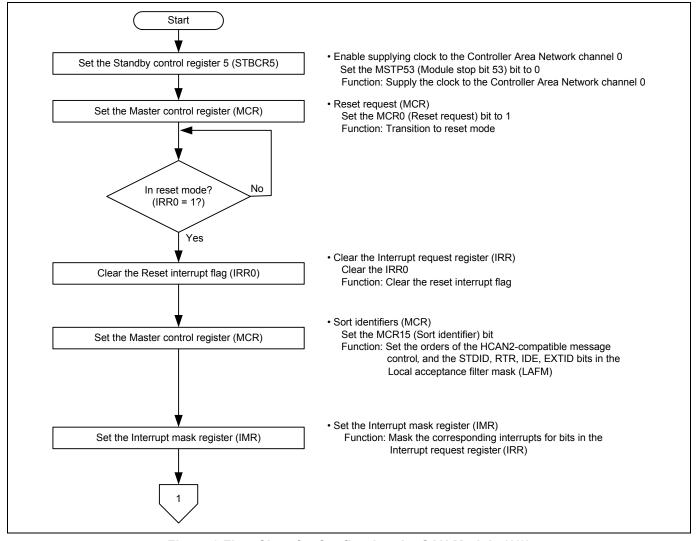


Figure 2 Flow Chart for Configuring the CAN Module (1/2)



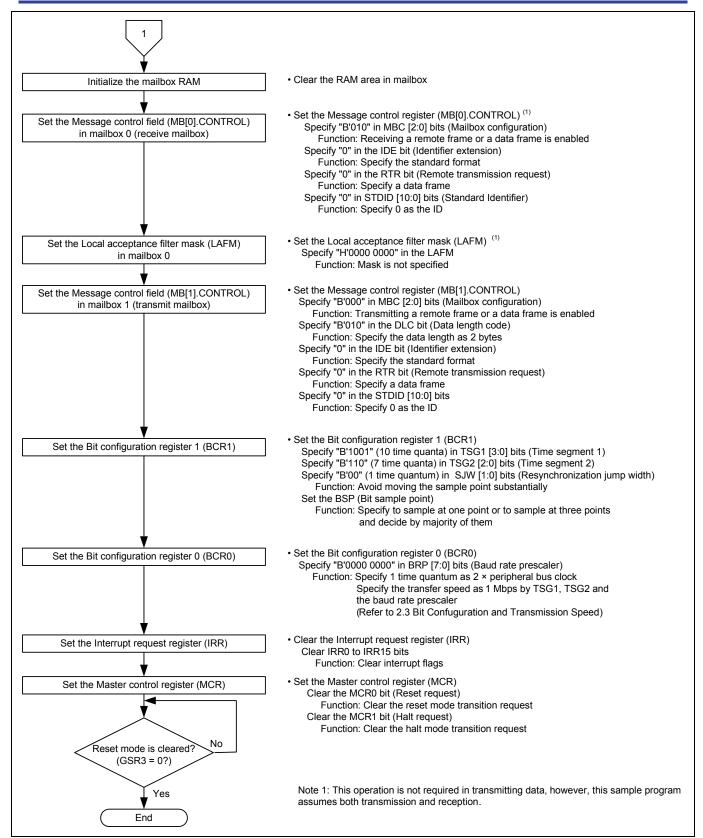


Figure 3 Flow Chart for Configuring the CAN Module (2/2)



2.3 Bit Configuration and Transmission Speed

One bit in the CAN module consists of the following four segments:

- 1. Synchronization segment (SS)
- 2. Propagation time segment (PRSEG)
- 3. Phase buffer segment 1 (PHSEG1)
- 4. Phase buffer segment 2 (PHSEG2)

Each segment is composed of the reference time Tq (time quanta). Figure 4 shows the bit configuration example when SS = 1 Tq, PRSEG = 8 Tq, PHSEG1 = 8 Tq, and PHSEG2 = 8 Tq.

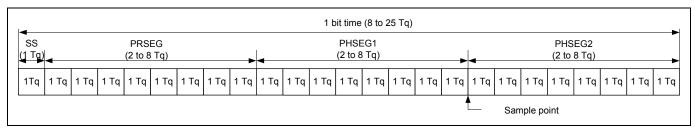


Figure 4 Bit Configuration

The CAN module sets the number of Tqs of PRSEG + PHSEG1 to bits TSG1 [3:0] in the BCR1 register, and the number of Tqs of PSEG2 to bits TSG2 [2:0] in this register (Value + 1 is the number of Tqs). Also, the number of peripheral bus clocks for 1 Tq is set to bits BRP [7:0] in the BCR0 register.

In the following description, bits BRP [7:0], TSEG1 [3:0], and TSEG2 [2:0] are register values, and bits BRP, TSEG1, TSEG2, and SJW are the corresponding values for the register values. For the corresponding values for register values, refer to the Controller Area Network chapter in the SH7262 Group, SH7264 Group Hardware Manual.

The CAN module defines ${}^{1}\text{Tq} = \frac{2 \times (BRP[7:0]+1)}{Peripheral bus clock}$ By this formula, the transmission speed is calculated as follows:

Following is the restrictions on setting the bit configuration register.

TSEG1 (Min.) > TSEG2
$$\geq$$
 SJW (Max.) (SJW = 1 to 4)

SJW is the resynchronization jump width. It is a segment that lengthens phase buffer segment 1 or shortens phase buffer segment 2 to correct the phase difference.

$$8 \le TSEG1 + TSEG2 + 1 \le 25$$
 time quanta $TSEG2 \ge 2$

As this sample program specifies the peripheral bus clock as 36 MHz, BRP [7:0] = 0, TSEG 1 [3:0] = 9, and TSEG2 [2:0] = 6, the transmission speed is calculated as follows:

Transmission speed =
$$\frac{36M}{2 \times (0+1) \times \{(9+1)+(6+1)+1\}} = 1M....1 \text{ Mbps}$$



2.4 Sample Program Operation

This sample program transmits a standard data frame from mailbox 1 with identifier 2, DLC 2, and H'C1C2 data at 1 Mbps. Figure 5 shows the transmission waveform.

Note: The sample program transmits and receives data frames, however, this application note describes only the transmission.

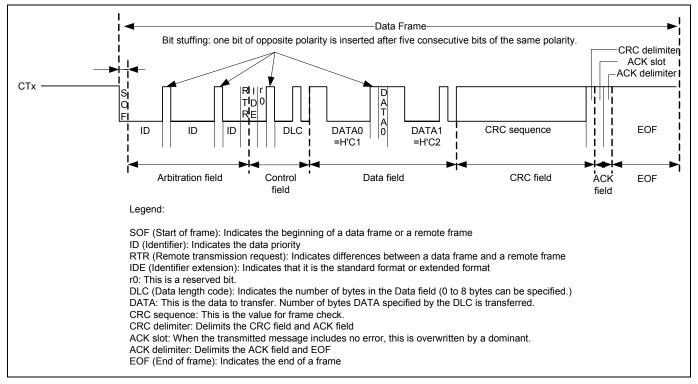


Figure 5 CAN Transmission Waveform



2.5 Sample Program Procedure

The following table lists setting example of the CAN. Figure 6 shows the configuration flow chart of this sample program.

Note: The sample program transmits and receives data frames, however, this application note describes only the transmission.

Table 1 Controller Area Network Settings

Register Name	Address	Setting	Description
Standby control register (STBCR5)	H'FFFE 0410	H'F7	MSTP53 = "0": Controller Area Network channel 0 is operating
	H'FFFF 5000	H'0001	MCR0 = "1": Reset mode transition request
Master control register (MCR)		H'8001	MCR15 = "1": The order of the RCAN message and of the HCAN2 message are different
		H'8000	MCR0 = "0": Reset mode is cleared
Interrupt mask register(IMR)	H'FFFF 500A	H'FFFF	All interrupts in the Controller Area Network are disabled
Bit configuration register 1 (BCR1)	H'FFFF 5004	H'9600	TSEG1 [3:0] = "B'1001": PRSEG + PHSEG1 = 10 Tq TSEG2 [2:0] = "B'110": PHSEG2 = 7 Tq SJW = "0": SJW = 1 Tq BSP = "0": Bit sampling at one point
Bit configuration register 0 (BCR0)	H'FFFF 5006	H'0000	BRP [7:0] = "0": 1 Tq = 2 × Pφ
Message control field in mailbox 0 (MB[0].CONTROL1)	H'FFFF 5110	H'0200	MBC [2:0] = "B'010": Receiving the data frame or remote frame is enabled
Message control field in mailbox 0 (MB[0].CONTROL0)	H'FFFE 5100	H'0000 0000	IDE = "0": Standard format RTR = "0": Data frame STDID [10:0] = "0": Standard identifier is 0
Message control field in mailbox 1 (MB[1].CONTROL1)	H'FFFF 5130	H'0002	MBC [2:0] = "B'000": Transmitting the data frame or remote frame is enabled DLC [3:0] = "B'0010": Data length is 2 bytes
Message control field in mailbox 1 (MB[1].CONTROL0)	H'FFFF 5120	H'0000 0000	IDE = "0": Standard format RTR = "0": Data frame STDID[10:0] = "0": Standard identifier is 0
Local acceptance filter mask in mailbox 0 (MB[0].LAFM)	H'FFFF 5104	H'0000 0000	Clear: Mask is not specified
Message data field in mailbox 1 (MB[1].MSG_DATA_0)	H'FFFF 5128	H'C1C2	Specify "H'C1C2" as the transmit data
Transmit pending register (TXPR)	H'FFFF 5020	H'0000 0002	TXPR [31:0] = H'0000 0002: A transmission request occurred in Mailbox 1
Transmit acknowledge register 0 (TXACK0)	H'FFFF 5032	H'0002	Clear the transmit acknowledge flag



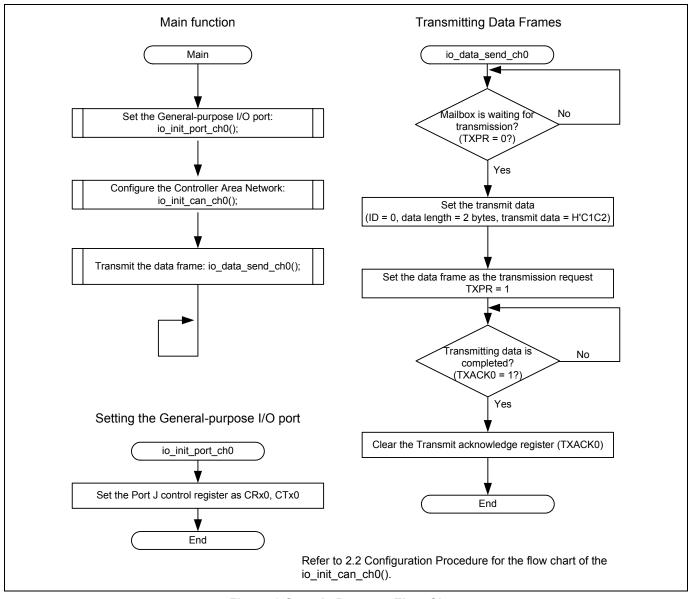


Figure 6 Sample Program Flow Chart



3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.



3.2 Sample Program Listing "main.c" (1/2)

```
/**********************************
1
2.
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27
28
          Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
       *""FILE COMMENT""******* Technical reference data ******************************
29
30
         System Name : SH7264 Sample Program
31
          File Name : main.c
32
          Abstract : CAN Module Application (Data Frame Transmit and Receive)
       * Version : 1.00.00
       * Device
34
                    : SH7262/SH7264
           Tool-Chain : High-performance Embedded Workshop (Ver.4.07.00).
35
                    : C/C++ compiler package for the SuperH RISC engine family
36
37
                                               (Ver.9.03 Release00).
       * OS
38
                     : None
39
          H/W Platform: M3A-HS64G50 (CPU board) + M3A-HS64G02 (IO board)
40
         Description :
       ******************
41
42
           History
                    : Nov.20,2009 ver.1.00.00
       4.3
        #include "iodefine.h"
                              /* SH7264 iodefine */
45
```



3.3 Sample Program Listing "main.c" (2/2)

```
/* ---- prototype declaration ---- */
     void main(void);
48
    extern void io_init_port_ch0(void);
49
   extern void io init port ch1(void);
    extern void io init can ch0(void);
50
51
   extern void io init can ch1(void);
52
    extern void io data send ch0(void);
53
     extern void io_data_receive_ch1(void);
54
    5.5
56
     * ID
57
     * Outline
                 : Sample program main
     *-----
                 : "iodefine.h"
59
      * Include
60
      * Declaration : void main(void);
61
      * Description : After configuring the Controller Area Network (RCAN), channel 0
64
                  : transmits the data frame, and channel 1 receives the data frame.
65
66
      * Argument
                  : void
68
      * Return Value : void
7.0
     71
72
     void main(void)
73
        /* ==== Initializing port ==== */
74
75
       io_init_port_ch1();
76
        io init port ch0();
77
78
        /* ==== Initializing CAN module ==== */
79
        io init can ch1();
80
        io_init_can_ch0();
81
82
       /* ==== CAN data frame transmission ==== */
       io data send ch0();
83
84
        /\star ==== CAN data frame reception ==== \star/
8.5
      io_data_receive_ch1();
86
87
88
        while(1){
           /* loop */
90
91
92
     /* End of File */
```



3.4 Sample Program Listing "can0.c" (1/5)

```
/****************************
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        DISCLAIMER
3
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5
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     *""FILE COMMENT""******* Technical reference data ******************************
29
30
        System Name : SH7264 Sample Program
31
        File Name : can0.c
     * Abstract : CAN Module Application (Data Frame Transmit)
32
33
     * Version : 1.00.00
34
         Device
                   : SH7262/SH7264
35
     * Tool-Chain : High-performance Embedded Workshop (Ver.4.07.00).
36
                  : C/C++ compiler package for the SuperH RISC engine family
37
                                              (Ver.9.03 Release00).
        OS
38
                   : None
39
     * H/W Platform: M3A-HS64G50 (CPU board) + M3A-HS64G02 (IO board)
40
        Description :
41
42
       History : Nov.20,2009 ver.1.00.00
     #include "iodefine.h" /* SH7264 iodefine */
44
```



3.5 Sample Program Listing "can0.c" (2/5)

```
46
     /* ---- prototype declaration ---- */
47
    void io_init_port_ch0(void);
48
     void io init can ch0(void);
     void io data send ch0(void);
49
50
51
     /* ---- symbol definition ---- */
52
     #define CAN GSR3 0x0008
53
     #define CAN IRR0 0x0001
54
     #define CAN MB0 0x0001
55
     #define CAN MB1 0x0002
56
     #define CAN MB01 0x00000002
57
    58
     * ID
59
     * Outline : PORT setting
60
61
62
      * Include
                  : "iodefine.h"
6.3
      * Declaration : void io init port ch0(void);
65
      * Description : Set pin functions (CRx0 input, and CTx0 output).
67
                  : void
69
70
      * Return Value : void
71
72
     73
74
     void io_init_port_ch0(void)
75
76
        /* ==== Setting of PORT ==== */
77
       PORT.PJCRO.BIT.PJOMD = 0x1; /* Set CTx0 */
78
                                 /* Set CRx0 */
       PORT.PJCR0.BIT.PJ1MD = 0x1;
79
     }
80
```



3.6 Sample Program Listing "can0.c" (3/5)

```
* ID
     * Outline : RCAN setting
     *-----
               : "iodefine.h"
     * Include
     *-----
87
     * Declaration : void io_init_can_ch0(void);
     * Description : Configure the Controller Area Network (RCAN) channel 0.
        : Transfer rate is set as 1 Mbps.
91
     * Argument
               : void
     *-----
93
     * Return Value : void
9.5
     98
    void io_init_can_ch0(void)
99
100
      int i, j;
101
102
     /* ==== Setting of power down mode(RCAN) ==== */
     CPG.STBCR5.BIT.MSTP53 = 0;
                                   /* Module Standby Clear (RCAN0)*/
103
104
     /* ==== Initializing CAN module ==== */
105
      RCANO.MCR.WORD |= 0x0001; /* CAN Interface reset mode */
106
      while((RCANO.IRR.WORD & CAN IRRO) != CAN IRRO) {
107
108
         /* Reset state waiting */
109
110
      /* ==== IRR = 1, GSR = 1 (Auto SET) ==== */
111
112
      /* ---- Clear IRRO ---- */
113
      RCANO.IRR.WORD = 0 \times 0001;
114
      /* ---- RCAN mode selection(MCR15) ---- */
115
116
      RCANO.MCR.WORD \mid = 0x8000; /* RCAN is not same as HCAN2 */
117
118
       /* ---- Disable all can interrupt ---- */
119
      RCANO.IMR.WORD = 0xffff;
120
```



3.7 Sample Program Listing "can0.c" (4/5)

```
121
          /* ----All mailbox init ---- */
122
          for(i = 0; i < 32; i++){
123
            RCANO.MB[i].CONTROLO.LONG = 0 \times 000000000;
            RCANO.MB[i].LAFM.LONG = 0 \times 000000000;
124
125
            for (j = 0; j < 8; j++) {
126
                 RCANO.MB[i].MSG DATA[j] = 0 \times 00;
127
            }
128
          }
129
130
         /* ---- Config mailbox0 as reception slot ---- */
131
         RCANO.MB[0].CONTROLO.LONG = 0 \times 000000000; /* Initialize the Message Control Field */
132
        RCANO.MB[0].LAFM.LONG = 0 \times 000000000;
133
134
        for(i = 0; i < 8; i++){
                                              /* data clear */
135
             RCANO.MB[0].MSG DATA[i] = 0 \times 00;
136
        /* ---- Config mailbox1 as transmission slot ---- */
137
        RCANO.MB[1].CONTROL1.WORD = 0x0002; /* CAN send data or remote frame, dlc=2 */
138
139
         RCANO.MB[1].CONTROLO.LONG = 0x00000000; /* standard data frame, id=0x000 */
        RCANO.MB[1].LAFM.LONG = 0 \times 000000000;
140
        for(i = 0; i < 8; i++){
                                              /* data clear */
142
             RCANO.MB[1].MSG DATA[i] = 0x00;
143
144
        /* ---- Config baudrate ---- */
145
        RCANO.BCR1.WORD = 0x9600; /* tsg1=9(10bit),tsg2=6(7bit),sjw=0(1bit),bsp=0 */
146
                                     /* 1 Mbps */
147
         RCANO.BCRO.WORD = 0 \times 0000;
148 // RCANO.BCRO.WORD = 0x0001;
                                     /* 500 Kbps */
149 // RCANO.BCRO.WORD = 0 \times 0003;
                                     /* 250 Kbps */
      // RCANO.BCRO.WORD = 0 \times 0007;
                                      /* 125 Kbps */
150
151
152
        /* ---- Clear interrupt flags ---- */
        RCANO.IRR.WORD = 0xffff;
153
154
        /* ---- Clear reset and halt ---- */
155
156
        RCANO.MCR.WORD &= 0xf8fc; /* MCR0, MCR1 clear */
          while ( (RCANO.GSR.WORD & CAN GSR3) != 0x0000 ) {
157
158
            /* Reset state is end */
159
        }
160
    }
161
```



3.8 Sample Program Listing "can0.c" (5/5)

```
162
163
    * ID
164
    * Outline : Data frame transmit
    *-----
165
               : "iodefine.h"
166
     * Include
167
     *-----
     * Declaration : void io_data_send_ch0(void);
168
169
170
     * Description : Transmit 2-byte data stored in mailbox 1.
     *-----
172
     * Argument
               : void
     *-----
173
174
     * Return Value : void
175
176
     177
178
    void io data send ch0(void)
179
180
       /* ---- Transmission waiting ---- */
       while((RCANO.TXPRO.LONG & CAN MB01) == CAN MB01) {
181
182
183
       /* ---- Transmission data set ---- */
184
      RCANO.MB[1].CONTROL1.WORD = 0x0002; /* CAN send data or remote frame, dlc=2 */
185
      RCANO.MB[1].CONTROLO.LONG = 0x00000000; /* standard data frame, id=0x000 */
186
      RCAN0.MB[1].MSG DATA[0] = 0xc1;
187
188
      RCANO.MB[1].MSG DATA[1] = 0xc2;
189
      /* ---- Transmit the data ---- */
190
191
      RCANO.TXPRO.LONG = CAN MB01;
192
193
      /* ---- Transmission completion waiting ---- */
194
      while((RCANO.TXACKO.WORD & CAN MB1) != CAN MB1) {
195
196
197
       /* ---- Transmission completion flag clear ---- */
       RCANO.TXACKO.WORD = CAN MB1;
198
199
   }
200
   /* End of File */
2.01
```



4. References

• Software Manual

SH-2A/SH2A-FPU Software Manual Rev. 3.00

The latest version of the software manual can be downloaded from the Renesas website.

• Hardware Manual

SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00

The latest version of the hardware manual can be downloaded from the Renesas website.



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Revision History

		Descript	ion
Rev.	Date	Page	Summary
1.00	Jan 08, 2010	_	First edition issued

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