SH7262/SH7264 Group

Connecting the NOR Flash Memory

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Summary

This application note introduces the normal space interface of the SH7262/SH7264 Bus State Controller (BSC), and describes how to connect an NOR flash memory.

Target Device

SH7262/7264 MCU (In this document, SH7262/SH7264 are described as SH7264.)

Contents

1. Introduction

1.1 Specifications

- Uses an NOR flash memory of 4 MB (2 Mwords × 16 bits) to connect with the SH7264 MCU in 16-bit bus wide
- Uses theSH7264 Bus State Controller to read and write the data from/to external NOR flash memory

1.2 Modules Used

- Bus State Controller

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequencies	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Electronics Corp. High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug-gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

- SH7262/SH7264 Group Example of Initialization

1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

2. Applications

This application uses the SH7264 MCU Bus State Controller (BSC) to control the externally-connected NOR flash memory.

2.1 Overview

The SH7264 BSC outputs control signals to memory devices and other external devices connected to external address space, which allow the MCU to connect external memory devices such as SRAM, SDRAM and other external devices directly.

Table 1 lists the features of the Bus State Controller. Table 2 lists the features of the normal space interface and burst ROM interface (clock asynchronous).

Table 1 Bus State Controller Features

Item	Description
Target space	Supports seven spaces from CS0 to CS6, up to 64 MB per space
Memory options	Following memory spaces can be specified: • Normal space interface • SRAM interface with byte selection • Burst ROM (clock synchronous or asynchronous) • MPX-I/O • SDRAM interface • PCMCIA interface
Data bus width	CS0 space: 16-bit, CS1 to CS6 spaces: 8-bit or 16-bit can be specified per space
Wait control	Controls to insert wait state cycles per space
Idle control	Specifies idle cycles independently during the sequential access: • In read-write in the same space • In read-write in different spaces • In read-read in the same space • In read-read in different spaces, or • When the first cycle is the write cycle

Table 2 Features of Interfaces

Item	Description
Normal space interface	Supports the interface which can be connected to SRAM directly
Burst ROM (clock asynchronous) interface	Supports the high-speed access to ROM which has the page mode function

Figure 1 shows the block diagram of the Bus State Controller.

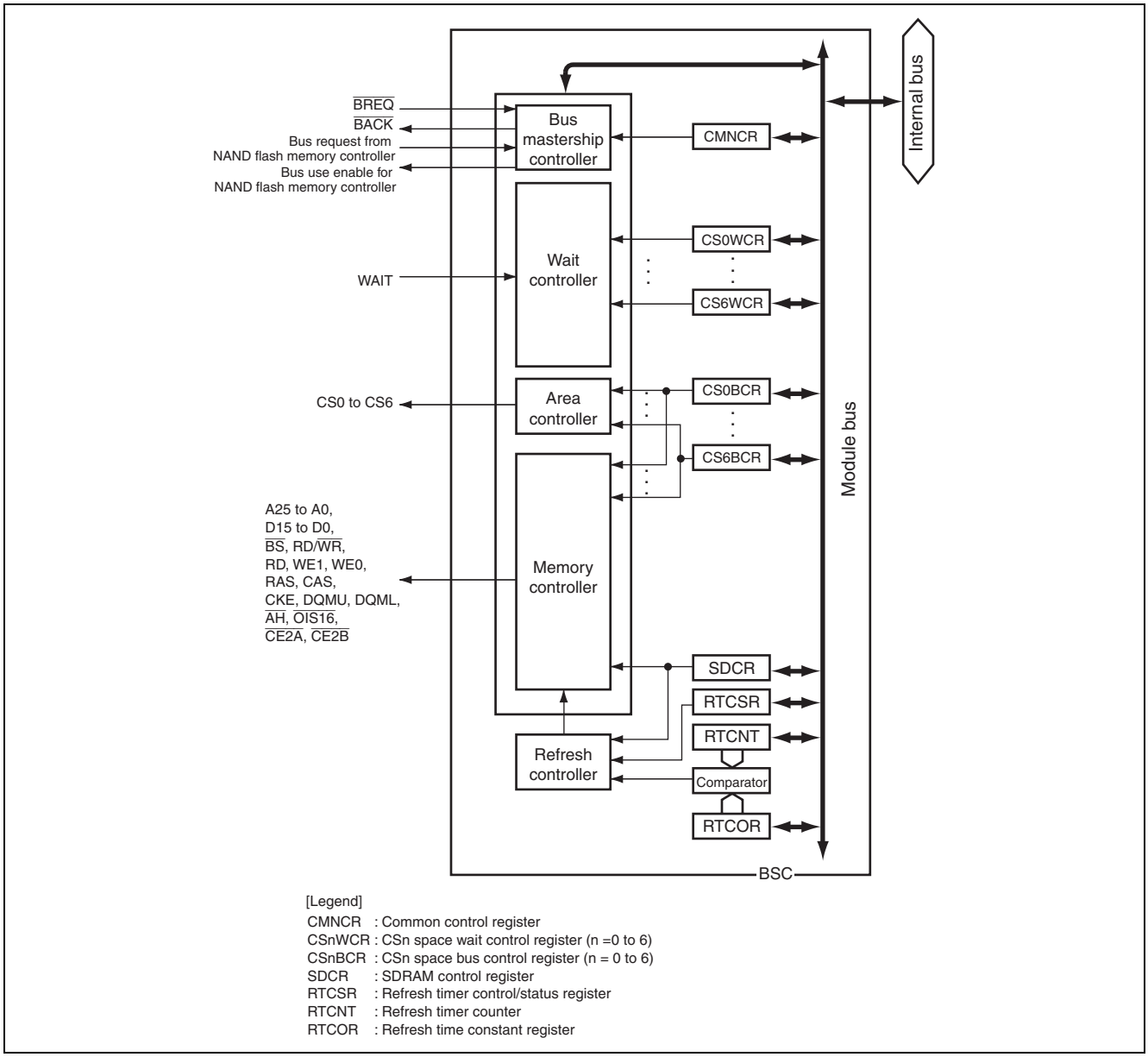


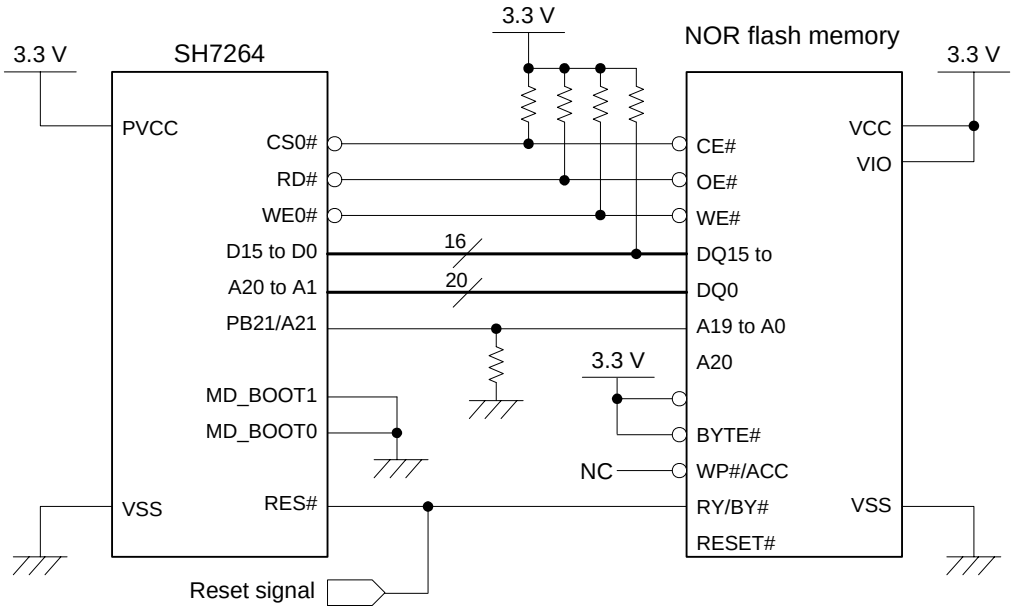
Figure 1 Bus State Controller Block Diagram

2.2 Interfacing Example

Table 3 lists the specifications of the NOR flash memory used in this application. Figure 2 shows the connection between the NOR flash memory and the SH7264. Figure 3 shows memory map related to the NOR flash memory.

Table 3 NOR Flash Memory Specifications

Item	Description
Part number	S29GL032N90
Density, organization	32 Mbits (2 Mwords × 16 bits): 1
Access time	Random access: 90 ns (at maximum) Page read: 25 ns (at maximum)
Boot block	Top boot or bottom boot can be identified by the model number of the memory



Note: Damping resistors on signal lines are not included. Install them according to the system configuration.

Figure 2 NOR Connection Circuit

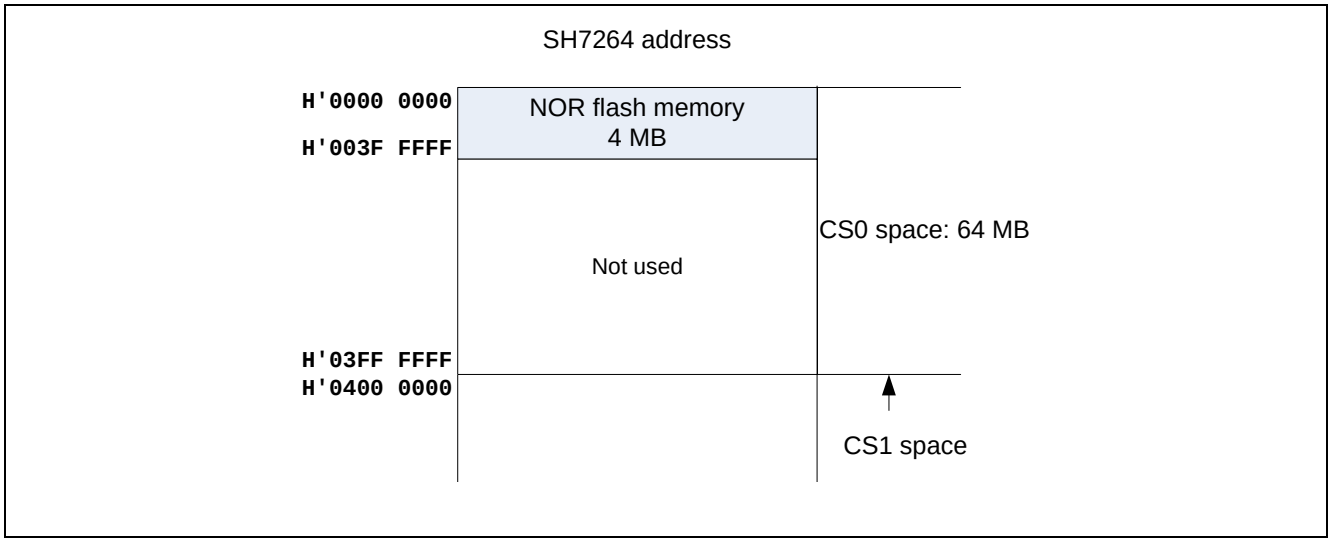


Figure 3 Memory Map associated with the NOR

Notes: 1 Data Bus Width and Boot Mode

On the SH7264 device, CS0 space (area 0) is fixed to 16-bit bus width. The NOR flash memory on CS0 must be connected to operate as 16-bit memory. The NOR flash memory is fixed to 16 bit operation by setting the BYTE# pin to high level.

To boot the SH7264 from NOR flash memory, fix the SH7264 MD_BOOT0 and MD_BOOT1 pins to low level (boot mode 0).

In boot mode 0, pins A20 to A1 are all set as address bus, however note that pins A21 to A25 are set as general-purpose I/O ports.

2. Pull up or pull down the control signal pins using the external resistors

Pins A21 to A25 and WE0# are configured as I/O port as default, and will be input by default on power up until the BSC is programmed, so a pull-up or pull-down is recommended to avoid improper operation of the NOR flash memory.

Pull down A21 to A25 to access address 0 in the NOR flash memory at power-on reset. Pins A22 to A25 are not used in this application.

In general, control signals will be undefined during the RESET period before the BSC is initialized, so to get more stable memory operation, pull up pins CS0#, RD#, and WE0# to high level using external resistors. Pull-ups are also recommended on any other CS# and WE# signals used in your design.

2.3 Setting Procedure

Figure 4 shows an example to configure the BSC when using CS0 space. For details on registers, refer to Chapter 9 Bus State Controller (BSC) in the SH7262 Group, SH7264 Group Hardware Manual.

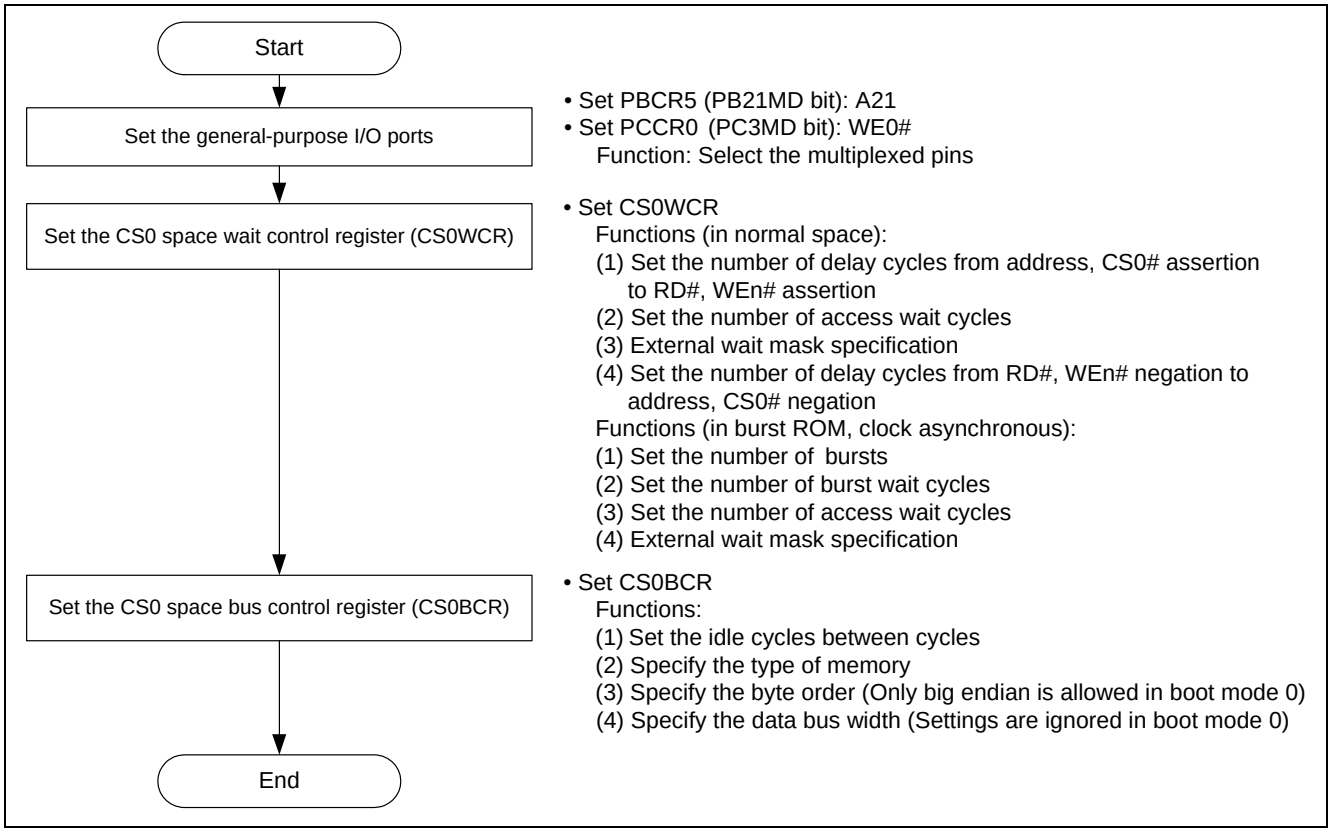


Figure 4 Bus State Controller and General-purpose I/O Port Setting Procedure (CS0 Space)

2.3.1 Setting Example When Using Random Access

Random access can be used in CS0 to CS6 spaces. Set bits TYPE [2:0] in the CSn space bus control register (CSnBCR), (n = 0 to 6) to "normal space (B'000)", according to the space to use.

Table 4 and Table 5 list examples to set the BSC when using CS0 space. For details on registers, refer to Chapter 9 Bus State Controller (BSC) and Chapter 32 General-purpose I/O ports in the SH7262 Group, SH7264 Group Hardware Manual.

Table 4 BSC Setting

Register Name	Address	Setting	Description
CS0 space bus control register (CS0BCR)	H'FFFC 0004	H'1240 0400	• IWW [2:0] = "B'001": Idle cycles between Write-Read and Write-Write: 1 idle cycle inserted • IWRWD [2:0], IWRWS [2:0] = "B'001": Idle cycles between Read-Write: 1 idle cycle inserted • IWRRD [2:0], IWRRS [2:0] = "B'000": Idle cycles between Read-Read: No idle cycles inserted • TYPE [2:0] = "B'000": Normal space • ENDIAN = "0": Big endian (note) • BSZ [1:0] = "B'10": 16-bit wide (note)
CS0 space wait control register (CS0WCR)	H'FFFC 0028	H'0000 0B41	• SW [1:0] = "B'01": Number of delay cycles from address, CS0# assertion to RD#, WE# Assertion: 1.5 cycles • WR [3:0] = "B'0110": Number of access wait cycles: 6 cycles • WM = "B'1": External wait input is ignored • HW [1:0] = "B'01": Number of delay cycles from RD#, WE# negation to address, CS# negation: 1.5 cycles

Note: In boot mode 0, data bus is fixed to 16-bit wide, and little endian cannot be set in area 0.

Table 5 General-purpose I/O Ports Setting

Register Name	Address	Setting	Description
Port B control register 5 (PBCR5)	H'FFFE 3824	H'0011	• PB21MD [1:0] = "B'01": Specify PB21 pin as A21
Port C control register 0 (PCCR0)	H'FFFE 384E	H'1011	• PC3MD [1:0] = "B'01": Specify PC3 pin as WE0#

2.3.2 Setting Example When Using Page Read

Page read can be used in CS0 and CS4 spaces. Set bits TYPE [2:0] in the CSn space bus control register (CSnBCR), (n = 0, 4) to "burst ROM, clock asynchronous (B'001)", according to the space to use.

Table 6 and Table 7 list examples to set the BSC when using CS0 space. For details on registers, refer to Chapter 9 Bus State Controller (BSC) and Chapter 32 General-purpose I/O ports in the SH7262 Group, SH7264 Group Hardware Manual.

Table 6 BSC Setting

Register Name	Address	Setting	Description
CS0 space bus control register (CS0BCR)	H'FFFC 0004	H'2480 1400	• IWW [2:0] = "B'010": Idle cycles between Write-Read/Write-Write: 2 idle cycles inserted • IWRWD [2:0], IWRWS [2:0] = "B'010": Idle cycles between Read-Write: 2 idle cycles inserted • IWRRD [2:0], IWRRS [2:0] = "B'000": Idle cycles between Read-Read: No idle cycles inserted • TYPE [2:0] = "B'001": Burst ROM (clock asynchronous) (1) • ENDIAN = "0" Big endian (2) • BSZ [1:0] = "B'10": 16-bit wide (2)
CS0 space wait control register (CS0WCR)	H'FFFC 0028	H'0022 03C0	• BST [1:0] = "B'10": 4-4 or 2-4-2 burst • BW [1:0] = "B'10": Number of burst wait cycles: 2 cycles • W [3:0] = "B'0111": Number of access wait cycles: 8 cycles • WM = "B'1": External wait input is ignored

Notes 1. Set bits TYPE [2:0] to burst ROM after setting the CS0WCR.
2. In boot mode 0, the data bus is fixed to 16-bit wide, and little endian cannot be set in area 0.

Table 7 General-purpose I/O Ports Setting

Register Name	Address	Setting	Description
Port B control register 5 (PBCR5)	H'FFFE 3824	H'0011	• PB21MD [1:0] = "B'01": Specify PB21 pin as A21
Port C control register 0 (PCCR0)	H'FFFE 384E	H'1011	• PC3MD [1:0] = "B'01": Specify PC3 pin as WE0#

2.4 NOR Flash Memory Timing Setting Example

When connecting a NOR flash memory, set the access speed of NOR flash memory, and wait cycles depending on the AC characteristics to the SH7264. This section describes setting examples when using random access, and page read.

For AC characteristics of the SH7264 and NOR flash memory, refer to the datasheet. In this example, the SH7264 operates at bus clock 72 MHz (tcyc = 13.9 ns).

Th and Tf values in the formulae in the following page use the number of delay cycles which is set either in bits SW [1:0] or HW [1:0] in the CS0 space wait control register (CS0WCR) −0.5. Assume that T1 = T2 = tcyc.

2.4.1 Timing Example When Using Random Access

This section describes an example to set the timing when using random access. Set registers to satisfy the following timing. Table 8 lists the setting example.

Table 8 Wait Setting Example

Item	Symbol	Number of cycles	Related register
Number of delay cycles from address, CS0# assertion to RD# and WEn# assertion	Th	1	Bits SW [1:0] in the CS0WCR register
Number of access wait cycles	Tw	6	Bits WR [3:0] in the CS0WCR register
Number of delay cycles from RD#, WEn# negation to address, CS0# negation	Tf	1	Bits HW [1:0] in the CS0WCR register
Idle cycles between Write-Read and Write-Write	Taw (w)	1	Bits IWW [2:0] in the CS0BCR register
Idle cycles for Read-Write in the same space	Taw (r)	1	Bits IWRWS [2:0] in the CS0BCR register

Read Timing:

- NOR flash memory tRC (Read cycle time)
  tRC (min.) ≤ (tcyc × Th − tAD1_max) + (T1) + (tcyc × Tw) + (T2) + (tcyc × Tf) + (tAD1_min): Figure 5

- NOR flash memory tACC (Address to output delay)
  tACC (max.) ≤ (tcyc × Th − tAD1_max) + (T1) + (tcyc × Tw) + (T2 − tRDS1_min): Figure 5

- NOR flash memory tCE (CE# access time)
  tCE (max.) ≤ (tcyc × Th − tCSD1_max) + (T1) + (tcyc × Tw) + (T2 − tRDS1_min): Figure 5

- NOR flash memory tOE (OE# access time)
  tOE (max.) ≤ (T1 − tRSD_max) + (tcyc × Tw) + (T2 − tRDS1_min): Figure 5

- NOR flash memory tOH (Output hold time from addresses CE# or OE#, whichever occurs first)
  tOH (min.) ≤ tRDH1 (min.): Figure 5

- NOR flash memory tDF (Output enable to output High Z)
  tDF (max.) ≤ T2 + (tcyc × Tf) + (tcyc × Taw (r)) − tRSD_max: Figure 6

Write Timing:

- NOR flash memory tCS (CE# setup time)
  tCS (min.) ≤ tCS_min: Figure 7

- NOR flash memory tAH (Address hold time)
  tAH(min) ≤ (T1 − tWED1_max) + (tcyc × Tw) + (T2) + (tcyc × Tf) + (tAD1_min): Figure 7

- NOR flash memory tWC (Write cycle time)
  tWC (min.) ≤ (tcyc × Th − tAD1_max) + (T1) + (tcyc × Tw) + (T2) + (tcyc × Tf) + (tAD1_min): Figure 7

- NOR flash memory tAS (Address setup time)
  tAS (min.) ≤ tAS_min: Figure 7

- NOR flash memory tWP (Write pulse width)
  tWP (min.) ≤ (T1 − tWED1_max) + (tcyc × Tw) + (tWED1_min): Figure 7

- NOR flash memory tDS (Data setup time)
  tDS (min.) ≤ (tcyc × Th − tWDD1_max) + (T1) + (tcyc × Tw) + (tWED1_min): Figure 7

- NOR flash memory tDH (Data hold time)
  tDH (min.) ≤ tWDH4_min: Figure 7

- NOR flash memory tWPH (Write pulse width high)
  tWPH (min.) ≤ (T2 − tWED1_max) + (tcyc × Tf) + [tcyc × Taw(w)] + (tcyc × Th) + (tWED1_min): Figure 8

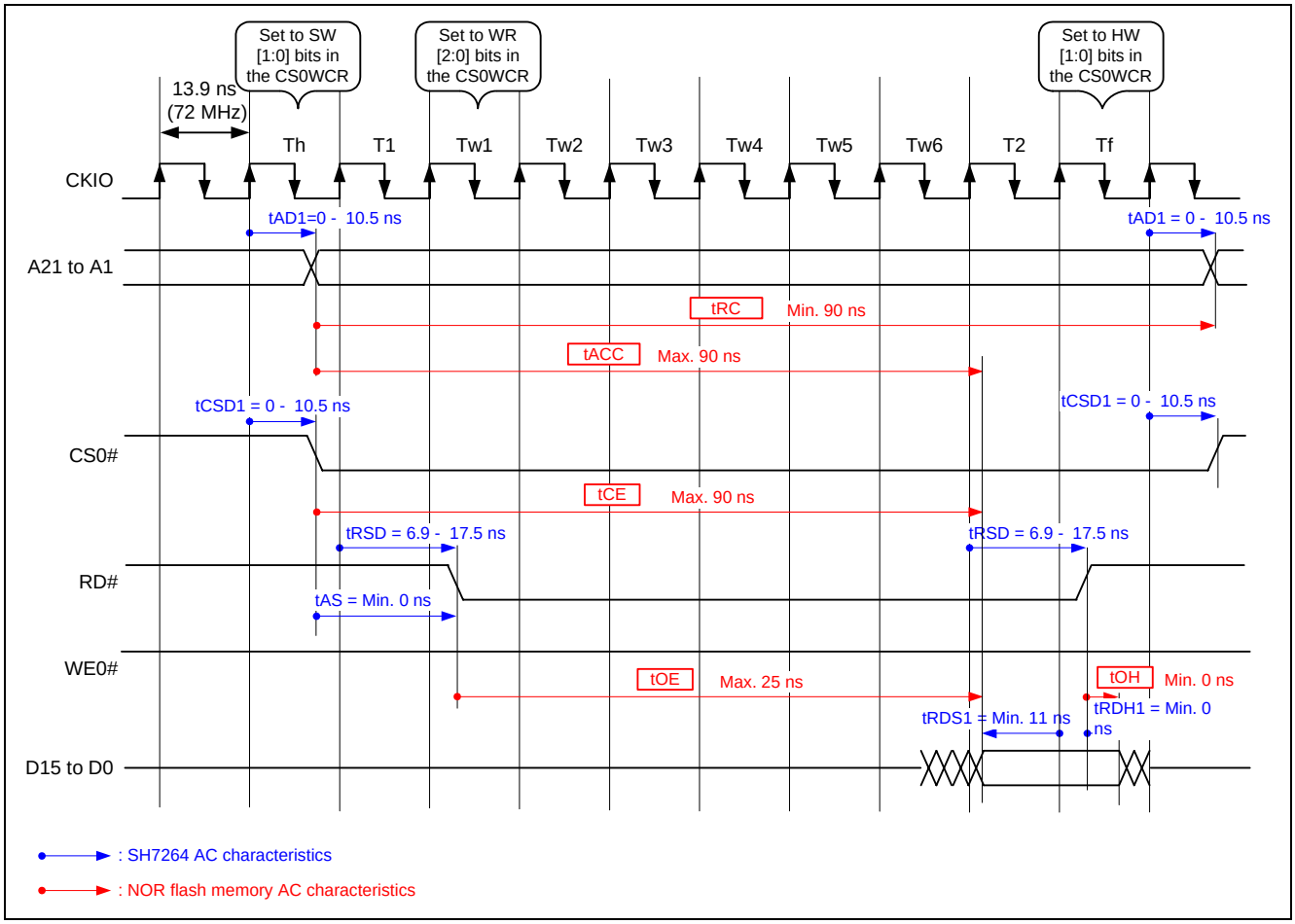


Figure 5 Read Timing Example When Using Random Access Read (1)

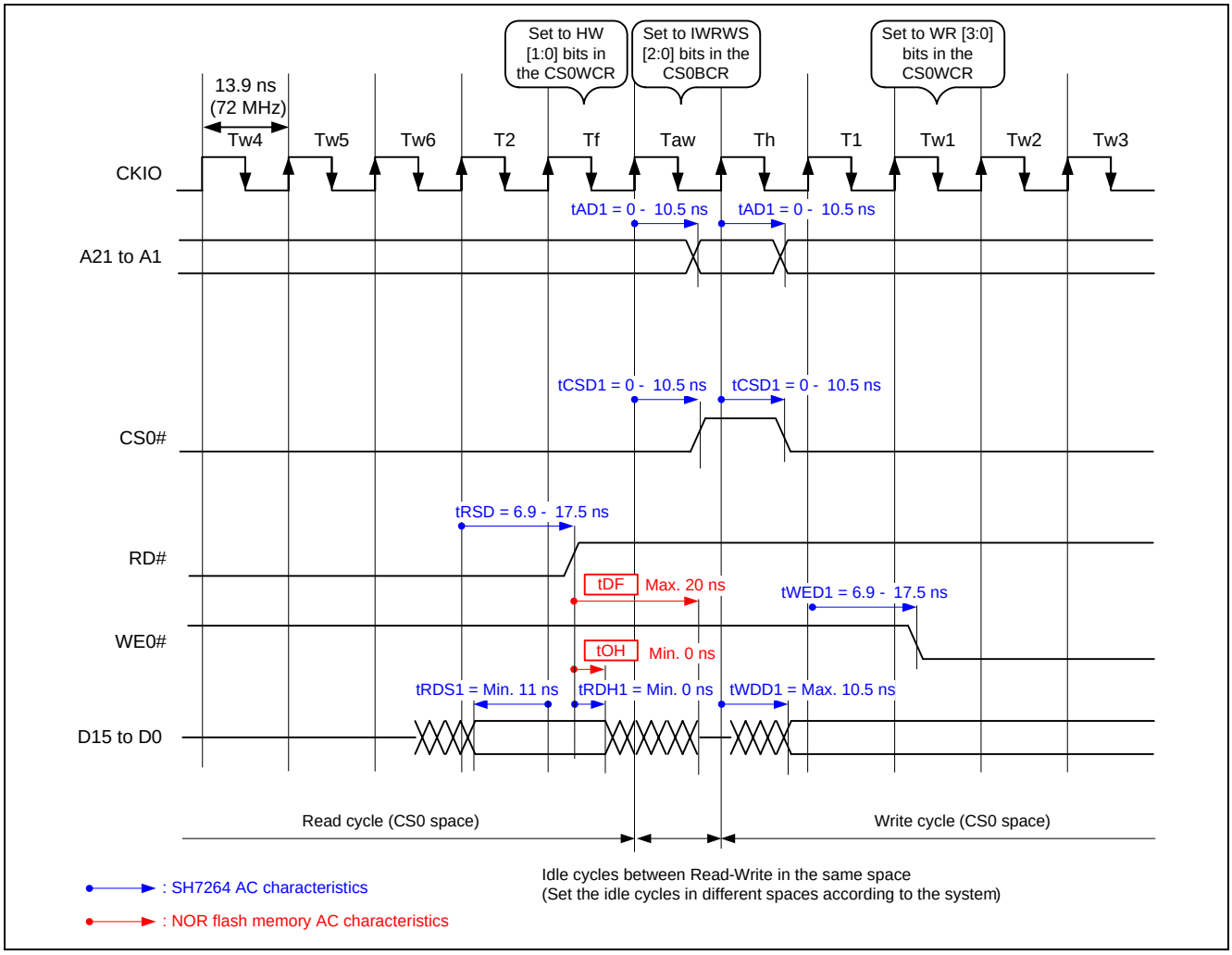


Figure 6 Read Timing Example When Using Random Access Read (2)

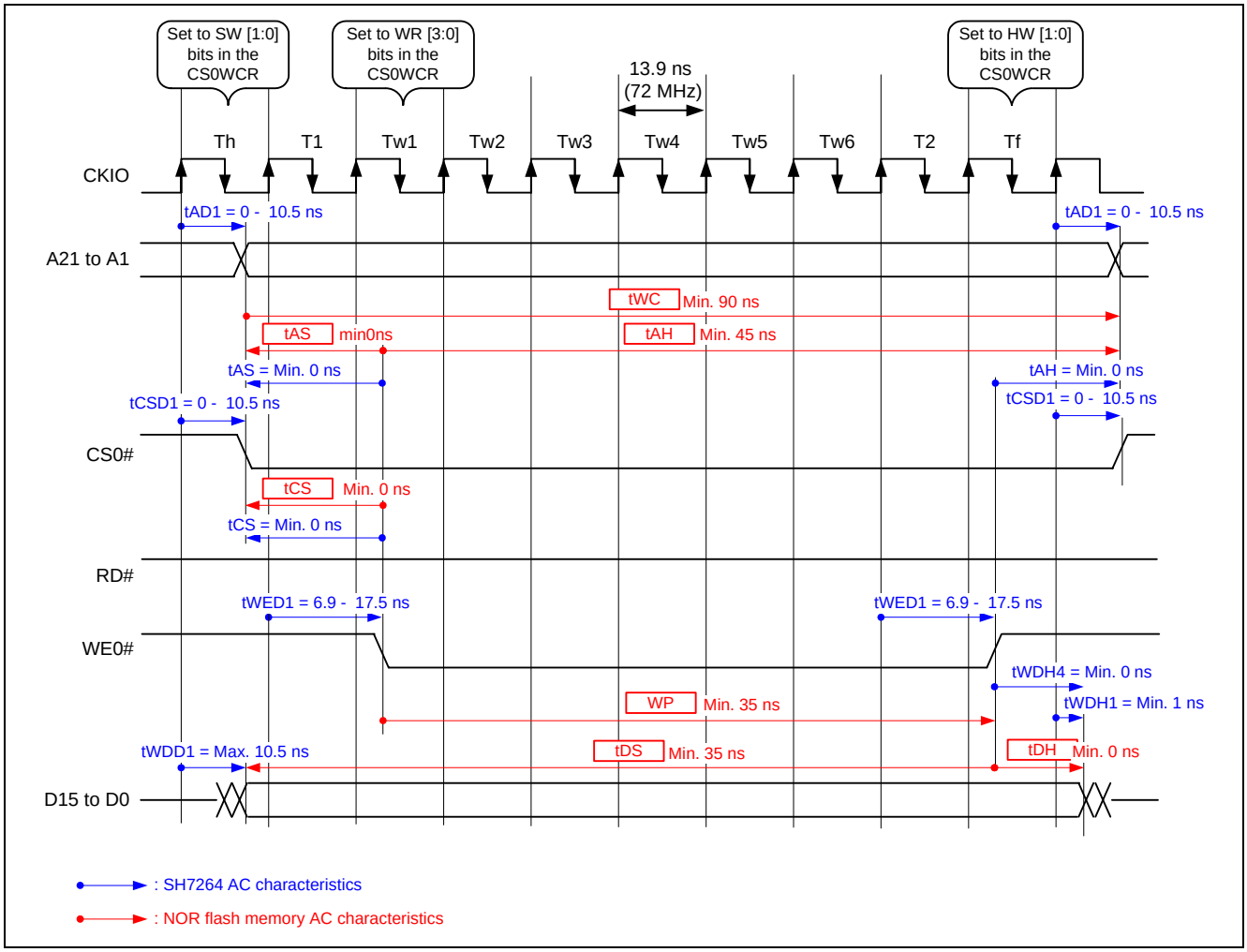


Figure 7 Write Timing Example When Using Random Access Read (1)

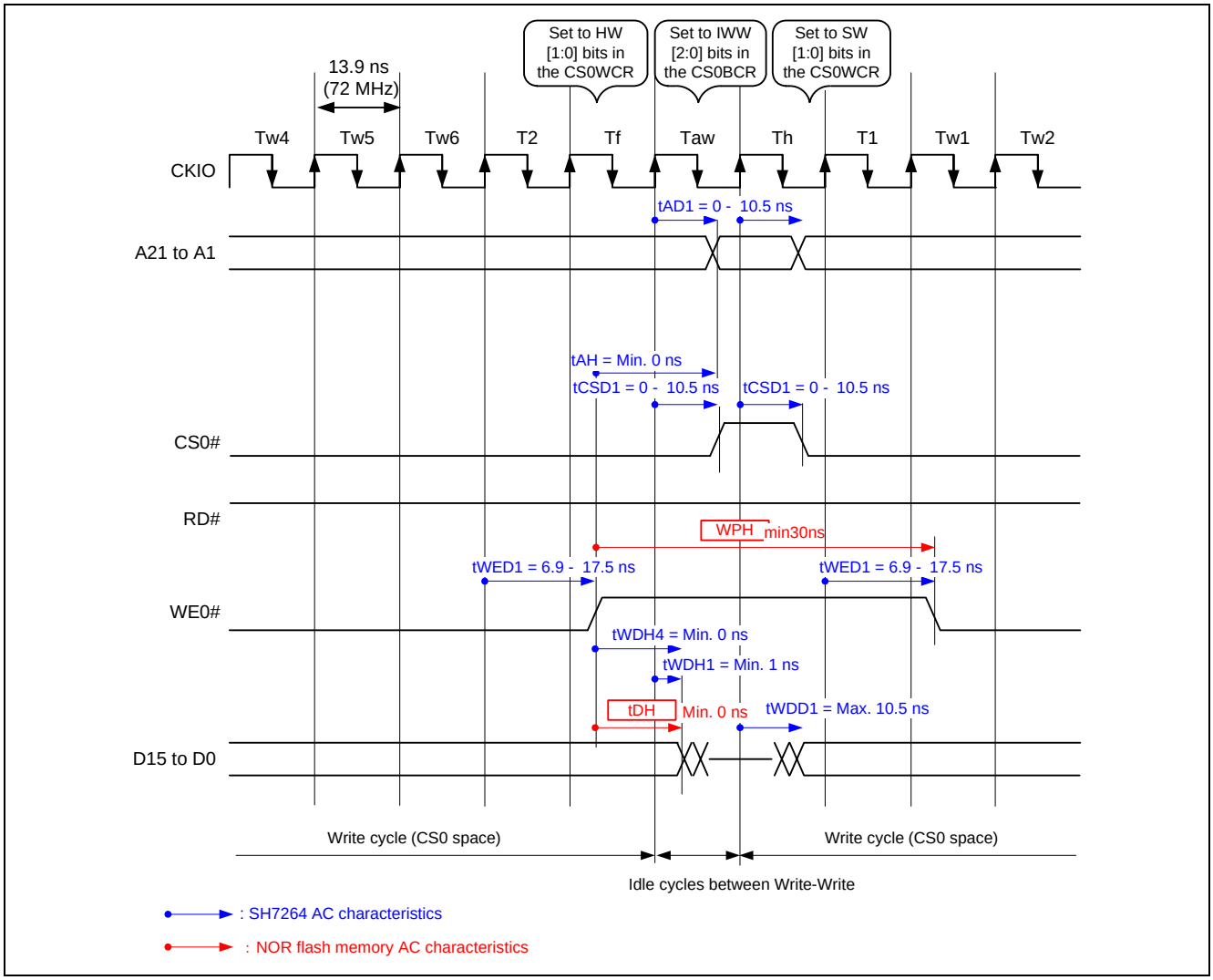


Figure 8 Write Timing Example When Using Random Access Read (2)

2.4.2 Timing Example When Using Page Read

This section describes an example to set the timing when using page read. Set registers to satisfy the following timing. Table 9 lists the setting example.

Table 9 Wait Setting Example

Item	Symbol	Number of cycles	Related register
Number of burst wait cycles	Twb	2	Bits BW [1:0] in the CS0WCR
Number of access wait cycles	Tw	8	Bits W [3:0] in the CS0WCR
Idle cycles between Write-Read and Write-Write	Taw(w)	2	Bits IWW [2:0] in the CS0BCR
Idle cycles between Read-Write in the same space	Taw(r)	2	Bits IWRWS [2:0] in the CS0BCR

Note: When using page read in CS0 space, CS assertion period cannot be extended. Therefore, Th and Tf values are 0 cycles.

Read Timing:

- NOR flash memory tRC (Read cycle time)
  tRC (min.) ≤ (T1 − tAD1_max) + (tcyc × Tw) + (tAD2_min): Figure 9

- NOR flash memory tACC (Address to output delay)
  tACC (max.) ≤ (T1 − tAD1_max) + (tcyc × Tw) + (T2B − tRDS3_min): Figure 9

- NOR flash memory tCE (Chip enable to output delay)
  tCE (max.) ≤ (T1 − tCSD1_max) + (tcyc × Tw) + (T2B − tRDS3_min): Figure 9

- NOR flash memory tOE (Output enable to output delay)
  tOE (max.) ≤ (T1 − tRSD_max) + (tcyc × Tw) + (T2B − tRDS3_min): Figure 9

- NOR flash memory tPACC (Page access time)
  tPACC (max.) ≤ (T2B − tAD2_max) + (tcyc × Twb) + (T2B − tRDS3_min): Figure 9

- NOR flash memory tOH (Output hold time from addresses, CE# or OE#, whichever occurs first)
  tOH (min.) ≤ tRDH3 (min.): Figure 9

- NOR flash memory tDF (Output enable to output High Z)
  tDF (max.) ≤ T2 + [tcyc × Taw (r)] − tRSD_max: Figure 10

Write Timing:

- NOR flash memory tCS (CE# setup time)
  tCS (min) ≤ tCS_min: Figure 11

- NOR flash memory tAH (Address hold time)
  tAH (min.) ≤ (T1 − tWED1_max) + (tcyc × Tw) + (T2) + (tAD1_min): Figure 11

- NOR flash memory tWC (Write cycle time)
  tWC (min.) ≤ (T1 − tAD1_max) + (tcyc × Tw) + (T2) + (tAD1_min): Figure 11

- NOR flash memory tAS (Address setup time)
  tAS (min.) ≤ tAS_min: Figure 11

- NOR flash memory tWP (Write pulse width)
  tWP (min.) ≤ (T1 − tWED1_max) + (tcyc × Tw) + (tWED1_min): Figure 11

- NOR flash memory tDS (Data setup time)
  tDS (min.) ≤ (T1 − tEDD1_max) + (tcyc × Tw) + (tWED1_min): Figure 11

- NOR flash memory tDH (Data hold time)
  tDH (min.) ≤ tWDH4_min: Figure 11

- NOR flash memory tWPH (Write pulse width high)
  tWPH (min.) ≤ (T2 − tWED1_max) + [tcyc × Taw (w)] + (tWED1_min): Figure 12

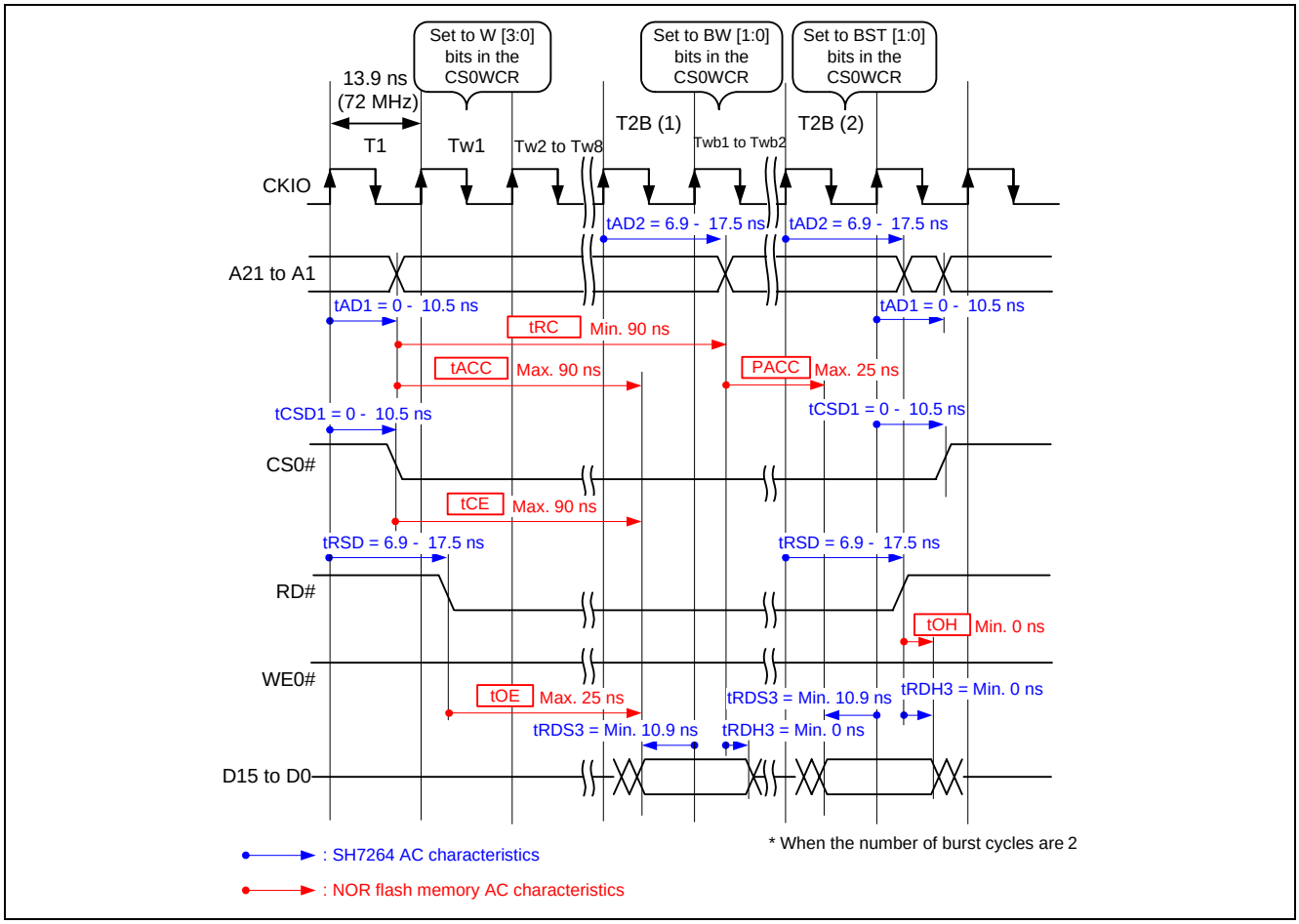


Figure 9 Read Timing Example When Using Page Read (1)

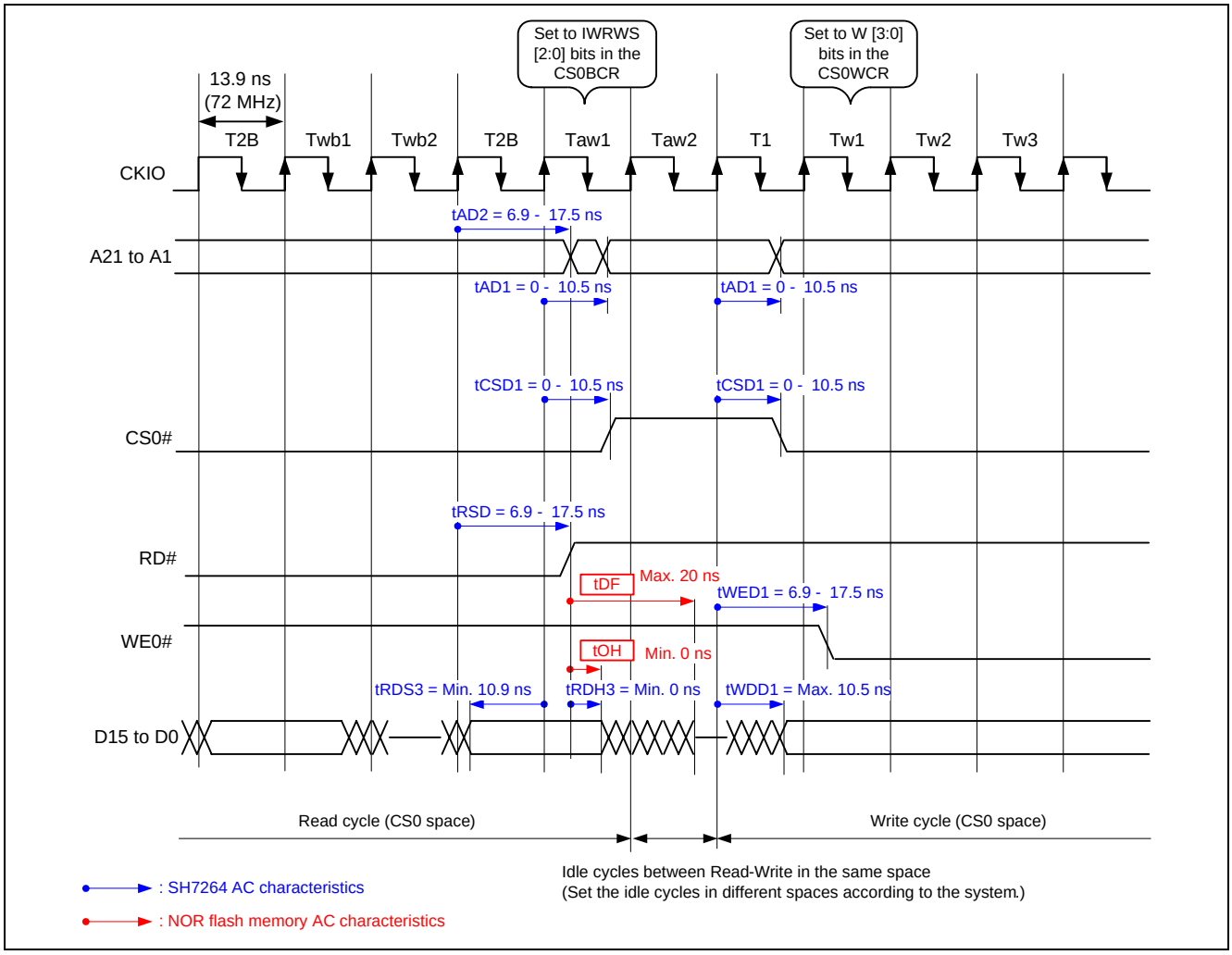


Figure 10 Read Timing Example When Using Page Read (2)

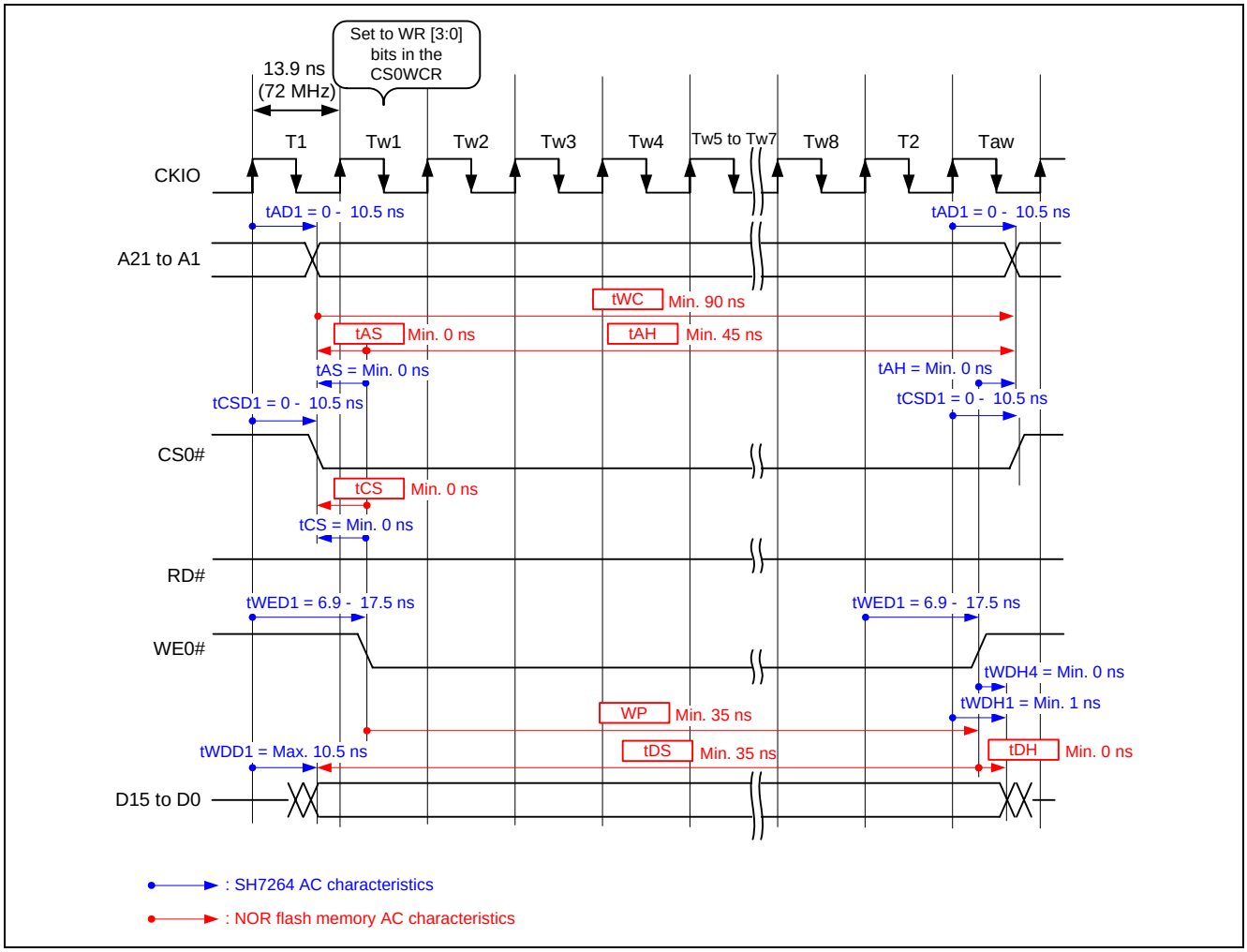


Figure 11 Write Timing Example When Using Page Read (1)

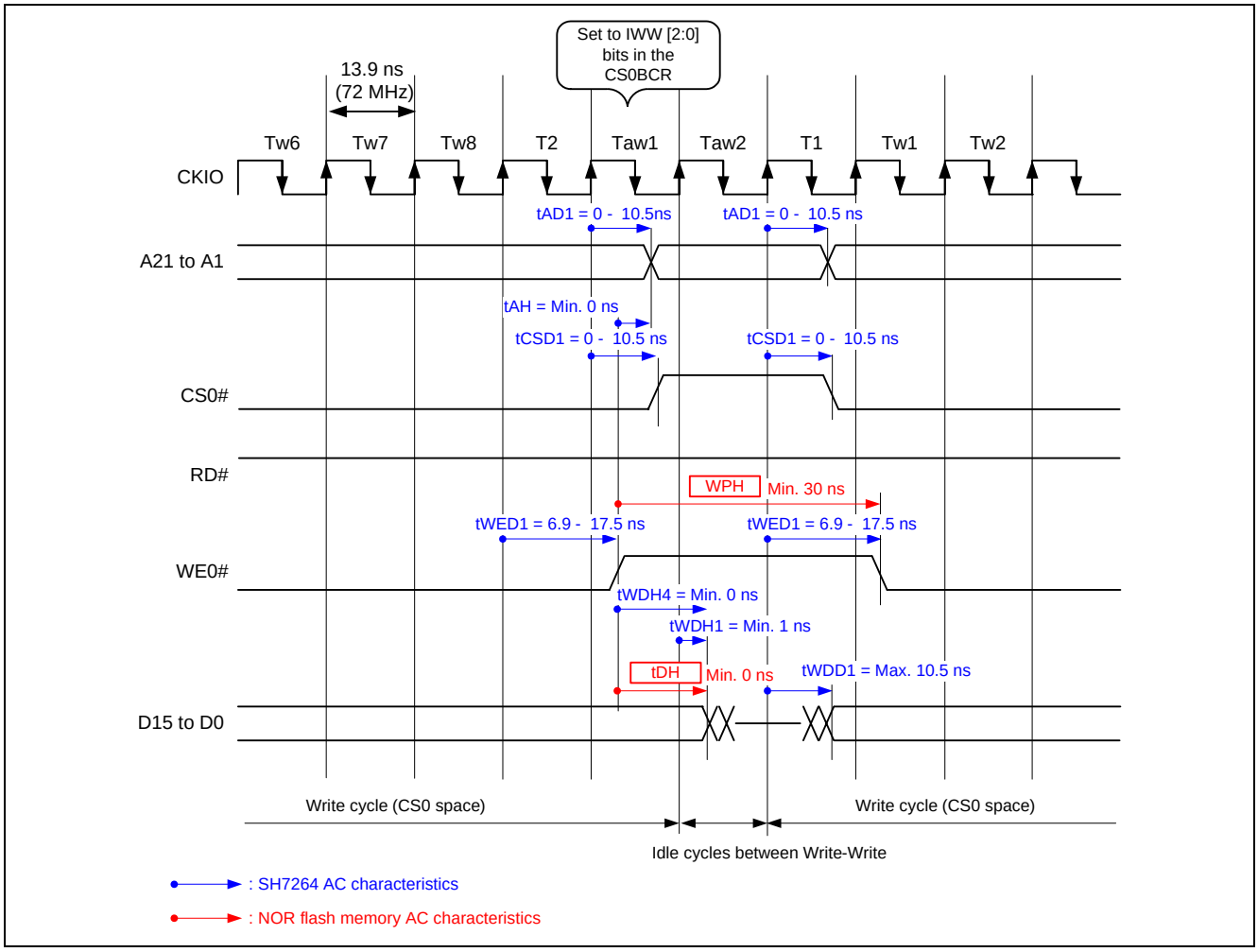


Figure 12 Write Timing Example When Using Page Read (2)

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "bsc_cs0.c" (1/3)

```
1       /***********************************************************************
2       *   DISCLAIMER
3       *
4       *   This software is supplied by Renesas Electronics Corp. and is only
5       *   intended for use with Renesas products. No other uses are authorized.
6       *
7       *   This software is owned by Renesas Electronics Corp. and is protected under
8       *   all applicable laws, including copyright laws.
9       *
10      *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11      *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12      *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13      *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14      *   DISCLAIMED.
15      *
16      *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
17      *   ELECTRONICS CORP. NOR ANY OF ITS AFFILIATED COMPANIES SHALL BE LIABLE
18      *   FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES
19      *   FOR ANY REASON RELATED TO THIS SOFTWARE, EVEN IF RENESAS OR ITS
20      *   AFFILIATES HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
21      *
22      *   Renesas reserves the right, without notice, to make changes to this
23      *   software and to discontinue the availability of this software.
24      *   By using this software, you agree to the additional terms and
25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      ************************************************************************
28      * (C) 2008(2010) Renesas Electronics Corporation. All rights reserved.
29      *""FILE COMMENT""************ Technical reference data *************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : bsc_cs0.c
32      *   Abstract    : SH7264 Initial Settings
33      *   Version     : 1.03.00
34      *   Device      : SH7262/SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *                 : C/C++ compiler package for the SuperH RISC engine family
37      *                 :                              (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50(CPU board)
40      *   Description :
41      ************************************************************************
42      *   History     : Dec.11,2008 Ver.1.00.00
43      *                 : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44      *                 : Mar.30,2010 Ver.1.02.00 Changed PAGEMODE setting
45      *                 : Apr.15,2010 Ver.1.03.00 Changed the company name
46      *""FILE COMMENT END""*****************************************************/
47      #include "iodefine.h"
48
49
```

3.3 Sample Program Listing "hwsetup.c" (2/3)

```
50    /*  CS0 PAGEMODE setting */
51    //#define PAGEMODE
52
53    /* ==== Prototype Declaration ==== */
54    void io_init_bsc_cs0(void);
55
56    #pragma section ResetPRG
57    /*""FUNC COMMENT""*****************************************************************
58     * ID           :
59     * Outline      : CS0 setting
60     *-------------------------------------------------------------------------------
61     * Include      : iodefine.h
62     *-------------------------------------------------------------------------------
63     * Declaration  : void io_init_bsc_cs0(void);
64     *-------------------------------------------------------------------------------
65     * Description  : Pin function controller (PFC) and bus state controller (BSC)
66     *                : are set, and the access timing to the Flash Memory of CS0 space
67     *                : is set.
68     *                : The PFC setting is set by bit manipulation not to change the PFC
69     *                : set value which is set by other process.
70     *-------------------------------------------------------------------------------
71     * Argument     : void
72     *-------------------------------------------------------------------------------
73     * Return Value : void
74     *-------------------------------------------------------------------------------
75     * Note         : None
76     *""FUNC COMMENT END""*************************************************************/
77    void io_init_bsc_cs0(void)
78    {
79      /* ==== PFC settings ==== */
80      PORT.PBCR5.BIT.PB21MD  = 1u;/* Set A21  */
81      PORT.PCCR0.BIT.PC3MD   = 1u;/* Set WE0# */
82
83
84    #ifdef PAGEMODE
85
86      /* ==== CS0WCR settings ====  */
87      BSC.CS0WCR.BROM_ASY.LONG = 0x002203C0ul;
88                                  /* Number of Burst: 4-4 or 2-4-2          */
89                                  /* Number of Burst Wait Cycles: 2 cycles  */
90                                  /* Number of Access Wait Cycles: 8 cycles     */
91
92
93
94      /* ==== CS0BCR settings ==== */
95      BSC.CS0BCR.LONG = 0x24801400ul;
96                                  /* Idle Cycles between Write-read Cycles  */
97                                  /*  and Write-write Cycles: 2 idle cycles     */
98                                  /* Idle Cycles between Read-write Cycls       */
99                                  /*                          : 2 idle cycles */
100                                 /* Type:Burst ROM (ASY)                    */
101                                 /* Data Bus Size: 16-bit                   */
```

3.4 Sample Program Listing "hwsetup.c" (3/4)

```
102
103   #else /* PAGEMODE */
104
105
106
107     /* ==== CS0WCR settings ====  */
108     BSC.CS0WCR.NORMAL.LONG = 0x00000b41ul;
109                                 /* Number of Delay Cycles from Address,   */
110                                 /*  CS0# Assertion to RD#,WEn Assertion   */
111                                 /*  : 1.5 cycles                          */
112                                 /* Number of Access Wait Cycles: 6 cycles    */
113                                 /* Delay Cycles from RD,WEn# negation to  */
114                                 /*  Address,CSn# negation: 1.5 cycles        */
115
116
117     /* ==== CS0BCR settings ==== */
118     BSC.CS0BCR.LONG = 0x12400400ul;
119                                 /* Idle Cycles between Write-read Cycles  */
120                                 /*  and Write-write Cycles : 1 idle cycle    */
121                                 /*  and read-write Cycles : 1 idle cycle  */
122                                 /* Type: Normal space                     */
123                                 /* Data Bus Size: 16-bit                  */
124
125   #endif /* PAGEMODE */
126   }
127
128   /* End of File */
129
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.05.09	—	First edition issued
2.00	Jul.23.10	All	Page read setting added Format changed

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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