Reliable Power Switch with Offline Memory for Privacy Applications

SLG47004

This application note describes how to design and build a reliable power switch with offline memory for privacy applications. It remembers its state even during power off for an indefinite time. The device also has an LED indicator with a fault monitoring system. Meaning, that if the LED malfunctions (brake or short circuit) the switch will go off.

The application note comes complete with a design file that can be found in the Reference section.

Contents

1. Terms and Definitions

ACMP	Analog Comparator
CNT/DLY	Counter-Delay
GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input / Output
I2C	Inter-Integrated Circuit Protocol
LED	Light Emitting Diode
MOSFET	Metal-oxide Semiconductor Field-effect Transistor
N-FET	N-type Field-effect Transistor
OSC	Oscillator
PCB	Printed Circuit Board
P-FET	P-type Field-effect Transistor
Pot	Potentiometer
SCL	Signal Clock
SDA	Signal Data
VREF	Voltage Reference
W&S	Wake and Sleep Timer

2. References

For related documents and software, please visit:

https://www.renesas.com/eu/en/products/programmable-mixed-signal-asic-ip-products/greenpak-programmable-mixed-signal-products/analogpak

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the AnalogPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide
[2] AN-CM-341 Reliable Power Switch with Offline Memory for Privacy Appications.gp, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47004 Datasheet, Renesas Electronics

3. Introduction

The circuit described in this document is designed for devices where privacy is prioritized. For example, in gadgets with a camera and/or microphone user has to be sure that the camera (microphone) is really turned off if the user wishes so even after the gadget was powered off and on again for a long period. Also, if someone with bad intentions wants to hide that the camera (microphone) is on by removing the LED indicator (or shortening it), the camera (mic) will be turned off automatically.

The circuit is not connected to the gadget's processor which makes it impossible to hack in and turn on/off the camera and/or microphone remotely.

Essentially, this circuit is a replacement for the mechanical toggle switch but uses a tiny pushbutton that allows easy integration into the gadget's design. See the block diagram in Figure 1 and the GreenPAK Designer project in Figure 2.

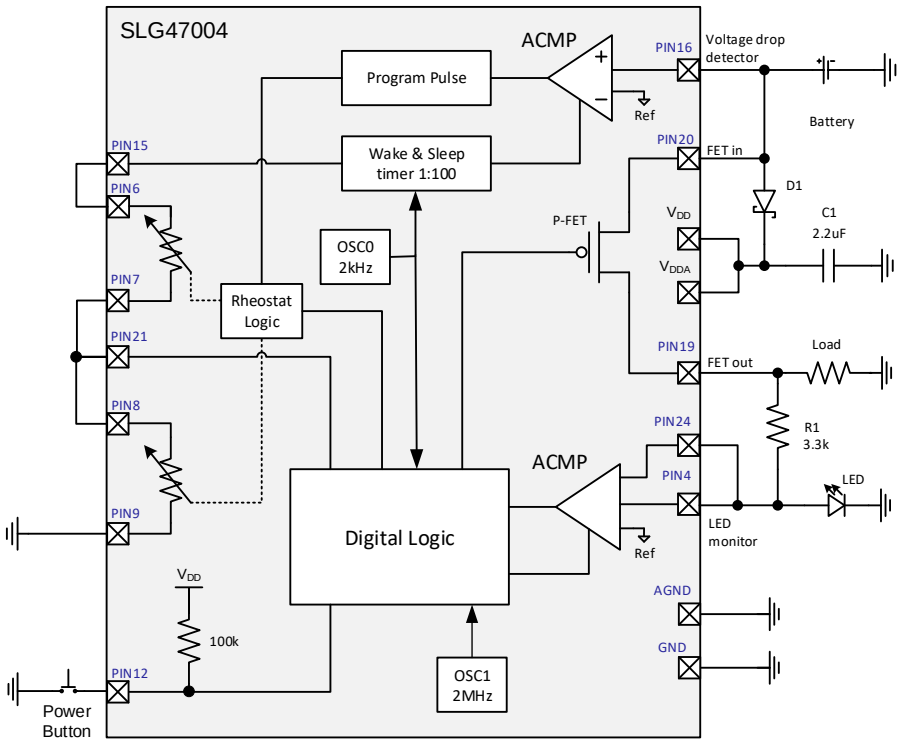

Figure 1: Reliable Power Switch with Offline Memory for Privacy Applications Block Diagram

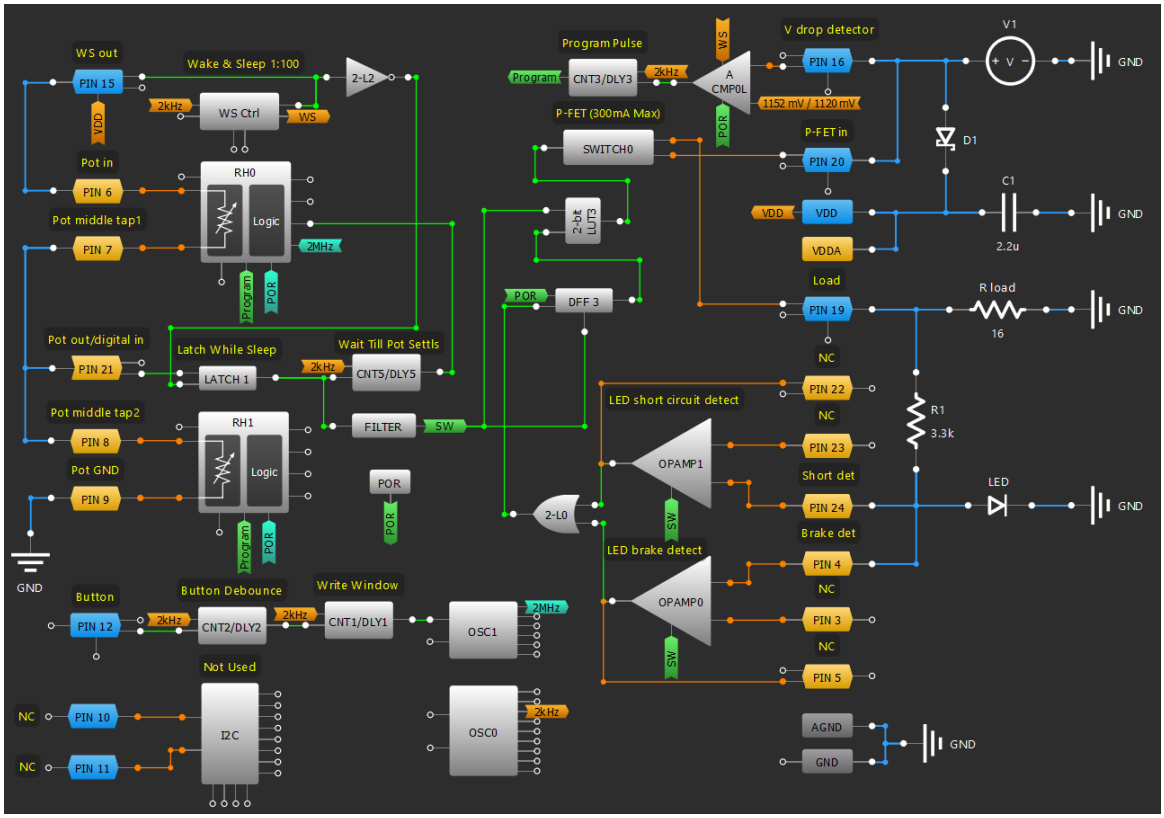

Figure 2: Reliable Power Switch with Offline Memory for Privacy Applications GreenPAK Designer Project

4. Design Operation

4.1 Schematic Design

The SLG47004 has two digital rheostats which can be configured as one digital potentiometer. One of its features is the ability to store its value after powering off. This feature is used in the current design as a 1-bit memory cell. Each time the button is pressed, the potentiometer RH0RH1 changes its value from 0 to 1023 or 1023 to 0 depending on the previous state. Resulting in changing voltage on the middle tap (Pins 7 and 8) from 0 to VDD and vice versa making it a simple switch that controls an internal power P-FET which in its turn is used to output the voltage to an external device. It is capable to deliver up to 300 mA.

The digital potentiometer (made from RH0 and RH1) has built-in memory with 1000 cycles which may not be enough for a long period of device usage if with every button pressed one cycle is used. So, in this circuit design memory writing sequence occurs only when the gadget (main device that this circuit is a part of) is powered off. For this purpose, ACMP0L is used as a voltage drop detector. If the power source voltage drops below 4.5 V, the ACMP will trigger the CNT3/DLY3 to form the «program» pulse initiating the memory writing sequence. Both VDD pins are connected to the source through the schottky diode and together with the 2.2 µF capacitor make power off delay. So, even if the source voltage drops rapidly to 0, the VDD voltage will slowly decay leaving enough time for the memory writing sequence to complete, see Figure 4. In order to measure the time required for the program sequence, a simple setup was used. It is known that the current consumption significantly increases during erase and write procedure. So, the power supply to the IC was connected through a 1 kΩ resistor with oscilloscope probes connected to it. As can be seen from Figure 5, the program time for both rheostats is 25.28 ms, and the current during the process is about 1 mA. It should be noted, that these values are very dependent on the voltage level, room temperature, and other factors. The program time may increase 2 to 3 times. So, the power-off delay must be longer than that. The program procedure starts when VDD drops below 4.5 V and should end at no less than 2.5 V (see the datasheet). The 2.2 µF capacitor ensures a long

enough power-off delay with room to spare, see Figure 4. Note that the capacitor type should be chosen with low leakage.

Also, since the potentiometer is connected between VDD and GND, there will be a constant current flowing through it: $\frac{5\ \text{V}}{100\ \text{k}\Omega} = 50\ \mu\text{A}$, which is in order of magnitude more than the quiescent current of the SLG47004. So, to reduce overall current consumption, the Wake and Sleep timer is used. It is set to 1:100, meaning that the current will flow through the potentiometer only once in a hundred of clocks of the OSC0. Approximately 0.49 ms wake and 49 ms sleep. As a result, the quiescent current of the device described here is close to 3 µA in an off state, which makes it perfect for battery-operated gadgets.

As previously mentioned, the designed device is equipped with the LED monitor. Two OPAMPs configured as ACMPs are used for this purpose. OPAMP0 senses the LED brake and OPAMP1 senses the LED short circuit. In both cases, it causes switching off of the P-FET and powering down the load (camera/mic). Also, both OPAMPs are enabled only when the switch is on allowing battery saving in an off state.

This design is also equipped with an internal button debounce delay (CNT2/DLY2) instead of the typical external RC filter in such cases.

4.2 Macrocells Operation

Pin12 is configured as a digital input with Schmitt trigger with a 100k pull-up resistor. It serves as an input for the pushbutton, see the block diagram in Figure 1. Then the signal goes through the 30 ms debounce delay (CNT2/DLY2) triggering the 1.46 ms one shot (CNT1/DLY1) which starts the OSC1 (2.048 MHz) forming a Write Window with a series of pulses in order to change the state of the potentiometer RH0RH1. See the oscilloscope screenshot in Figure 3.

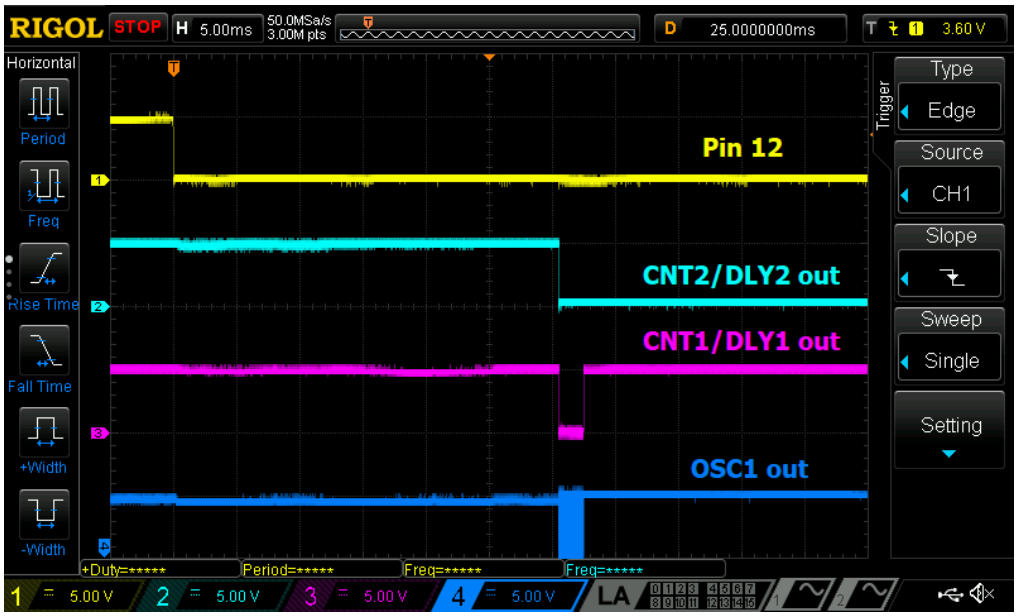

Figure 3: Write Window

OSC0 serves as a clock for all counter-delays in this design. Since it has a very low power consumption (0.44 µA), it is set to Force Power On.

As mentioned in section 4.1 Schematic Design, the SLG47004 has two rheostats which in this project are configured as one digital potentiometer. Its upper and lower pins (Pins 6 and 9) are connected in-between ground and Pin 15, which is an output for the W&S timer. The middle tap (Pins 7 and 8) is connected to Latch 1 through a digital input with Schmitt trigger Pin 21. The Latch 1 latches the potentiometer state while sleep (using an inverted W&S signal) making an appearance as if the potentiometer is constantly connected to VDD but consumes a hundred times less current. After the latch, the signal goes to a potentiometer's Up/Down input through a 2.44 ms delay (CNT5/DLY5) needed for the pot to settle in. This signal flips the potentiometer's count

up or down with every next write window. Simultaneously, this signal goes through the filter (filtering a 20 ns spike appearing due to latche's lag) to 2-bit LUT3. The LUT controls the output power P-FET (Pins 19 and 20).

The LED monitor is built of OPAMP0 and OPAMP1 and analog inputs Pins 4 and 24. It detects LED's short circuit or circuit brake and with the help of 2-bit LUT0 and DFF3 shuts down the P-FET if the LED malfunctions.

The Wake and Sleep timer (WS Ctrl) plays an important role in saving energy if the device is battery operated. Since this project is using analog macrocells which are the most «energy-hungry», the W&S allows saving energy by powering on those macrocells for a short period of time. The wake-to-sleep ratio is set to 1:100.

The CNT3/DLY3 together with ACMP0L start the pot's «program sequence» as described in section 4.1 Schematic Design, see the block diagram in Figure 1 and the oscilloscope screenshots in Figure 4.

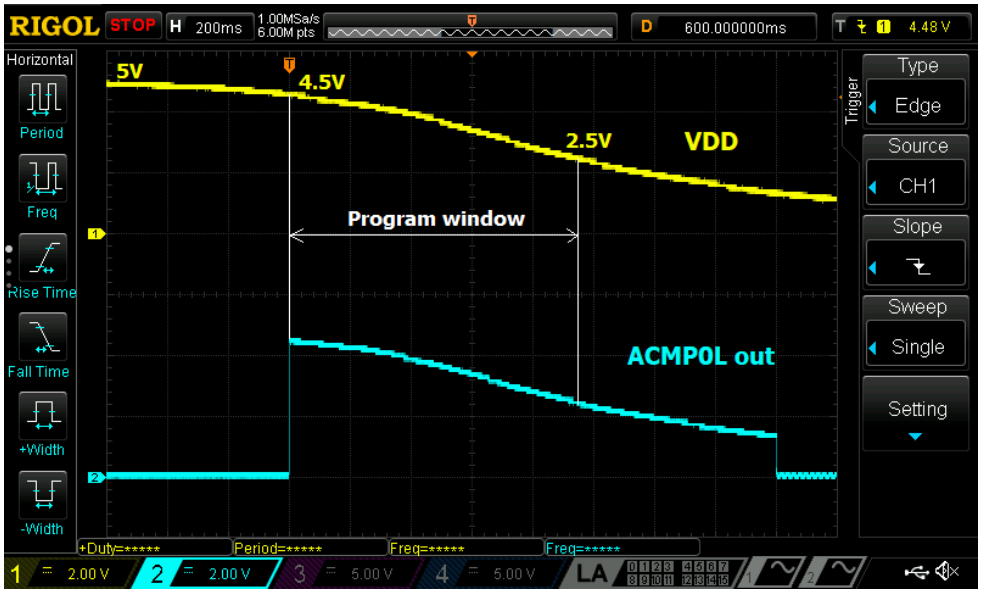

Figure 4: Voltage Drop Detection and Program Pulse

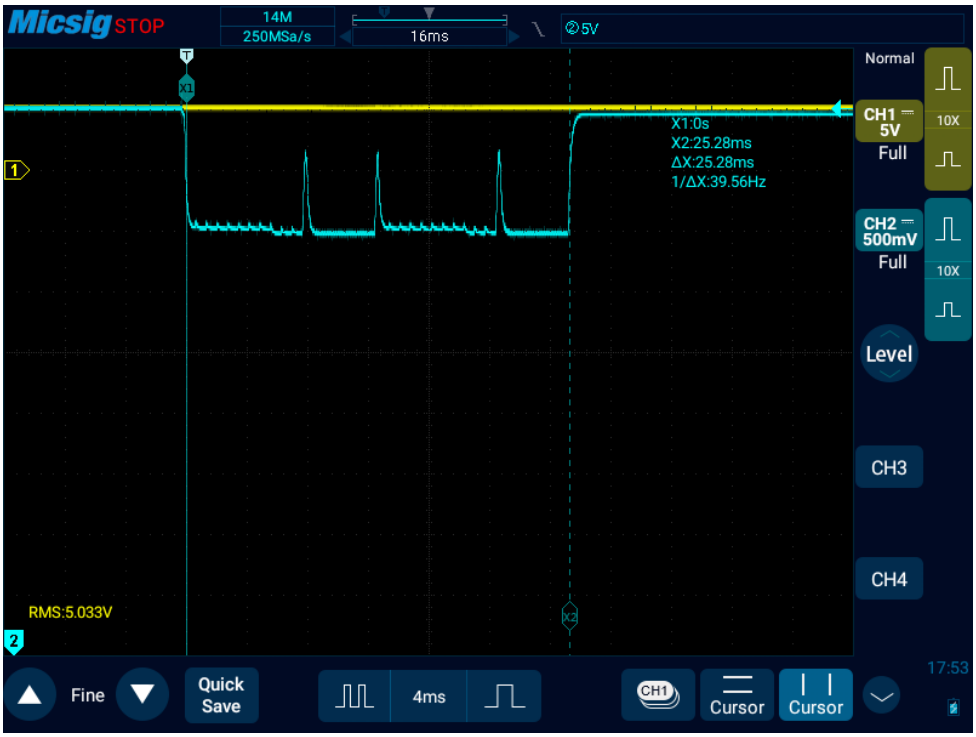

Figure 5: Voltage Drop During Program Procedure

It should be noted that the I²C macrocell along with its Pins 10 and 11 are used only to program the chip during production and should not be used during device operation. Pins 10 and 11 should be left unconnected on the PCB.

4.3 Macrocell Configuration

Table 1: PINs

Properties	PIN µto 9, 16, and 20, 22 to 24	PIN 19	PIN 10 and 11	PIN 12	PIN 15	PIN 21
I/O selection	Analog input/output	Analog input/output	Digital input	Digital input	Digital output	Digital input
Input mode OE=0	Analog input/output	Analog input/output	Digital in without Schmitt trigger	Digital in with Schmitt trigger	None	Digital in with Schmitt trigger
Output mode OE=1	Analog input/output	Analog input/output	None	None	1x push pull	None
Resistor	Floating	Pull Down	Floating	Pull Up	Floating	Floating
Resistor value	Floating	1M	Floating	100K	Floating	Floating

Table 2: FILTER/EDGE DETECT

FILTER/EDGE DET	
Type	FILTER
Output polarity	Inverted (nOUT)

Table 3: LUT

IN1	IN0	2-bit LUT0	2-bit LUT2	2-bit LUT3
0	0	0	Inverter	0
0	1	1		0
1	0	1		1
1	1	1		0

Table 4: DFF/LATCH

Properties	2-bit LUT1/DFF/LATCH1	3-bit LUT0/DFF/LATCH3
Type	DFF/LATCH	DFF/LATCH
Mode	LATCH	DFF
Second Q select	--	Q of first DFF
nSet/nReset option	None	nRESET
Initial polarity	Low	Low

Properties	2-bit LUT1/DFF/LATCH1	3-bit LUT0/DFF/LATCH3
Q output polarity	Inverted (nQ)	Non-inverted (Q)
Active level for RST/SET	--	Low level

Table 5: Oscillators

Properties	OSC0	OSC1
Control pin mode	Power down	Power down
OSC power mode	Force Power On	Force Power On
Clock selector	OSC	OSC
CLK predivider by:	1	1
OUT0 second divider by:	1	1
OUT1 second divider by:	1	1

Table 6: Digital Rheostat

Properties	RH0	RN1
Mode	None	Potentiometer
Charge Pump Enable	From matrix	From matrix
Charge Pump Clock	Auto selection	Auto selection
Auto-Trim	Disable	--
Active level for UP/DOWN	Up when LOW	--
Resistance (initial data)	0	--
UP/DOWN source	Ext. (From matrix)	--
Clock	Ext. Clock (From matrix)	--

Table 7: Analog Switch

Properties	SWITCH0
Mode	Analog Switch
Big PMOS control	By Matrix
Small NMOS enable	Disable
Half Bridge Dead Time Select	Bypass

Table 8: CNT/DLY

Properties	16-bit WS Ctrl (MF0)	8-bit CNT1/DLY1 (MF1)	8-bit CNT2/DLY2 (MF2)	8-bit CNT3/DLY3 (MF3)	8-bit CNT5/DLY5 (MF5)
Multi-function mode	CNT/DLY	CNT/DLY	CNT/DLY	CNT/DLY	CNT/DLY
Type	Wake sleep controller	--	--	--	--
Mode	--	One shot	Delay	One shot	Delay
Counter data	100	2	61	1	4
Edge select	High level reset	Falling	Both	Falling	Both
DLY IN init. value	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial

Properties	16-bit WS Ctrl (MF0)	8-bit CNT1/DLY1 (MF1)	8-bit CNT2/DLY2 (MF2)	8-bit CNT3/DLY3 (MF3)	8-bit CNT5/DLY5 (MF5)
Output polarity	Non-inverted (OUT)	Inverted (nOUT)	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)
ACMP0L wake sleep	Enable	--	--	--	--
ACMP1L wake sleep	Enable	--	--	--	--
At OSC0 power down	Force sleep (Low)	--	--	--	--
ACMP0L wake time selection	Short wake time	--	--	--	--
ACMP1L wake time selection	Short wake time	--	--	--	--
Up signal sync	Bypass	--	--	--	--
Keep signal sync	Bypass	--	--	--	--
Mode signal sync.	Bypass	Bypass	Bypass	Bypass	Bypass
FSM SET/RST Selection	Reset to 0	--	--	--	--
Clock	OSC0	OSC0	OSC0	OSC0	OSC0

Table 9: ACMP

Properties	ACMP0L
IN+ gain	x0.25
Vref LPF	Disable
Low power start up	Disable
Sampling mode	Disable
Vref source selection	2.048 V
Connections	
IN+ source	PIN 16 (GPIO2)
IN- Low to High source	1152 mV
IN- Low to Low source	1120 mV

Table 10: OPAMP

Properties	OPAMP0	OPAMP1
Mode	ACMP mode	ACMP mode
Bandwidth Selection	128 kHz	128 kHz
Charge Pump	Enable CP	Enable CP
Supporting Blocks On/Off	Follows OPAMP	Follows OPAMP
Vref connection	To IN+	To IN-
Vref	1024 mV	VDDA * (50 / 60)

Table 11: VREF

Properties	VREF OPAMP0	VREF OPAMP1
Enable selection	From register	From register
Register enable	Dynamic On/Off	Dynamic On/Off
Input voltage selection	VDDA	2.048 V
Output selection	VDDA * (50 / 60)	1024 mV

I²C Settings: default

5. Conclusions

Nowadays in modern society privacy concern is raised more often than ever. Big tech companies are constantly being accused of secretly gathering users' personal information and even selling it to third-party entities. In times when nearly every household has at least one gadget with a camera and microphone, besides smartphones, people start thinking twice about the trust they give to the manufacturer and service provider before buying another device. There were countless times when cameras were hacked and controlled remotely. People began installing external camera covers and taping a microphone hole. As a solution to this problem, a mechanical toggle switch can be installed on a camera/mic by the manufacturer ensuring protection against hackers and also serving as a visual indicator of the on/off state. But the downside is bad design and ergonomics.

The circuit described in this document does all the mechanical toggle switch can do, but uses a micro pushbutton that can be easily integrated into the gadget’s design. The described power switch just like a mechanical one has a memory, meaning if the user turned it off – it stays off. In the case of this design, an LED is used as a power indicator. It has fault protection, so for whatever reason, if the LED is not glowing, the load (camera/mic) will be also off ensuring desired privacy protection. Also, the device has a very low current consumption in an off state of approximately 3 µA which is perfect for most battery-powered devices.

6. Revision History

Revision	Date	Description
1.00	Jan 19, 2022	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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