

Application Note

SLG51000 GPIO Use Cases

AN-CM-267

Abstract

This application note presents several examples on how to use the GPIOs in SLG51000 for various applications.

SLG51000 GPIO Use Cases

Contents

Abstract	1
Contents	2
Figures	2
Tables	2
1 Terms and Definitions	3
2 References	3
3 Introduction	4
4 GPIO Use Cases as Inputs	5
4.1 Single GPIO Global Control	5
4.2 Manual Discrete Control of Individual LDOs	6
4.3 I ² C Control.....	7
4.4 Combinational Logic Control	8
4.5 Automatic Power Sequencing.....	9
5 GPIO Use Cases as Outputs	11
5.1 Fault Signal Output	11
6 Conclusions	13
Revision History	13

Figures

Figure 1: SLG51000 Pinout.....	4
Figure 2: Block Diagram of Single GPIO Use Case.....	5
Figure 3: Screenshot of Single GPIO Use Case (w/ Labels)	5
Figure 4: Block Diagram of Discrete Equivalent Use Case.....	6
Figure 5: Screenshot of Discrete Equivalent Use Case (w/ Labels)	6
Figure 6: Block Diagram of I ² C Software Control Use Case	7
Figure 7: Screenshot of I ² C Software Control Use Case	7
Figure 8: Screenshot of I ² C Software Control Use Case (w/ Labels).....	7
Figure 9: Block Diagram of Combinational Logic Control Use Case	8
Figure 10: Screenshot of Combinational Logic Control Use Case.....	8
Figure 11: Block Diagram of Power Sequence Trigger Use Case (Multiple GPIO)	9
Figure 12: Screenshot of Power Sequence Trigger Use Case (Multiple GPIO)	10
Figure 13: Resource Connection (w/ Labels).....	10
Figure 14: Screenshot of Timing Diagram between each Slot.....	11
Figure 15: Block Diagram of Fault Signal Output Use Case.....	12
Figure 16: Screenshot of Fault Signal Output Use Case	12

Tables

Table 1: GPIO Pin Descriptions	4
Table 2: Matrix Interconnect Input Ports	12

SLG51000 GPIO Use Cases

1 Terms and Definitions

GPIO	General purpose input output
GPI	General purpose input
LDO	Low drop out regulator
LUT	Look-up table
CS	Chip select
SDA	Serial data
SCL	Serial clock
ILIM	Current limit

2 References

- [1] SLG51000 Datasheet
- [2] [AN-CM-267 GPIO Use Cases.gp Design file](#)

Author: Yu-han Sun

SLG51000 GPIO Use Cases

3 Introduction

The SLG51000 is a 20-pin device that has 7 LDOs with 5 GPIOs, 1 GPI, and a Chip Select pin to control them. This document will depict the many ways to use the SLG51000's GPIOs in a system.

In all the following examples, it is assumed that VDD, CS, and GND are appropriately connected. Please also note that any combination of the following examples can be used simultaneously.

Screenshots are taken directly from the SLG51000 Development Software which is available to users as a simple yet effective tool to configure the SLG51000 for specific application requirements.

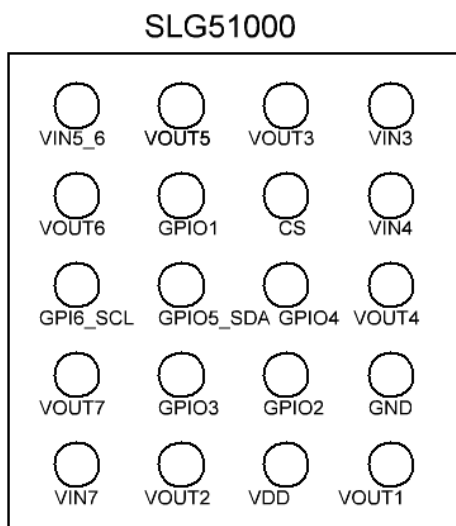


Figure 1: SLG51000 Pinout

Table 1: GPIO Pin Descriptions

Pin Name	Type	Description
GPIO1	Digital Input/Output Open Drain	1.2 V/1.8 V input cell, open-drain output
GPIO2	Digital Input/Output Open Drain	1.2 V/1.8 V input cell, open-drain output
GPIO3	Digital Input/Output Open Drain	1.2 V/1.8 V input cell, open-drain output
GPIO4	Digital Input/Output Open Drain	1.2 V/1.8 V input cell, open-drain output
GPIO5_SDA	Digital Input/Output Open Drain	1.2 V/1.8 V input cell, open-drain output, or I ² C Serial Clock Line (SDA)
GPI6_SCL	Digital Input	1.2 V/1.8 V input cell, or I ² C Serial Clock Line (SCL)

SLG51000 GPIO Use Cases

4 GPIO Use Cases as Inputs

In the following section, we will explore ways to use GPIOs configured as inputs for different applications.

4.1 Single GPIO Global Control

In cases where the number of GPIOs are limited, a single GPI(O) can be used to enable/disable any number of LDOs.

Resources:

- One GPI(O)
- Seven LDOs

Connect any one GPI(O)s to up to seven LDO Enable inputs.

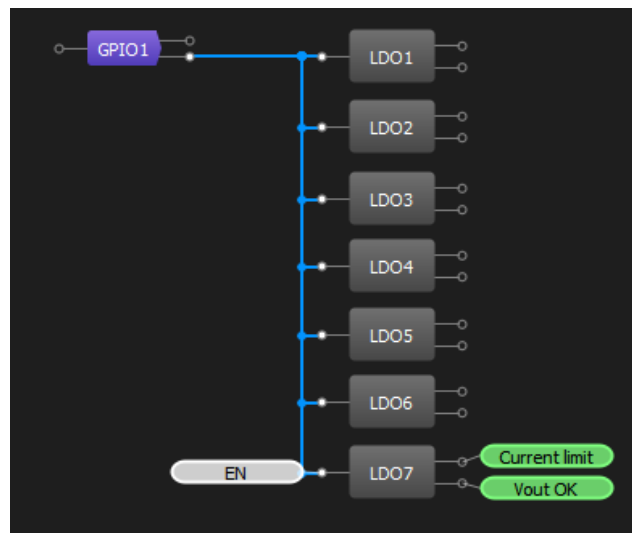
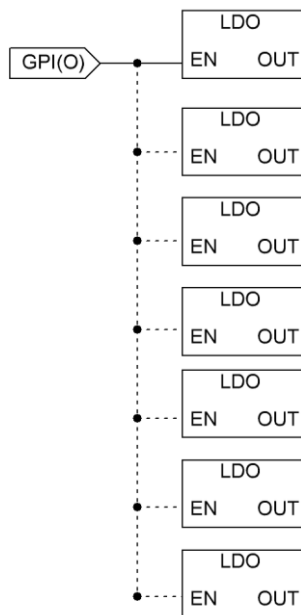


Figure 2: Block Diagram of Single GPIO Use Case

Figure 3: Screenshot of Single GPIO Use Case (w/ Labels)

SLG51000 GPIO Use Cases

4.2 Manual Discrete Control of Individual LDOs

GPIO inputs can individually enable/disable an LDO, similar to manual control of discrete LDOs.

Resources:

- Six GPI(O)s
- Seven LDOs

Connect each GPI(O)s to the enable inputs of any six LDOs. To enable all seven LDOs, two must share the same GPI(O).

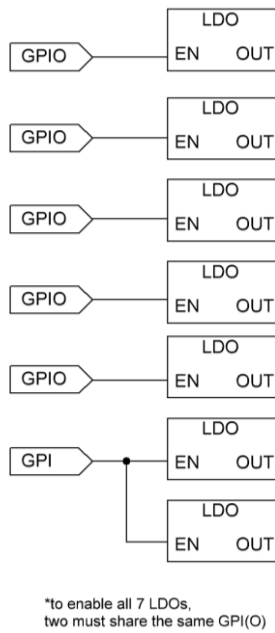


Figure 4: Block Diagram of Discrete Equivalent Use Case

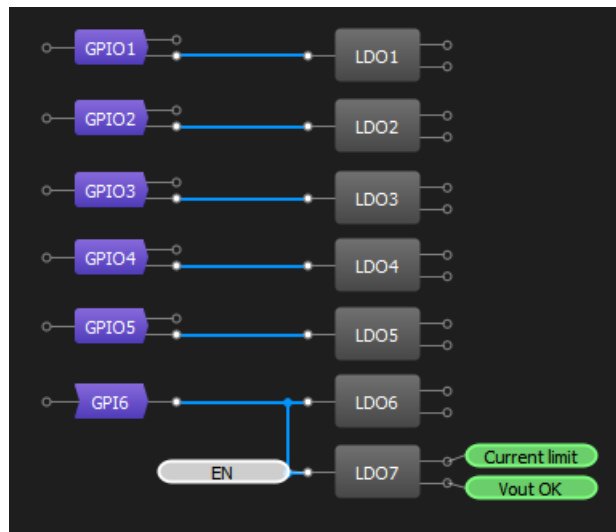


Figure 5: Screenshot of Discrete Equivalent Use Case (w/ Labels)

SLG51000 GPIO Use Cases

4.3 I²C Control

The SLG51000 can be controlled by an I²C Master using GPIO5 for SDA and GPI6 for SCL.

Resources:

- GPIO5_SDA
- GPI6_SCL
- Resource Control
- Seven LDOs

Configure GPIO5 as I²C DATA, and GPI6 as I²C CLOCK. Connect the I²C Resource Control Outputs to any or all seven LDO Enables.

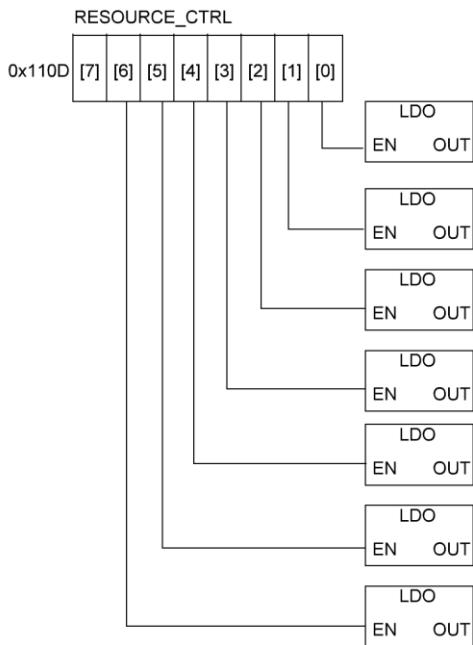


Figure 6: Block Diagram of I²C Software Control Use Case

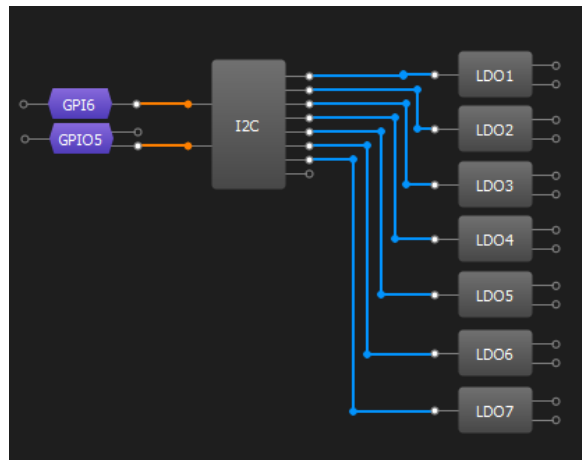


Figure 7: Screenshot of I²C Software Control Use Case

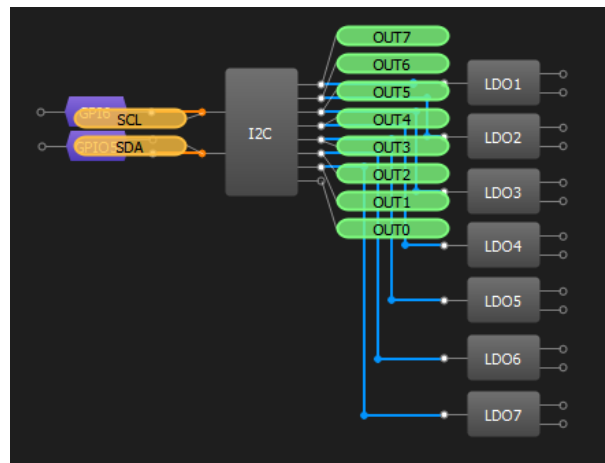


Figure 8: Screenshot of I²C Software Control Use Case (w/ Labels)

SLG51000 GPIO Use Cases

4.4 Combinational Logic Control

Use a Look Up Table to create any combination of GPIOs and/or internal signals to enable/disable an LDO.

Resources:

- Two or more GPI(O)s
- Any number of LDOs
- Any two internal signals (i.e. Temp Sense and one LDO VOUT OK)

Connect more than one GPI(O)s to the 3-bit LUT inputs. Each 3-bit LUT can be used as a basic logic gate (AND, NAND, OR, NOR, XOR, XNOR, INV, BUF) or filled in with desired logic. Connect the output of the 3-bit LUT to the enable of any number of LDOs.

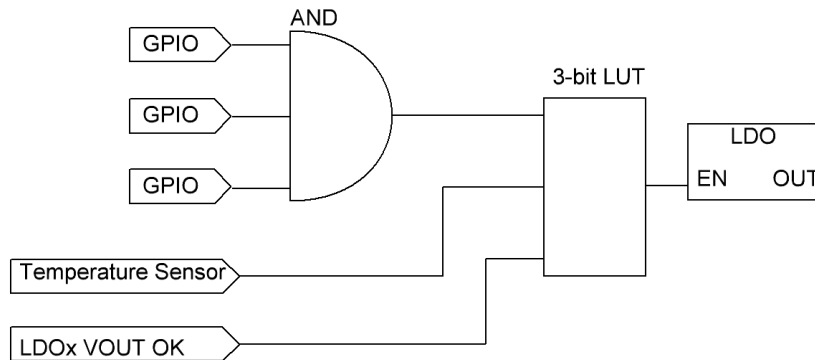


Figure 9: Block Diagram of Combinational Logic Control Use Case

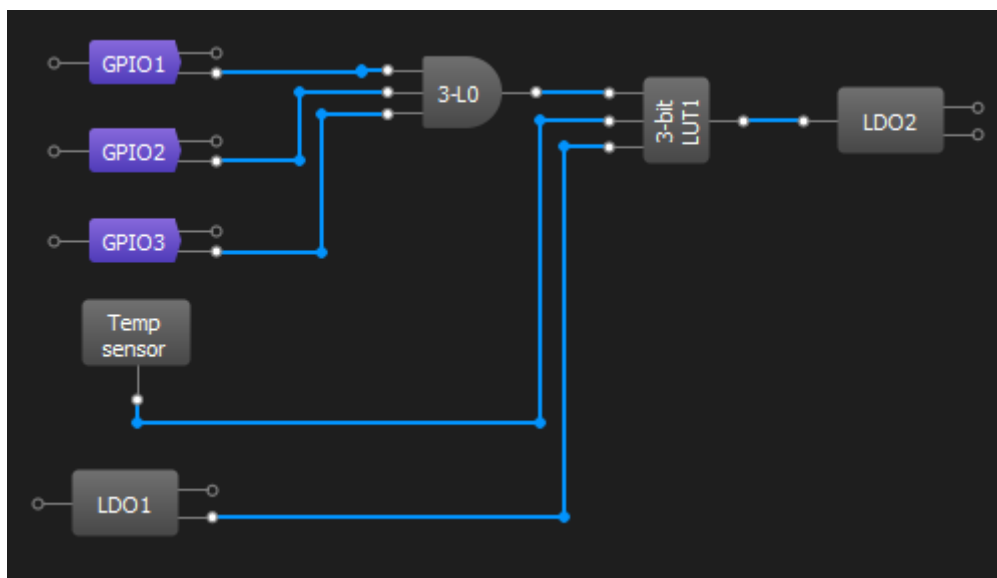


Figure 10: Screenshot of Combinational Logic Control Use Case

SLG51000 GPIO Use Cases

4.5 Automatic Power Sequencing

A GPI(O) input can trigger the power up/down sequence and advance each slot state to the next.

Resources:

- One or more GPI(O)s
- Three Power Sequencer Slots

Connect one GPI(O) to Power Sequencer Trigger Up and Trigger Down inputs which will trigger the state machine to exit IDLE and SEQ_UP states.

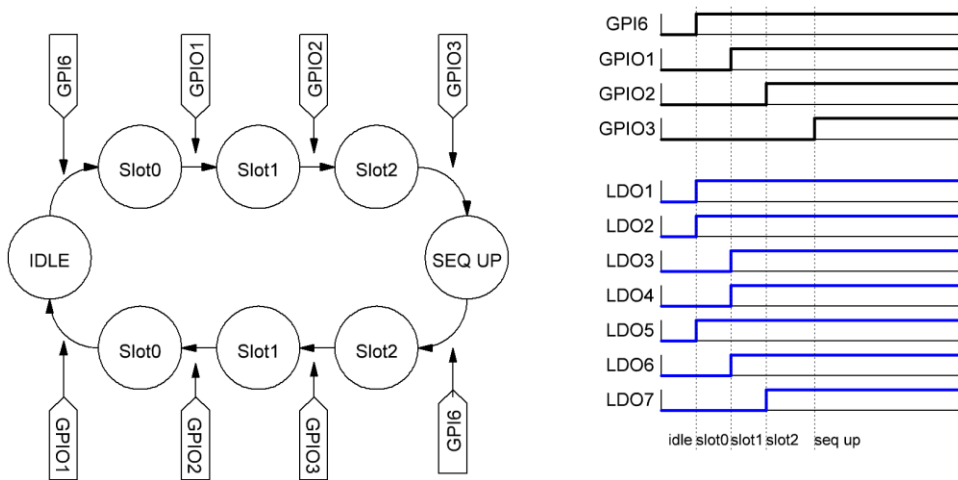


Figure 11: Block Diagram of Power Sequence Trigger Use Case (Multiple GPIO)

SLG51000 GPIO Use Cases

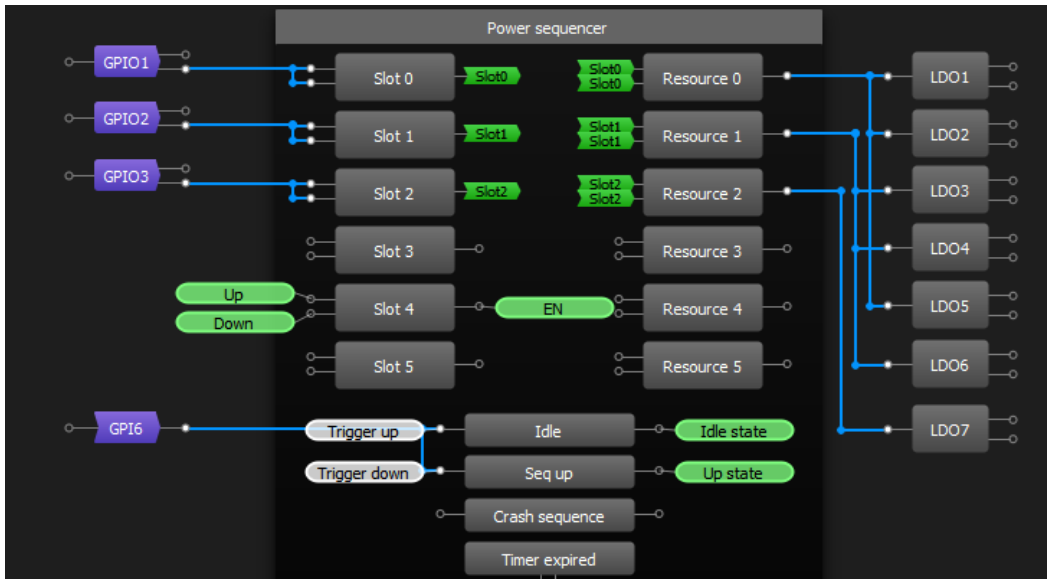


Figure 12: Screenshot of Power Sequence Trigger Use Case (Multiple GPIO)

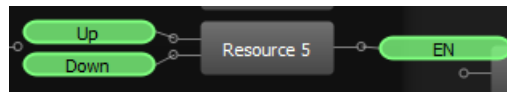


Figure 13: Resource Connection (w/ Labels)

Connect one GPI(O) to each Slot up/down input which will trigger state advancement between Slots. Each Slot output is triggered by its GPIO input and with its minimum timer, or by timeout.

Connect the UP input of the Resources to the Slot output in which they will be enabled. Connect the DOWN input of the Resources to the Slot output in which they will be disabled.

Connect the Resource outputs to LDOs that will share the same power up and power down timings. In this example, LDO1, LDO2 and LDO5 will share Resource 0. LDO3, LDO4, and LDO6 will share Resource 1. And LDO7 is using Resource 2.

For any Slots that will be skipped, set the minimum timer to 0ms.

Configure the Up/Down inputs with active high and active low sensitivity, if desired.

To visualize the timings between Slots, the SLG51000 Development Software has an available State Control Timing Diagram built-in feature as shown in [Figure 14](#).

SLG51000 GPIO Use Cases

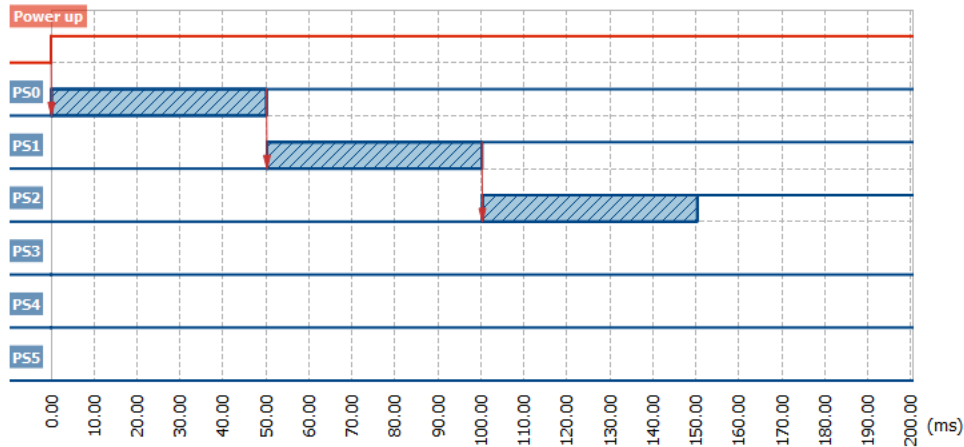


Figure 14: Screenshot of Timing Diagram between each Slot

5 GPIO Use Cases as Outputs

In the following section, we will explore ways to use GPIOs configured as outputs for different applications.

5.1 Fault Signal Output

If any of the SLG51000's LDOs has an over-current fault or power good fault, the power sequencer's crash sequence is initiated, or there is a high temperature warning which must signal a system alert or shutdown to the main applications processor, use a GPIO to bring this signal out of the SLG51000 device.

Resources:

- Up to five GPI(O)
- Any LDO
- Power sequencer
- Temp Sense
- Device Interrupt Request (DIR)

Each LDO has an Over-Current Limit Flag (ILIM) and a Power Good OK Flag (VOUT_OK). The supply controller's power sequencer has a Crash Flag. The built-in temperature monitor can be configured to different user-preset levels which will trigger the Temp Sensor output accordingly. Connect any of these signals to any GPIO.

SLG51000 GPIO Use Cases

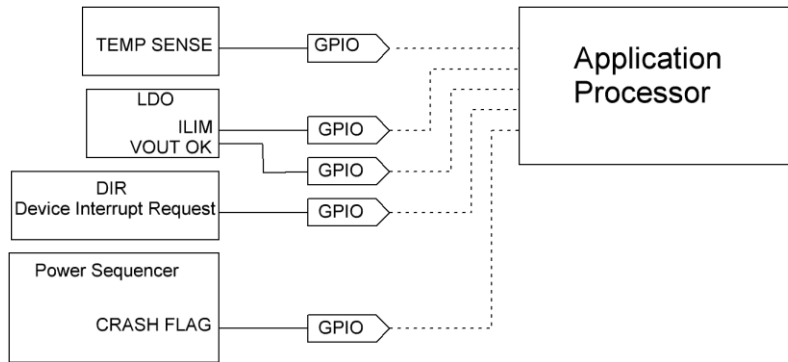


Figure 15: Block Diagram of Fault Signal Output Use Case

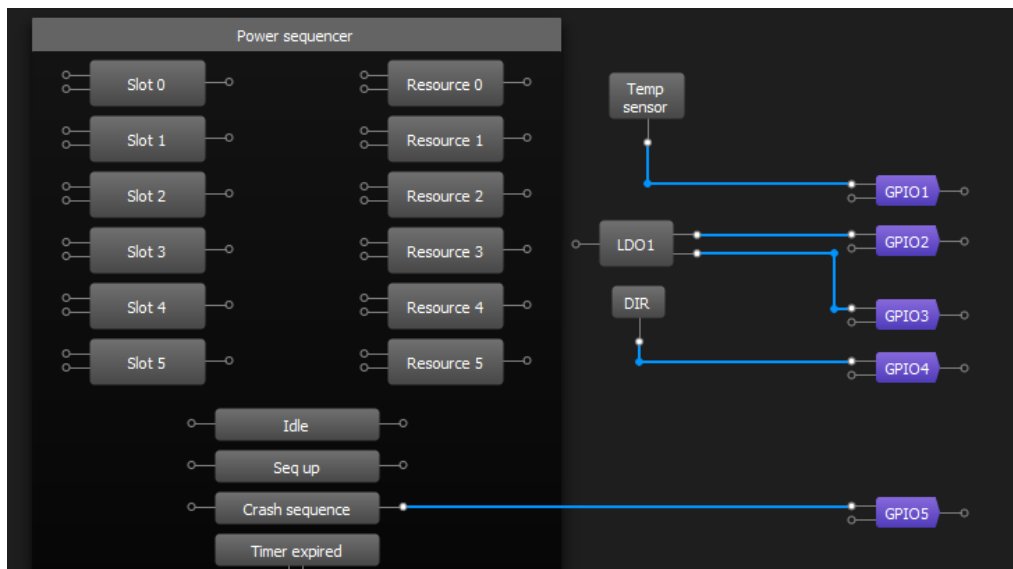


Figure 16: Screenshot of Fault Signal Output Use Case

Refer to the table below for all possible Matrix Outputs that can be used as signal outputs.

Table 2: Matrix Interconnect Input Ports

Input Port	Type
0	Constant Logic '0'
1	Constant Logic '1'
2-9	Register bit RESOURCE_CTRL (8-bit value)
10	Temperature Warning Flag
11-16	GPIO Inputs 1 to 6
17-23	LDO OK Flags 1 to 7
24-30	LDO Current Limit Flags 1 to 7

SLG51000 GPIO Use Cases

Input Port	Type
31-36	Power Sequencer Resource Enable Outputs 0 to 5
37	Power Sequencer in IDLE State Indicator Flag
38	Power Sequencer in SEQ_UP State Indicator Flag
39	Power Sequencer Slot Time Min Expired Flag
40	Power Sequencer Slot Time Max Expired Flag
41	Power Sequencer Crash Indicator Flag
42	Interrupt request from device's event registers (DIR)
43-54	LUT Array LUT outputs 0 to 11

6 Conclusions

This application note presents example use cases for GPIOs. Any combination of the GPIO Use Cases can be used in a single SLG51000.

Revision History

Revision	Date	Description
1.1	18-Aug-2020	Updated Figure 11
1.0	14-Jan-2019	Initial Version

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.