Application Note

Digital Magnitude/Identity Comparator

AN-CM-259

Abstract

This application note describes how to implement the two types of digital comparators: Identity comparator and Magnitude comparator. It uses the SLG46533V Renesas GreenPAK IC to construct both circuits.

This application note comes complete with design files which can be found in the References section.

Contents

Figures

Tables

1   Terms and Definitions

LSB   Least significant bit
LUT   Look-up table
MSB   Most significant bit
XNOR   A digital logic gate that gives a true (1 or high) output if the two inputs are
                  identical (both 1s or both 0s)

2   References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/products/greenpak.

Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the IC.

[1]   GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics

[2]   AN-CM-259 Digital Magnitude/Identity Comparator.gp, GreenPAK Design File, Renesas Electronics

[3]   GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4]   GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

[5]   SLG64533V, Datasheet, Renesas Electronics

3   Introduction

Digital comparison is considered as one of the important methods that are used in digital systems while executing arithmetic or logical operations. It is widely used in CPU, microcontroller, combinational and communication systems and is specially designed to compare the relative magnitudes of binary numbers. This comparison is used for testing whether one number represented by one binary word is greater than, equal, or less than the other number. There are two main types of digital comparators available: Identity comparator and Magnitude comparator.

This app note describes how to implement an 8-bit Identity comparator and a 4-bit Magnitude comparator. This application note covers the concept and the circuit design.

GreenPAK IC offers all the necessary components and more in low cost programmable ICs which can be configured within minutes. Another advantage of GreenPAK is availability of remaining circuitry inside for other uses.

This note demonstrates a Digital comparator IC with complete testing for verification. The design is robust and commercially viable.

We have used an Arduino program to execute an Automatic test for this design. The program presents all possible binary combinations to the GreenPAK comparator inputs and checks the matching output. See Results section 7.

4   8-Bit Identity Comparator

4.1   Theory

Identity Comparator is a digital comparator that has only one output. It goes high when A = B, either both 1s (High) or both 0s (Low). This comparator can be implemented by a combination of logic gates (XNOR and AND gates) as shown in Figure 1. With 8-bit numbers, the comparator compares each bit of the number with an XNOR gate. Two 8-bit numbers are only equal if each bit is identical.

Inputs: The bits of two numbers which need to be compared (A, B), 8 bits for each number.

Outputs: one output terminal, it goes High if A = B.

The circuit of the equality comparator is made up from an exclusive NOR gate (XNOR) per pair of input bits. If the two inputs are equal (both logic 1 or both logic 0) then a logic 1 is output. The outputs of the XNOR gates are combined in an AND gate, the output of which will be high only when all the XNOR gate outputs are high (XNOR inputs are matched).
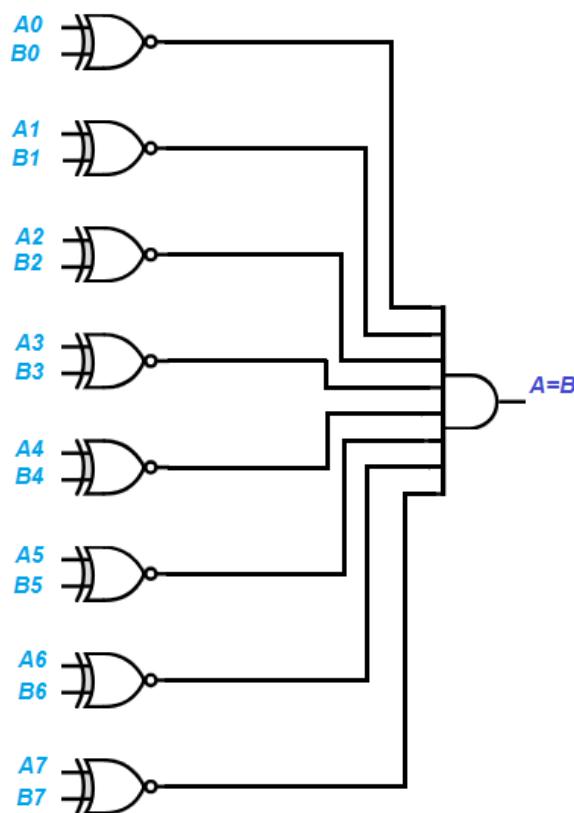
Figure 1: Logic Diagram of 8-Bit Identity Comparator

4.2   GreenPAK Design

The circuit intended to be designed requires 18 pins; 8 pins as inputs for the first number (A for example), 8 pins for the second number, and a single output that goes High at its output if both numbers are equal, otherwise it is Low. It also includes an Enable input to activate the circuit.

The GreenPAK SLG46533V has 18 inputs/outputs in addition to 25 blocks which can be configured to operate as logic gates. It is therefore suitable for constructing the circuit's functions.

The logic function XNOR is considered responsible to detect the similarity of the bits; i.e. its output gives a logic 1 if the two bits at the input are equal (whether 0 or 1); the XNOR gate therefore is a 1-bit comparator.

The complete comparator has been built in the form of sections which means a 1-bit comparator was constructed using a XNOR gate; the XNOR output was then connected to a 3-bit LUT in order to create a 2-bit comparator. This process has been repeated four times with the aim to create four 2-bit comparators.

The outputs of those four comparators were connected to a 4-Bit AND gate to build an 8-bit comparator, where the final result is obtained through PIN19, while PIN20 is an enable input as illustrated in Figure 2.

Table 1 shows the pin numbers and the function matching each pin, where PIN19 is the circuit's sole output.

Digital Magnitude/Identity Comparator
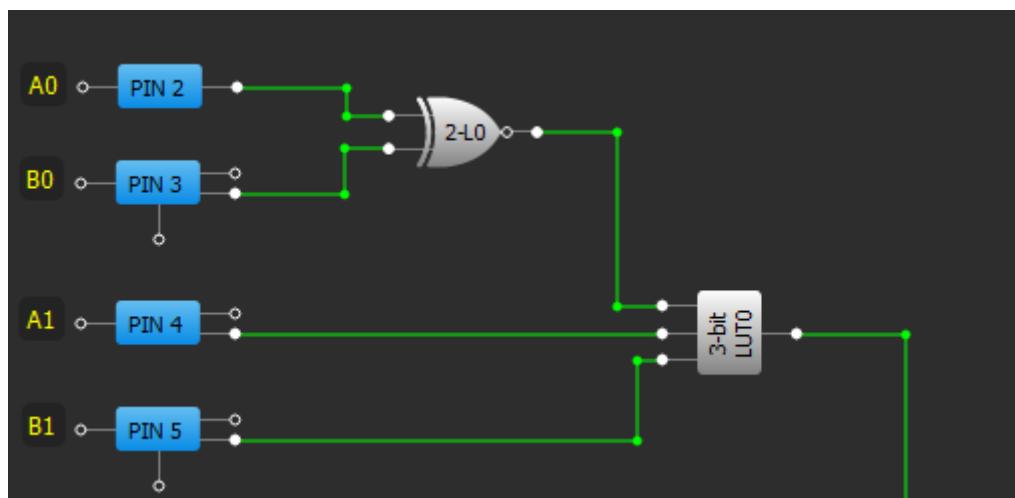
Figure 2: 2-Bit Identity Comparator Blocks
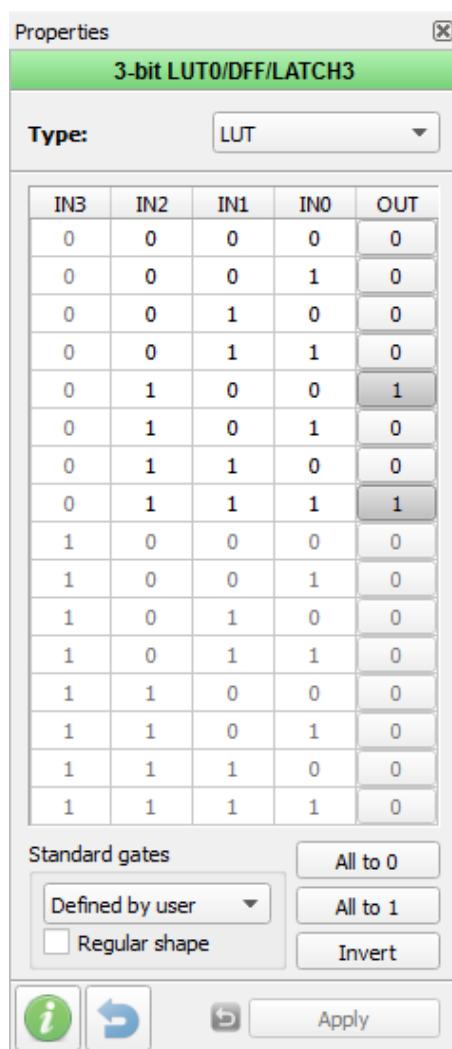
Figure 3: 3-bit LUT0 Configuration

Digital Magnitude/Identity Comparator
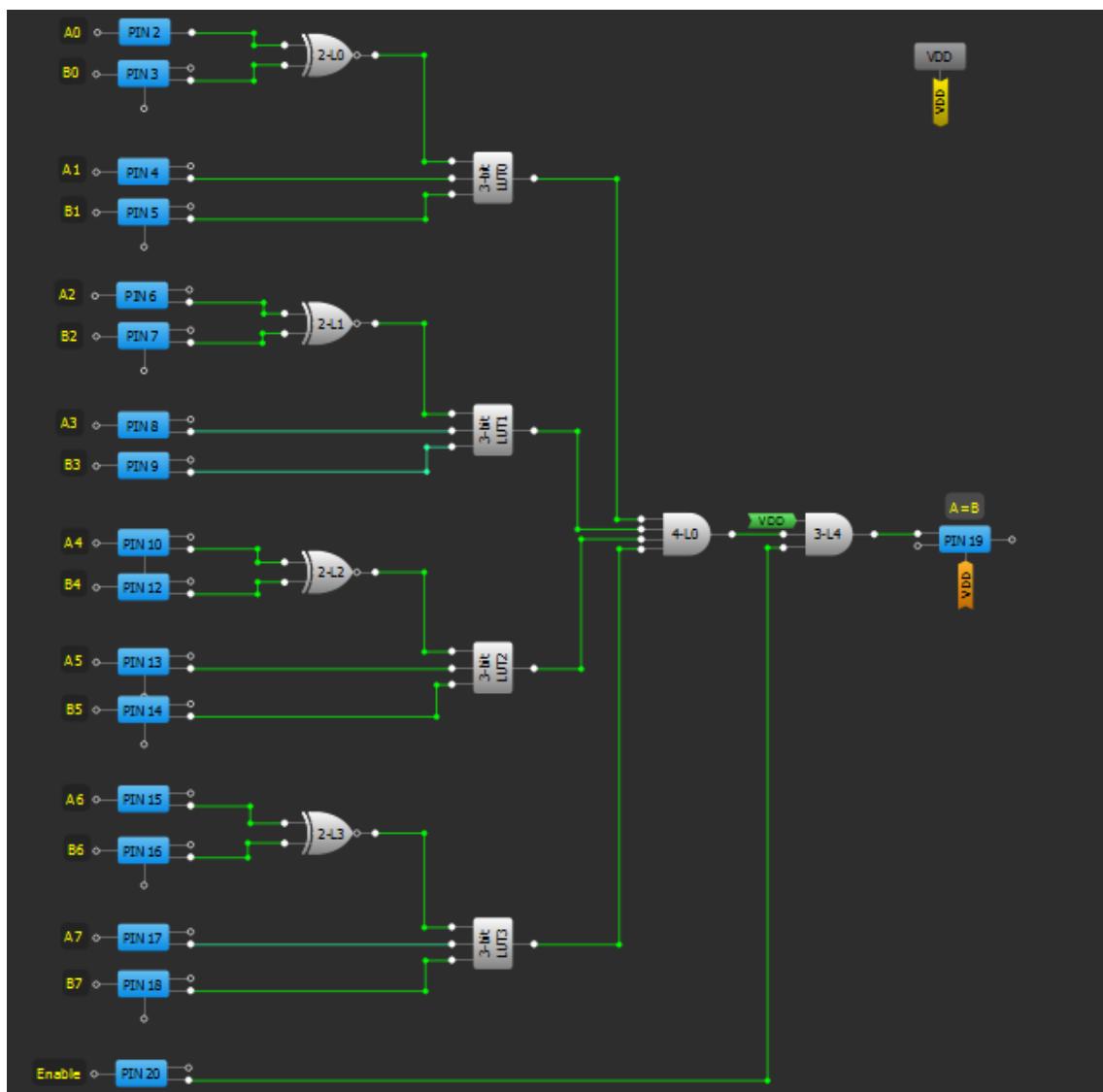
Figure 4: Identity Comparator Design

Table 1: GreenPAK PINs Map for Identity Comparator

GreenPAK PIN	Function	GreenPAK PIN	Function	GreenPAK PIN	Function
1	VDD	8	A3	15	A6
2	A0	9	B3	16	B6
3	B0	10	A4	17	A7
4	A1	11	GND	18	B7
5	B1	12	B4	19	Equality (Output)
6	A2	13	A5	20	Enable
7	B2	14	B5		

5   4-Bit Magnitude Comparator

5.1   Theory

The magnitude comparator circuit compares two digital or binary numbers (consider A and B) and determines their relative magnitude. It can also be used to indicate equality, but has two additional outputs, one that is logic 1 when word A is greater than word B, and another that is logic 1 when word A is less than word B.

Three binary Pins are used to indicate the output of the comparison as A > B, A < B, or A = B.

Figure 5 shows the block diagram of a 4-bit comparator which compares the two numbers of 4-bit length. Its output indicates the relationship between A, B.

The comparison process starts by comparing the most significant bit (MSB) first in comparing 4-bit binary numbers.

If equality A = B exists, then the next lowest bit is compared and so on until it reaches the last bit, (LSB). If equality still exists, then the two numbers are considered equal.

Otherwise, if inequality is found, either A > B or A < B, and the relationship between the two numbers is determined and the comparison between any additional lower order bits is ignored.

The output logic statements of this comparator are:

If A3 = 1 and B3 = 0 ---> A is greater than B (A>B). Or

If A3 = B3, and A2 = 1 and B2 = 0, ---> A > B. Or

If A3 = B3, A2 = B2, and A1 = 1, and B1 = 0 -------------------------------> A>B. Or

If A3 = B3, A2 = B2, A1 = B1, and A0 = 1 and B0 = 0 ---------------------> A > B.

The output A > B logic expression can be written according to the above statements as

G=A3 B3' + (A3 XNOR B3) A2 B2' +(A3 XNOR B3) (A2 XNOR B2) A1 B1' + (A3 XNOR B3) (A2 XNOR B2) (A1 XNOR B1) A0 B0'

In a similar way, the logic expression for the L (A<B output) can be written as

L= A3' B3 + (A3 XNOR B3) A2' B2 + (A3 XNOR B3) (A2 XNOR B2) A1' B1 + (A3 XNOR B3) (A2 XNOR B2) (A1 XNOR B1) A0' B0

The equal output turns high when all the individual bits of one number exactly matches the corresponding bits of another number. Then the logic expression for A=B output is written as

E = (A3 XNOR B3) (A2 XNOR B2) (A1 XNOR B1) (A0 XNOR B0)

According to the above output Boolean expressions, the circuit of this comparator can be implemented by using standard logic gates as shown in Fig. 5 below. Here, the four outputs from XNOR gates are then combined in an AND gate to give the binary variable E (A = B). A>B and A<B outputs also use XNOR outputs to produce the functional results as shown.

Inputs: The bits of two numbers which need to be compared (A, B), 4 bits for each number, I2C pins, cascading inputs if connecting two ICs for comparing 8-bit numbers.

Outputs: Three output terminals, one each for equality (A = B), greater than (A > B), and less than (A < B).

![RENESAS]

Digital Magnitude/Identity Comparator
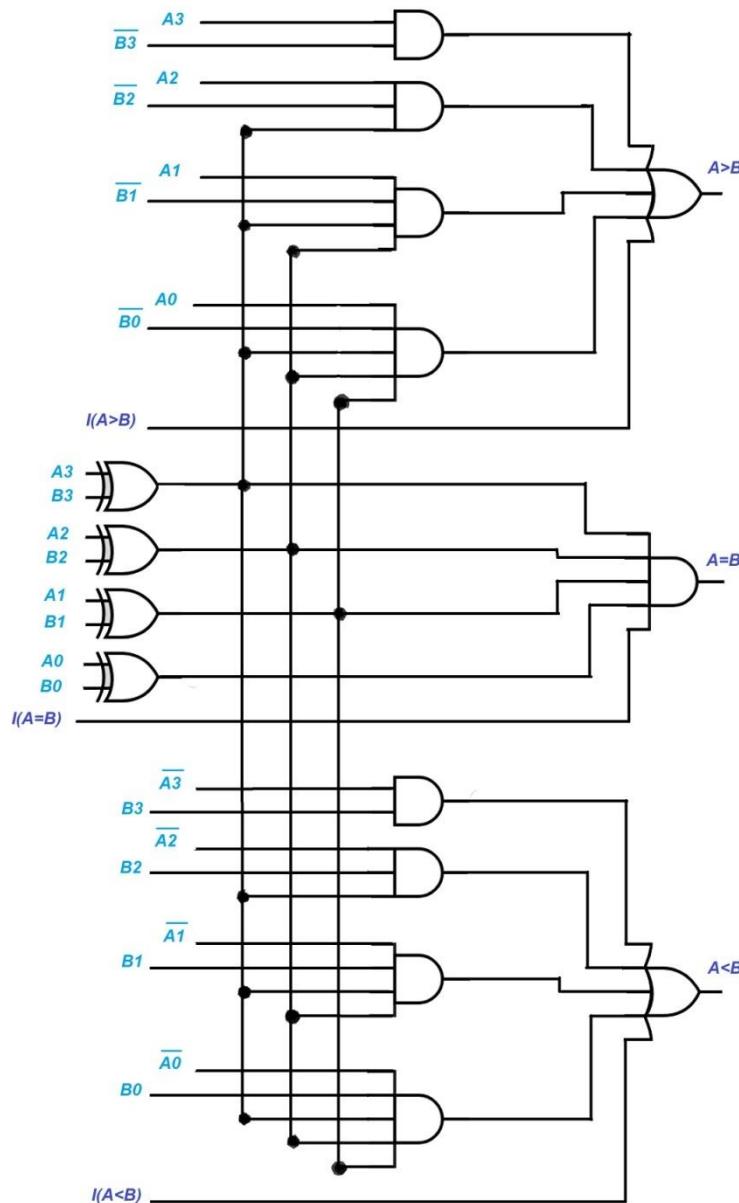
Figure 5: Magnitude Comparator Logic Diagram

5.2 GreenPAK Design

The design consists of three sections; the first is responsible to detect that the A > B condition was found; the second is responsible to examine that equality (A = B) was found, while the last has the task to check the A < B condition was reached.

The blocks 2L0, 2L1, 2L2, and 2L3 were configured to operate as XNOR gates which compare the pairs of bits of both numbers and detecting equality.

The blocks 3L0 ,3L1, 3L2, and 3L3 detect whether the A > B condition was attained, where the A3 and B3 are tested at the outset through 3-Bit LUT0.If A3 > B3 (that is A3 = 1, B3 = 0) a High signal appears on PIN17, but if they are equal, there will be a move towards the less significant of two bits A2, B2 and a comparison occurs via 3-Bit LUT1; and so on for the rest of the bits.

Digital Magnitude/Identity Comparator

The blocks 3L5,3L14, 3L15, and 3L16 check if A < B condition was fulfilled as the previous method is repeated, but concentration this time will be on A > B (that is Ax = 0, Bx = 1).

The design has been equipped with pins for cascading, enabling several circuits to be connected together and numbers greater than 4 bits could be compared.

These inputs are examined for the case of A = B condition for all the higher significance inputs of the circuit; and consequently, there is a move towards the lower significant bits of the other circuit for holding a comparison.

According to the result of such comparison, the result for the whole-number comparison is taken via the higher-significant outputs of the circuit.

The cascading bits are tested using the blocks 3L3, 3L12 and 3L6 as illustrated in Figure 6.

Table 2 represents the truth table for the final circuit of the Magnitude comparator.
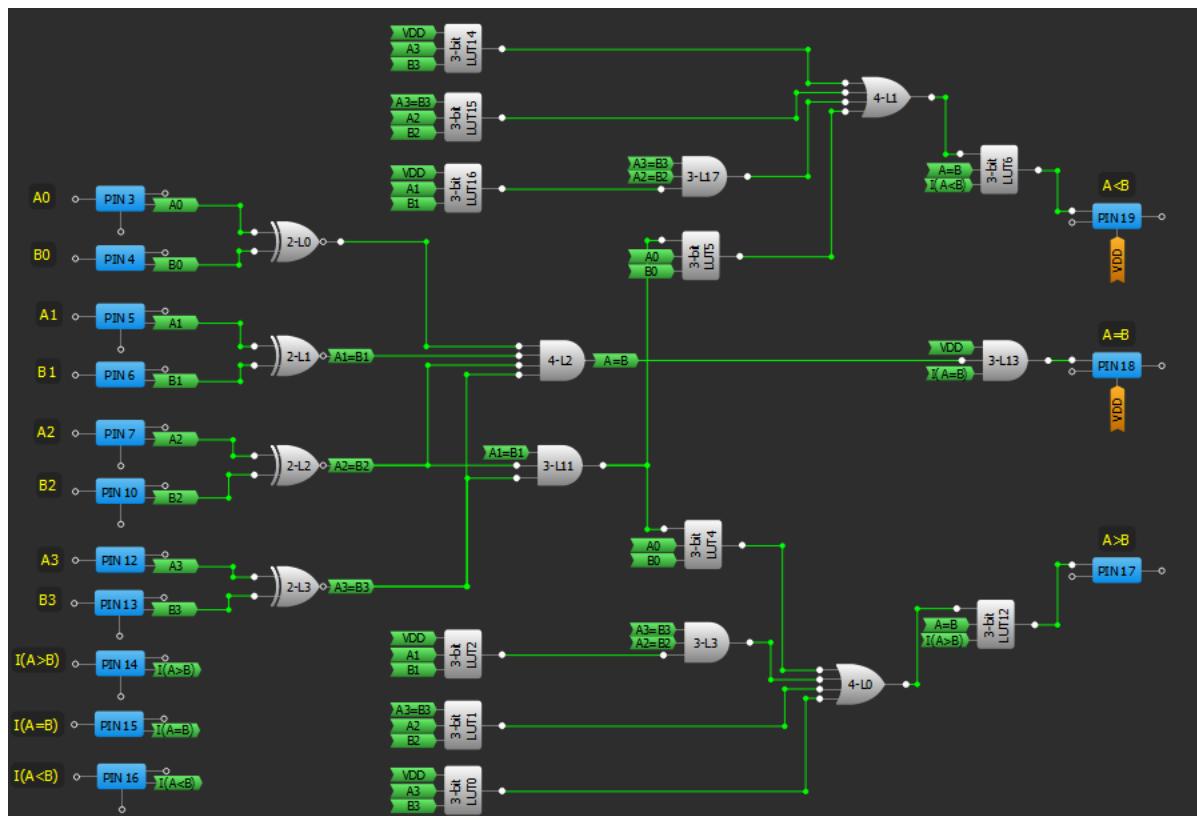
Figure 6: Magnitude Comparator Design

Table 2: Truth Table of Magnitude Comparator

INPUTS							OUTPUTS		
Comparing				Cascading					
A3 B3	A2 B2	A1 B1	A0 B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1

Digital Magnitude/Identity Comparator

INPUTS							OUTPUTS		
Comparing				Cascading					
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0

Table 3: GreenPAK PINs Map of Magnitude Comparator

GreenPAK PIN	Function	GreenPAK PIN	Function	GreenPAK PIN	Function
1	VDD	8	SCL	15	I (A=B)
2	-	9	SDA	16	I(A<B)
3	A0	10	B2	17	A>B
4	B0	11	GND	18	A=B
5	A1	12	A3	19	A<B
6	B1	13	B3	20	-
7	A2	14	I (A>B)		
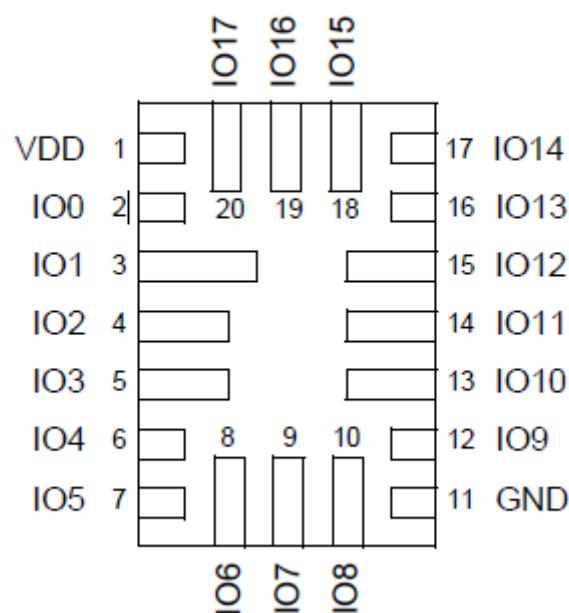
Figure 7: SLG46533V PINs Schematic

6   Comparators in Cascade

An 8-bit comparator can be built by cascading of two 4-bit comparators to compare two 8-bit numbers. Figure 8 below shows the circuit connection of this comparator in which the outputs of the lower order comparator is linked to the respective cascade inputs of the higher comparator I (A < B), I(A = B), and I(A > B).

A high signal must be connected to the A = B cascade input of the lower comparator, while the other two cascading inputs A < B & A > B must be connected to a low signal. This also applies to a single IC if only two 4-bit words are being compared. The final result of the comparison appears on the three outputs of the higher order 4-bit comparator.
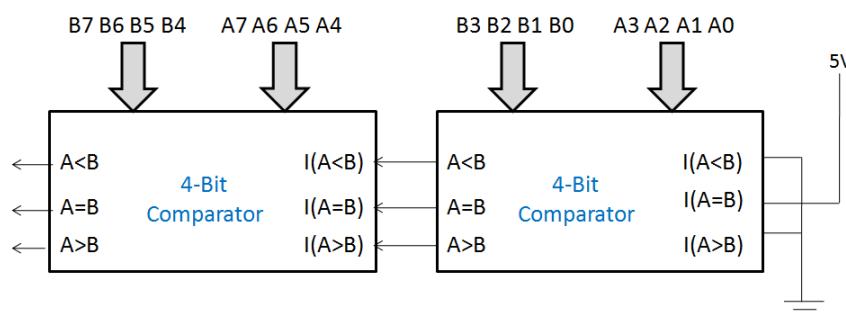
Figure 8: 8-Bit Magnitude Comparator Composition

7   Results

To make sure that the design operates properly, assistance of an external microcontroller circuit was employed to carry out an automatic test for all the possible cases to which such a circuit might be subject.

The comparator contains 8 inputs, 4 for each number; hence the number of the cases which could be created is 256.

A program has been written for an Arduino board and it was connected to the final design. The program's function is to generate all the possible binary formations for the inputs, to read each case's output, and to verify its correctness. Figure 9 below shows a serial monitor after testing.

The applied code could be found in the files enclosed with the project.

Digital Magnitude/Identity Comparator
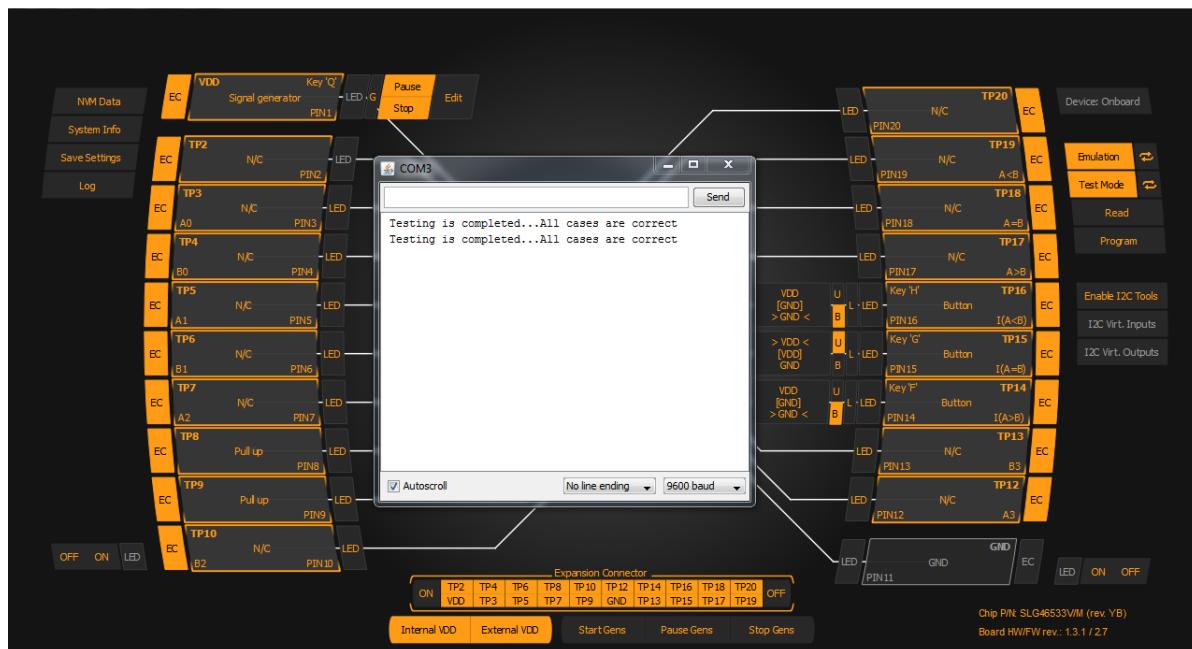
Figure 9: Serial Monitor Output After Testing Process

8   Conclusion

This application note has described the design of a digital comparator circuit of 2 types; Identity and Magnitude. The GreenPAK IC has shown a high efficiency as to construction of the desired digital circuits. Additionally, the circuit's design is inexpensive, has a short design time, and delivers a complete tested IC.

Revision History

Revision	Date	Description
1.0	22-Oct-2018	Initial Version

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