ClockMatrix™

Methods for Changing DPLL Settings during a Reference Switch

Abstract

This document explains how to configure a ClockMatrix to have different DPLL settings for different references.

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Related Information

For more information, visit our website: ClockMatrix™ Timing Solutions.

1. Introduction

A user of a ClockMatrix DPLL may need to change the configuration of a DPLL as it switches references because of input frequency or a required standard compliance. For two different configurations, the DPLL can change its settings during a reference switch automatically using predefined configurations or using manual register writes. For more than two DPLL configurations, the user must use the manual register write method.

2. Using Predefined Configurations

For this method, the DPLL settings are included in the loaded .tcs file.

There are two predefined configurations for each DPLL. They include Loop Bandwidth, Damping Factor, and Phase Slope Limiting. (There is also a Decimation Factor, which the GUI sets to “4x”.) The GUI sets each reference for group Predefined Config 0 or Predefined Config 1. The use of predefined configurations is set on a per DPLL basis, which are different references.

2.1 Using Predefined Configurations in the GUI

For cases with only two configurations, use the predefined configuration feature in ClockMatrix. When configuring the device through the configuration (.tcs) file, the user does not need to do any additional register writes after the system is running.

2.2 Example Predefined Configuration for 25MHz and 1 PPS (1Hz)

For this application, the device requires a high bandwidth for 25MHz on CLK0 and requires a low bandwidth for 1Hz input on CLK1. The example uses channel/DPLL 0. In Figure 1, the 25MHz input is set to predefined configuration 0 (pred0), and in Figure 2, the 1 PPS input is set to predefined configuration 1 (pred1). Channel 0 uses automatic switching between 0 and 1, and this also works with a manual reference selection. For DPLL parameters not listed under predefined configuration, both references use the same parameters.

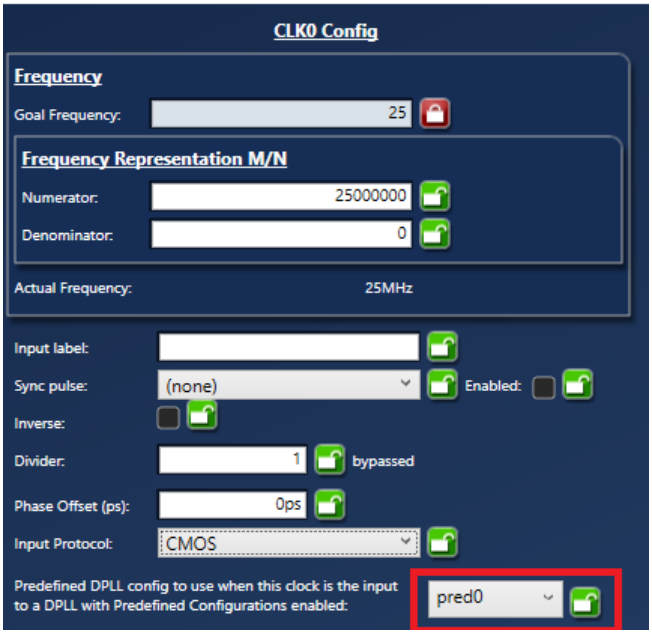

Figure 1. CLK0 Configuration

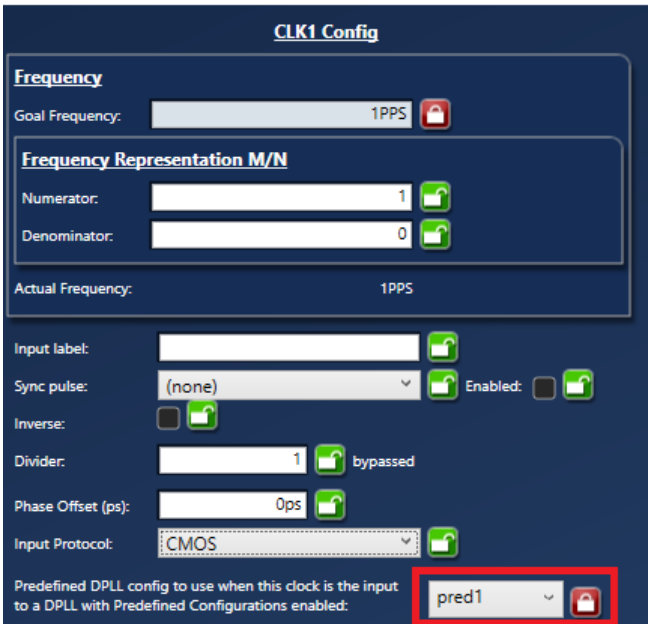

Figure 2. CLK1 Configuration

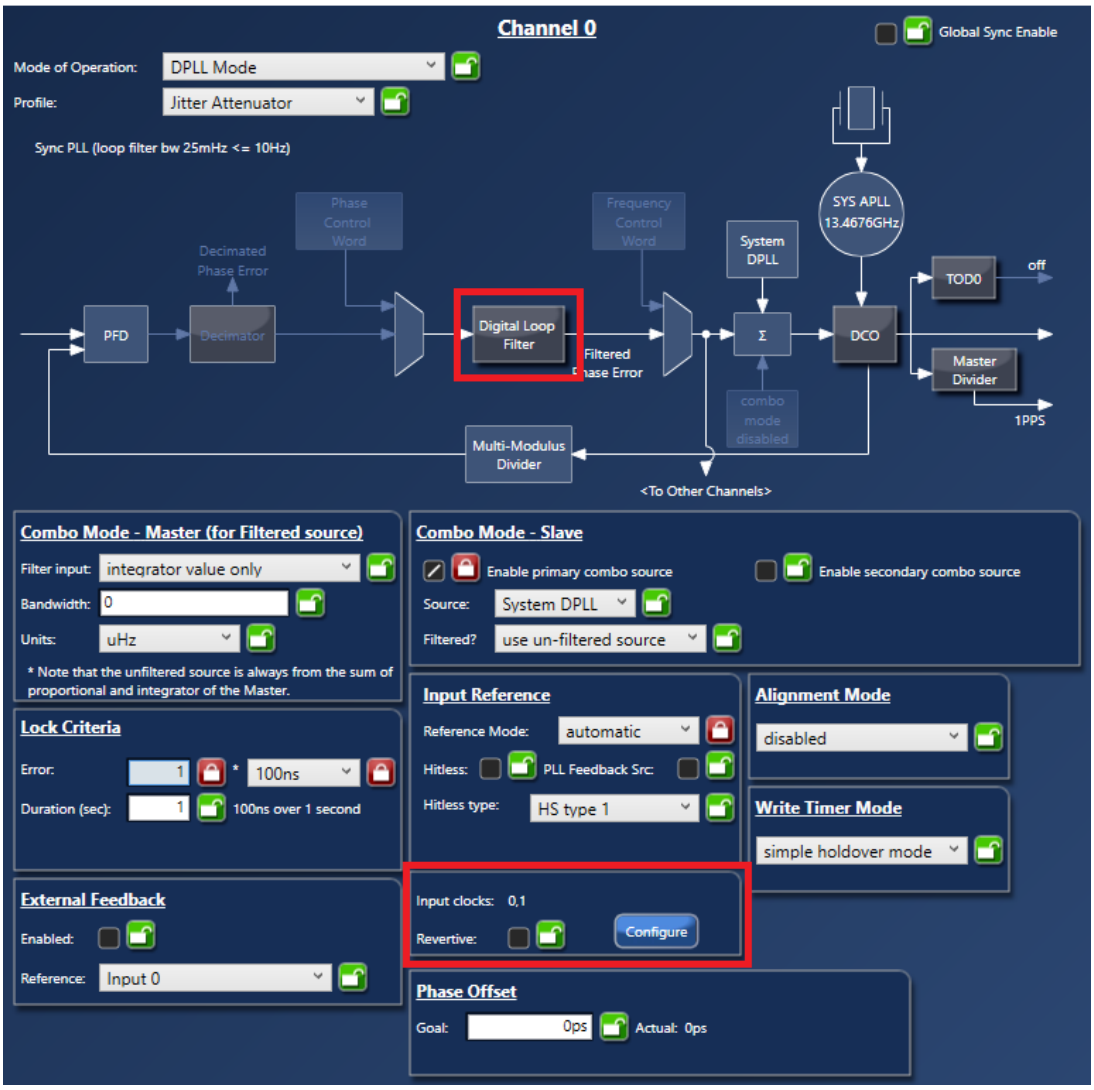

Figure 3. Channel 0

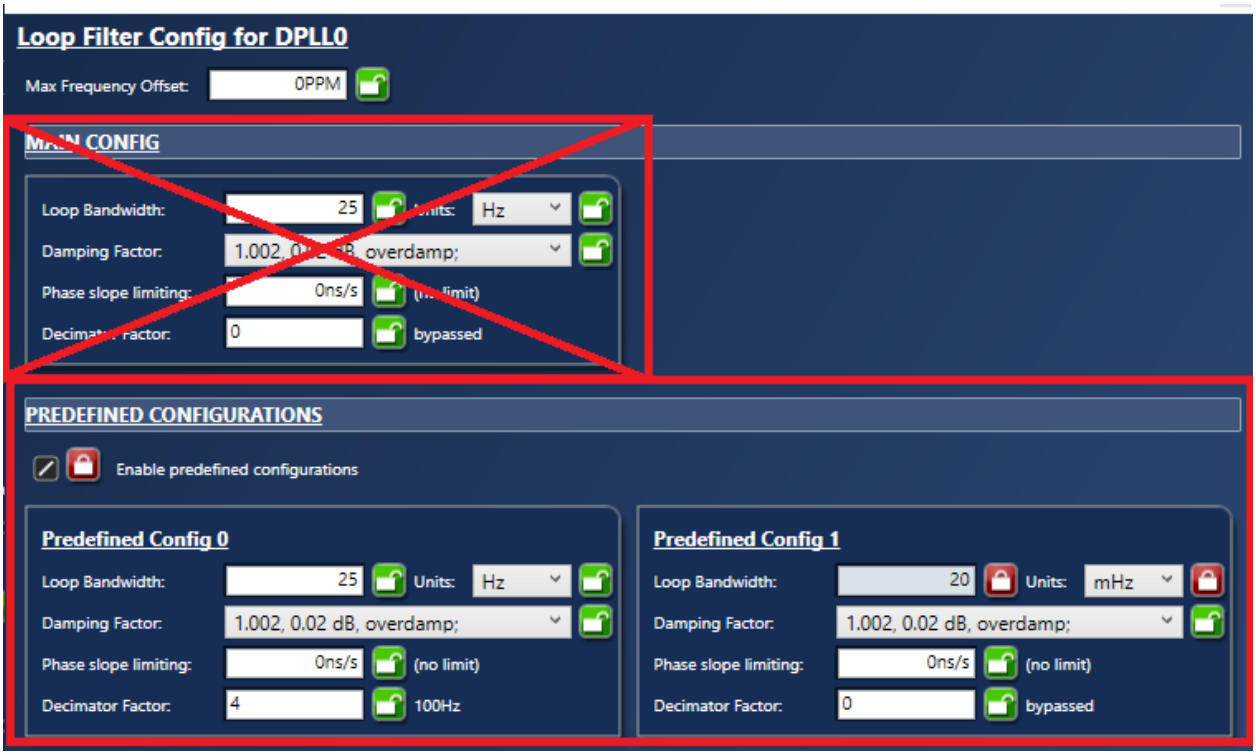

Figure 4. Loop Filter Configuration for DPLL0

3. Using Register Writes

Procedure:

1. Check that the DPLL is locked before starting the procedure using STATUS.DPLLn_STATUS.DPLL0_STATE[3:0].
2. Put the DPLL in holdover mode: DPLL_0.DPLL_MODE.STATE_MODE[2:0] → force holdover.
3. Change the settings on the DPLL:
   - Loop bandwidth, damping factor, phase slope limiting (PSL), decimation factor
   - Lock criteria
   - Fast lock settings
4. Change the reference for the DPLL.
5. Put the DPLL in automatic/manual mode to lock to new reference.
6. Change the DPLL mode to allow relocking process to begin by setting DPLLn_State_mode → automatic.

The automatic reference mode and the automatic DPLL state mode work differently. For a reference, the automatic mode selects a reference using the reference priority list. (Alternatively, a manual mode can be used to either select a reference or to use holdover if that reference is unavailable.) For a DPLL, automatic mode allows the DPLL to switch between its states automatically instead of being locked to a mode (such as forced holdover). **Note:** The DPLL state machine operates when the DPLL is in PLL_MODE = “PLL_MODE” rather than synthesizer or DCO modes.

Category	Register[1]	Trigger Register
Set DPLL State	DPLL_n.DPLL_MODE.STATE_MODE[2:0]	DPLL_n.DPLL_MODE
Get DPLL State	STATUS.DPLLn_STATUS.DPLL0_STATE[3:0]	N/A
Loop Bandwidth - value	DPLL_CTRL_n.DPLL_BW.DPLL _BW[13:0]	Self-triggering
Loop Bandwidth - unit	DPLL_CTRL_n.DPLL_BW.BW_UNIT[15:14]	Self-triggering
Damping factor	DPLL_CTRL_n.DPLL_DAMPING.DAMP_FTR[3:0]	Self-triggering
PSL	DPLL_CTRL_0.DPLL_PSL.DPLL_PSL[15:0]	Self-triggering
Decimation Factor	DPLL_CTRL_n.DPLL_BW_MULT. MULT[7:0]	Self-triggering
Lock Criteria - Value	DPLL_n.DPLL_LOCK_1. PHASE_LOCK_MAX_ERROR[5:0]	DPLL_n.DPLL_MODE
Lock Criteria - Unit	DPLL_n.DPLL_LOCK_1. PHASE_UNIT[7:6]	DPLL_n.DPLL_MODE
Fast lock – fast acquisition	DPLL_n.DPLL_FASTLOCK_CFG_0. LOCK_REC_FAST_ACQ_EN[6]	DPLL_n.DPLL_MODE
Fast lock – frequency snap	DPLL_n.DPLL_FASTLOCK_CFG_0. LOCK_REC_FREQ_SNAP_EN[4]	DPLL_n.DPLL_MODE
Fast lock – phase snap	DPLL_n.DPLL_FASTLOCK_CFG_0. LOCK_REC_PHASE_SNAP_EN[5]	DPLL_n.DPLL_MODE

1. In the ClockMatrix, the settings for a group of related registers (such as DPLL configuration) will not be applied until a trigger register is written. Other registers are self-triggering so their impact on the device is immediate. Trigger mode does not apply to status registers.

3.1 Example Manual Configurations

This example uses an application with three requested configurations for DPLL0: a very low bandwidth for GNSS (1Hz) up-convert, a SyncE compliant DPLL, and a high bandwidth for locking to a PTP clock.

Profile	Input Frequency	Bandwidth (Hz)	PSL (us/s)	Max Freq. Offset (ppm)	Lock Criteria (ns/s)	Fast Lock Enabled?
G.8262 option 2	25MHz	0.1	0.885	52	600	Yes – fast acquisition
GNSS Up-convert Lock to 1Hz	1 PPS (1Hz)	0.02	0.01	1	100	Yes – frequency snap/phase snap
PTP Clock	25MHz	25	Unlimited	244	10	No - Not required

All profiles use DPLL mode with hitless reference switching.

A user can dynamically change the DPLL BW settings while locked to a reference, however, Renesas does not recommended this method. This change can cause a change of state especially when changing the lock criteria. During the DPLL reconfiguration, the output should not glitch. **Note**: The DPLL does not check the criteria for fast lock until the next state transition (e.g., from locked to holdover to LOCKREQ (lock recovery) state). Renesas recommends setting the DPLL to holdover when making changes the DPLL configuration.

3.2 DPLL Performance for the Example Configuration

The following plots show a TIE (time interval error) capture for a DPLL switching between the profiles in the previous section.

Figure	From Profile	To Profile	Time of Switch	Notes
Figure 5	JA	8262	30 seconds	Lock immediate
Figure 6	JA	GNSS	30 seconds	Lock after 15 seconds
Figure 7	8262	JA	6 minutes	Lock immediate
Figure 8	GNSS	JA	12 minutes	Lock immediate
Figure 9	8262	GNSS	30 seconds	Lock after 15 seconds
Figure 10	GNSS	8262	15 minutes	Lock immediate

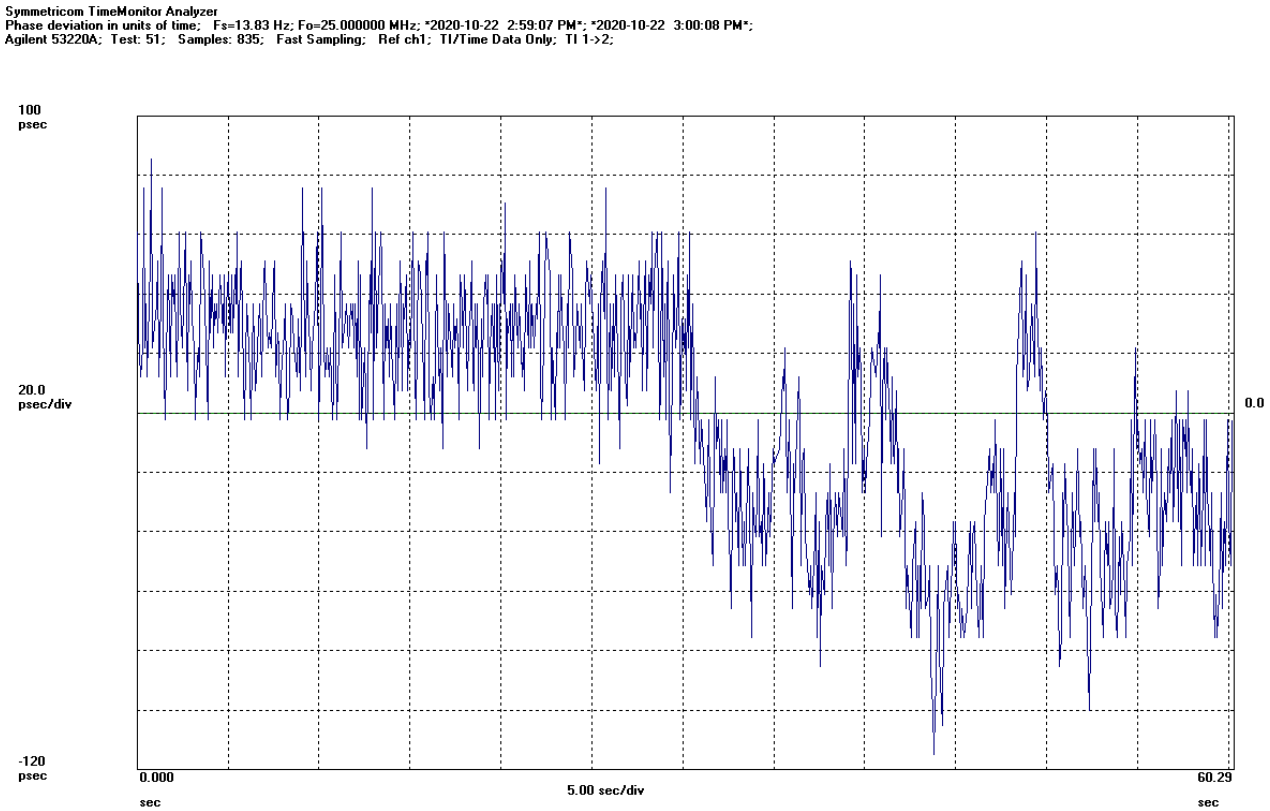

Figure 5. Example TIE from JA to 8262 with Switch at 30 Seconds

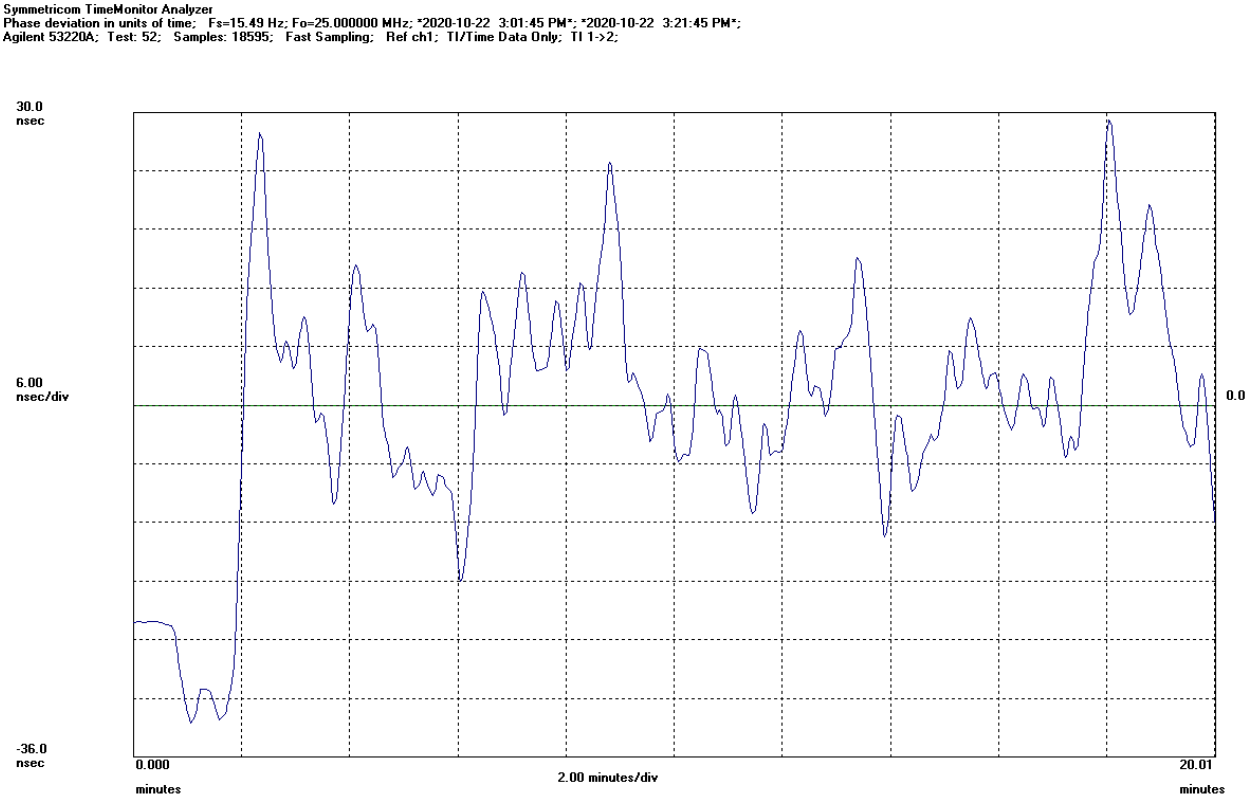

Figure 6. Example TIE from JA to GNSS with Switch at 30 Seconds

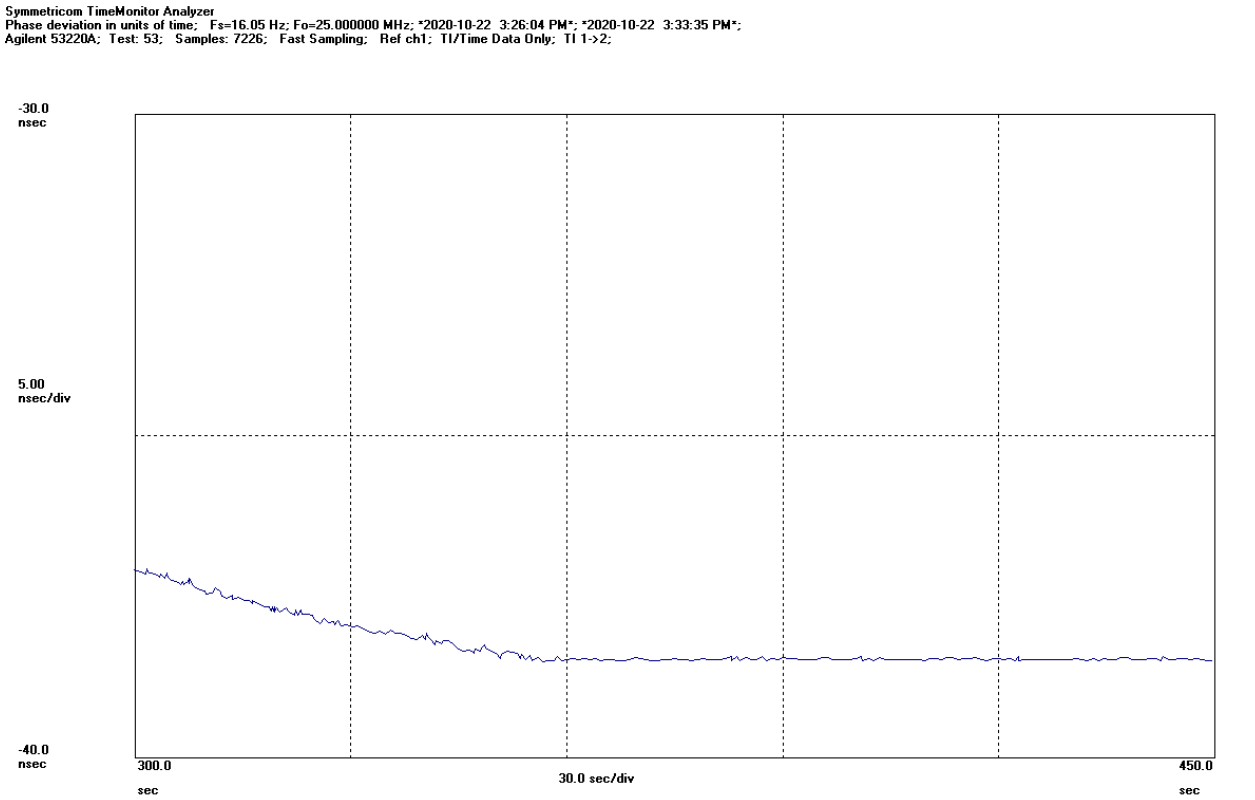

Figure 7. Example TIE from 8262 to JA with Switch at 360 Seconds (6 Minutes)

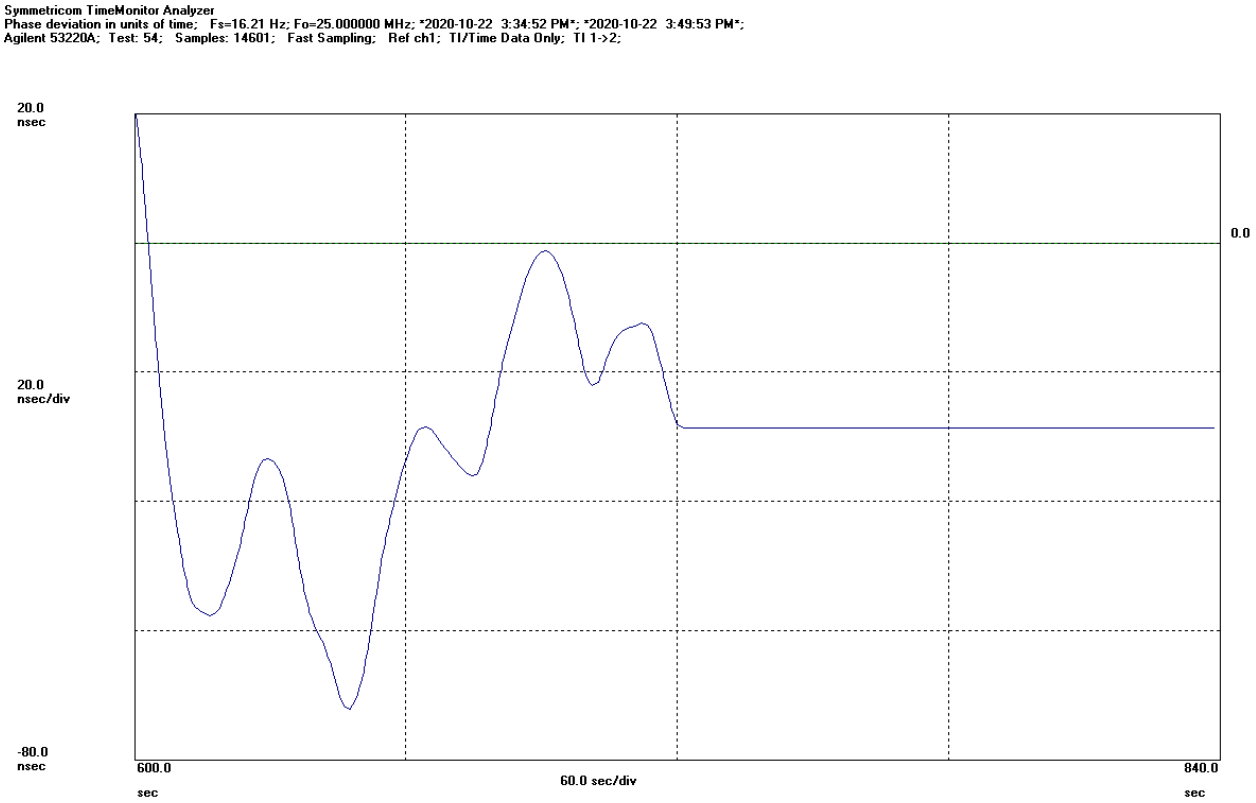

Figure 8. Example TIE from GNSS to JA

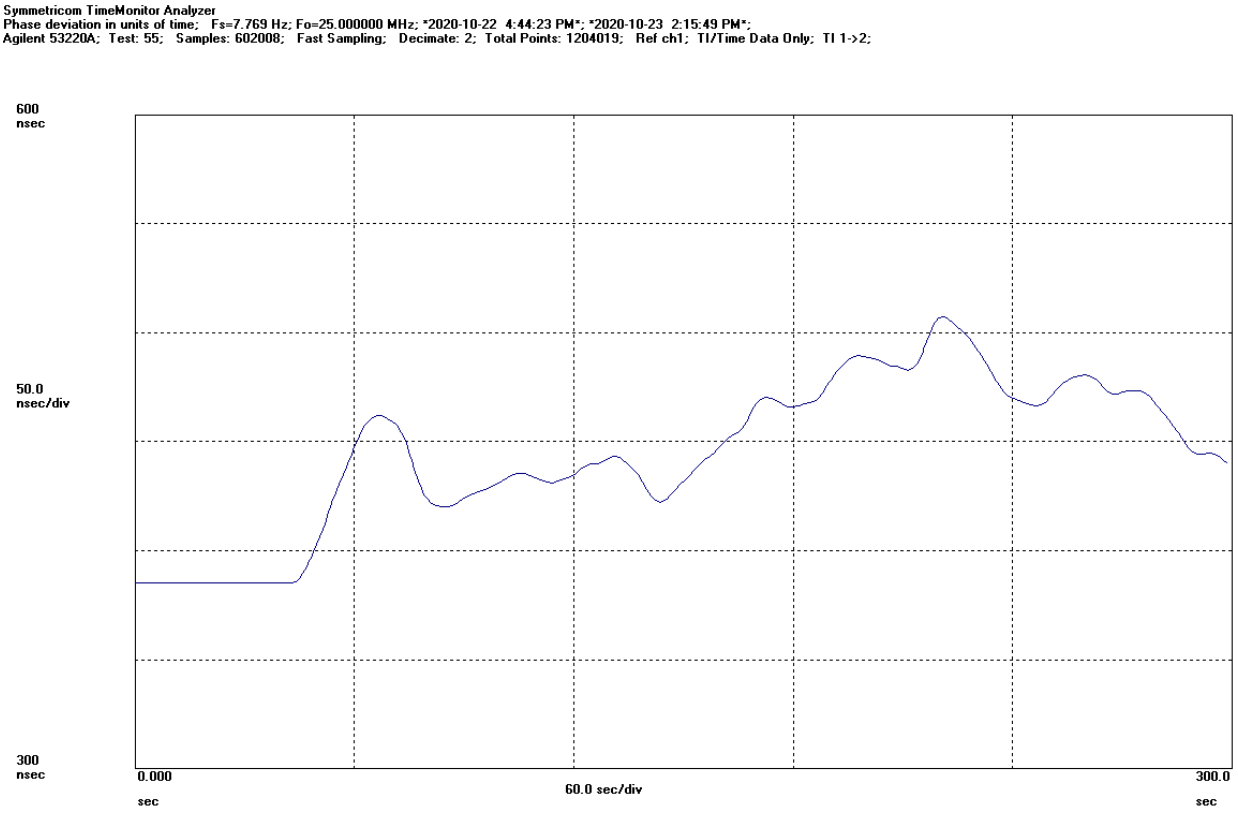

Figure 9. Example TIE from 8262 to GNSS with Switch at 30 Seconds

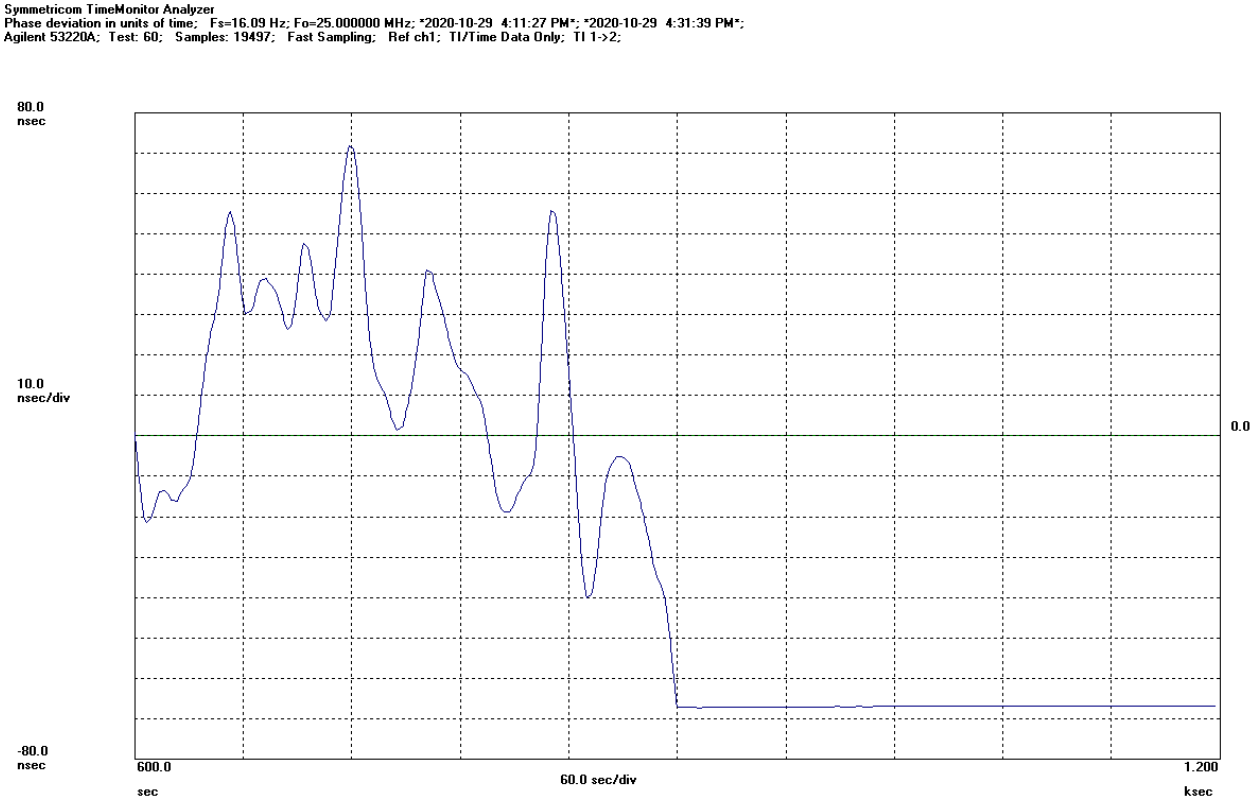

Figure 10. Example TIE from GNSS to 8262 with Switch at 900 Seconds (15 Minutes)

4. Revision History

Revision	Date	Description
1.0	Nov.4.20	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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