RENESAS

Application Note

Check List for Designing RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S Circuit Boards

R01AN6021EJ0121
Rev.1.21
Mar 18, 2024

Introduction

This document summarizes the knowledge gained from boards designed by Renesas Electronics, provides specific design examples, and provides a checklist for designing circuits with RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S including peripheral components. This document includes information that is mentioned as restrictions or recommendations in the hardware manuals, but also includes know-how and hints in order to reduce trouble in hardware development. Although the items of know-how and hints do not necessarily have to be observed, it is important to be aware of them during design.

Target Device

- RZ/G2L
- RZ/G2LC
- RZ/V2L
- RZ/G2UL
- RZ/Five
- RZ/A3UL
- RZ/G3S

Notes on Using This Document

The design of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S evaluation board kit might not meet the items for checking listed in this document due to the evaluation of multiplexed functions and board configurations. If you design hardware in a manner that differs from the advice given in this document, you do so at your own discretion and risk.

Be sure to keep the technical documents for the components of your hardware, including RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S up to date. This document is based on the latest information at the time of writing, but discrepancies with the contents may arise due to changes to product specifications, the lifting of restrictions, and for other reasons. In such cases, give priority to using the latest technical information.

In the figure, the 🚫 mark indicates a prohibited item, and the ⚠ mark indicates an item to note.

Table of Contents

1. Points Related to Reset Signals

1.1 Circuits for Generating PRST# Inputs

💡 Points

ALL

- The PRST# signal of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL is a Schmitt trigger input signal which is in the 3.3-V power domain. The PRST# signal of RZ/G3S is a Schmitt trigger input signal which is in the 1.8-V power domain.

- For the PRST# signal, RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL do not support high-level input while the 3.3-V power supply is turned off. RZ/G3S does not support high-level input while the 1.8-V power supply is turned off, and is tolerant of 3.3-V signal input.

- Logic for the TRST# signal from an enhanced JTAG ICE and other signals must be considered in terms of connection with the PRST# signal, and the voltages of the individual signals must be confirmed.

- Since the input through the PRST# pin passes through a Schmitt trigger, signals generated by open-drain sources can be input to the PRST# pin as they are. Note that RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S do not include a means for internally pulling up/down the signal.

- Some peripheral devices may require being reset with the same timing as the reset of the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S by the PRST# signal. In such cases, confirm that there is no problem with the voltages of the individual signals for the peripheral devices. When an open-drain circuit is used to generate the PRST# signal, also confirm that the waveform of the PRST# signal is not corrupted to the extent that this creates problems.
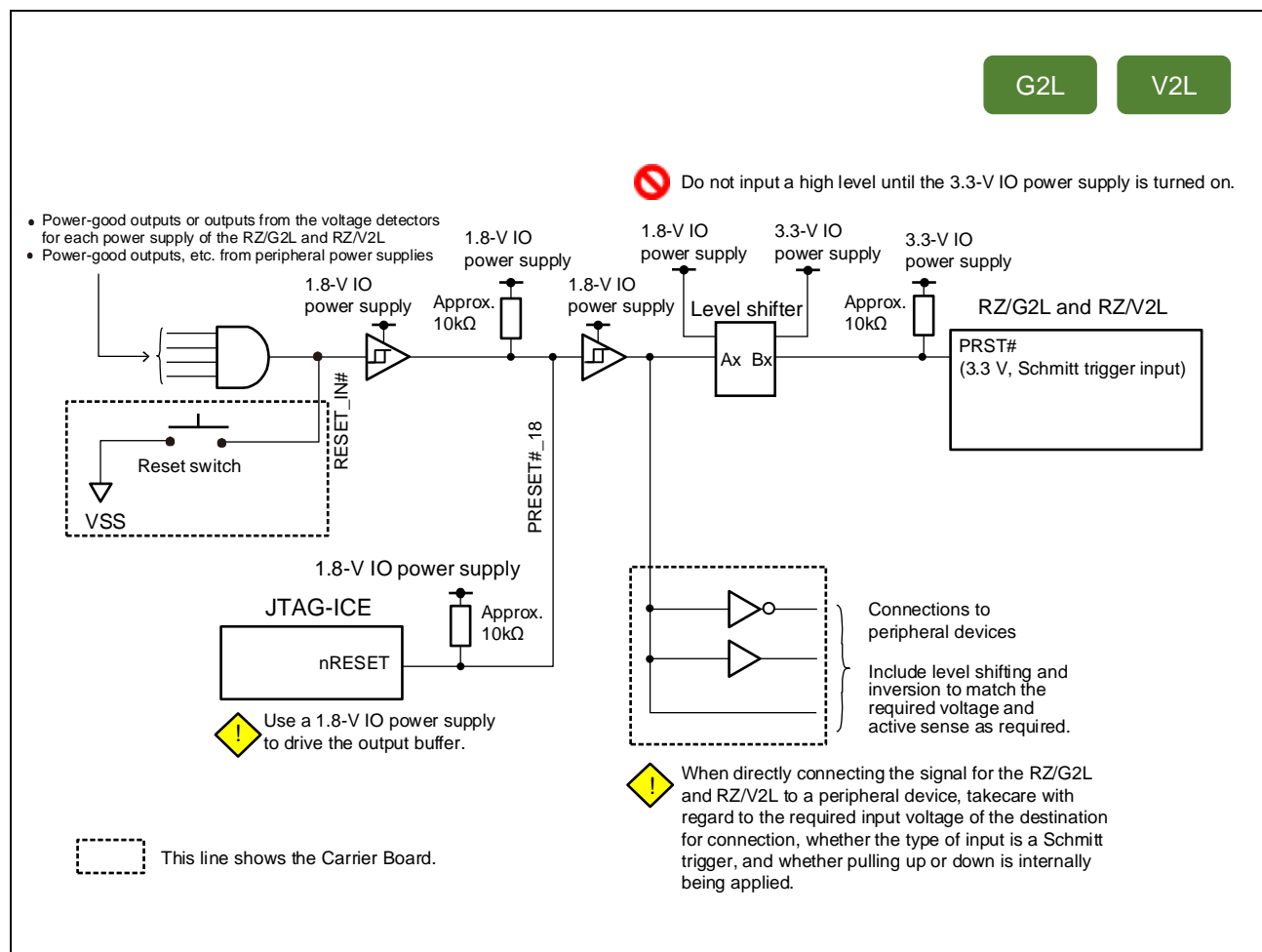
Figure 1.1(a)   Example of a Discrete Edition Circuit Configuration Related to the PRST# Signal of RZ/G2L and RZ/V2L
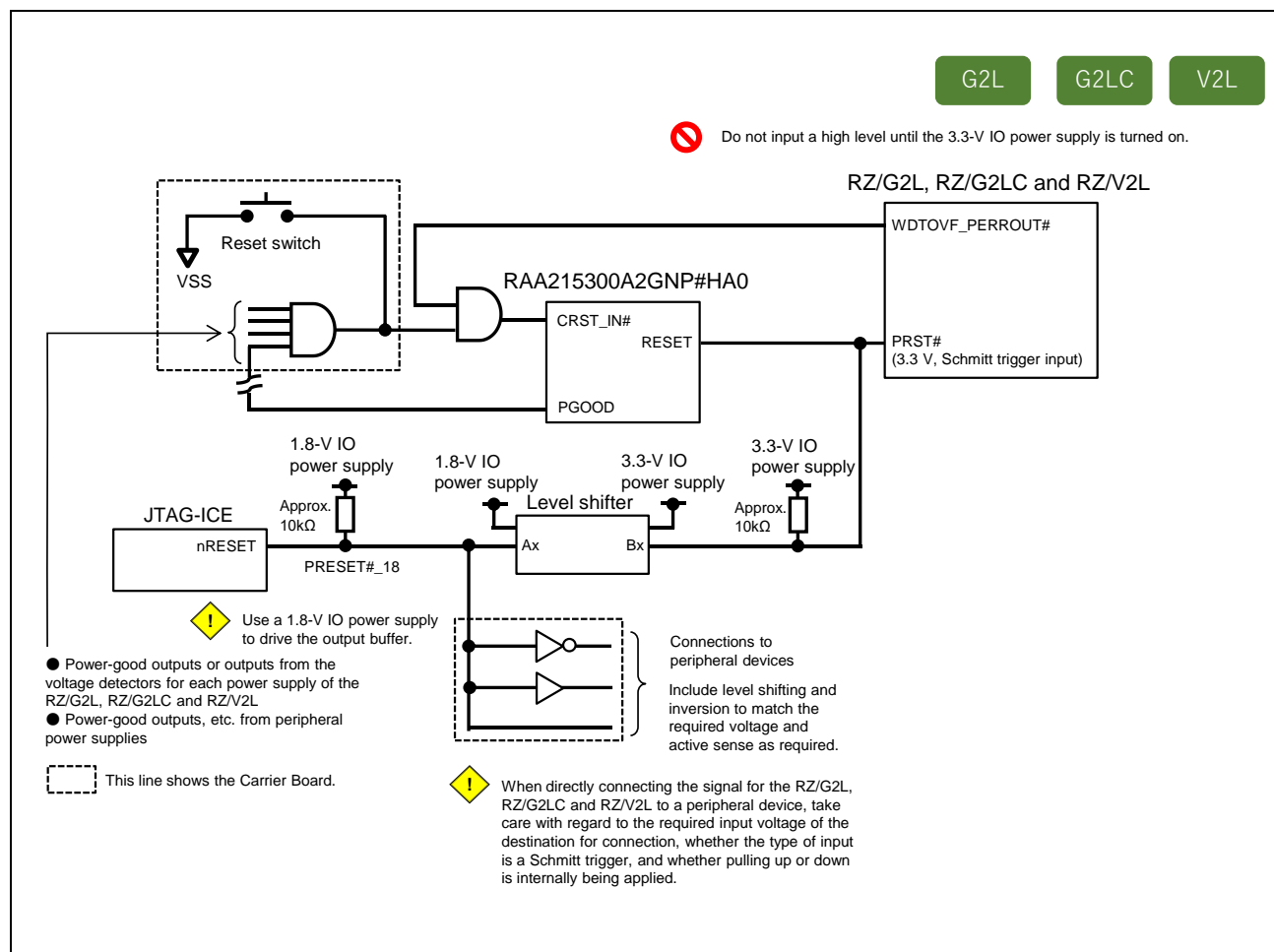
Figure 1.1(b)   Example of a PMIC Edition Circuit Configuration Related to the PRST# Signal of RZ/G2L, RZ/G2LC, and RZ/V2L
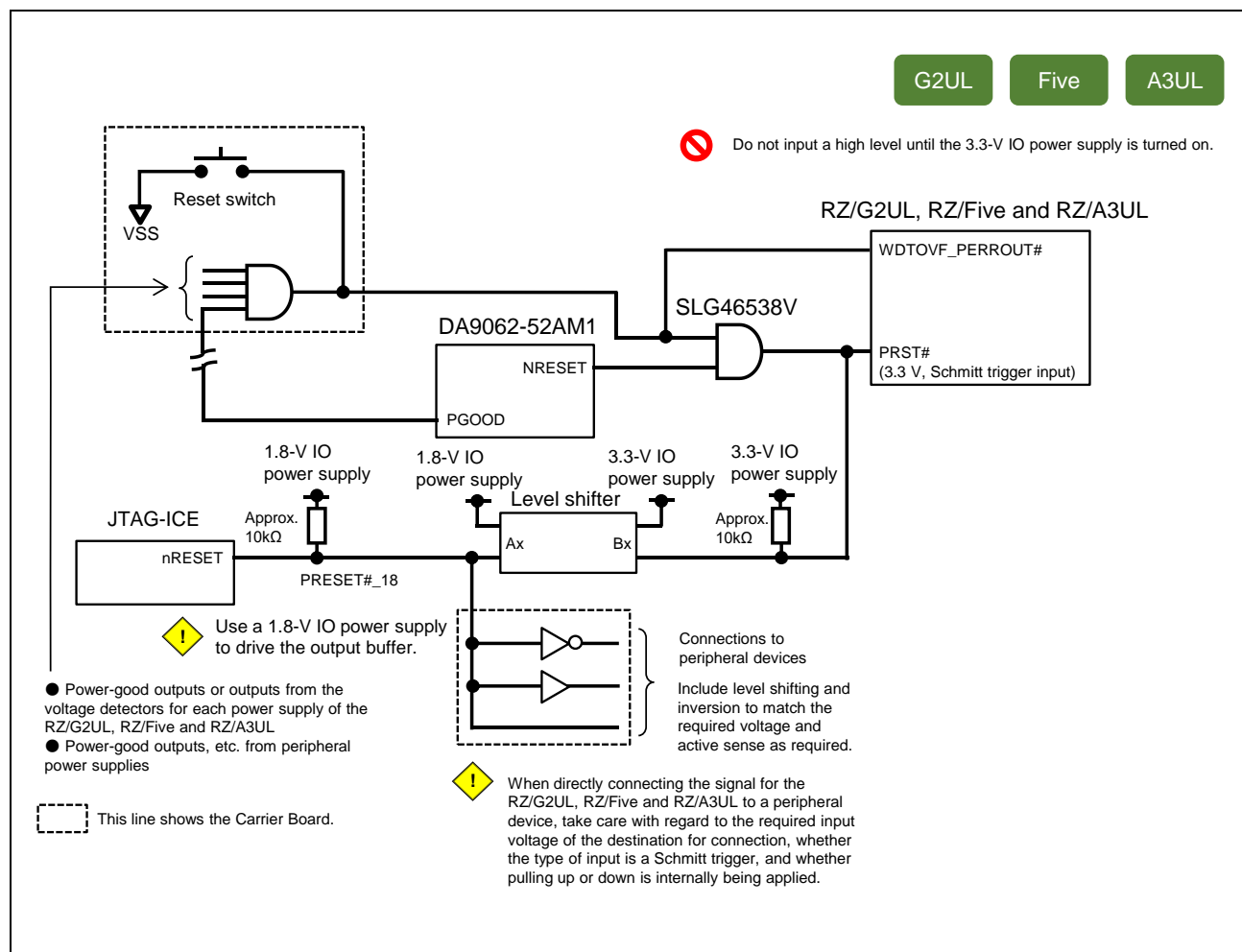
Figure 1.1(c)   Example of a Circuit Configuration Related to the PRST# Signal of RZ/G2UL, RZ/Five, and RZ/A3UL

Note 1.   To ensure the high level of the PRST# signal by pulling up, we recommend the use of a pull-up resistor with a value no greater than 10kΩ for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL.
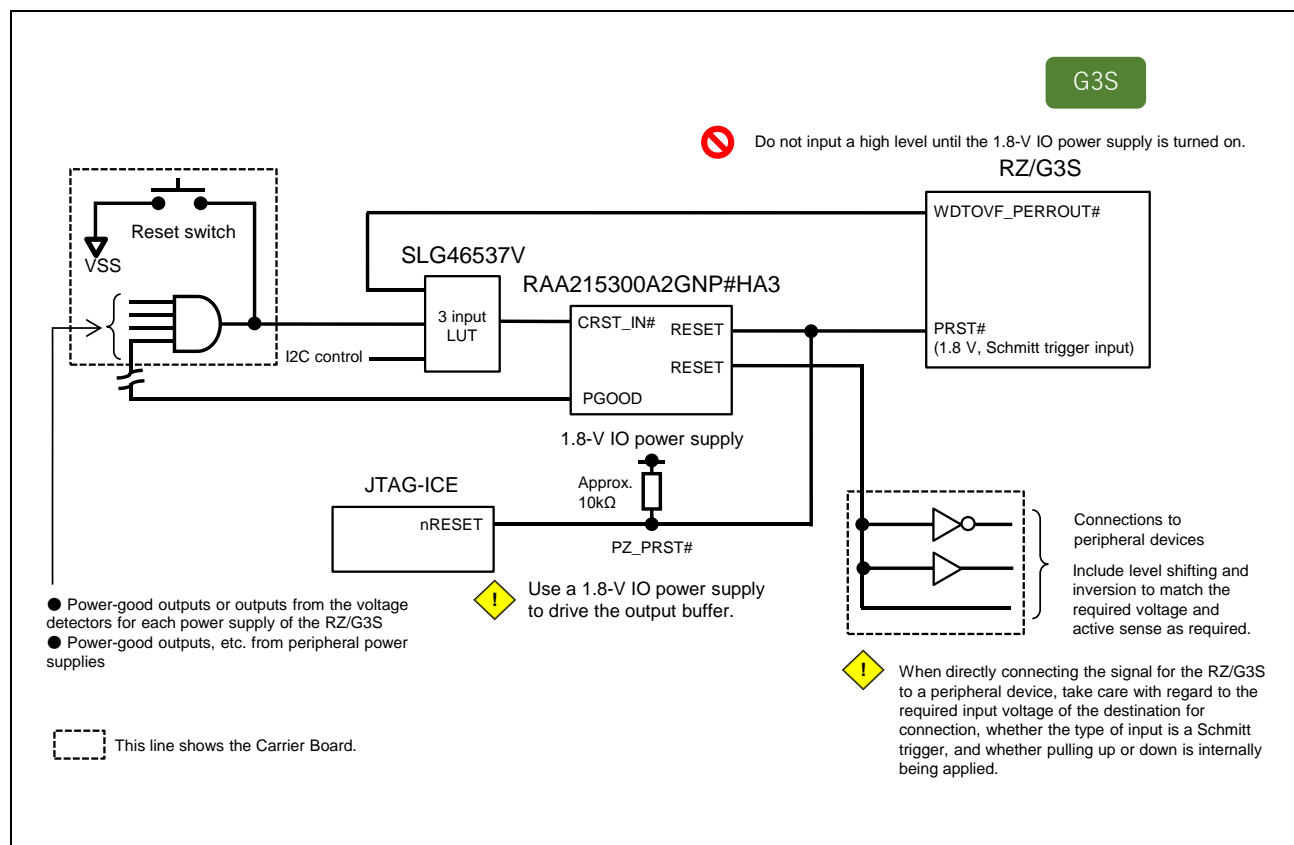
Figure 1.1(d)   Example of a Circuit Configuration Related to the PRST# Signal of RZ/G3S

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of multiplexed pins for individual target devices

- Circuit diagrams of individual evaluation board kits

1.2 Reset Timing

💡 Points
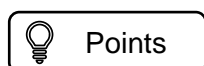
ALL

- At the time of initially supplying power, the PRST# signal must remain at the low level during the period from before the first power supply being turned on until all power supplies have been turned on.

- At the time of turning power off, the PRST# signal must similarly remain at the low level during the period from before any power supply being turned off until all power supplies have been turned off.

- At the time of initially supplying power, the PRST# signal must remain at the low level for at least an additional 1 ms after the last power supply(3.3 V) has been turned on. RZ/G3S is 2 ms.

- When using the PRST# signal to reset RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL while power is being supplied, hold the signal low for at least 100 ns. RZ/G3S is 0 ms.

Figure 1.2   Timing of PRST# Input

Documents for Reference

- Hardware user's manuals for individual target devices

- Application notes for individual target devices

1.3 Adjusting the Timing between Release from the Reset State and the Operation of Clock Oscillators

💡 Points

| G2L | G2LC | V2L |
| G2UL | Five | A3UL |

- When an external oscillator is to be used to input a clock signal through the EXCLK pin, de-assert the PRST# signal after oscillation by the external oscillator has settled.
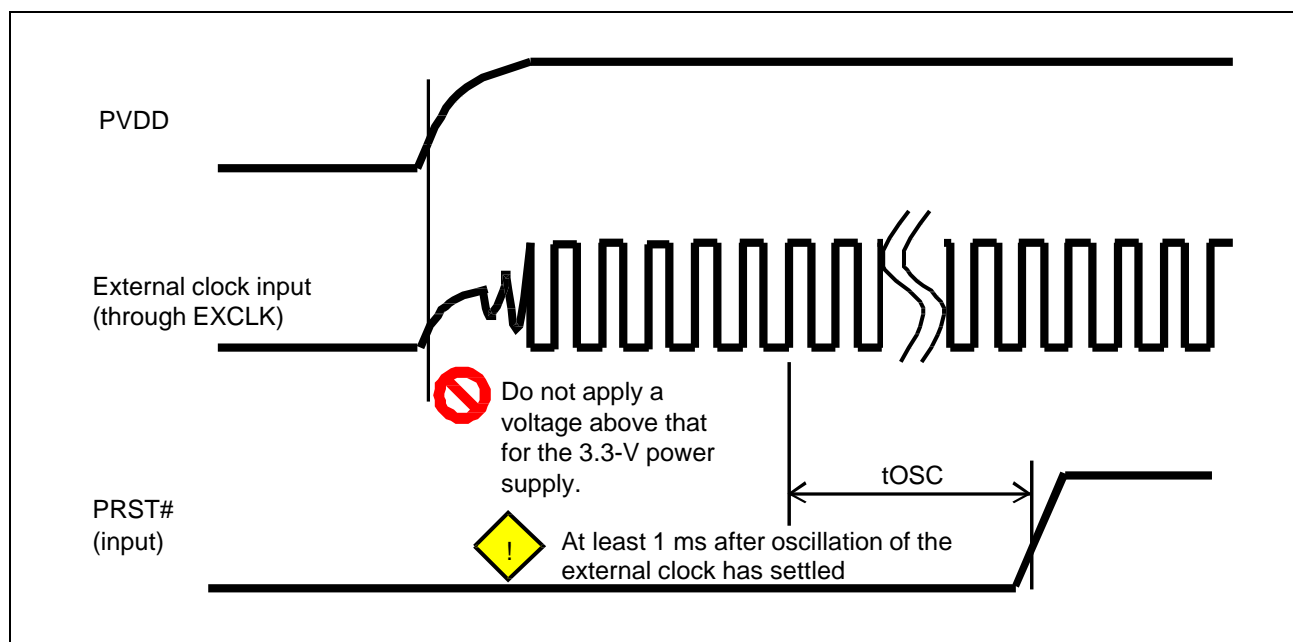
Figure 1.3   Timing between External Clock Input (through EXCLK) and De-assertion of PRST#

Documents for Reference

- Hardware user's manuals for individual target devices

- Application notes for individual target devices

1.4   Resetting Peripheral Devices

💡 Points

ALL

- When using the main reset signals of an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S (the PRST# signal used to reset the device) to reset a peripheral device, take care on the following points.

  – Is power to the peripheral device turned on?

  – Are you observing the correct reset sequence for the peripheral device?

  – Is the active sense of the reset signal for the peripheral device correct?

  – When multiple peripheral devices are connected, are you sure that pull-up or pull-down resistors within the individual devices will not cause the voltage of the reset signal to be at an intermediate level?

  – Is the driving ability (in terms of degree of fan-out) of the reset signals sufficient?

- When the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S have reset pins for exclusive use with specific modules such as the DDR_RESET# pin for DRAM and the QSPI_RESET# pin for the SPI Multi I/O interface the SD0_RST# pin for the SD/MMC host interface, use these pins instead of the PRST# pin.
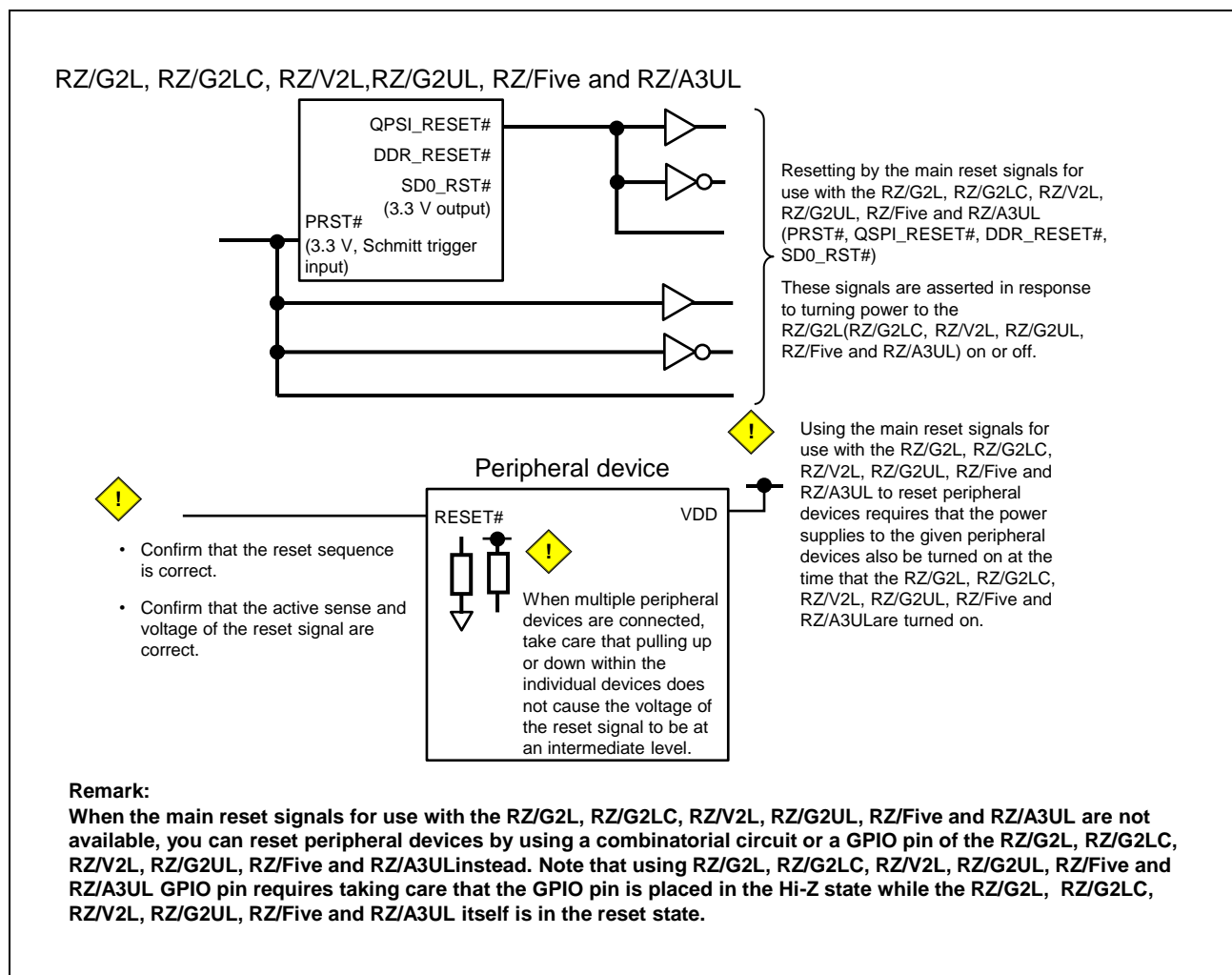
Figure 1.4(a)   Resetting Peripheral Devices
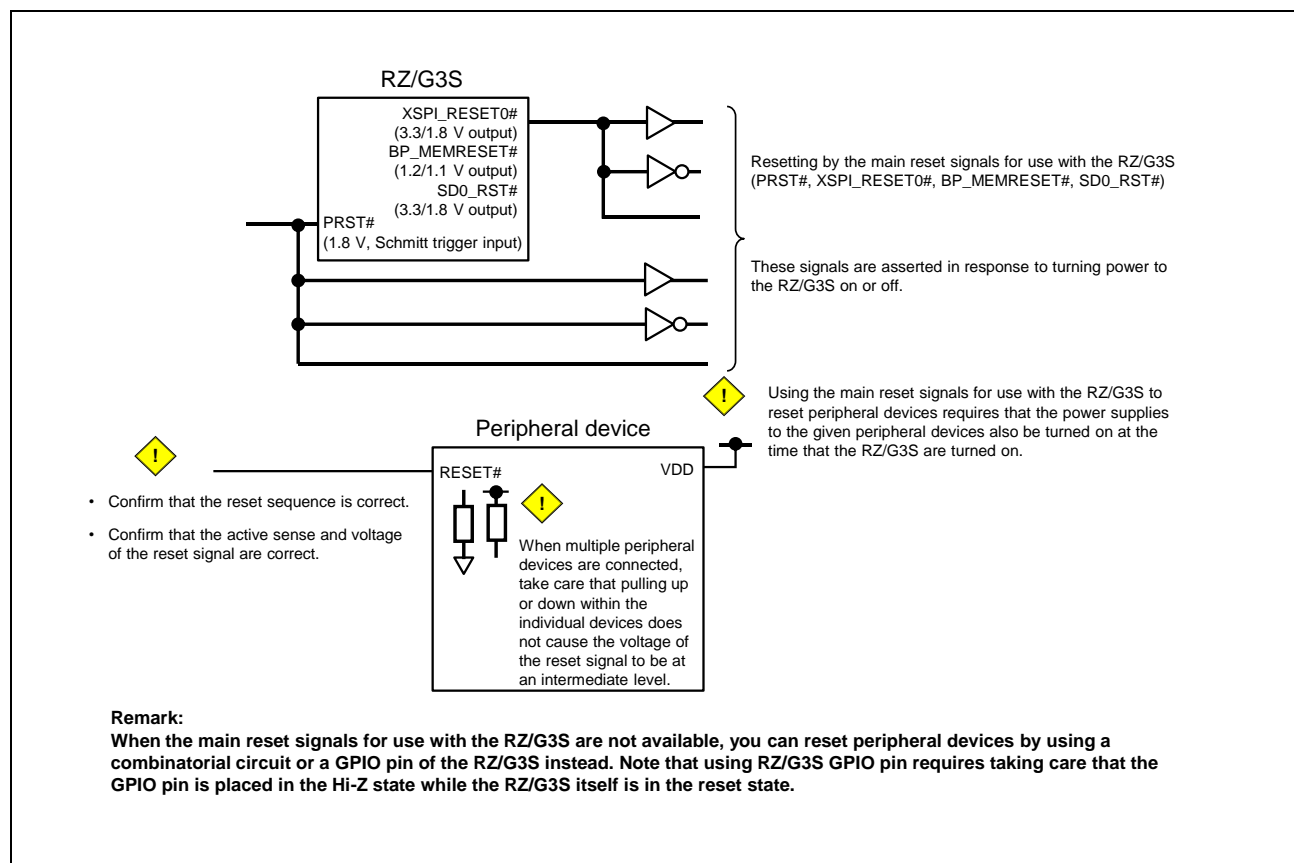
Figure 1.4(b)   Resetting Peripheral Devices

Documents for Reference

- Hardware user's manuals for individual target devices

- Application notes for individual target devices

- Datasheets or technical documents for the individual peripheral devices

1.5　Circuits for Generating TRST# from JTAG-ICE

Points

ALL

- The TRST# signal of a JTAG-ICE is generally controlled by the ICE.

- To use the ICE to reset RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, take the logical AND of the TRST# signal and the PRST# signal for the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

- The circuit configuration must also be such that the PRST# signal does not remain asserted (low) at the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S when the JTAG-ICE is not connected.

- The input on the PRST# pin of the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL are 3.3-V IO. When the voltage at high level of the reset signal from the ICE is different from that of the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL, adjust the voltage of the signal from the ICE to 3.3-V.

- The input on the PRST# pin of the RZ/G3S is 1.8 V and the circuit is 3.3-V tolerant.
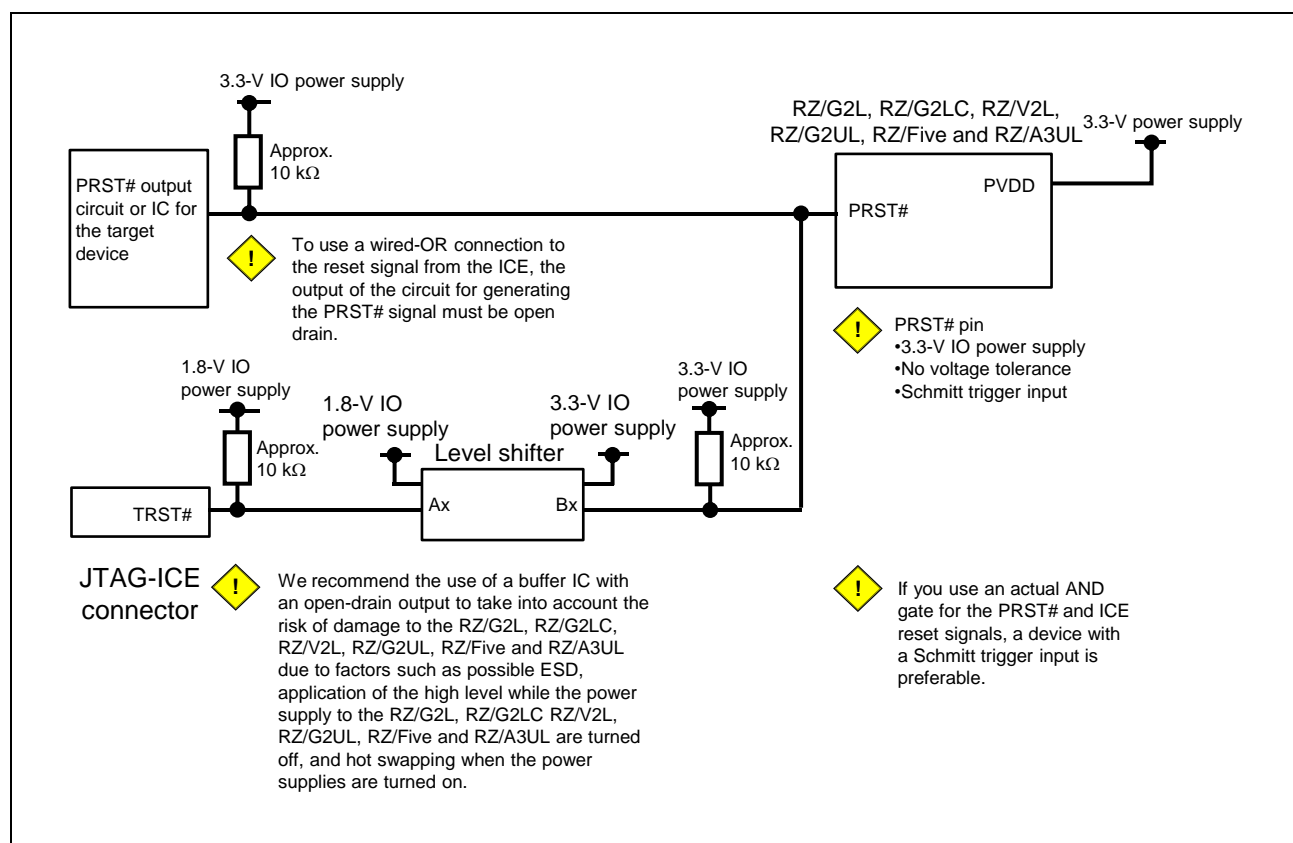
Figure 1.5(a)　Example of the Configuration of a Reset Circuit for Use with a JTAG-ICE
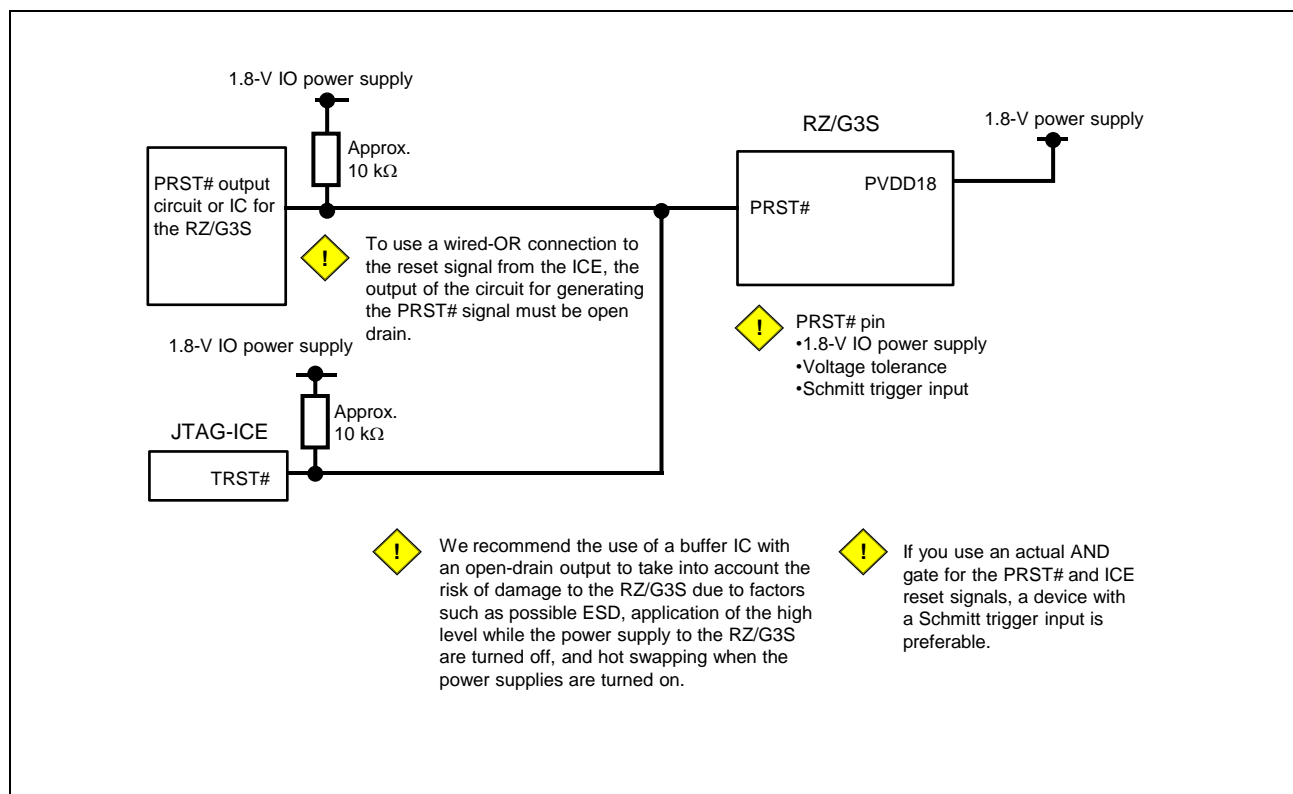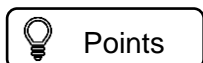
Figure 1.5(b)   Example of the Configuration of a Reset Circuit for Use with a JTAG-ICE

Documents for Reference

- Hardware user's manuals for individual target devices

- Manual of the JTAG-ICE to be used

1.6   Making Reset Signals Open-Drain Outputs

Points

ALL

- When an open-drain output, wired OR, and voltage level shifter are used in the circuits for generating the reset signals for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S (PRST#) and for peripheral devices, take care on the following points.

  − As signals from an open-drain circuit rise relatively slowly, we recommend the use of a Schmitt trigger input on the receiving side.

  − The effect of noise such as crosstalk is very likely to lead to the incorrect behavior of reset signals. Therefore, apply countermeasures for noise such as separating the reset signal from other signals and applying a grounded guard.

  − The overall length of the wiring of a reset signal tends to become greater because of branches to connectors at the edge of a board and so on. This makes dullness of the signal waveform due to stray capacitance more likely. Take this into account in determining the values of pull-up resistors for use with open-drain outputs.

  − When a circuit diagram is spread over multiple pages, distributing the pull-up or pull-down resistors for use with reset signals across multiple pages, that is, the presence of multiple resistors on multiple pages, may lead to operation that is not as intended.

  − We recommend countermeasures such as collecting the resistors for pulling up or down in one region of generation and stating the placement of resistors in a note or notes, and taking into consideration the readability of the circuit diagram.

  − To clarify when initialization by software starts after de-assertion of a reset signal, we recommend taking possible dullness of the rising edge of the signal into consideration in specifying the waiting time.
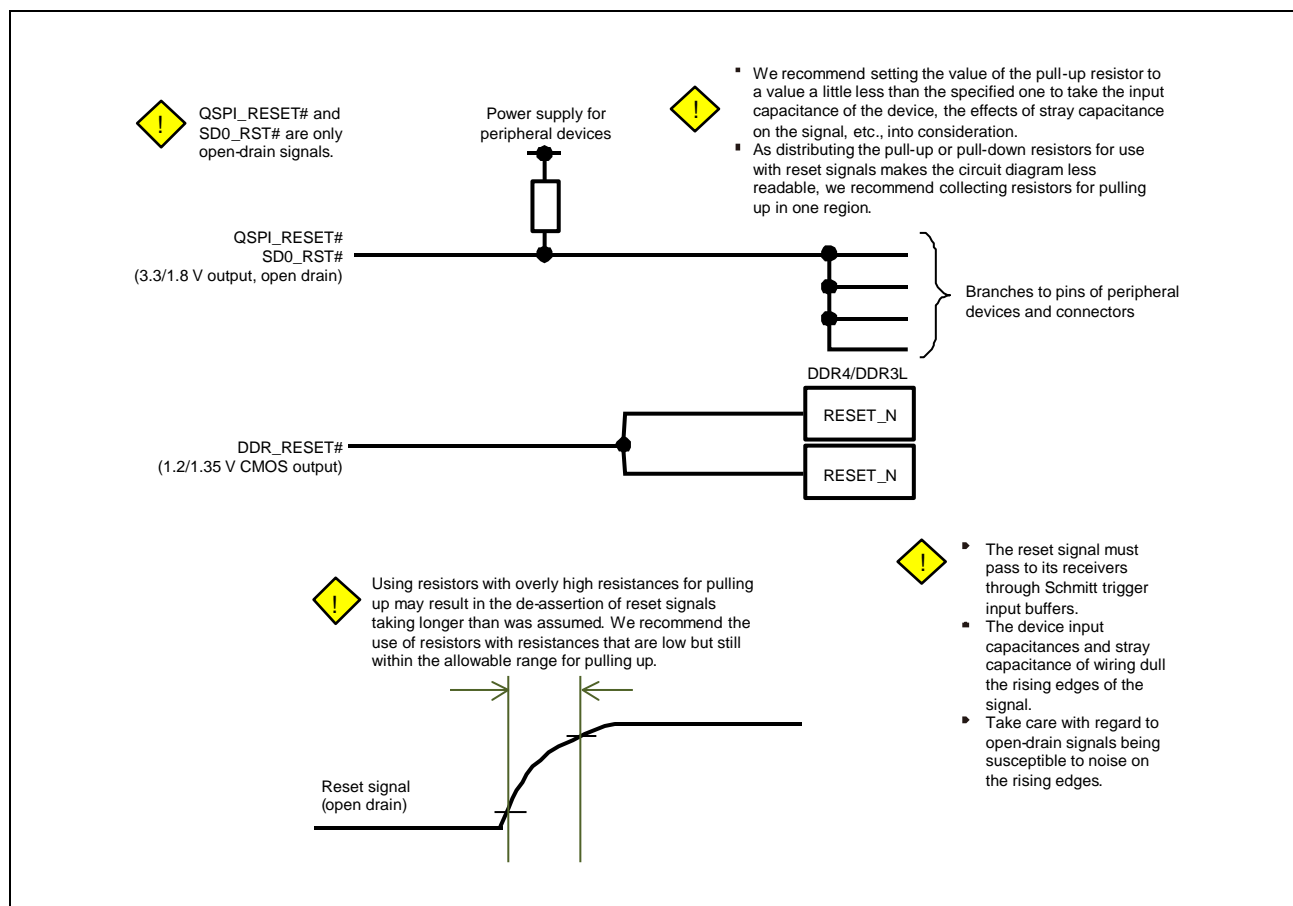
Figure 1.6(a)   Making Reset Signals Open-Drain Outputs
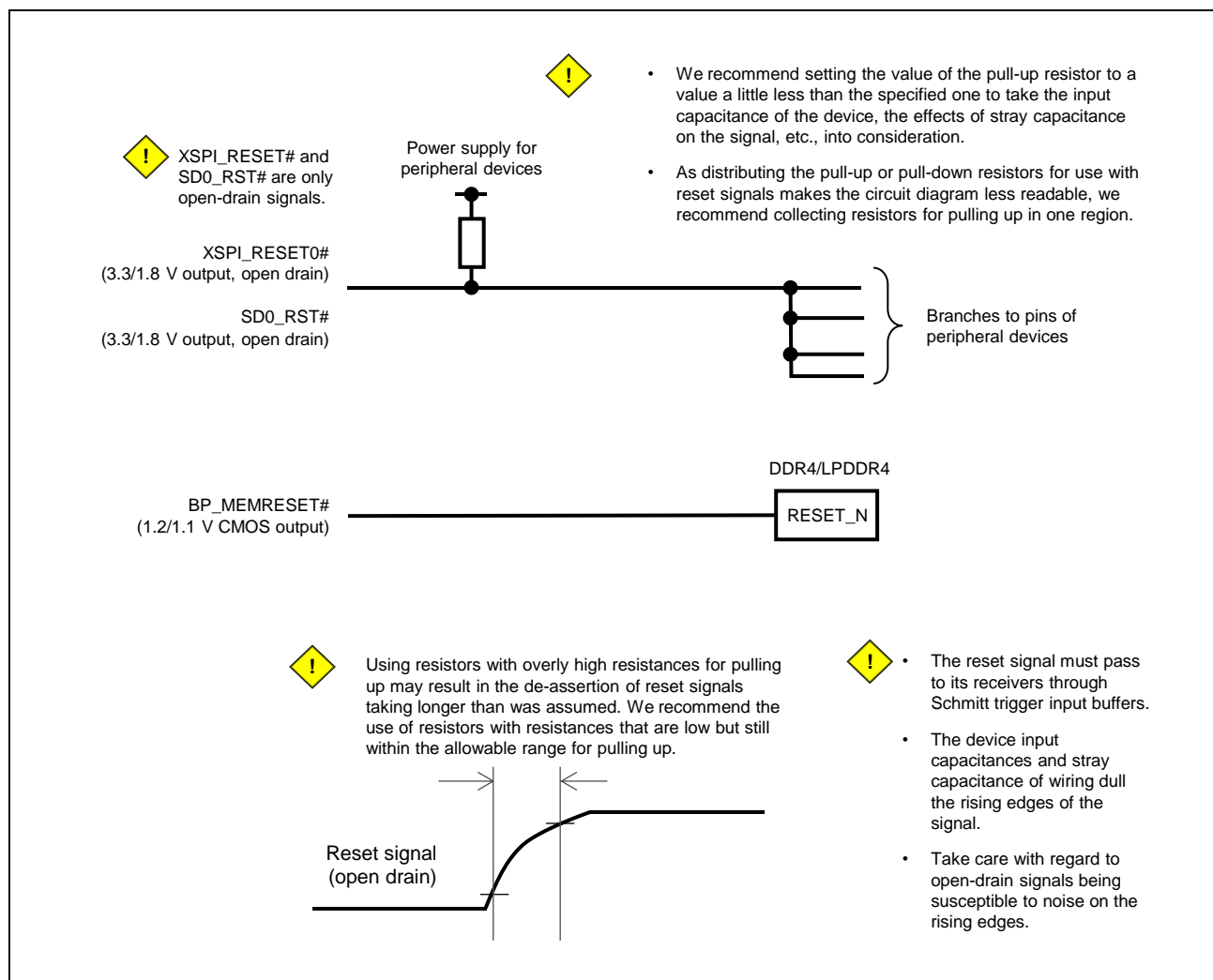
Figure 1.6(b)   Making Reset Signals Open-Drain Outputs

Document for Reference

• Datasheets or technical documents for the individual peripheral devices

1.7   Handling the Mode Pins

Points

ALL

- RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S have mode pins (MDn pins) that are used to set the initial operating mode after de-assertion of the PRST# signal.

- It is capable of setting the voltage levels of the mode pins by using pull-up or pull-down resistors.

- The levels on the mode pins can be held for up to 100ns after the level on the PRST# pin changes from low to high. RZ/G3S is 12 μs.

- The levels on the mode pins are only captured after de-assertion of the PRST# signal. Capture does not proceed in response to other types of reset, such as a software reset.
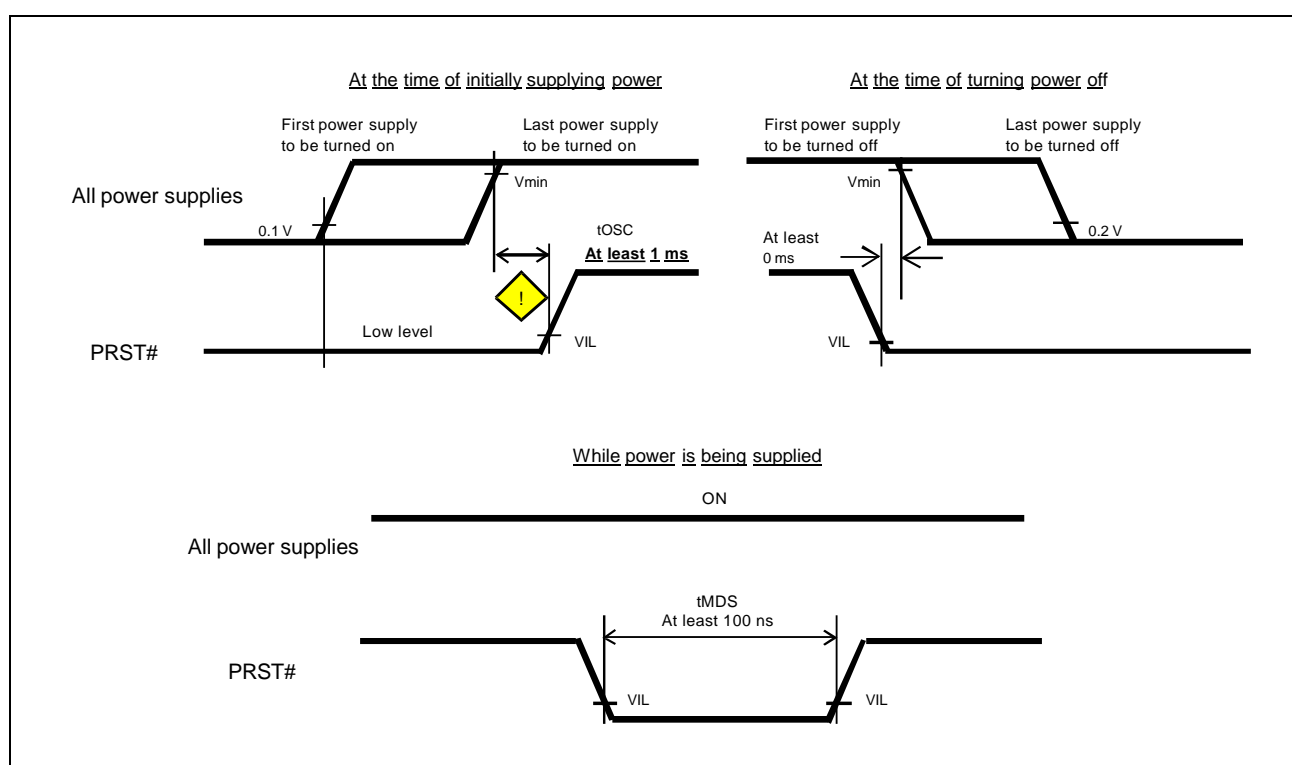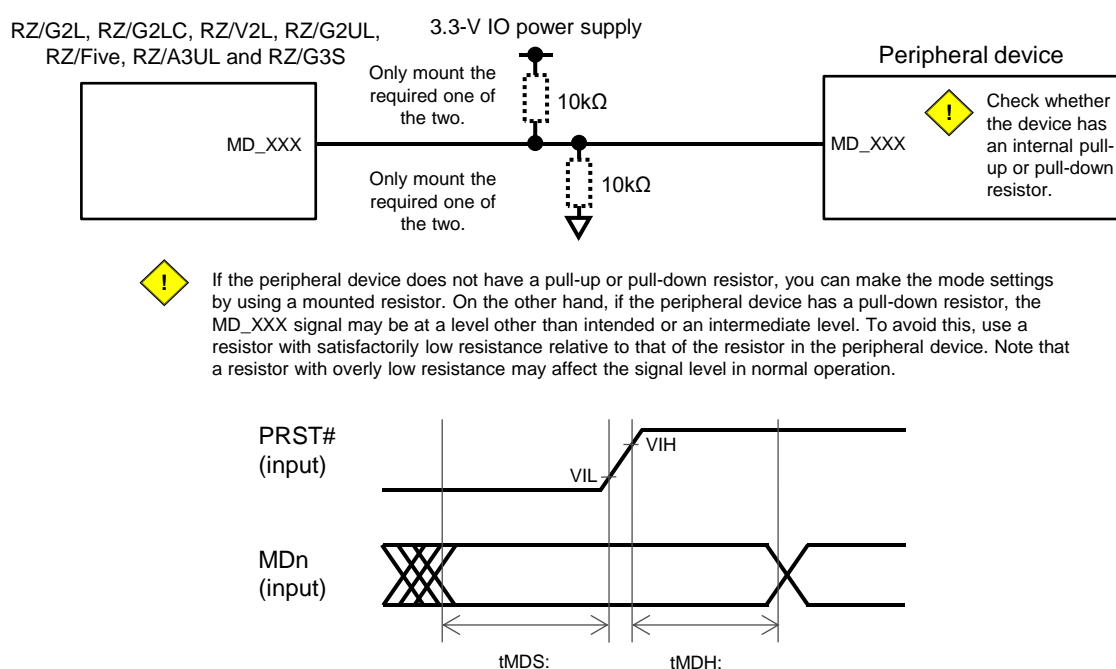

Figure 1.7   Handling the Mode Pins

Documents for Reference

- Hardware user's manuals for individual target devices

- Application notes for individual devices

- Datasheets or technical documents for the individual peripheral devices

2. Points Related to Clock Signals

2.1 Voltage for Clock Input

> 💡 Points

ALL
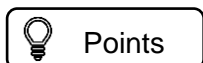
- RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL connect a external clock and a crystal oscillator for a system clock, audio clock, and display clock. RZ/G3S connects a crystal oscillator for a system clock.

- Clock input must conform to the voltage specified by the power domain to which the pin belongs.

- As examples, in the RZ/G2L, the system clock (EXCLK or XIN) is in the 3.3-V IO power domain, AUDIO_CLKn (n = 1, 2) is also in the 3.3-V IO power domain, but CSI_CLKN/P and DSI_CLKN/P are in the 1.8-V IO power domain. That is, the power domain may vary with the clock source.

- Refer to the "Power" column of the pin functions of the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S to confirm to which power domain each clock input belongs in the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, and apply the correct voltage.

- Using a clock input with an incorrect voltage may cause device damage due to a violation of the absolute maximum ratings or malfunction due to insufficient amplitude level.

Table 2.1   Voltage for Clock Input of the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S
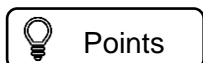
Typical Clock Input Pin		Input Voltage						
		RZ/G2L	RZ/G2LC	RZ/V2L	RZ/G2UL	RZ/Five	RZ/A3UL	RZ/G3S
EXCLK	External System Clock	3.3 V[1]	3.3 V[1]	3.3 V[1]	3.3 V[1]	3.3 V[1]	3.3 V[1]	—
XIN	Crystal Oscillator System Clock	3.3 V[1]	3.3 V[1]	3.3 V[1]	3.3 V[1]	3.3 V[1]	3.3 V[1]	1.8 V[1]
CSI_CLKN/P	Camera Clock	1.8 V	1.8 V	1.8 V	1.8 V	—	1.8 V	—
DSI_CLKN/P	Display Clock	1.8 V	1.8 V	1.8 V	1.8 V	—	1.8 V	—
DISP_CLK	Display Clock	3.3 V	—	3.3 V	3.3 V	—	3.3 V	—
AUDIO_CLK1/2	Audio Clock	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
SCIFn_SCK [n = 0 to 4]	Serial Clock	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
ET0/1_TXC/TX_CLK	Ether Clock	1.8/2.5/ 3.3 V	1.8/2.5/ 3.3 V	1.8/2.5/ 3.3 V	1.8/2.5/ 3.3 V	1.8/2.5/ 3.3 V	1.8/2.5/ 3.3 V	1.8/2.5/ 3.3 V
PCIE_REFCLKP0/N0	PCIe Clock	—	—	—	—	—	—	1.8 V

Note 1.   Fixed to 24 MHz.

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of multiplexed pins for individual target devices

- Circuit diagrams of individual evaluation board kits

2.2 Frequency of the Input Clock

💡 Points

ALL

- The input clock of an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S is frequency-divided by a divider, or frequency-multiplied by the internal PLL and then divided, and then used as the clock for the internal peripheral modules or as external clock output.

- SSCG (spread spectrum clock generator) type oscillators cannot be connected as the input clock of an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S unless specifically stated otherwise in the hardware manual.

- When you use the output clock of an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S as the input clock for external peripheral devices or the operating clock for various interfaces, refer to the section on the CPG in the hardware manual to confirm whether required clock signals can be generated.

- The system clock is frequency-multiplied to obtain each kind of clock. Deviation of the oscillation frequency (center frequency) of the input clock (the system clock) affects the center frequency and deviation of the DDR_CK.

Documents for Reference

- Hardware user's manuals for individual target devices
- Lists of multiplexed pins for individual target devices

2.3 Accuracy and Deviation of the Input Clocks

Points

ALL

- In many cases, the input clock of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S is frequency-multiplied by the internal PLL and then divided, and then used as the clock for the internal peripheral modules or as external clock output.

- In general, the specifications of crystal resonators are based on the temperature characteristics, the degree to which oscillation may deviate from the oscillation frequency (center frequency), and so on.

- As with crystal resonators, the specifications of crystal oscillators and clock synthesizers are also based on the degree to which oscillation may deviate from the oscillation frequency (center frequency).

- When using the clock generated by the internal PLL or divider of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S as the clock source of external peripheral devices or modules, you might have to consider the deviation of the input clock.

- The system clock provides the source of each kind of clock through frequency-multiplication. Any deviation in the frequency of the input clock (the system clock) thus produces deviation in the frequency of clock after multiplication.

- To design a system such that the maximum frequency of the DDR_CK does not exceed the maximum frequency specified for the DRAM, you must select the center frequency of the system clock input in consideration of possible deviation.

- When using either or both MIPI DSI and USB for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL, the jitter of the EXCLK should be less than 40ps. On the other hands, when not using both MIPI DSI and USB, the jitter of the EXCLK should be less than 80ps.

Table 2.2   Accuracy and Deviation of the Input Clocks of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S

Typical Clock Input Pin		Frequency Deviation (Recommended Value)[1]						
		RZ/G2L	RZ/G2LC	RZ/V2L	RZ/G2UL	RZ/Five	RZ/A3UL	RZ/G3S
EXCLK	External System Clock	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]	—
XIN	Crystal Oscillator System Clock	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]	±50ppm[2]

Note 1.   SSCG (spread spectrum clock generator) type oscillators cannot be connected as the input clock of an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S unless specifically stated otherwise in the hardware manual.

Note 2.   When using RGMII interface. If not using RGMII mode, this spec is ±100 ppm.

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of multiplexed pins for individual target devices

2.4   Notes on Crystal Oscillator Circuits

Points

ALL

- For the load capacitance, damping resistance and feedback resistance of the crystal oscillator circuit, determine appropriate values based on the evaluation of oscillation by the selected crystal resonator manufacturer.

- For the provisional value of the load capacitance before evaluating the oscillation, select a value that meets the characteristics of the resonator.

- A feedback resistance can be removed, but depends on the characteristics of a crystal oscillator and circuit configuration and layout. Please make your decision based on the oscillation evaluation.

- In evaluating the oscillation, adding a feedback resistance is relatively easy, but adding a damping resistance is difficult. Select the value of the damping resistor in consideration of adjustment in evaluating the oscillation.

- Observe the following notes for the crystal oscillator circuit, even though they are not stated in the hardware manual:

  - Bypass Capacitors
    Insert laminated ceramic capacitors as bypass capacitors for each VSS/VCC pair. Mount the bypass capacitor near the power supply pins of the LSI. Use components with a frequency characteristic suitable for the operating frequency of the LSI, as well as a suitable capacitance value.

  - Notes on Using a PLL Oscillation Circuit
    Keep the wiring from the PLL VDD and VSS connection pattern to the power supply pins short, and make the pattern width large, to minimize the inductance component. The analog power supply system of the PLL circuits is sensitive to noise. Therefore, system malfunction may occur by the intervention with another power supply. Do not supply the analog power supply with the same resource as the digital power supply of VDD and VCC.

  - When Using an External Crystal Resonator
    Place the crystal resonator, capacitors Cin and Cout, and damping resistor Rd as close to the XIN and XOUT pins as possible. To minimize induction and thus obtain oscillation at the correct frequency, the capacitors to be attached to the resonator must be grounded to the same ground. Do not bring wiring patterns close to these components.

- Observe the following other notes for the crystal oscillator circuit:

  - Do not cross the circuit with other signal lines.

  - Keep the circuit away from lines that carry large currents.

  - Do not ground the circuit to ground patterns that carry large currents.

  - Do not bring signals out from the oscillator circuit.

- The result of our crystal marching evaluation is shown below as a reference example. In our case, a feedback resistance is implemented after evaluation. Please check the specification of the crystal oscillator to be used, and implement the appropriate load capacitance, damping resistor and feedback resistor.
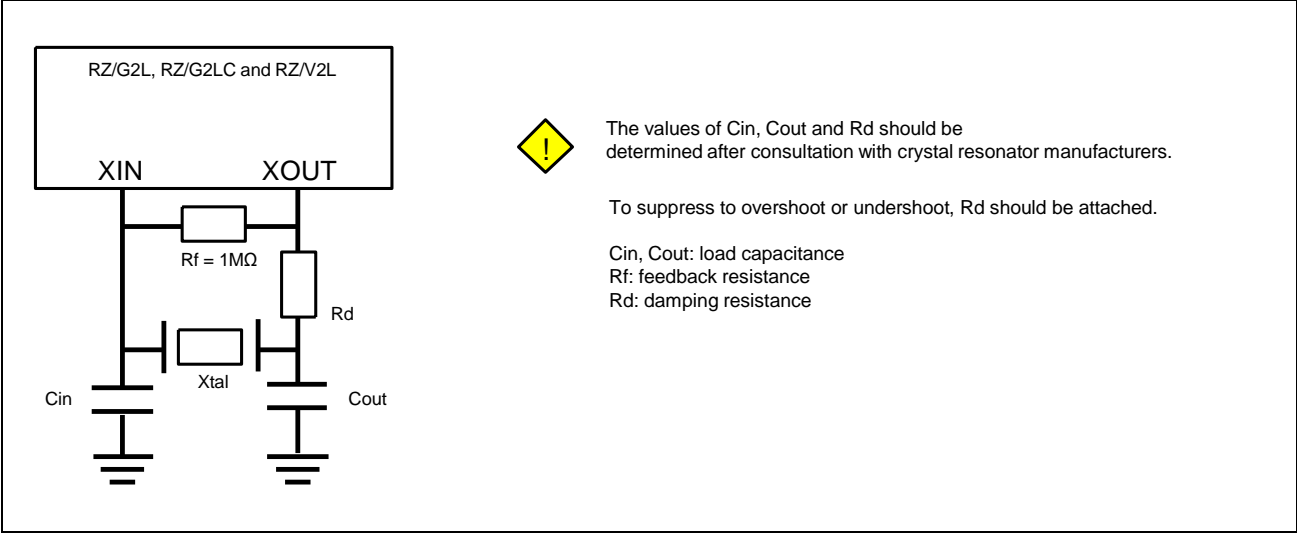
Figure 2.1(a)   Crystal Oscillator Circuit

Table 2.3(a)   Characteristics by Recommended Constants (CL = 8 pF)

Condition			
Xtal	Rd	Cin	Cout
CX1612DB 24 MHz	0Ω	6 pF	6 pF
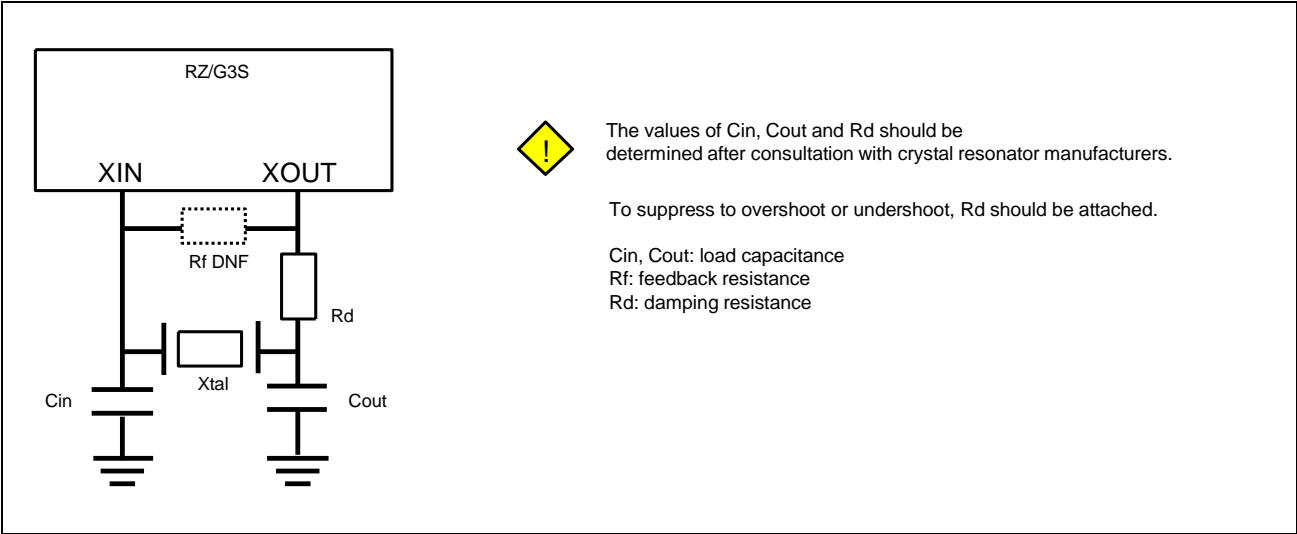
Figure 2.1(b)   Crystal Oscillator Circuit

Table 2.3(b)   Characteristics by Recommended Constants (CL = 8 pF)
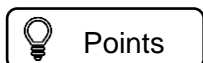
Condition			
Xtal	Rd	Cin	Cout
CX2016SA 24 MHz	0Ω	6 pF	6 pF

Documents for Reference

- Lists of multiplexed pins for individual target devices

- Circuit diagrams of individual evaluation board kits

- Application notes for individual target devices

2.5   Terminal Processing for External Clock Input of the System Clock

Points

ALL

- The system clock of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL consists of the XIN and EXCLK pins to support external clock input. The system clock of RZ/G3S only consists of XIN.

- Set by terminal processing to set whether to connect a crystal resonator or an external crystal oscillator to the system clock pins.

Table 2.4(a)   Terminal Processing for System Clock Input for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

Device	System Clock Operation	External Clock Input Pin
RZ/G2L	Connecting a crystal resonator	
RZ/G2LC RZ/V2L RZ/G2UL RZ/Five RZ/A3UL	Inputting an external clock	EXCLK pin[1]

Note 1.   The XIN pin can be pull-down if external clock input is used. The XOUT pin can be left open-circuit.

Table 2.4(b)   Terminal Processing for System Clock Input for RZ/G3S

Device	MD_BYPASS Pin Setting for System Clock Input	System Clock Operation
RZ/G3S	MD_BYPASS = L	Connecting a crystal resonator
	MD_BYPASS = H	Connecting a crystal oscillator

Documents for Reference

- Circuit diagrams of individual evaluation board kits

2.6 Selecting Oscillator Drive Strength

💡 Points
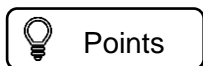
G2L   G2LC   V2L

G2UL   Five   A3UL

- The MD_OSCDRV[0:1] terminals of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five and RZ/A3UL are function of arranging the drive strength of crystal oscillators.

- Please use 24 MHz for the crystal and connect these terminals to ground.

- Other settings are not supported.

RZ/G2L, RZ/G2LC, RZ/V2L,
RZ/G2UL, RZ/Five and RZ/A3UL

⚠️ Connect these terminals to ground.

MD_OSCDRV0

MD_OSCDRV1

GND
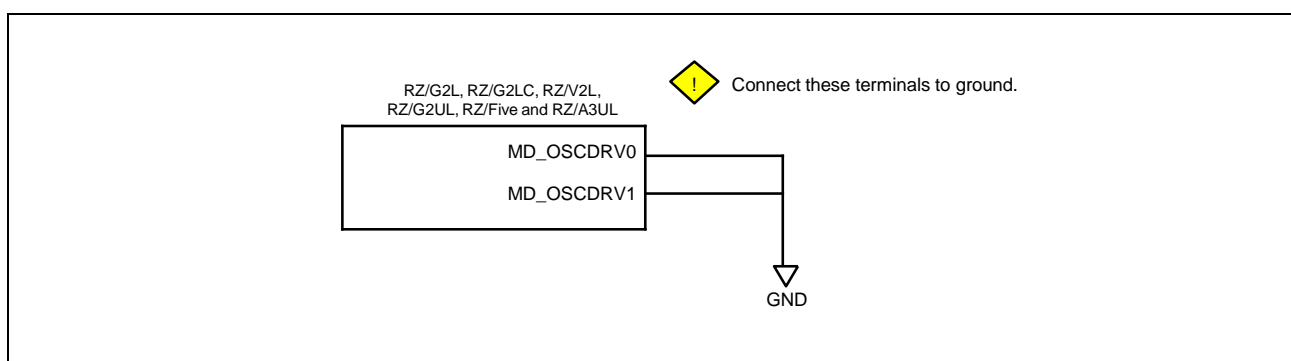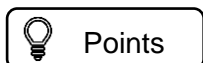
Figure 2.2   Handling the MD_OSCDRV[1:0]

Documents for Reference

- Circuit diagrams of individual evaluation board kits

2.7 Clock Input for Peripheral Devices

Points

ALL

- It is also necessary to pay attention to the clock input and clock oscillator circuit of peripheral devices, as with RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S. Read the data sheets and manuals of the individual peripheral devices carefully to avoid improper design.

- If you intend to use the output clock of an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S as the input clock for a peripheral device, pay attention to the voltage of the clock output (the power domain to which the clock pin belongs and the interface level), and the clock frequency and accuracy.

- Please refer to the datasheet of the peripheral devices to be used.

Documents for Reference

- Circuit diagrams of individual evaluation board kits

2.8   General Notes on the Clock Circuit and Wiring

💡 Points

`ALL`
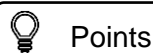
- Pay attention to the following general notes when designing the clock input and clock output circuits. In addition, important points to be considered in PCB pattern design, such as the GND shield, are helpful in circuit diagram review and evaluation after the board is completed. State the important points as notes on the circuit diagram as far as possible.

  - Properly reduce the load on the clock line to prevent malfunctions due to rounding of the clock signals on rising or falling edges. When the load is too large, take measures such as inserting a clock buffer.

  - Avoid unnecessary branches and stubs as much as possible to avoid degradation of the signal quality caused by reflection. Use continuous patterns for branching as much as possible. When the wiring requires a T branch, take measures such as inserting a clock buffer.

  - When inserting a clock buffer, be sure to consider the effect of clock delay. When delay is a problem, take measures such as using a zero-delay buffer.

  - Prepare circuits and pads in consideration of adjustment of the clock quality after the board is completed.
    - Insert a damping resistor such that the resistor is near to the outputting terminal of the clock signal
    - Placing a termination circuit such as a Thevenin termination near to the receiving terminal of the clock signal

  - Use routes that minimize variations in characteristic impedance. Measures for this include keeping routes in the same PCB wiring layer and minimizing the use of via holes in clock wiring.

  - Prevent the wiring for the clock and other signals from running side by side to avoid crosstalk noise and take measures such as applying a ground shield where appropriate.

  - Consider the layout in terms of avoiding excessive noise from switched-mode power circuits and so on.

  - In the case of circuits for selecting from among two or more clock signals, use chip jumper blocks with 0-Ω resistors and use a pattern that minimizes the number of stubs.
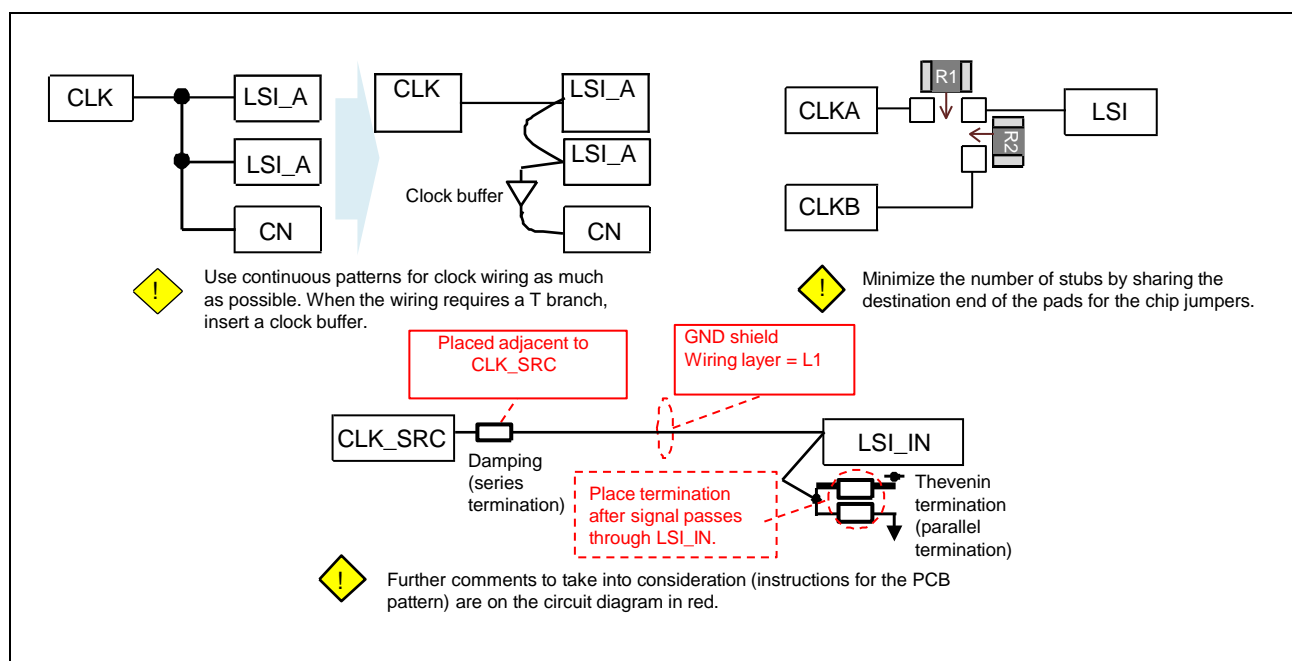
Figure 2.3   General Notes on the Clock Circuit and Wiring

Document for Reference

- Circuit diagrams of individual evaluation board kits

3. Points Related to Power Supplies

3.1 Power Supply Capacity for Targeted Devices and Peripheral Devices

💡 Points

ALL

- The RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S system, which includes extended functions such as SD cards and USB memory, and peripheral devices such as memory devices and communications devices, requires a wide variety of power supplies.

- For RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S in the development phase, values for current drawn are provisional, so they might vary during the course of development.

- The logic power supply has to be able to provide particularly large currents, so its capacity to supply power should be designed with a margin that allows for increases above the estimate of current drawn.

- For a power supply that is to be the source of multiple power supply voltages, take measures in consideration of the efficiency of each power supply IC, such as stepping down voltages in two stages.

- In order to "visualize" the possibility of power capacity being insufficient, we recommend that you create a calculation sheet, such as a power tree.

- Please refer to the datasheet for the electrical characteristics of the power supply IC and peripheral devices to be used.
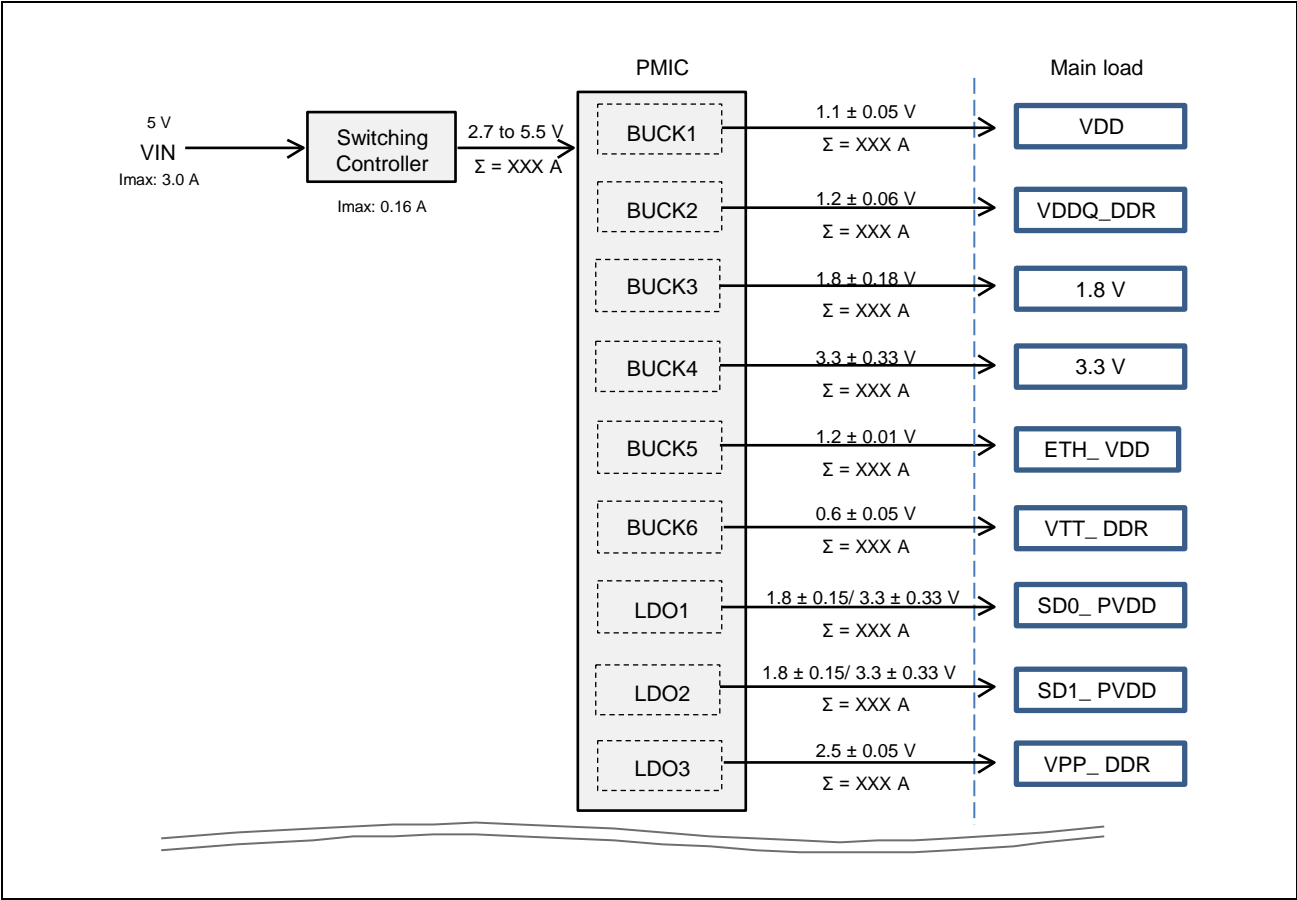
Figure 3.1   Example of a Power Tree (Image)

Documents for Reference

- Hardware user's manuals for individual target devices

3.2 Power Supply Capacity of VDD

Points

ALL

- When selecting a power supply IC for the logic power supply, make sure that its specifications satisfy all power supply voltage specifications of the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S to be used, including the load regulation specifications and load response specifications of the power supply IC. Although it is not a recommendation or guide in particular, the power supply IC must have the following performance so that the power supply voltage supplied to the logic power supply can meet the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL and RZ/G3S specifications.

    - Load regulation specifications including load fluctuations in steady state:
      less than ±50mV under VDD (1.1V) @RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

    - less than TBD under VDD (0.9V) @RZ/G3S

- Simply calculating, on a desk, the maximum current drawn from the electrical characteristics, and designing the power supply capacity with a margin based on the results of calculation is desirable. However, designing a power supply that allows a margin of two or three times for the maximum current is not easy without significantly increasing costs. The following methods can be used to reduce the cost of the power supply by estimating the details of the standard power consumption.

    - Setting the power supply voltage to TYP + α (allowing for the accuracy of the power supply voltage) to be set for the power supply IC, rather than to the maximum value in the specification

    - Excluding (from the estimate) modules that are not to be used among the internal modules

    - Using duty ratios based on anticipated use cases rather than current drawn during full operation

    - Implementing a margin based on addition rather than multiplication (for example, using +1 A or 2 A instead of two to three times the maximum value)

- If the margin is reduced, the instantaneous peak of the current drawn might exceed the power supply capacity. The following methods can be used to compensate for this.

    - Using several capacitors with large capacitances, such as 10 to 100 μF, to absorb sudden increases in load current

    - Increasing the response of the power supply IC, by increasing the switching frequency of the power supply IC by a value of the order of several MHz, and implementing a multi-channel power supply IC configuration

    - Limiting the overcurrent protection of the power supply IC to the original maximum current + α to prevent unexpected shutdowns

- Finally, if you have not secured adequate margins on your desk, perform sufficient evaluation with the actual machine and software by increasing the number of boards to be evaluated and verify whether power supply integrity is maintained. In addition, you must consider advance measures for shortages of power capacity.

- Please refer to the datasheet of the power supply IC to be used.

Documents for Reference

- Hardware user's manuals for individual target devices

3.3 Power Supply Voltage and Power Sequence of Targeted Devices and Peripheral Devices

💡 Points

ALL

- To turn RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S on or off, follow the sequence stated in the electrical characteristics of hardware manual.

- The signal pins of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL are not voltage tolerant. The signal pins of RZ/G3S is not voltage tolerant, except to the voltages in some types of I2C, PRST# and USB0_VBUSIN. Therefore, note that pull-up and signal input exceeding the power supply voltage might exceed the rated values and damage the LSI chip. In some cases, however, peripheral devices will have the same specifications as RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

- In order to prevent errors in the sequence and power supply voltage, we recommend you to chart the sequences of all the power supplies of the system including resets of RZ/G2L (or RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, RZ/G3S) and peripheral devices for all the power supplies defined in the power tree and confirm that there is no problem.

- With regard to the sequence of switching power off, the before-and-after relations of items in the sequence might change depending on whether a discharge circuit is present. Therefore, also consider the effect of a discharge circuit on the sequence.

- For the power sequence of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, a condition for the next time power is switched on is that the power supply voltage has dropped below a specified value the last time the power was turned off. Therefore, note that turning the power on again while discharge is insufficient so that the power supply voltage has not dropped sufficiently is technically a rated-values violation.

- Although there are no specifications for the slope (mV/s) of the rising or falling of the power supply voltages, monotonic increases are assumed for rising. Make sure that there is no excessively long step or voltage drop as rising proceeds.

- We recommend that you configure the initial hardware to allow adjustment for imperfections in the power supply sequence in the initial phases of evaluation. For example, use power supply ICs (PMICs) and power management microcontrollers which allow changing of the control programs, and prepare a pattern for a discharge circuit to allow for the possibility that one may be required.

- Please refer to the datasheet of the power supply IC and peripheral devices to be used.

Documents for Reference

- Hardware user's manuals for individual target devices

3.4 Noise Filter Circuits for Power Supplies

Points

ALL
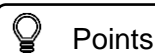
- For RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S filters are recommended in the evaluation board kits or guidelines for power supply filter circuits to take account of the noise-sensitivity of dedicated power supplies such as the PLL and analog power supplies.

- Refer to the related guidelines and make sure that the recommended power supply filter circuit is installed for each power supply.

- The CPG PLL power supply circuits on the evaluation board kits have a proven track record, so we recommend that you insert an LPF with the same configuration as on an evaluation board for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S you will be using.

- From the viewpoint of noise superimposition between PLL power supplies, we do not recommend the merging of multiple CPG-PLL power supplies.
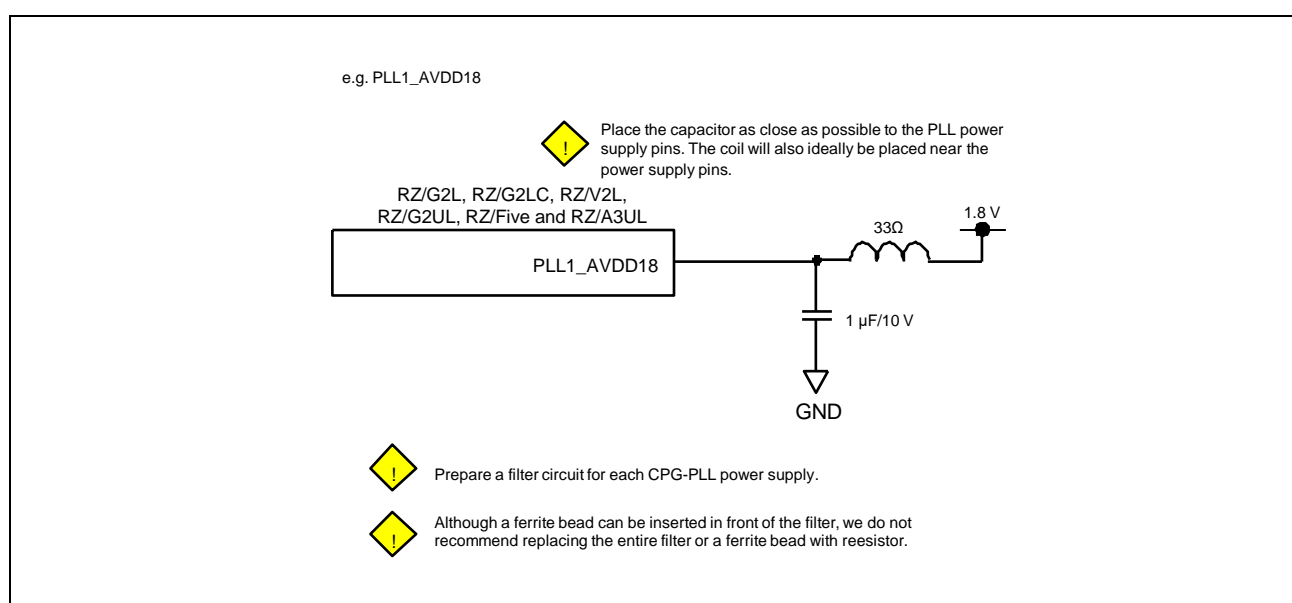
Figure 3.2   Filter Circuit for the CPG-PLL Power Supply Used on the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL Evaluation Board Kit

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

3.5   Impedance Design for the Power Supplies

Points

ALL

- For RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, the logic power supplies such as VDD, noise-sensitive DRAM IO power supply, and the power supplies of the high-speed serial interfaces are represented as power supply impedances or inductances.

- The values Renesas indicates are only target values and are not guaranteed. Use these values as guides in the design of power supplies.

- Although a malfunction may not occur immediately if a target value is not observed, there is an increased risk of malfunction.

Table 3.1   Guidelines Covering Descriptions Related to the Impedance Design for the Power Supplies of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S

Device	Guideline
RZ/G2L RZ/G2LC RZ/V2L RZ/G2UL RZ/Five RZ/A3UL	[VDD] • PCB verification guide for Core VDD [DDR4 IO Power] • PCB verification guide for DDR4/DDR3L • PCB design guideline for DDR4/DDR3L [USB 2.0/CSI/DSI] • PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2
RZ/G3S	[VDD] • PCB verification guide for Core VDD [DDR IO Power] • PCB verification guide for LPDDR4/DDR4 • PCB design guideline for LPDDR4/DDR4 [USB 2.0/PCIe] • PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

Documents for Reference

- Hardware user's manuals for individual target devices

- PCB verification guides for individual target devices

- PCB design guidelines for individual target devices

- Circuit diagrams of individual evaluation board kits

3.6 Bypass Capacitors for the IO Power Supplies and Peripheral Devices

💡 Points
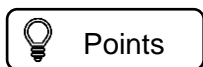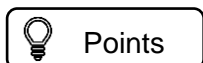
ALL

- There are no recommended capacities for bypass capacitors for the general-purpose digital IO power supplies of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S. However, use the evaluation board kit as a reference to determine the appropriate number and capacity of bypass capacitors.

- It is desirable to use a single ceramic 0.1-µF capacitor per pin of the IO power supply as a bypass capacitor. However, arrange the appropriate number of capacitors in consideration of the signal operating frequencies, the number of operations that will simultaneously be in progress, and the priority of other power bypass capacitors and filter circuits.

- If many signals will be operating simultaneously, place a capacitor with a relatively large value of about 10 µF at the end of the PCB IO power supply pattern.

- Confirm that the bypass capacitors for peripheral devices are appropriate, as well as RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S. The recommended capacities and PCB wiring patterns might be stated in the provided data sheets and technical documents of some devices.

- Coordinate with the PCB pattern designer with regard to obtaining the best implementation of bypass capacitors, such as their placement near the target power supply pins and the capacitance values, by stating them in notes. For example, bypass capacitors for the BGA parts should be 0.1 µF or less when located within the area on the other side of the board under the LSI, and at least 1 µF when not located within the area on the other side of the board under the LSI.

- Please refer to the datasheet of the peripheral devices to be used.

Documents for Reference

- Circuit diagrams of individual evaluation board kits

3.7 Selecting Ceramic Capacitors

Points

ALL

- When a multilayer ceramic capacitor is used as a bypass capacitor, the effective capacitance decreases depending on the DC bias characteristics and temperature characteristics.

- For details, check the characteristics provided by the manufacturer of a capacitor. However, the trends are as follows:

  - The rate of decrease of the effective capacitance depends on the dielectric of the capacitor in use.

  - The effective capacitance tends to decrease with the working voltage margin for withstand voltage.

  - For capacitors with relatively high capacitance (10 μF or higher), the effective capacitance decreases significantly with the body size.

- Note that when a capacitor with a large capacitance is used to support sudden changes in the load current, the desired effect might not be fully obtained due to a decrease in the effective capacitance.

- Make sure that the withstand voltage of the capacitor is at least three times the working voltage.

- If the decrease in the effective capacitance is a problem, also consider the capacitor characteristics: F, X5R (= the dielectric in use).

- When you select a capacitor with a small body, pay attention to the decrease in the effective capacitance. In terms of the effective capacitance, the effective capacitance of two small capacitors can correspond to that of a single larger capacitor.

- Please refer to the datasheet for the electrical characteristics of the multilayer ceramic capacitor to be used.

3.8   Design of the Power Supply IC Circuit

Points

ALL

- The datasheets and technical documents for power supply ICs usually cover the reference circuits useful for configuring power supply circuits.

- Especially for switching regulators, the power supply quality might be significantly degraded depending on the circuit constants, or oscillation might occur. Therefore, the manufacturer and model number of the components used in the provided reference circuits are amply stated in many cases.

- Verifying the selection of specific components and the margins (for phase and gain) by using a simulation tool might be possible.

- When you design power supply circuits, use the technical information and reference circuits provided by the power supply IC manufacturers to make sure that the recommended circuits and constants are observed.

- The recommended designs for PCB wiring patterns and heat dissipation might also be stated, follow the recommendations.

- Carefully confirm the specifications of the coils, FETs, diodes, and other components that need to be selected according to the current drawn in the actual use cases so that they do not violate the ratings. We also recommend writing comments regarding the confirmed characteristics on the circuit diagram to help in component selection at design reviews and in response to changes of specifications.

- Pay attention to the allowable losses (W) when inserting a shunt resistor into the power supply line for current measurement.

- Please refer to the datasheet of the power supply IC or peripheral device to be used for the electrical characteristics.

- Please refer to the datasheet for the electrical characteristics of the components used in power supply circuits and power supply IC to be used.
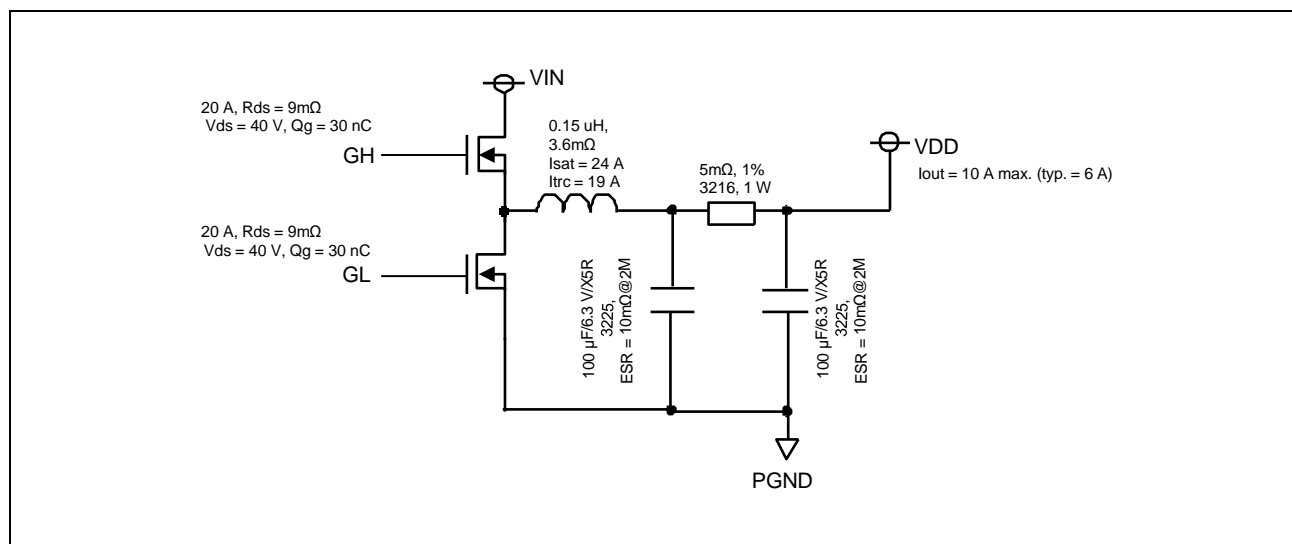
Figure 3.3   Example of Stating the Characteristics of Peripheral Power Supply Components

3.9   Remote Sensing of Output Voltage from the Power Supply IC

Points Points

ALL

- In recent LSIs, the logic power supply currents have increased and the power supply voltage range has narrowed, and power supply ICs that have a remote sensing function for the output voltage to improve the quality of a power supply have been appearing.

- The quality of a power supply can be maintained by placing a remote sensing pin near the load (the LSI) and canceling out IR drops in the power supply line.

- For details on the function of the remote sensing signal, refer to the manual for the power supply IC in use. General notes are given below.

  – Feeding back the voltage on the end of the current path is desirable in terms of fully utilizing a remote sensing function.

  – If sensing at the end is difficult because of the pattern design, handle sensing at least in the vicinity of the input capacitor near the LSI and cancel out IR drops between the power supply IC and LSI.

  – As with other noise-sensitive signals, apply countermeasures such as avoiding parallel runs of the remote sensing and other signal wiring or applying ground shields in order to prevent noise from applying to the remote sensing signal.

  – If a paired GND signal is provided, wire the GND signal and the remote sensing signal in a pair, and take the above precautions against noise as well.

- Please refer to the datasheet of the power supply IC to be used.
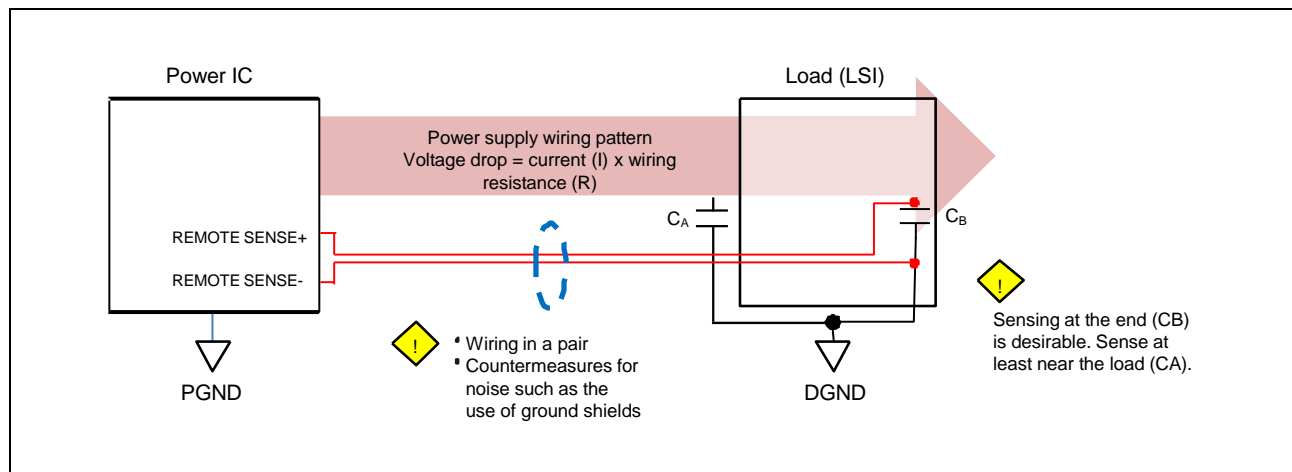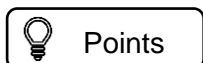
Figure 3.4   Remote Sensing Input of a Power Supply IC

Documents for Reference

- Circuit diagrams of individual evaluation board kits

3.10 Notes on Supplying Power through Connectors

Points

ALL

- When supplying power through a connector, be sure to provide sufficient power supply pins and GND pins for the maximum current value.

- Calculate the amount of current per pin from the allowable current and contact resistance of the connector pin.

- According to the amount of current near the connector, place a capacitor with a relatively large capacitance and generally consider the design in terms of making sure that changes in the power supply voltage due to changes in the current drawn will not become a problem.

- Please refer to the datasheet of the connectors to be used.

3.11 Power Supply Circuit for the SD card Interface

Points
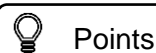
ALL

- When power is applied to an SD card, the inrush current may place a heavy load on the source power supply and make the system unstable.

- Depending on the card in use, the current may have large fluctuations. Determine the capacitance of a bypass capacitor for the card power supply based on actual evaluation.

- If the inrush current when the power is turned on is excessively large, you can reduce it by using a high-side switch with a soft start function.

- If the bypass capacitor placed adjacent to the SD card and SD card power connector needs to be discharged quickly when power to the SD card is switched off due to removal of the card, use a high-side switch with a discharge function. If quickly discharging the capacitor is not necessary, discharge it through a resistor with a value of about 1kΩ.

- Please refer to the datasheet of the peripheral devices to be used.
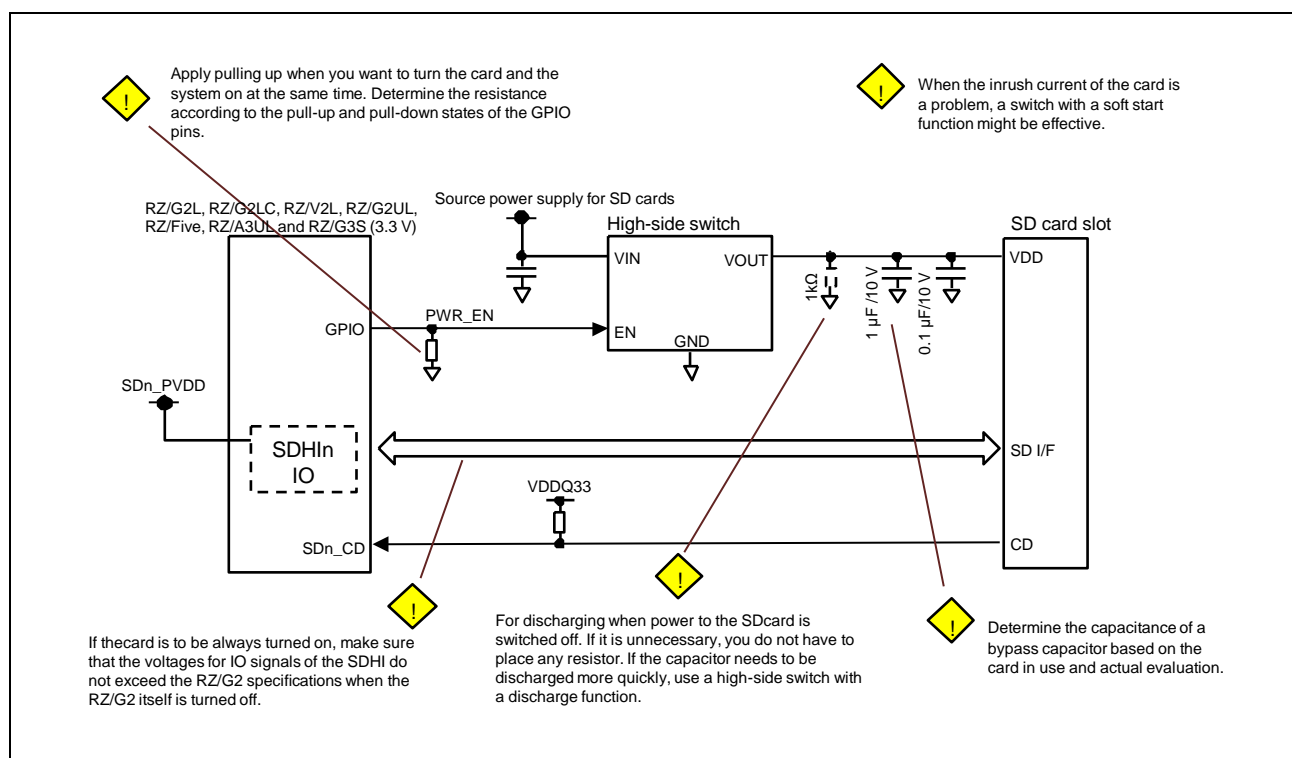
Figure 3.5   Example of a Power Supply Configuration for an SD Card Slot

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

3.12   Switching the IO Power Supply Voltage of the SDHI

Points

ALL

- RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL support 1.8 V and 3.3 V as the IO power supply voltage of the SDHI.

- When dynamically switching the IO power supply voltage of the SDHI, make sure that the power supply voltage does not exceed the specifications of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

- In particular, if you are using a high-side switch for switching between two power supply inputs, pay attention to the period during which the switches are turned off at the same time to prevent them from being turned on simultaneously at the time of switching.

- Please refer to the datasheet of the peripheral devices to be used.
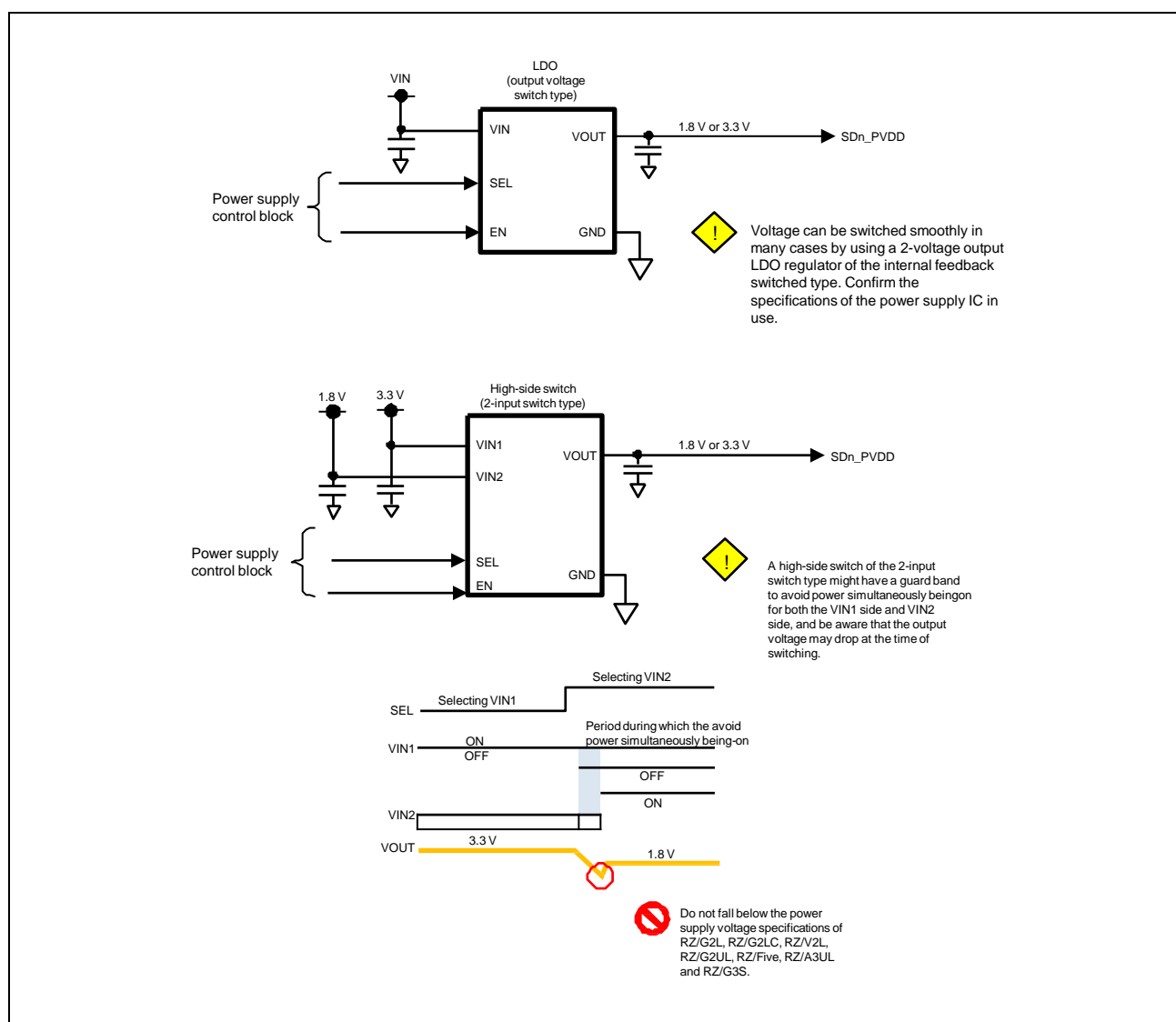
Figure 3.6   Switching the IO Power Supply Voltage of the SDHI

Documents for Reference

• Hardware user's manuals for individual target devices

• Circuit diagrams of individual evaluation board kits

4. Points Related to High-Speed Interfaces

4.1 DRAM Supported by Targeted Devices

💡 Points

ALL

- The following table shows DRAM that can be connected to RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

Table 4.1(a)   DRAM Supported by RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

LSI	Type	Configuration	Speed (Mbps)	Maximum Number of Ranks
RZ/G2L	DDR4	Up to 32 Gbits	1333 to 1600	2
RZ/G2LC	DDR3L	Up to 32 Gbits	800 to 1333	
RZ/V2L				
RZ/G2UL				
RZ/Five				
RZ/A3UL				

Table 4.1(b)   DRAM Supported by RZ/G3S

LSI	Type	Configuration	Speed (Mbps)	Maximum Number of Ranks
RZ/G3S	LPDDR4	Up to 8 Gbits	1600	2
	DDR4	Up to 32 Gbits	1600	

Documents for Reference

- Hardware user's manuals for individual target devices

- Data sheets for the given DRAM

- DDR board config structure generation tools for individual target devices

4.2 PCB Verification Guide

Points

ALL

- RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL have guidelines for performing SI verification, timing verification, and PI verification for DDR4, DDR3L circuit and pattern design.

- RZ/G3S has guidelines for performing SI verification, timing verification, and PI verification for LPDDR4, DDR4 circuit and pattern design.

- Be sure to follow the guidelines to verify the design.

Table 4.2　　List of PCB Verification Guidelines Related to DRAM Interface Design

Device	Guideline
RZ/G2L RZ/G2LC RZ/V2L RZ/G2UL RZ/Five RZ/A3UL	• PCB verification guide for DDR4/DDR3L • PCB design guideline for DDR4/DDR3L
RZ/G3S	• PCB verification guide for LPDDR4/DD4 • PCB design guideline for LPDDR4/DDR4

The respective PCB design guideline for DDR4/DDR3L and LPDDR4/DDR4 is a design example of an evaluation board manufactured by Renesas Electronics.

4.3   Model Number of Mounted DRAM

Points

ALL

- The DRAM to be mounted must match the model number of the DRAM that is used as a model in the simulation during preliminary design verification. If the model numbers do not match, the DRAM might not operate properly.

- If you install multiple types of DRAM on the same board in order to use a variety of capacity configurations and ensure stability in the acquisition of components, verify the feasibility of the design with all model numbers of DRAM that you are using in accord with the PCB Verification guide.

- Even with DRAM from the same vendor and having the same capacity, shrinkage of the silicon die or changes to the internal structure may make determining that this has led to no problems just by observing the waveforms on a current actual machine risky. Be sure to obtain the actual new model from the DRAM vendor and verify the suitability according to the PCB Verification guide.

Documents for Reference

- Hardware user's manuals for individual target devices

- PCB verification guide for DDR4/DDR3L

- PCB verification guide for LPDDR4/DDR4

- Data sheets for the given DRAM

4.4 Wiring Topologies for Connecting with DRAM
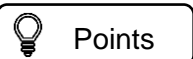
Points

ALL

- Command and address wiring connection between a target device and DRAM is only supported point-to-point on our reference board. Data wiring connection between a target device and DRAM is shown below. The topology of our reference board is C-011.

- If you support wiring connection other than that of our reference board, please refer to the PCB verification guide for DRAM and perform simulation by yourself. Even if you support wiring connection of our reference board, it is strongly recommended to perform simulation because a PCB structure, material, and target DRAM are not exactly the same.
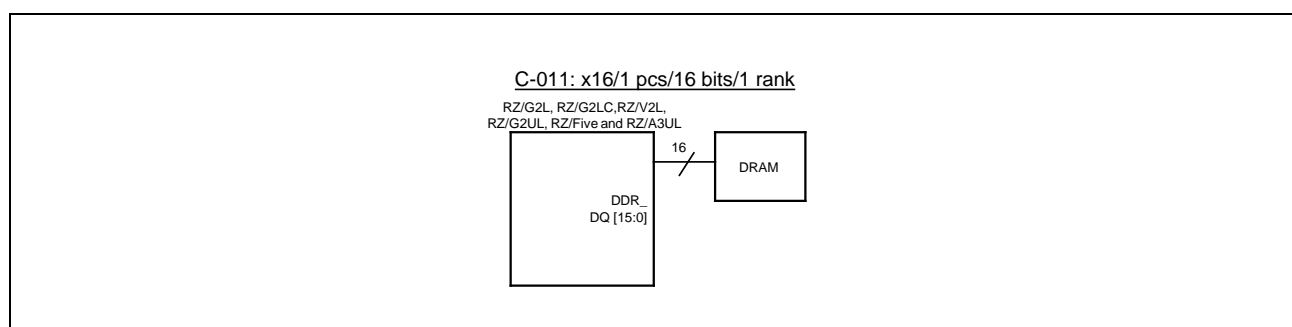
Figure 4.1(a)   Data Wiring Topology for DRAM
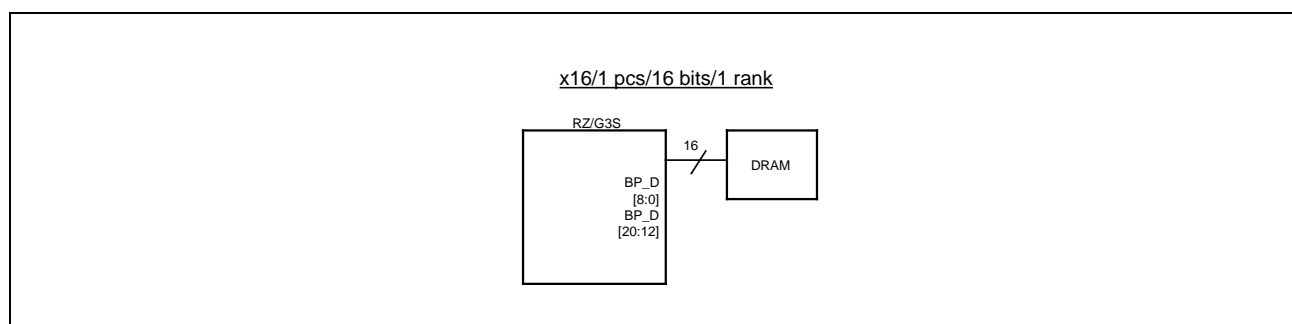
Figure 4.1(b)   Data Wiring Topology for DRAM

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB verification guide for DDR4/DDR3L

- PCB verification guide for LPDDR4/DDR4

- Data sheets for the given DRAM

- DDR board config structure generation tools for individual target devices

4.5 DRAM Interface Circuits

Points

ALL

- Each circuit constant for the DRAM interface circuit is stated in the PCB verification guide for DDR4/DDR3L and PCB verification guide for LPDDR4/DDR4.

- Refer to the latest guidelines according to the DRAM in use to make sure that the circuit constants are correct.

- This document also covers items that supplement hardware design for some DRAM interfaces. However, for the constants, check the contents of the latest "PCB verification guide for DDR4/DDR3L" and "PCB verification guide for LPDDR4/DDR4". As a general rule, we recommend process shown in the following example constants, but the process may vary depending on boards.

Constant examples

  - Differential signal (CLK, DQS) termination handling

  - Address/command signal termination handling (Rs resistor)

  - Address/command signal VTT termination handling

  - MEMn_RESET# signal termination handling (Rs resistor, pull-up resistor)

  - VREF generation circuit

  - ZQ pin handling

and so on

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB verification guide for DDR4/DDR3L

- PCB verification guide for LPDDR4/DDR4

- Data sheets for the given DRAM

4.6 DDR3L SDRAM VREF Circuit

Points
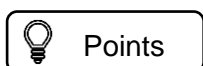
G2L G2LC V2L

G2UL Five A3UL

- For the VREF circuit on the DDR3L SDRAM side, contact the DRAM vendor and use an appropriate circuit configuration. The RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL evaluation board generates VREF for each VREF pin by the dedicated power supply, with 1.0 µF capacitors connected between the power supply and GND.

- The VREF circuit has two ways to generate VREF which are dividing resistors or dedicated power supply. Our reference board uses the latter, so it is recommended to generate VREF from the dedicated power supply.
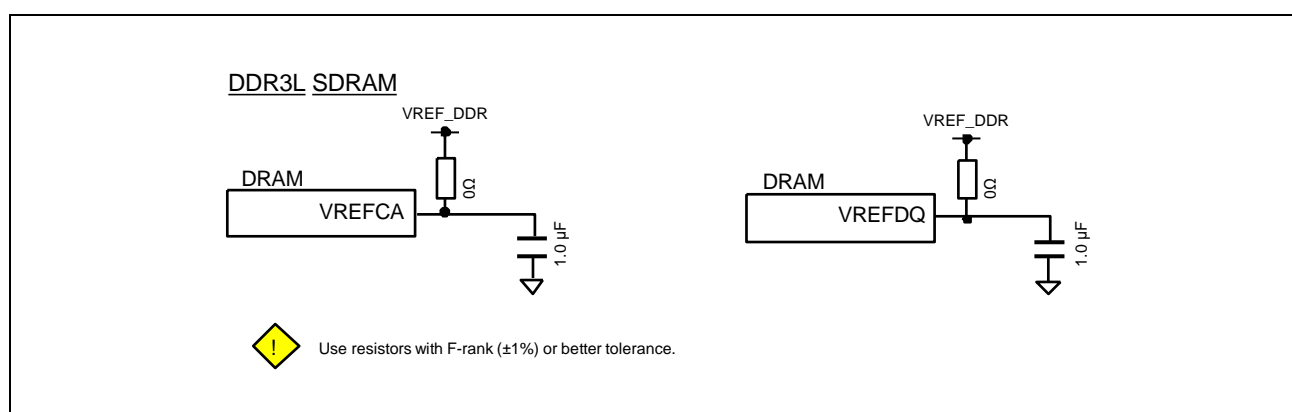
Figure 4.2   VREF Generation Circuit of the DDR3L interface

Documents for Reference

- Hardware user's manuals for individual target devices

- PCB verification guide for DDR4/DDR3L

- Data sheets for the given DRAM

4.7 DDR4 SDRAM VREF Circuit

Points

ALL

- For the VREF circuit on the DDR4 SDRAM side, contact the DRAM vendor and use an appropriate circuit configuration. The RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL evaluation board kit generates VREF for each VREF pin by the dedicated power supply, with 1.0 µF capacitors connected between the power supply and GND. The RZ/G3S evaluation board generates VREF for each VREF pin by resistive division, with 1.0 µF capacitors connected in parallel between the power supply and GND for stabilization.

VREF generation by resistive division

- To generate VREF input from the VDD/GND pin nearest to each VREF input pin, the VREF voltages can be generated by using the VDD/GND in the presence of noise. The VREF generated by a VREF power supply IC, etc. near the DRAM power supply may be inferior in precision to VREF independently generated by resistive division in terms of the reference VDD/GND being near a DRAM power supply IC and at a distance from each VREF input pin and of the effect of the application of noise to the VREF wiring.

- The VREF generation circuit must be placed as close as possible to the DRAM VREF pin.

- Input leakage current on the VREF pin leads to a voltage shift that depends on the dividing resistor values.

- Current flows through the resistor during backup.
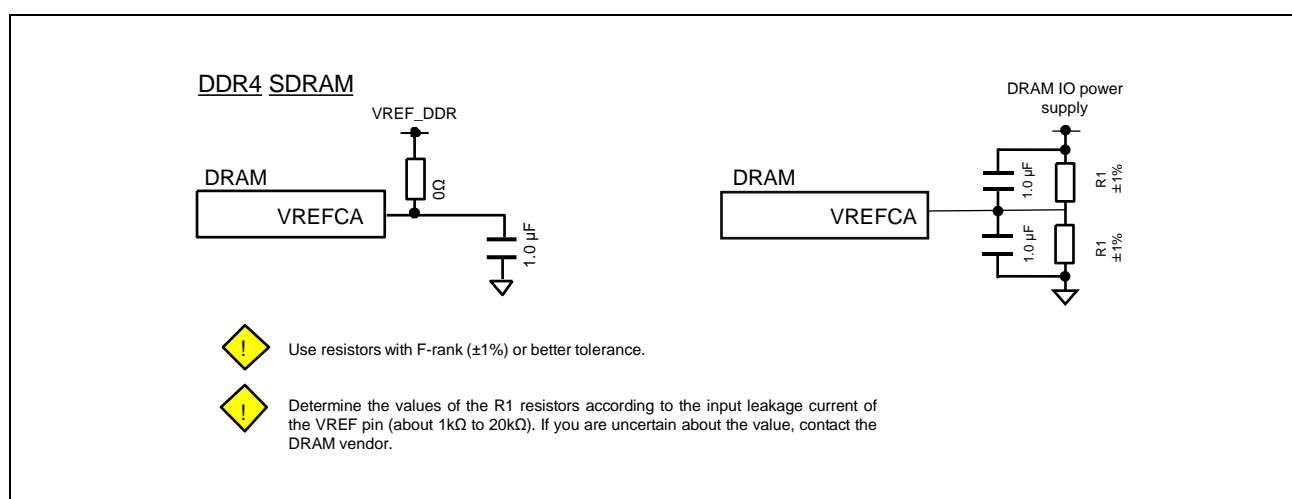
Figure 4.3   VREF Generation Circuit of the DDR4 Interface

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB verification guide for DDR4/DDR3L

- Data sheets for the given DRAM

4.8 ZQ Resistor of the DRAM Interface (Resistance Value/Resistance Tolerance)

Points

ALL

- Install resistors with the value specified in the PCB verification guide for DDR4/DDR3L as the ZQ resistors (on the SoC side and DRAM side) of the DRAM interface of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL.

- Install resistors with the value specified in the PCB verification guide for LPDDR4/DDR4 as the ZQ resistors (on the SoC side and DRAM side) of the DRAM interface of RZ/G3S.

- Select a resistor with a tolerance of ± 1% or better and place it as close as possible to the pin.
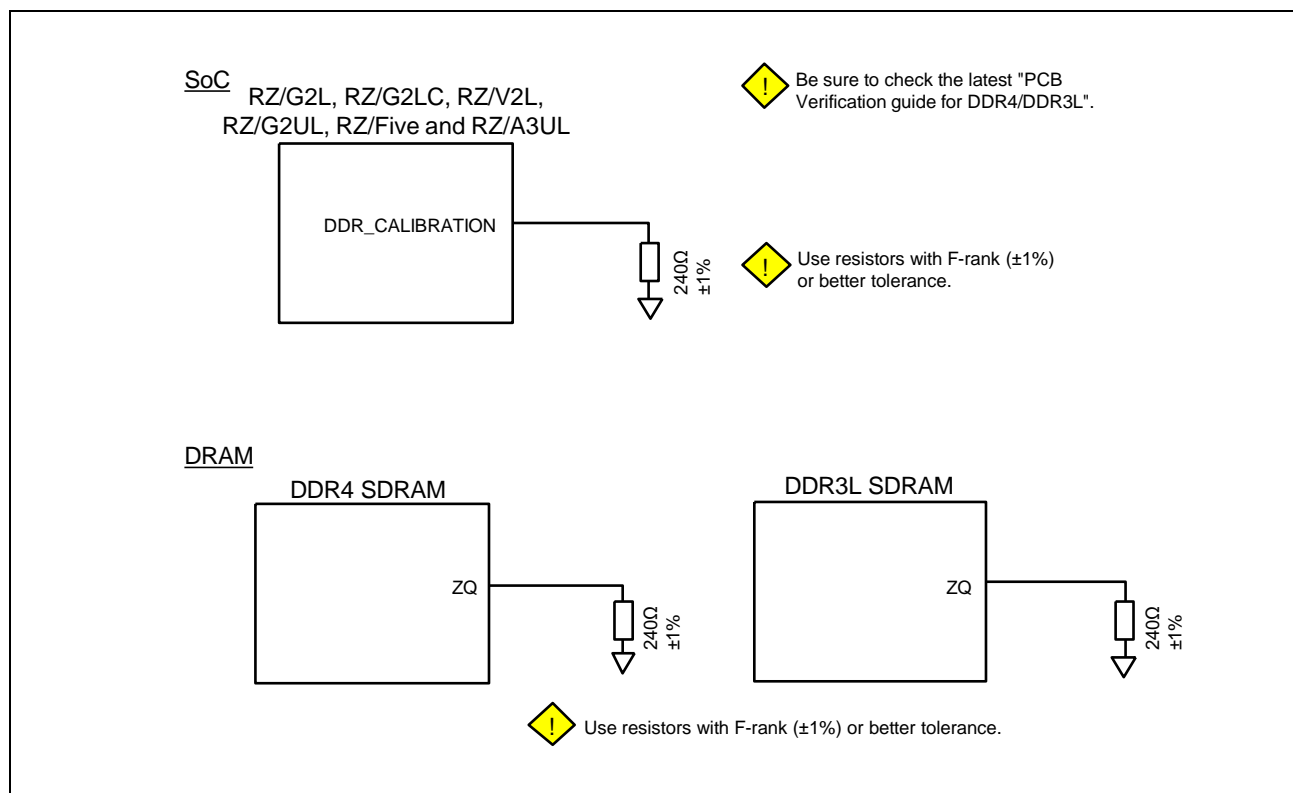
Figure 4.4(a)   ZQ Resistance Value of the DRAM Interface
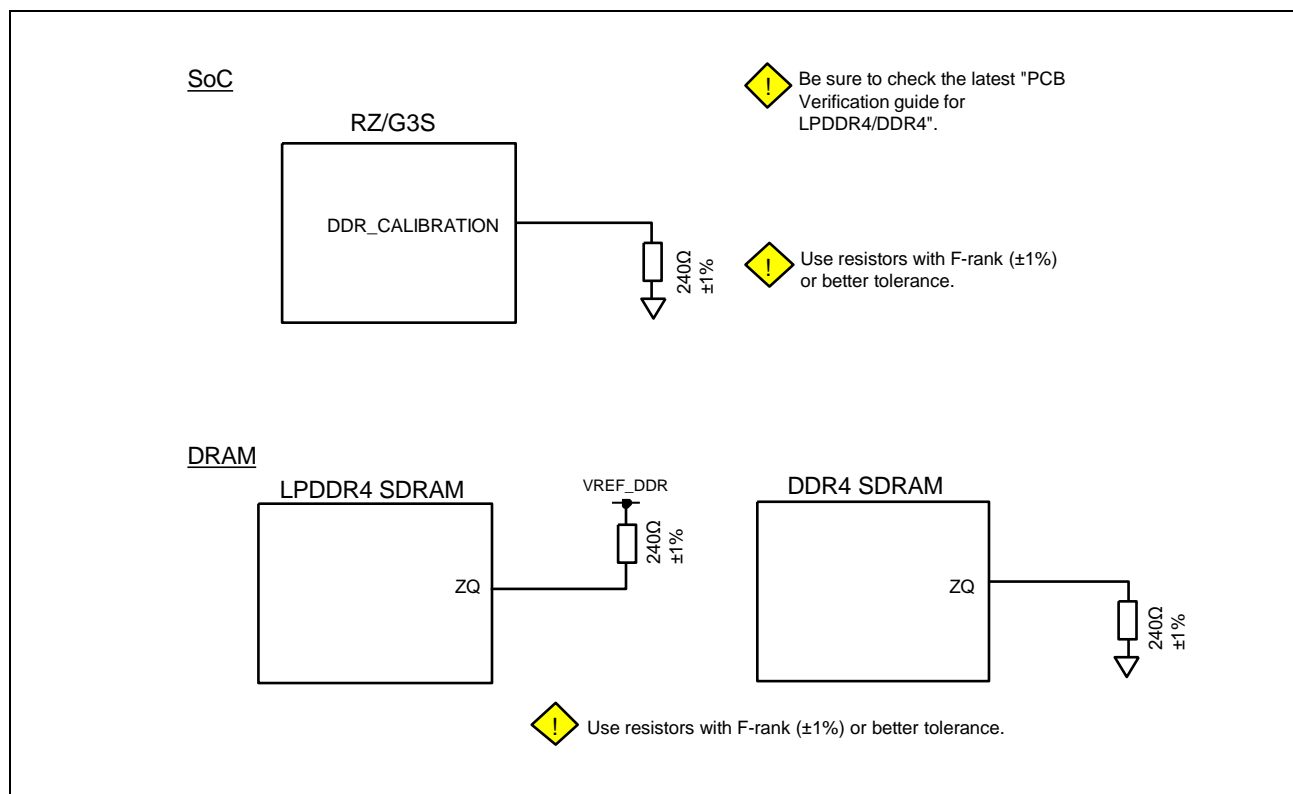
Figure 4.4(b)   ZQ Resistance Value of the DRAM Interface

Documents for Reference

• Hardware user's manuals for individual target devices

• Circuit diagrams of individual evaluation board kits

• PCB verification guide for DDR4/DDR3L

• PCB verification guide for LPDDR4/DDR4

• Data sheets for the given DRAM

4.9   Pin Swapping in Targeted Devices and DDR3L Interface

Points

| G2L | G2LC | V2L |
| G2UL | Five | A3UL |

- The RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL) and DDR3L interface has the signal pin swapping function.

- Signals of DDR_A[15:0], DDR_BA[2:0], DDR_ODT[1:0], DDR_CS[1:0]#, DDR_RAS#, DDR_CAS#, DDR_WE# can be swapped.

- During write leveling, the SoC side monitors changes in all DQ signals. Designers can switch DQ signals in the same byte lane at their own discretion.

- The DQS/DQS#[1:0] signals can be swapped per differential pair. The positive or negative logic of the DQS signals cannot be swapped.

- DM signals cannot be swapped with DQ signals.

- The initialization software must contain information about pin swapping (a generation tool is provided).
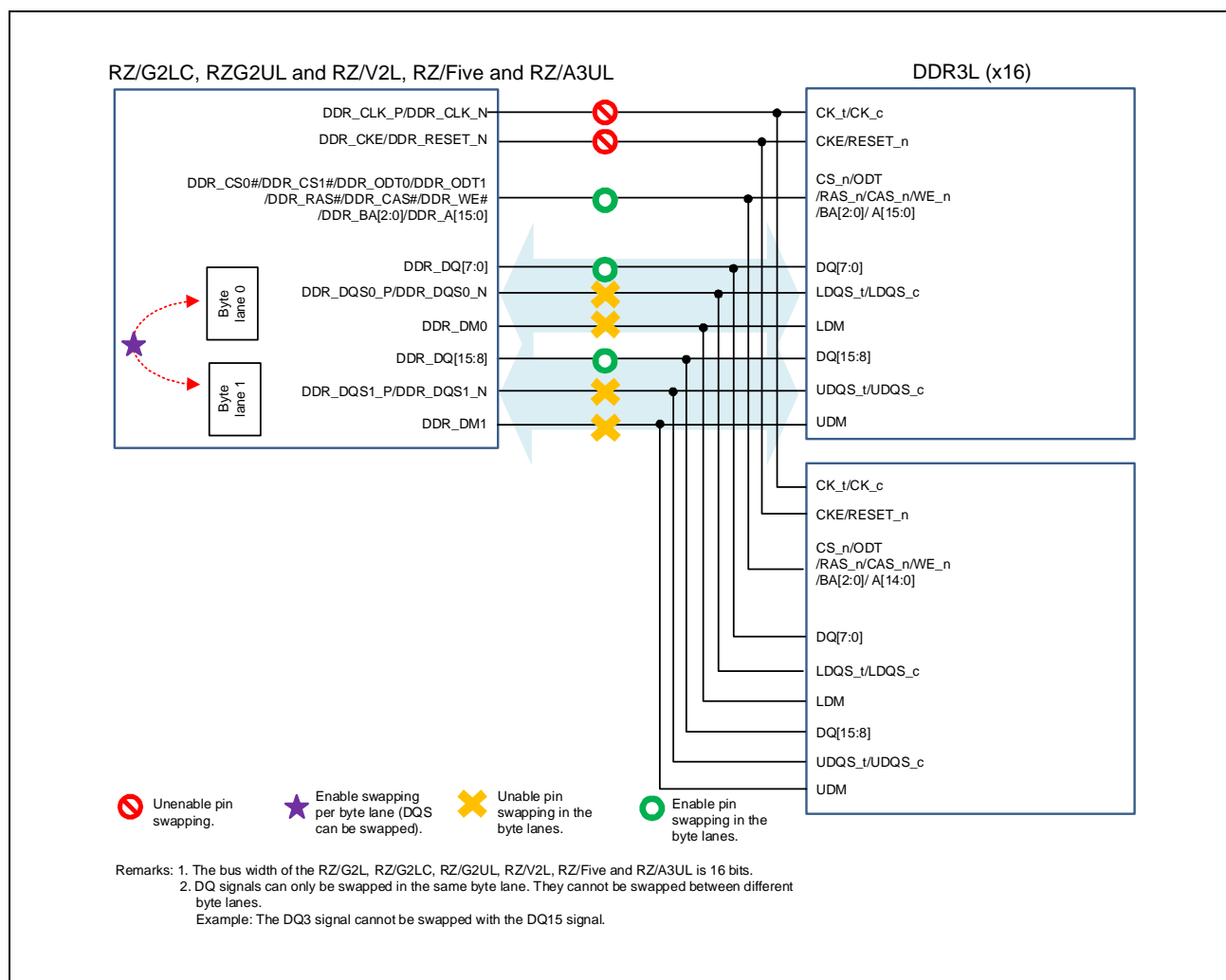
Figure 4.5   Pin Swapping in the RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL) and DDR3L Interface

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB verification guide for DDR4/DDR3L

- Data sheets for the given DRAM

- DDR board config structure generation tools for individual target devices
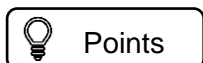
4.10 Pin Swapping in Targeted Devices and DDR4 Interface

Points

ALL

- The RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S) and DDR4 interface has the signal pin swapping function.

- Signals of DDR_A[15:0], DDR_BA[2:0], DDR_ODT[1:0], DDR_CS[1:0]#, DDR_RAS#, DDR_CAS#, DDR_WE# can be swapped.

- During write leveling, the SoC side monitors changes in all DQ signals. Designers can switch DQ signals in the same byte lane at their own discretion.

- DM signals cannot be swapped with DQ signals.

- The initialization software must contain information about pin swapping(a generation tool is provided).
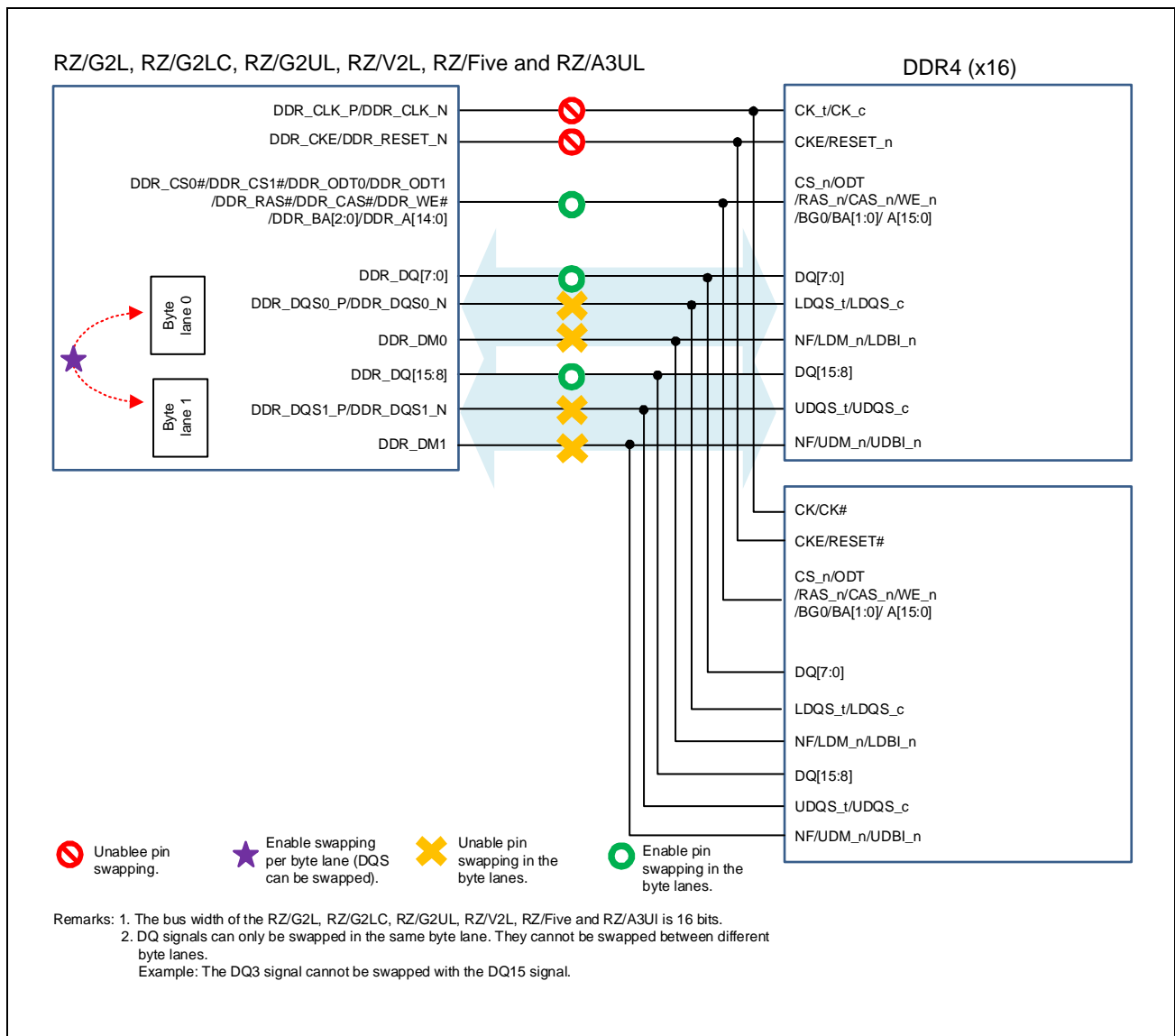
Figure 4.6(a)   Pin Swapping in the RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL) and DDR4 Interface
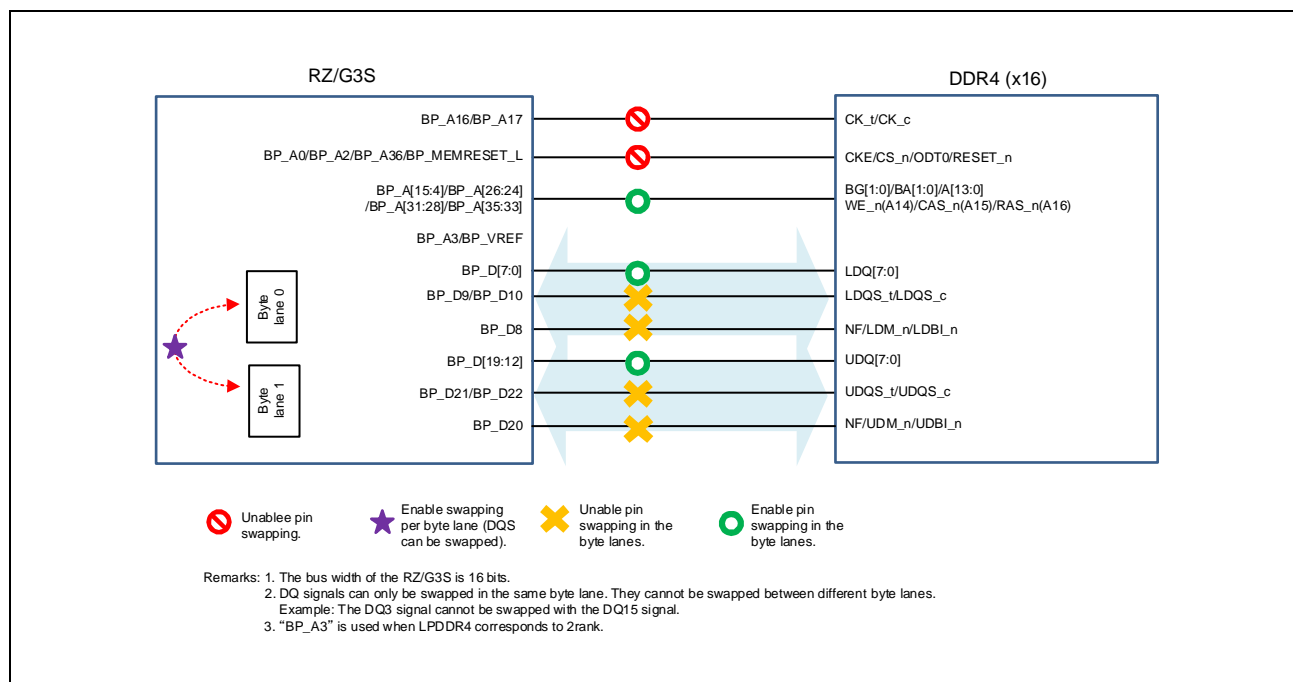
Figure 4.6(b)   Pin Swapping in the RZ/G3S and DDR4 Interface

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB verification guide for DDR4/DDR3L

- PCB verification guide for LPDDR4/DDR4

- Data sheets for the given DRAM

- DDR board config structure generation tools for individual target devices

4.11 Pin Swapping in Targeted Devices and LPDDR4 Interface

Points

ALL

- The RZ/G3S and LPDDR4 interfaces have the signal pin swapping function.

- Address signals CA[5:0] can be swapped within that range.

- Control signals cannot be swapped.

- The positive or negative logic of the DQS signals cannot be swapped.

- DMI signals cannot be swapped with DQ signals.

- The initialization software must contain information about pin swapping.
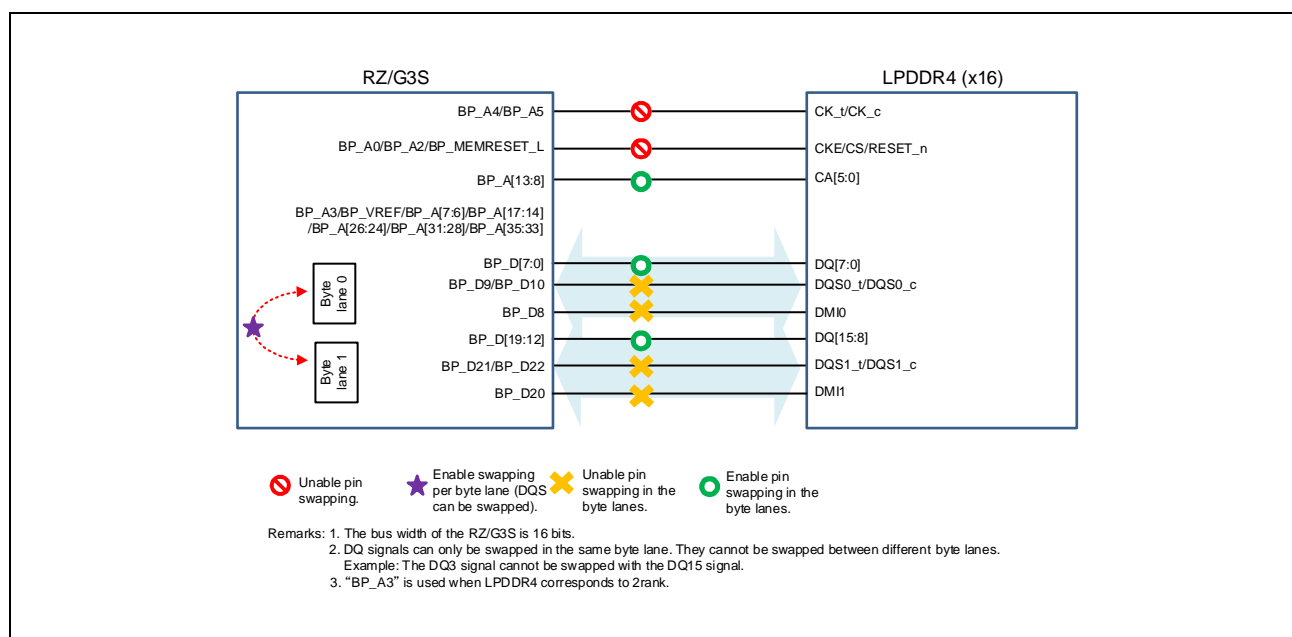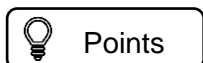
Figure 4.7   Pin Swapping in the RZ/G3S and LPDDR4 Interface

4.12 Power-on Sequence for DDR4/DDR3L SDRAM

Points

ALL

- DDR4 and DDR3L SDRAM have VDDn (n = 0 to 9, typ.1.2 V), VDDQn (n = 0 to 9, typ.1.2 V) as power supply pins.

- Please supply VDDn (n = 0 to 9) and VDDQn (n = 0 to 9) for DDR4 and DDR3L from the same power supply system.

- When DDR4 is connected to an RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S) and both the power supplies are shared with RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S), the power supply must be adjusted for the power supply interface of the DDR4 SDRAM.

- When DDR3L is connected to an RZ/G2L(RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL) and both the power supplies are shared with RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL), the power supply must be adjusted for the power supply interface of the DDR3L SDRAM.

- Please refer to JEDEC (JESD79-4A, JESD79-4C, JESSD79-3F, and JESD79-3-1A.01) for more information on power-on order restrictions.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- Data sheets for the given DRAM

4.13 Power-on Sequence for LPDDR4 SDRAM

☐ Points

G3S

- LPDDR4 SDRAM has VDD1 (typ.1.8 V), VDDQ, and VDD2 (typ.1.1 V) as power supply pins.

- The power-on sequence is defined for each power supply of LPDDR4.

- When LPDDR4 is connected to an RZ/G3S, and both the power supplies are shared with the RZ/G3S, the power supply must be adjusted for the power supply interface of the LPDDR4 SDRAM.

- Please refer to JEDEC (JESD209-4) for more information on power-on order restrictions.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- Data sheets for the given DRAM

4.14 PCB Design Guide for High-Speed Serial Interfaces

Points

ALL

- For RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, we provide the design guidelines for high-speed serial interfaces.

- Be sure to follow the guidelines to verify the design.

Table 4.3 Guidelines Related to the PCB Design of High-Speed Serial Interfaces

Interface	Guideline/External Guideline Documentation Referred to by the Renesas Guidelines
USB 2.0	• PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2 Section2 • High Speed USB Platform Design Guidelines Rev1.0 Download from https://www.usb.org/
CSI	• PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2 Section1
DSI	• PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2 Section1
PCIe	• PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2 Section3 • Board Design Guidelines for PCI Express™ Architecture Download from https://members.pcisig.com/

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

4.15 Recommended Circuits and Circuit Constants for the High-Speed Interface

Points

ALL
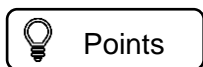
- The high-speed interfaces of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S have the dedicated power supply pins.

- The high-speed interface design guidelines provide the recommended capacitance values of the bypass capacitors for the dedicated power supply pins, so follow the guidelines for designing.

- As with the decoupling of power supplies in general, bypass capacitors should be placed with a smaller capacitance nearer the given power supply pin of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

- The PCIE of RZ/G3S requires external clock input.

- The high-speed interface design guidelines provide recommended requirements for external clock input, so follow the guidelines for designing. A spread-spectrum clock (SSC) cannot be connected as the external clock.

- Make sure that a clock is not input before the power of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S is turned on.

- For use in reference regarding current, not only the resistance of the resistor element, but also the recommended accuracy and temperature coefficient might be indicated, so follow the guidelines for designing.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

4.16 Signal Coupling for PCIe

Points

G3S

- The PCI Express interface requires coupling at the transmitting end.

RZ/G3S

0.1 µF/10 V

PCIE TX_P

PCIE TX_M

⚠ Coupling capacitor
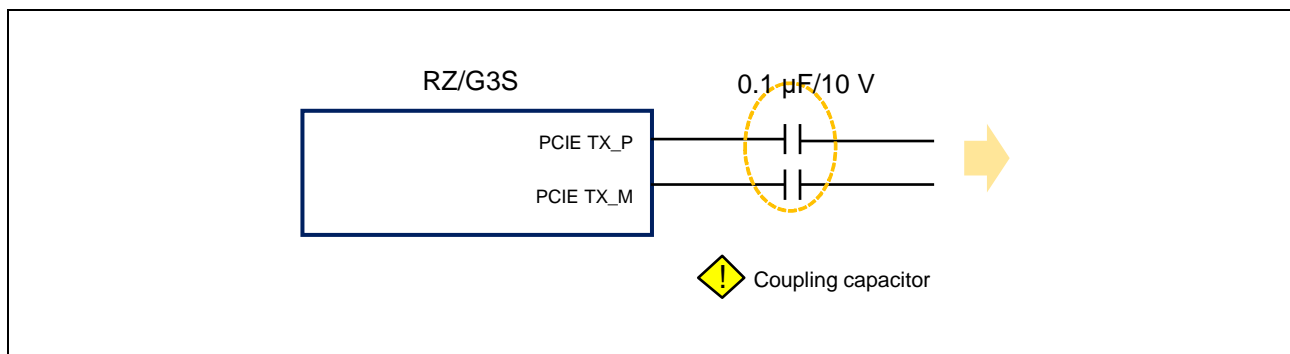
Figure 4.8   Coupling at the Transmitting End for the PCIE

Documents for Reference

- RZ/G3S Group User's Manual: Hardware

- Circuit diagram of the RZ/G3S evaluation board kit

4.17   Instructions for PCB Pattern Design

Points

ALL

- The high-speed interface design guidelines for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S provide recommendations and restrictions for wiring patterns.

- We recommend that you include indications in the circuit diagram to give pattern designers a secure understanding of how recommendations and restrictions in the guidelines have been applied.

- For general reference information on PCB pattern design, see **section 6, Points to Note in Designing PCB Wiring Patterns** in this guideline.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

4.18 Observing High-Speed Serial Interface Signals

Points

ALL

- Note that installation of an observation pad on high-speed serial signal wiring may cause degradation in the signal quality.
  - Unnecessary stubs are constructed to set observation points.
  - Wiring runs that can only be arranged in the inner layer is brought out to the surface layer to set observation points on the surface layer.
  - Setting observation points for differential signals may lead to the symmetry of the differential wiring collapsing.

- The possibility of signal degradation increases with the signal speed, due to the addition of observation circuits. In order to improve the design quality, avoiding the unjustifiable setting of observation points is also necessary.

- High-speed signals might be distorted due to ISI or reflection deriving from observation points. In such cases, ideal waveforms such as are shown in the documents for reference might not be observed.

- In cases such as the above, you must proceed with advanced simulation of the intended observation points and the input circuits of the observation equipment by using the S parameter of the wiring and confirm the suitability by using the observation point movement function of the observation equipment.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

4.19 Measures against Disturbance Noises and Static Electricity for High-Speed Serial Interfaces

Points

ALL

- For interfaces such as USB2.0, that can be hot-plugged or connected to external devices, insert components for countermeasures against static electricity and external common mode noise.

- Dedicated components that can handle the signal level and signal frequency of each of the interfaces and components with noise filters having an ESD protection function are also available. Select components by reference to the circuit diagram of the evaluation board kits for RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.
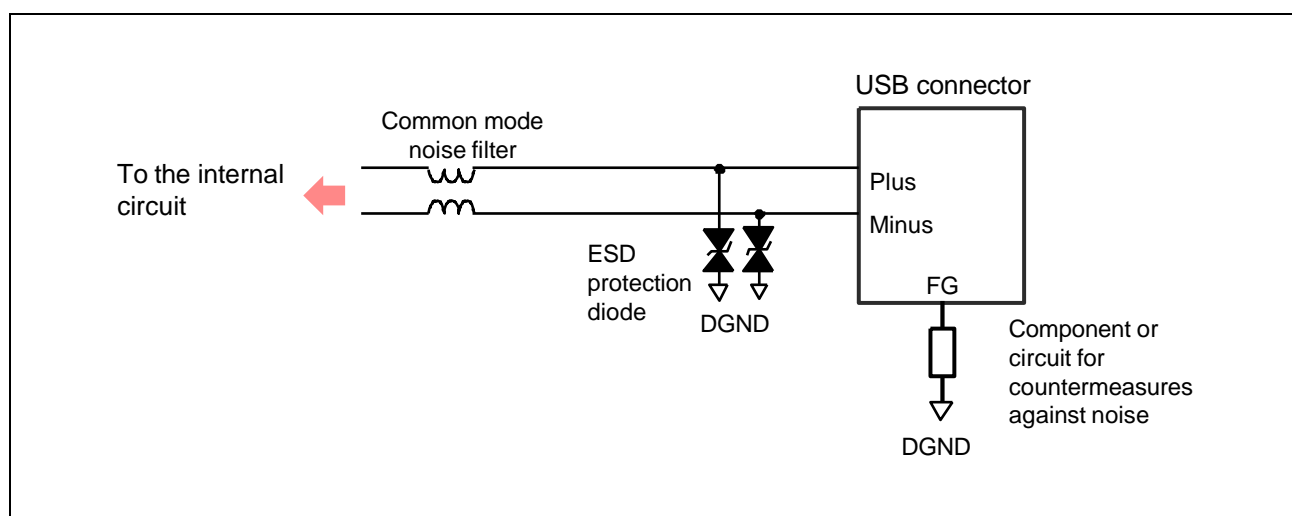
Figure 4.9   Example of a Circuit for Measures against Disturbance Noises and Static Electricity for High-Speed Serial Signals

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2

4.20 Voltage for the overcurrent or VBUS Input of the USB

Points

ALL

- When USBn_OVRCUR# (n = 0, 1) input is to be used, the input signal level should be set to 3.3 V. On the other hands, when USB host is to be used but USBn_OVRCUR# (n = 0, 1) input is not to be used, these pins should be pulled up on the board because the USBn_OVRCUR# (n = 0, 1) pin interrupted cannot be disabled.

- While the power supply to the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL is turned off, USBn_OVRCUR# (n = 0, 1) input must not be high-level.

- When the VBUS input is used, connect it to an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S through external dividing resistors with a value of 1kΩ ± 1% and 1.8kΩ ±1%.

- It is shown a design example of an evaluation board manufactured by Renesas Electronics. Please refer to the datasheet of the USB VBUS control IC to be used.
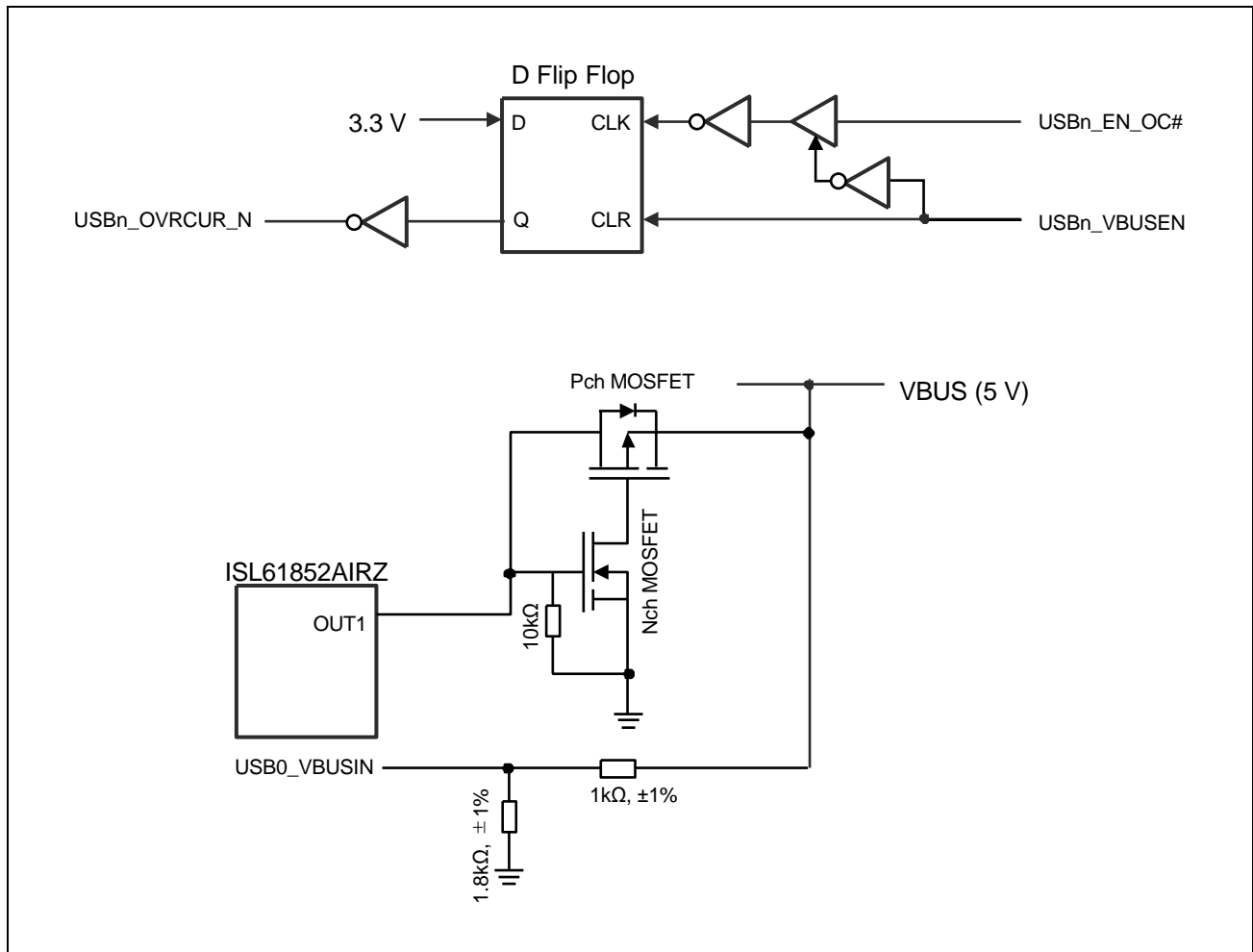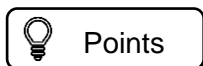
Figure 4.10   Overcurrent or VBUS Input of the USB

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

4.21 USB VBUSEN

Points

ALL

- For RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, the USBn_VBUSEN (n = 0, 1) signal of the USB interface is assumed as active high.

- During a hardware reset (PRST# = L) of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, the high impedance is output on the USBn_VBUSEN (n = 0, 1) pin.

- Select an IC that has an active-high EN input as a USB VBUS control IC.

- It is shown a design example of an evaluation board manufactured by Renesas Electronics. Please refer to the datasheet of the USB VBUS control IC to be used.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

5. Others

5.1 Handling Unused Pins

💡 Points

G2L   G2LC   V2L

- If there are unused function pins of RZ/G2L, RZ/G2LC, and RZ/V2L, handle these pins in accord with the statements on the handling of unused pins in the hardware manual.

- Please connect to GND via 1 μF capacitor about the terminal processing of ABG_NCP_OUT.

- Even if you do not use all the functions, be sure to turn on the relevant power supplies.

RZ/G2L, RZ/G2LC and RZ/V2L

ABG_NCP_OUT

1 μF
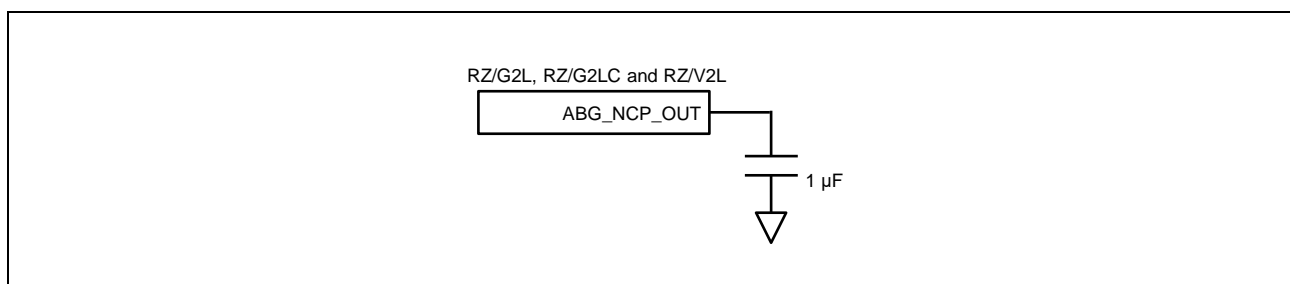
Figure 5.1   Terminal Processing of ABG_NCP_OUT

Documents for Reference

- RZ/G2L Group, RZ/G2LC Group User's Manual: Hardware

- RZ/V2L Group User's Manual: Hardware

- Lists of pin functions for RZ/G2L, RZ/G2LC, and RZ/V2L

5.2 Countermeasures against Signal Overshoots and Undershoots

Points
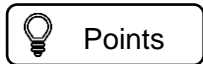
ALL

- Larger than expected signal overshoots and undershoots must be prevented from causing the device ratings to be exceeded.

- A common method of doing so is to insert damping resistors near the signal outputting ends before determining the necessity and, if one is required, value of the resistor through evaluation. However, in such cases, you must pay attention to the following points.

  - The placement of damping resistors increases the number of parts near the RZ/G2L (RZG2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S) and peripheral devices, significantly affecting the placement of other important parts.

  - The connection of damping resistors necessitates the movement of signals to the surface layer. As a result, via holes and through holes significantly affect the properties of the wiring.

- When inserting a damping resistor to prevent overshooting and undershooting, carefully determine their necessity rather than inserting them unnecessarily.

  - Obtain IBIS models of the buffers, simulate typical transmission paths such as the longest one and shortest one, and estimate the possible amounts of overshoot and undershoot in advance.

  - Reduce the amounts of overshoot and undershoot by bringing the wiring layer (surface layer/inner layer) and wiring width close to the output impedance of the buffer.

  - Check if the driving ability of the output buffers is adjustable or can be set.

  - Apply impedance matching with parallel termination at the receiving ends instead of inserting damping resistors.

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

5.3   Level Shifting of Signal Voltages

Points

ALL

- Some types of IO of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S such as SD/MMC and QSPI allow two power supply voltages. The IO type of Gigabit Ethernet allows three power supply voltages.

- When the signal voltage differs between RZ/G2L (RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S) and a peripheral device, so that a general-purpose logic IC is to be used for level shifting, pay attention to the following points.

    - Is the IC to be used voltage tolerant?

    - Does the high-level voltage of signals and the VIH of the IC raise a problem?

    - Does the IC operate at a speed sufficient for the operating frequency of the signals?

- Pay attention to the power supply and output enable of the IC used for level shifting so that the signals do not go to the high level while power for the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S is cut off.

- In order to prevent misuse and misconnection of signals before and after level shifting, we recommend using net names that include signal voltages on the circuit diagram.

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

5.4 Checking the AC and DC Characteristics of Signal Input and Output between Targeted Devices and Connected Devices

Points

ALL

- When connecting RZ/G2L (RZ/G2LC RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S) and a peripheral device, there will generally be no problem if the CMOS inputs and outputs have the same power supply voltage, even if the connections are direct at the DC level. If the AC timing also raises no problems, the connection will be problem-free. However, the DC specifications might differ slightly from device to device, so we recommended checking the AC and DC margins of both sides.

- The main external factors that may reduce the AC and DC level margins are as follows.

    - Minor differences in power supply voltage, such as where different power supply sources are used, or an FET switch is used

    - Superimposition of ground bounce and signal reflections due to simultaneous switching output (SSO) on rising and falling of the signals

    - Signal rounding due to excessive wiring length or load capacitance

    - Under-driving of the output buffers due to excessive resistive loads

    - Degradation in the signal quality due to crosstalk or ISI

- If there is a possibility that the AC and DC margins for the connected device is insufficient, consider measures such as inserting a pull-up resistor or buffer in the circuit design stage.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

5.5 Conflict between Pulling Up and Down for Targeted Devices and Board or Peripheral Devices

Points

ALL

- Many devices, including RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, might have pulling up and down. Although internal pulling up and down help to reduce the number of parts, conflicts may occur when devices are connected to each other, leading to unexpected problems.

- The following is a common case. Device A has a pull-up resistor and device B has a pull-down resistor. Connecting A and B leads to the signal potential becoming intermediate.

Cases

  – An intermediate potential is produced because the internal pulling up and down compete against each other.

  – The internal pulling up or down competes with the pulling down or up in an external circuit.

  – When a device is turned off, pulling up in another device may apply a voltage exceeding the standard, and the power that should have been turned off does not become 0 V because of external pulling up or a device-protection diode.

- In particular, pay attention to pulling up and down for use in setting the mode of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

- Check the data sheets and technical documentation of each device for details to avoid conflicts.

  – The presence of internal pulling up or down, values of the resistors used, and method of control (such as in terms of always being on, and pin and register settings)

  – Interface equivalent circuit including pulling up or down

  – Behavior in special cases such as during and immediately after a reset, etc.

- The pin function table of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S describes the information and control of the internal pulling up and down, and the pull-up or -down resistor values are described in the electrical characteristics.
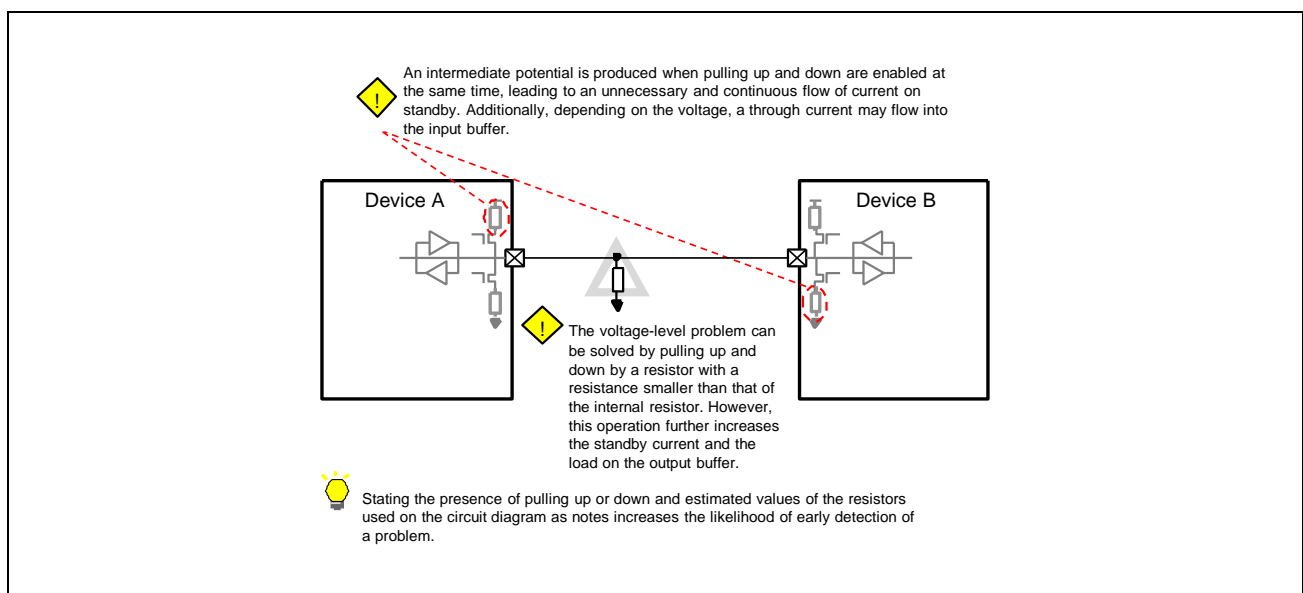
Figure 5.2   Conflict between Internal Pulling Up and Down

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

5.6 Instructions for the Wiring of Relatively High-Speed (about 10 to 100 MHz) Interfaces

💡 Points

ALL

- Renesas Electronics provides design guidelines for high-speed serial interfaces such as MIPI-CSI, MIPI DSI, and USB2.0, but does not specially provide those for relatively high-speed synchronous parallel interfaces (such as Parallel Input/Output, Ether MII, SD/MMC, and QSPI).

- Observe the following general precautions when designing relatively high-speed synchronous interfaces for which design guidelines are not provided.

  – Include instructions about wiring, such as equal-length wiring, in the circuit diagram to prevent problems in pattern design.

  – For interfaces that operate at around 100 MHz, to prevent differential delays between layers, specify all wiring in a single layer and provide instructions for equal-delay pattern design from an advance transmission simulation.

  – Provide instructions for lines and spaces so that the spacing between wires is sufficient (preferably three times the distance to the reference layer), in order to prevent crosstalk.

- When using a flexible cable for connection to a peripheral device, be sure to arrange a sufficient number of grounds to secure the return path and prevent crosstalk and unnecessary radiation.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

5.7 Notes on Signal Connection
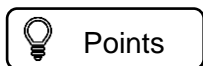
Points

ALL

- Make sure that the CMOS input ports including RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S are not left open-circuit (Hi-Z).
  - If they are left open-circuit, a through current may continue to flow, leading to deterioration and destruction of elements.
  - Also pay attention to hidden open-circuit states of input ports, such as when a part or IC that is a destination for connection is not mounted.

- Confirm that output signals do not conflict between devices including RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.
  - If such conflict continues for a long time, elements may deteriorate or be destroyed.
  - Also, pay attention to hidden conflicts arising from special situations such as during a reset.

- Be careful when connecting ICs that operate under special conditions, such as ICs that operate with the power of an external USB bus even if the main power of the board is not on.
  - Do not drive high or pull up pins that do not have tolerance, including RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL and RZ/G3S.
  - In the Renesas evaluation board kits, the USB-UART bridge IC is an LSI chip that partially operates with USB bus power.

- Be careful when using WDTOVR_PERROUT# terminal of RZ/G3S. When PRST# signal level is low, the pin condition of WDTOVR_PERROUT# terminal is Hi-Z, not the high-level. So, an external pull-up resister is required.

Remarks:

Technically, RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S pins that are capable of pulling up and down control remain open-circuit from when the power is turned on until reset is released or until pulling up or down is enabled by the PFC settings, if there is no external component or IC that determines the signal level.

If the reset period is short and the PFC settings proceed quickly after startup, deterioration and destruction due to heat generated by the IO through current will not occur. If you do not need the LSI to perform any processing, we consider turning off the power to be normal. However, if there is a special circumstance, such as when it is necessary to leave the power on or have a longer reset period, use an external device for additional pin handling, although this will increase the number of components.

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

5.8 Interrupt Signals

Points

ALL

RZ/G2L, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S have the NMI and IRQ0 to IRQ7 signals as general interrupt inputs. RZ/G2LC has the NMI and IRQ0 to IRQ7 signals excluding IRQ2 and IRQ3 as general interrupt inputs.

Note that the pin assignment of these signals is slightly different among RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S. Be careful when adapting an interrupt circuit for another product.

Table 5.1(a)   Specifications of the NMI Signal of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

NMI	G2L / G2LC / V2L / G2UL / Five / A3UL
Dedicated/shared	Dedicated
IO voltage	3.3 V (PVDD)
Input buffer	Schmit
Internal pull-up	None
Internal pull-down	None

Table 5.1(b)   Specifications of the NMI Signal of RZ/G3S

NMI	G3S
Dedicated/shared	Dedicated
IO voltage	3.3 V (PVDD33)
Input buffer	Schmit
Internal pull-up	None
Internal pull-down	None

Table 5.2(a)   Specifications of the IRQ0 and IRQ1 Signals of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

IRQ0 IRQ1	G2L / G2LC / V2L / G2UL / Five / A3UL
Dedicated/shared	Partially shared
IO voltage	3.3 V (VDDQ33)
Input buffer	Normal
Internal pull-up	Available[1]
Internal pull-down	Available[1]

Note 1.   The PFC enables control to switch pulling up and down on or off.

Table 5.2(b)   Specifications of the IRQ0 Signal of RZ/G3S

IRQ0 IRQ1	G3S
Dedicated/shared	Partially shared
IO voltage	3.3 V (PDD33) 3.3 V (PDD33 or PVDD182533_1
Input buffer	Normal
Internal pull-up	Available*1
Internal pull-down	Available*1

Note 1.   The PFC enables control to switch pulling up and down on or off.

Table 5.3(a)   Specifications of the IRQ2 and IRQ3 Signals of RZ/G2L, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

IRQ2 IRQ3	G2L / V2L / G2UL / Five / A3UL
Dedicated/shared	Partially shared
IO voltage	3.3 V (VDDQ33)
Input buffer	Normal
Internal pull-up	Available*1
Internal pull-down	Available*1

Note 1.   The PFC enables control to switch pulling up and down on or off.

Table 5.3(b)   Specifications of the IRQ2 Signal of RZ/G3S

IRQ2 IRQ3	G3S
Dedicated/shared	Partially shared
IO voltage	3.3 V (PVDD33 or PVDD182533_1)
Input buffer	Normal
Internal pull-up	Available*1
Internal pull-down	Available*1

Note 1.   The PFC enables control to switch pulling up and down on or off.

Table 5.4(a)   Specifications of the IRQ4 and IRQ7 Signals of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL

IRQ4 IRQ5 IRQ6 IRQ7	G2L / G2LC / V2L / G2UL / Five / A3UL
Dedicated/shared	Partially shared
IO voltage	3.3 V (VDDQ33)
Input buffer	Normal
Internal pull-up	Available*1
Internal pull-down	Available*1

Note 1.   The PFC enables control to switch pulling up and down on or off.

Table 5.4(b)   Specifications of the IRQ4 Signal of RZ/G3S

IRQ4 IRQ5	G3S
Dedicated/shared	Partially shared
IO voltage	3.3 V (PVDD33 or PVDD182533_1)
Input buffer	Normal or Schmit (PVDD33)
Internal pull-up	Available[1]
Internal pull-down	Available[1]

Note 1.   The PFC enables control to switch pulling up and down on or off.

Table 5.4(c)   Specifications of the IRQ6 and IRQ7 Signals of RZ/G3S

IRQ6 IRQ7	G3S
Dedicated/shared	Partially shared
IO voltage	3.3 V (VDDQ33)
Input buffer	Normal
Internal pull-up	Available[1]
Internal pull-down	Available[1]

Note 1.   The PFC enables control to switch pulling up and down on or off.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual valuation board kits

- Lists of pin functions for individual target devices

5.9 Connecting an eMMC

Points

ALL

- The eMMC interfaces of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S are 1 channel and up to HS200 in terms of the maximum number of channels and supported speed grade.

- Since the eMMC interface is a relatively high-speed parallel interface, we recommend that you perform SI simulation with the use of an IBIS model.

- When booting from an eMMC is used in RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, if you are concerned about overshooting or undershooting during boot, add a series damping resistor to the interface.

- When using an eMMC as a boot device, the output impedance is set to 50Ω. So please design the C load to meet the electrical specification written in the User's Manual and the transmission line of the board to be 50Ω.

Table 5.5   eMMC Interface of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S

Device	Speed Grade	Maximum Number of Channels
RZ/G2L	Up to HS200 (eMMC 4.51 base)	1
RZ/G2LC	Up to HS200 (eMMC 4.51 base)	1
RZ/V2L	Up to HS200 (eMMC 4.51 base)	1
RZ/G2UL	Up to HS200 (eMMC 4.51 base)	1
RZ/Five	Up to HS200 (eMMC 4.51 base)	1
RZ/A3UL	Up to HS200 (eMMC 4.51 base)	1
RZ/G3S	Up to HS200 (eMMC 4.51 base)	1

Document for Reference

- Hardware user's manuals for individual target devices

5.10 eMMC Interface Circuit

Points
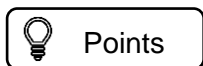
ALL

- Determine the pull-up resistor values for the CMD and DAT signals according to the operating voltage in reference to the recommended values provided in the eMMC standard documentation.

- Insert a series termination resistor (series resistor) for the CLK signal as necessary.

- We recommend that you confirm that the signal quality is free of problems by simulating transmission.

- When booting from an eMMC is used, eMMC must be reset before the start of booting up the CPU. [1]

Note 1. Some eMMC devices may not activate reset pin function just after the factory shipping.

- Please refer to JEDEC(JESD84-B51) for more information.

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

- eMMC Standard Documentation (JESD84-B51)

- eMMC data sheets

5.11 SPI Multi I/O Interface

Points

G2L   G2LC   V2L

G2UL   Five   A3UL

- The SPI multi I/O interface enables the direct connection of, Quad/Octal-SPI flash memory and HyperFlash^{TM} to RZ/G2L, RZ/G2LC, and RZ/V2L.

- This interface consists of two internal QSPI interfaces that together provide 8-bit width access.

- The two QSPI interfaces do not support independent operation.

  - When QSPI0 is used as the Single-SPI or Quad-SPI interface, QSPI1 cannot be used.

  - Although connecting two units of Quad-SPI flash memory to QSPI0 and QSPI1 in parallel and using them as 8-bit width is possible, QSPI0 and QSPI1 cannot be used as two independent interfaces for Quad-SPI flash memory.

  - The QSPI boot mode only supports QSPI0 interface. In order to use octal SPI interface by combination of QSPI0 and 1, software should change configuration after boot.

- The SPI multi I/O interface is a relatively high-speed interface. Although we do not provide any guide in particular, we recommend that you confirm that the signal timing and quality are free of problems by providing instructions about equal-delay (equal-length) wiring or simulating transmission in advance.
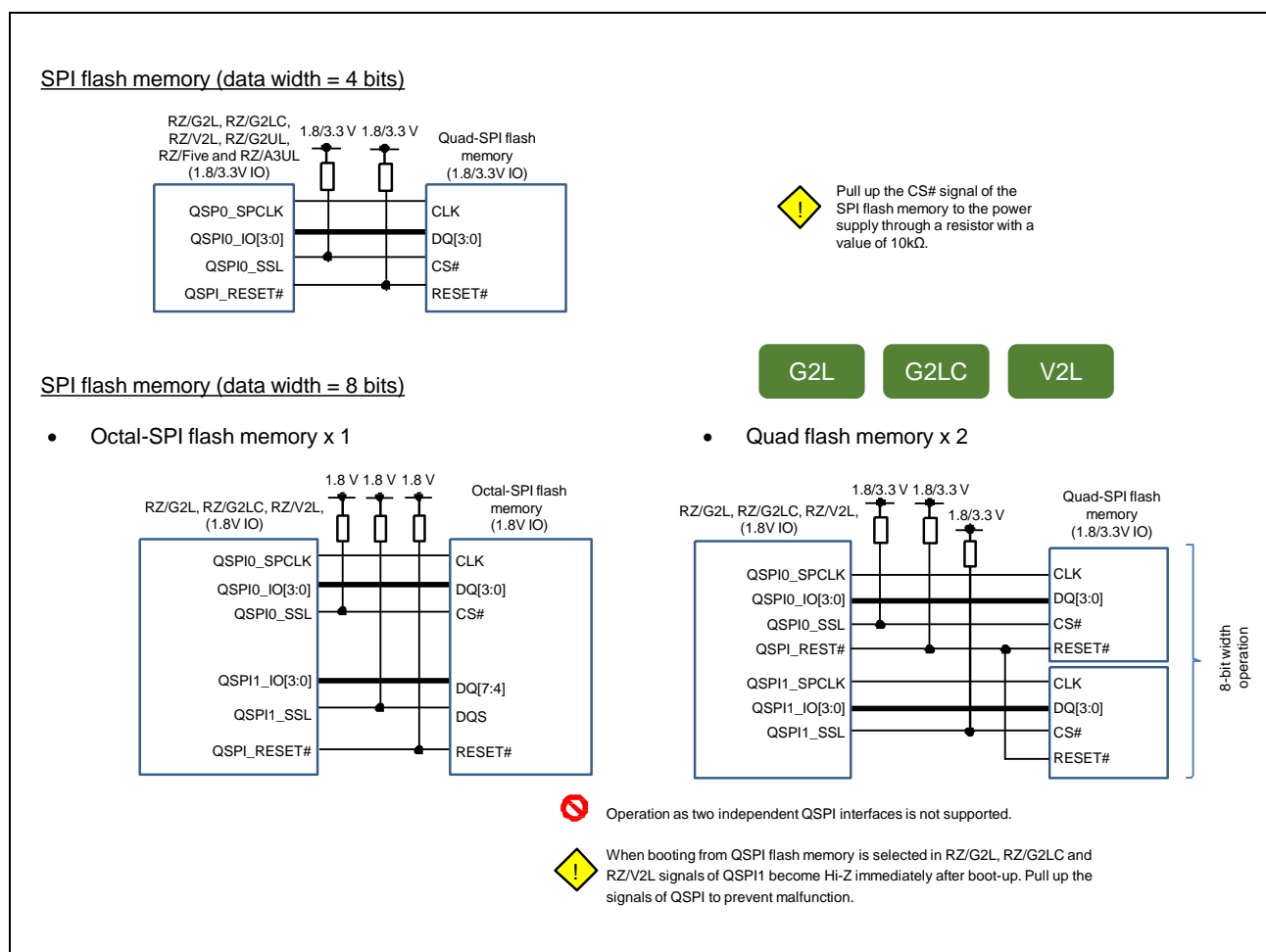
Figure 5.3   Connection of SPI Flash Memory
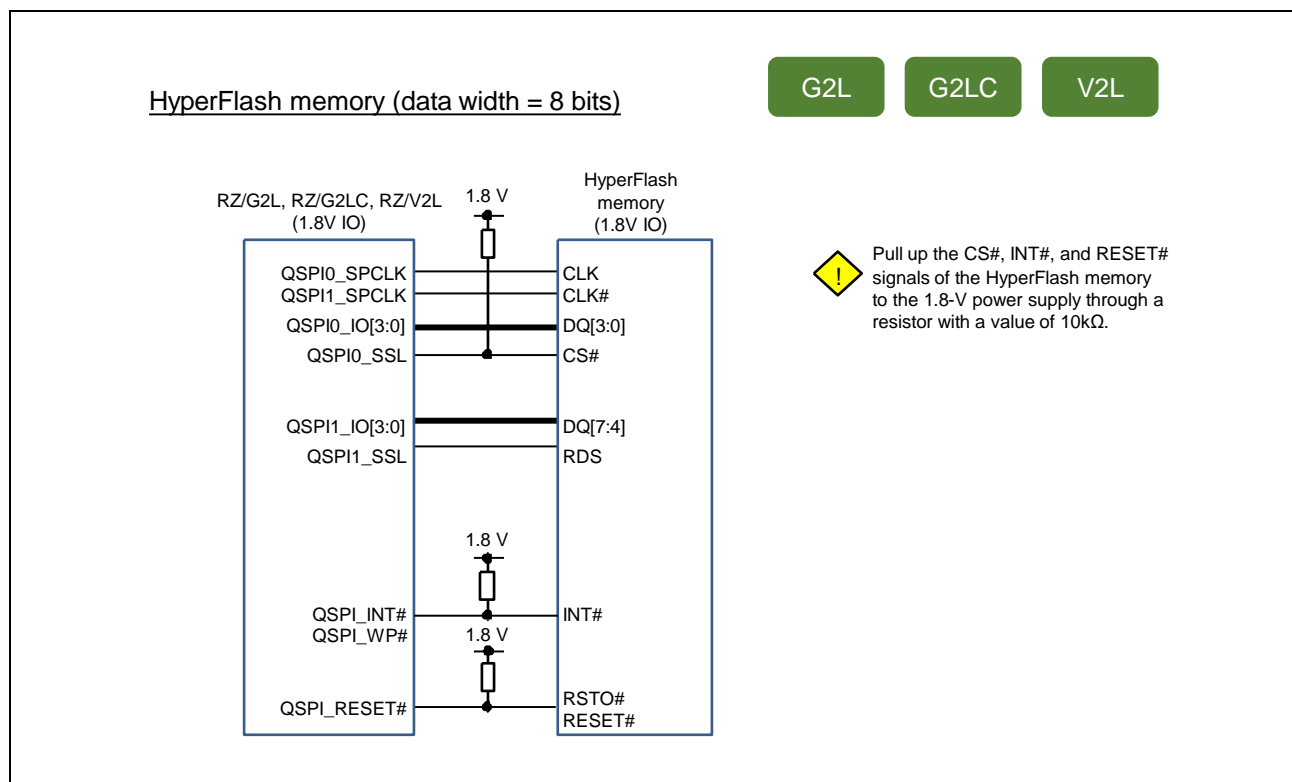
Figure 5.4   Connection of HyperFlash Memory

Documents for Reference

- Hardware user's manuals for individual target devices

- Datasheets or technical documents for HyperFlash memory or SPI flash memory

5.12 eXpanded Serial Peripheral Interface (xSPI)

💡 Points

G3S

- The xSPI enables the direct connection of Quad/Octal-SPI flash memory and OctaRAM to RZ/G3S.

- This interface consists of two internal QSPI interfaces that together provide 8-bit width access.

- The two QSPI interfaces do not support independent operation.

  - Although connecting two units of Quad-SPI flash memory to xSPI_IO[3:0] and xSPI_IO[7:4] in parallel and using them as 8-bit width is possible, xSPI_IO[3:0] and xSPI_[7:4] cannot be used as two independent interfaces for Quad-SPI flash memory.

  - The SPI boot mode supports a device connected to XSPI_CS0# terminal.

- The xSPI is a relatively high-speed interface. Although we do not provide any guide in particular, we recommend that you confirm that the signal timing and quality are free of problems by providing instructions about equal-delay (equal-length) wiring or simulating transmission in advance.
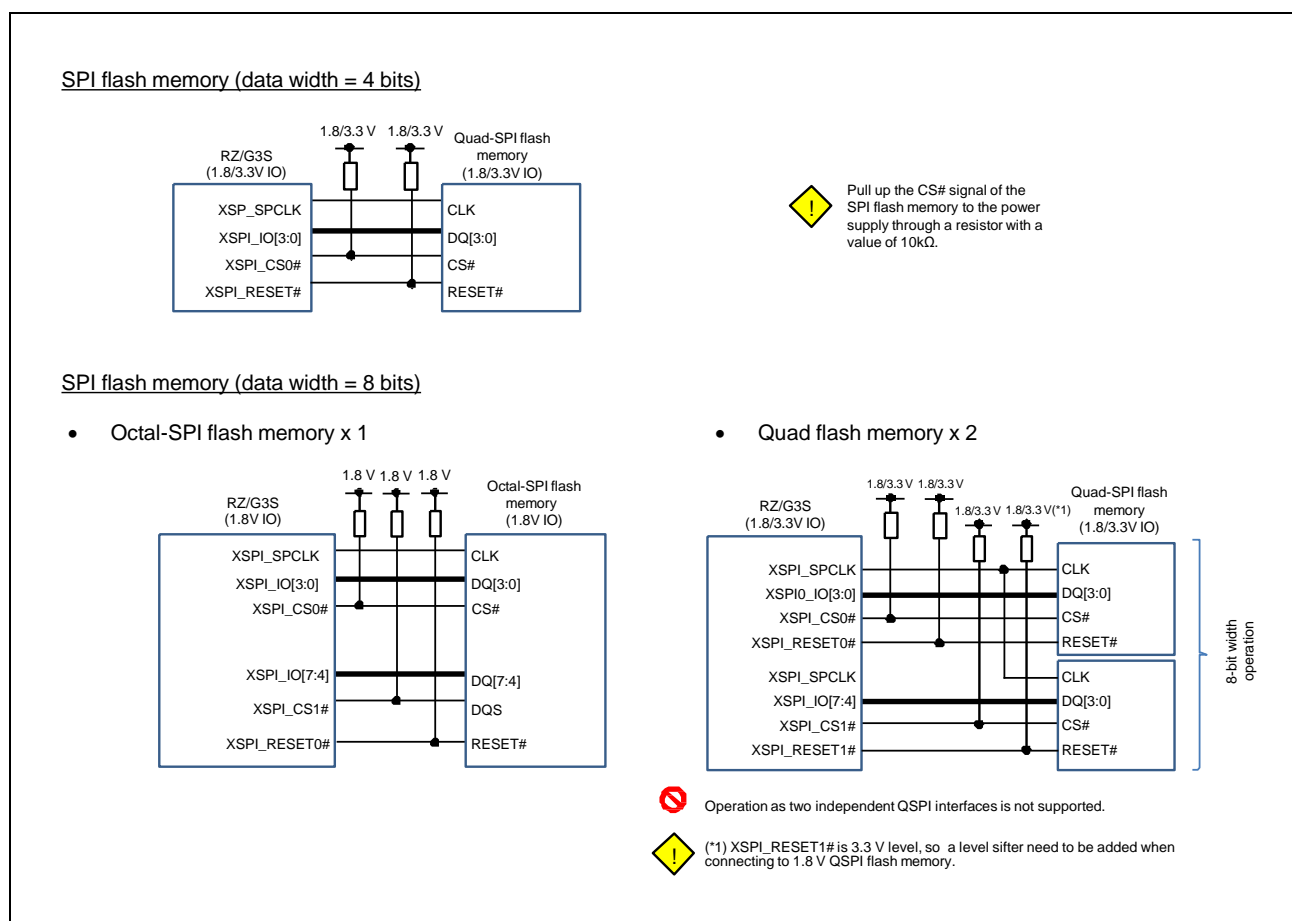
Figure 5.5   Connection of SPI Flash Memory
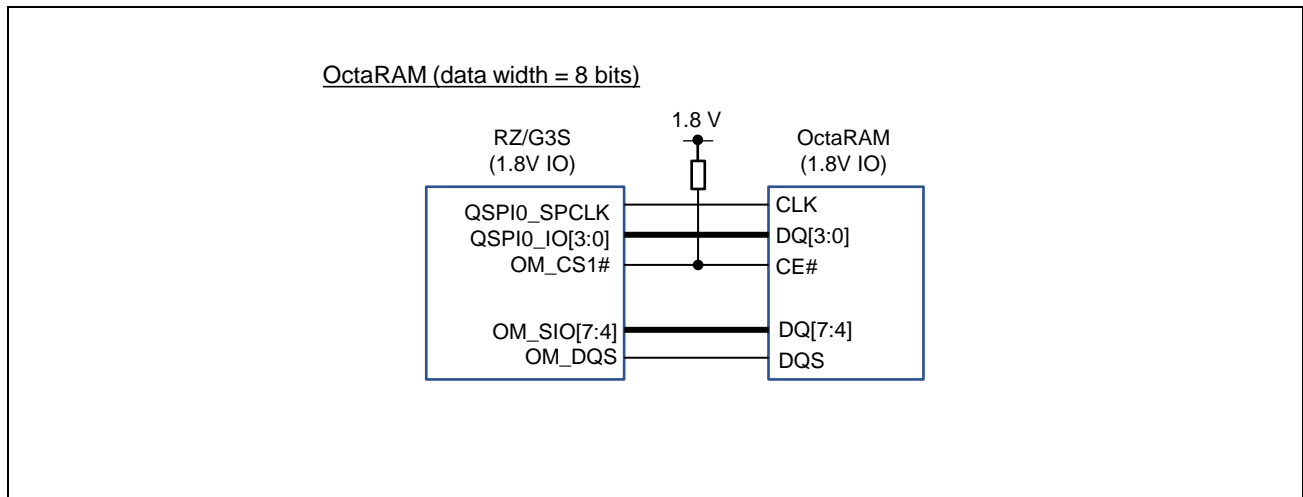
Figure 5.6   Connection of OctaRAM

Documents for Reference

- RZ/G3S Group Hardware User's Manual

- Datasheets or technical documents for SPI flash memory

5.13 CD and WP Signals of the SDHI

Points

ALL

- The CD (card detect) and WP (write protect) input signals of the SDHI are 3.3V IO (3.3 V) signals.

- When pulling up these signals with an external circuit, be sure to use 3.3 V.
  Do not pull these signals up to the SD card power supply (SDn_PVDD) (n = 0, 1).
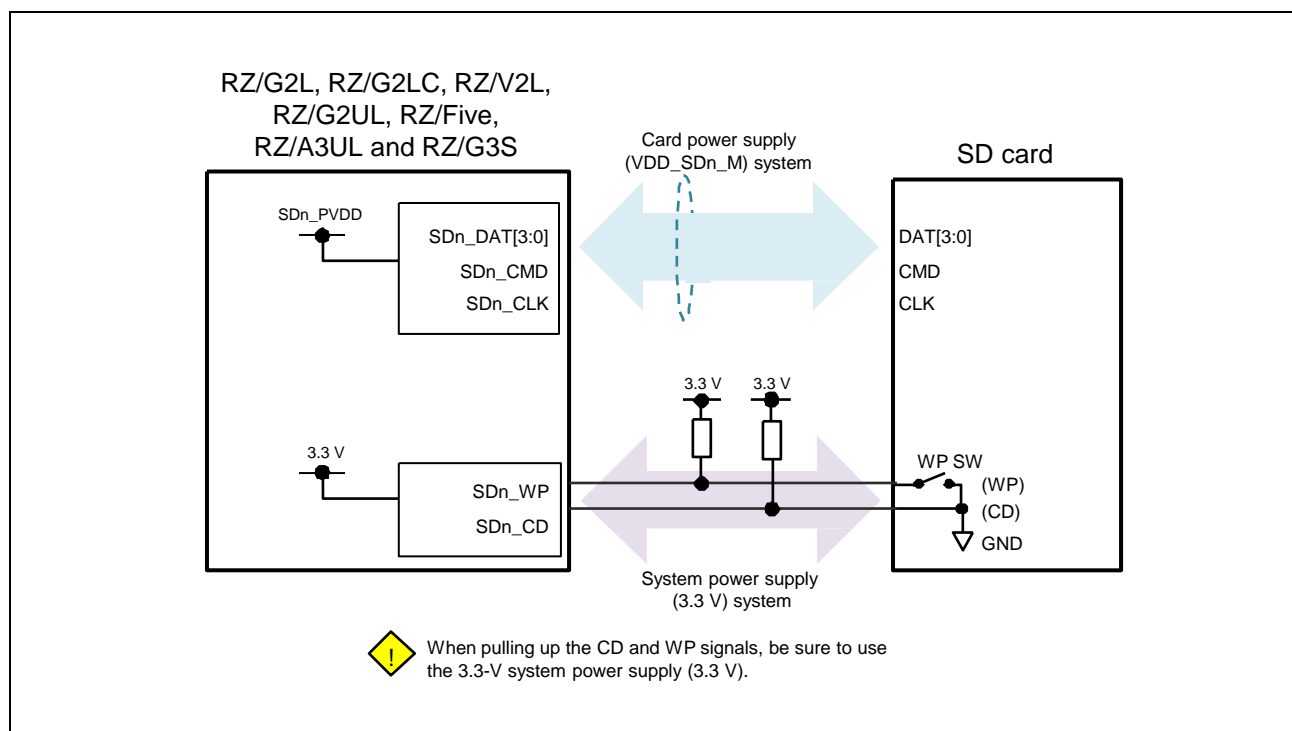
Figure 5.7　　CD and WP Signals of the SDHI

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

5.14 SDHI Circuit

Points

ALL

- Since SDHI (MMC) is a relatively high-speed parallel interface, we recommend that you perform SI simulation with the use of an IBIS model.

- When pulling up the CMD and DAT3 to DAT0 signals of the SDHI, use the SDHI IO power supply (SDn_PVDD) (n = 0, 1).
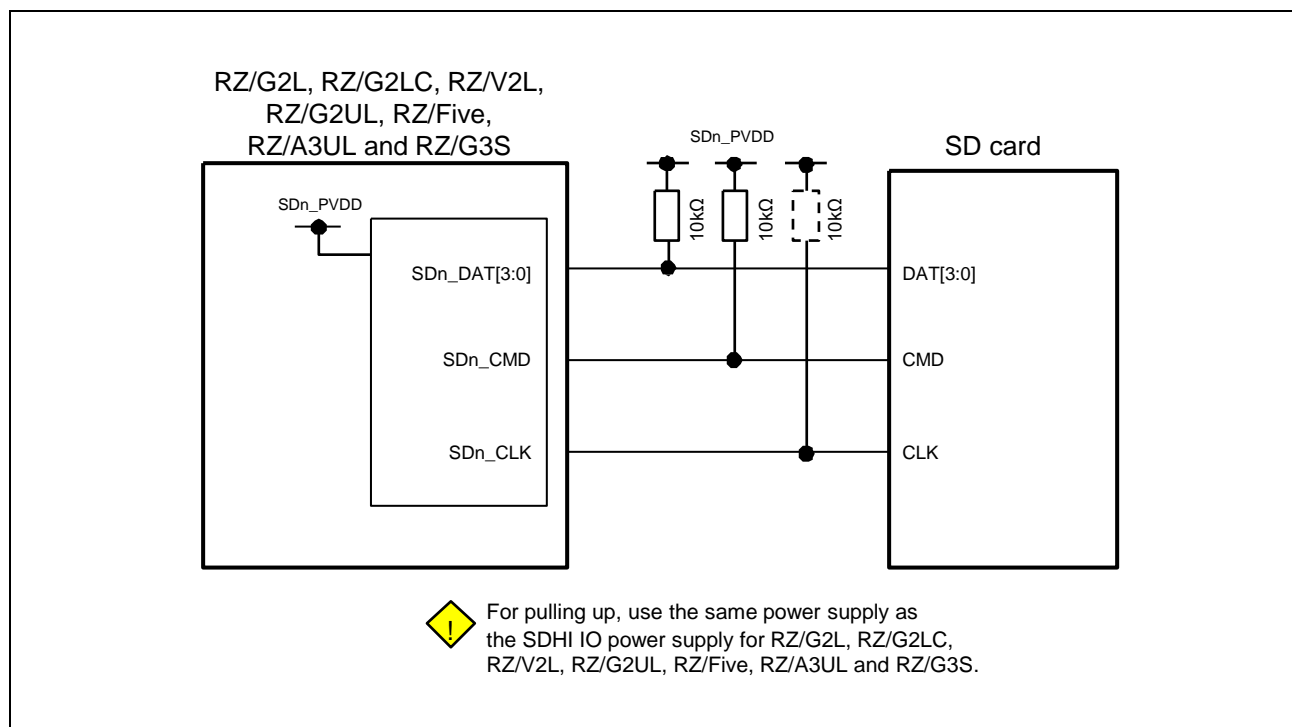
Figure 5.8   Pulling up of SDHI Signals

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

5.15   Connecting an Ethernet PHY Module

Points
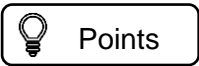
ALL

- Using Ether RGMII requires connection to an external PHY module via the RGMII.

- For connection of RGMII, refer to the following application notes.

- Please refer to the datasheet of the peripheral devices to be used.

Table 5.6   Guidelines for Connection of the Ethernet PHY

Interface	Guideline
RGMII	• Guide to Using RGMII in Making an Ethernet-IF Connection

Documents for Reference

- Hardware user's manuals for individual target devices

- Guide to Using RGMII in Making an Ethernet-IF Connection

- Circuit diagrams of individual evaluation board kits

5.16 JTAG Circuit

Points

ALL

- JTAG can be used as a normal operation mode or a debug mode by switching a mode setting (DEBUGEN).

- If using as a debug mode, DEBUGEN must be pulled high. If using as a normal operation mode, DEBUGEN must be pulled low.

Table 5.7   Pull-Up/Pull-Down Processing of JTAG

Signal	Pull-up/Pull-down Processing
	JTAG
TDO	—
TRST	Pull-up
TCK/SWDCLK	Pull-up
TMS/SWDIO	Pull-up
TDI	Pull-up

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

- Circuit diagrams of individual evaluation board kits

5.17 I2C Interfaces

Points

ALL

- RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S have multiple I2C bus interfaces.

- Two types of buffer are available: low-driving with LVTTL buffers and open-drain buffers.

  RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL

  − Open-drain type: This belongs to the 3.3V IO power domain and can be used with a 3.3 V I2C bus.

  − LVTTL-buffer type: This belongs to the 3.3V IO power domain and can be used with a 3.3 V I2C bus.

  RZ/G3S

  − Open-drain type: This belongs to the 1.8V IO power domain but has 3.3 V tolerance, so can be used with a 1.8 V or 3.3 V I2C bus.

  − LVTTL-buffer type: This belongs to the 3.3V IO power domain and can be used with a 3.3 V I2C bus.

- The I2C does not have 5 V tolerance. The voltage level shifting is required to use I2C with 5 V.

- When the LSI is powered off, the pull-up power of the bus also must be off.

- Select an optimal pull-up resistor for the bus in terms of the number of connected devices. For LVTTL-buffer type I2C, when the I2C function is to be used, internal pulling up of the LSI is always off regardless of the pull-up and pull-down settings.

Table 5.8   Specifications of Output Buffer of I2C of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL and RZ/G3S

I2C	Output Buffer Type (LVTTL, OD = Open Drain)						
	RZ/G2L	RZ/G2LC	RZ/V2L	RZ/G2UL	RZ/Five	RZ/A3UL	RZ/G3S
I2C ch. 0	OD	OD	OD	OD	OD	OD	OD
I2C ch. 1	OD	OD	OD	OD	OD	OD	OD
I2C ch. 2	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL
I2C ch. 3	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL

Remarks

In short, the LVTTL output is used to achieve open-drain-like operation by turning off the output enable when the normal output buffer is driven to the high level.
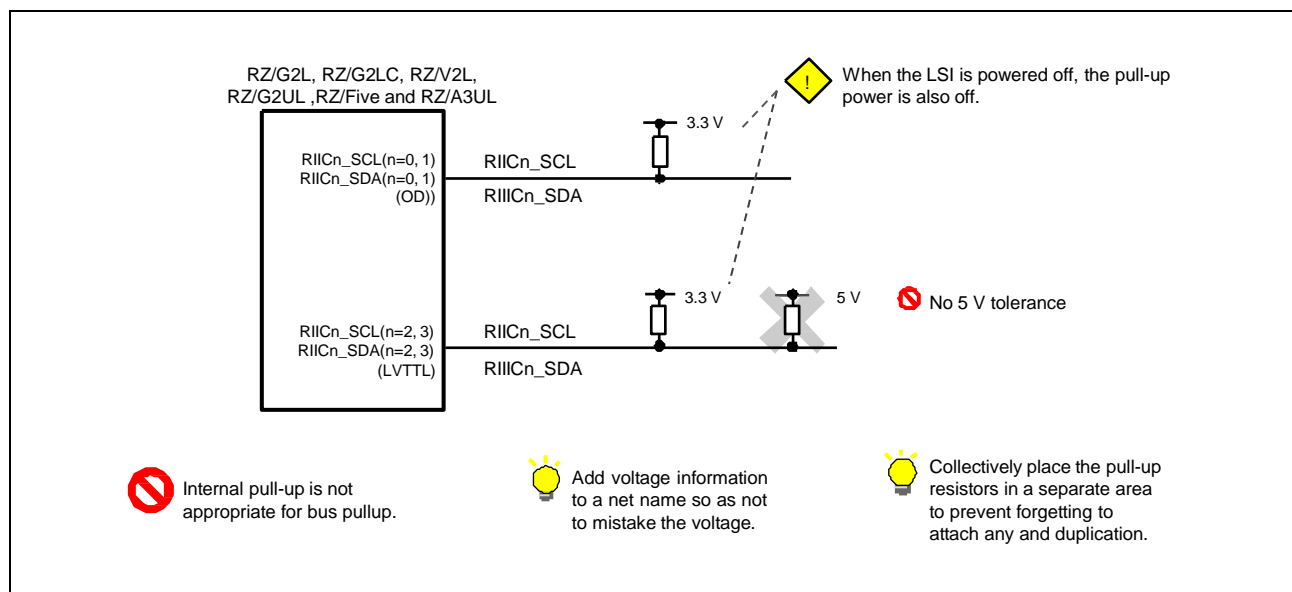
Figure 5.9(a)   Example of a Circuit Configuration for I2C
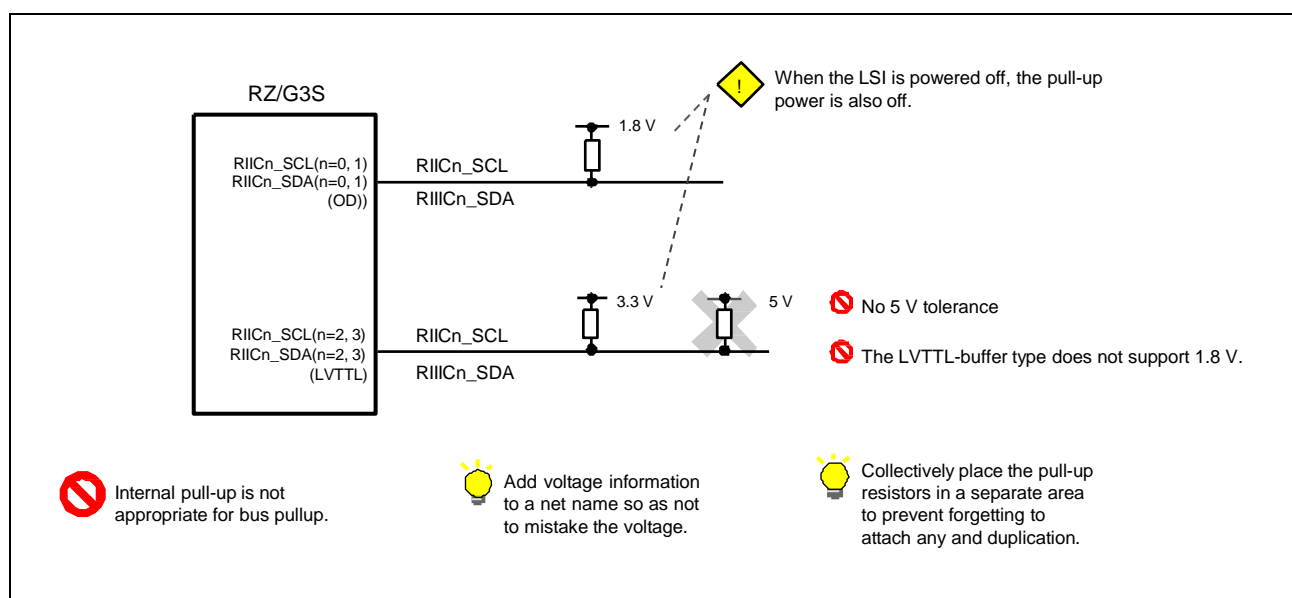
Figure 5.9(b)   Example of a Circuit Configuration for I2C

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

- Circuit diagrams of individual evaluation board kits

- Datasheets or technical documents for the individual peripheral devices

5.18   Slave Address Settings for the I2C Interface

Points

ALL

- I2C devices are identified by slave addresses.

- When connecting multiple I2C devices to the same I2C bus, be careful not to set the same slave address. If there is an I2C device with the same slave address in the same I2C bus, malfunction may occur.

- When using multiple I2C devices for which addresses cannot be set, you need to take measures such as connecting each device to a different I2C bus and using an I2C bus address translator IC.

- We recommend that you specify slave addresses and connected an I2C bus on the circuit diagram to allow efficiency in software development by driver engineers, in circuit reviews and in debugging by third parties.
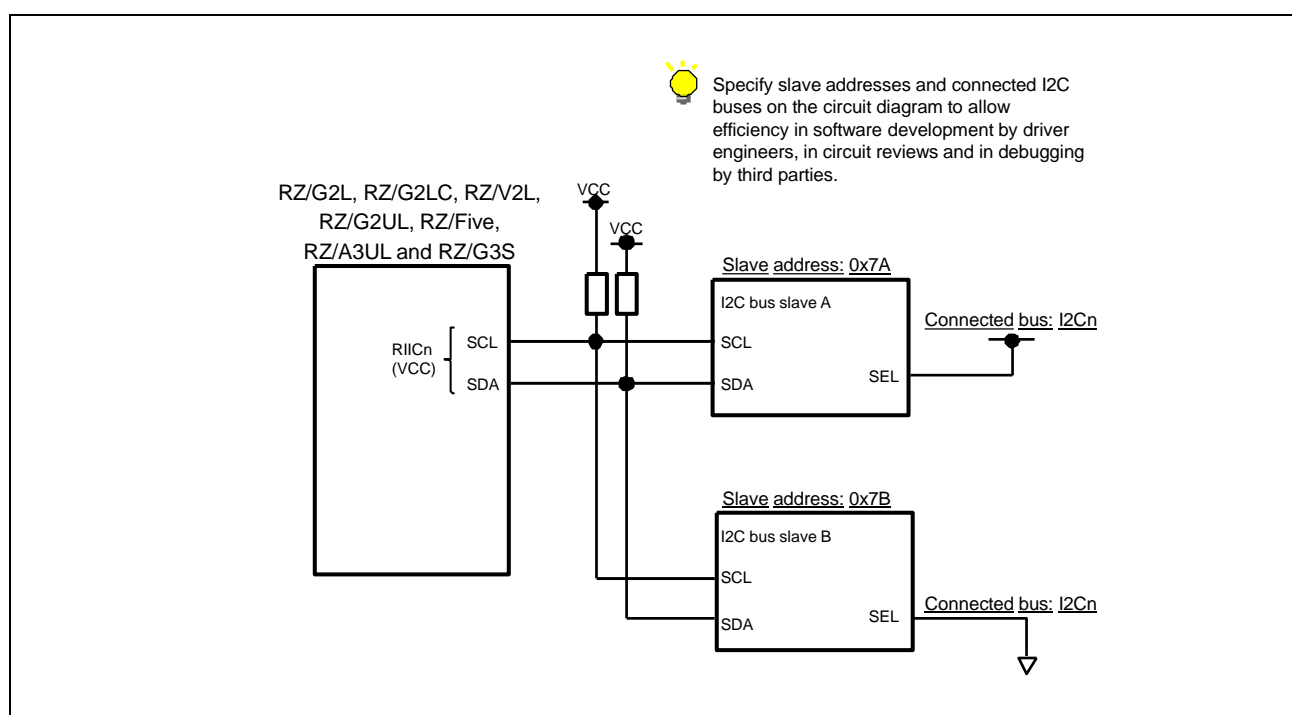
Figure 5.10   Example of a Circuit Diagram of I2C Devices

Document for Reference

- Datasheets or technical documents for the individual peripheral devices

5.19 Master and Slave Settings of the SPI

Points

ALL

- In RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, the SPI Multi I/O interface supports only master mode and the Renesas Serial Peripheral interface supports master and slave modes.

- When the Renesas Serial Peripheral interface is used in master mode, the SSL signal is fixed to the low level.

- When the Renesas Serial Peripheral interface is used in slave mode, the SCK input is not a Schmitt-trigger input. Therefore, pay attention to glitches and rounding of the clock waveform due to pin capacitances and wiring branches.

- When the Renesas Serial Peripheral interface of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S is to be used in both master and slave modes, such as on a multi-master SPI bus, make sure that the two outputs do not become short-circuited.
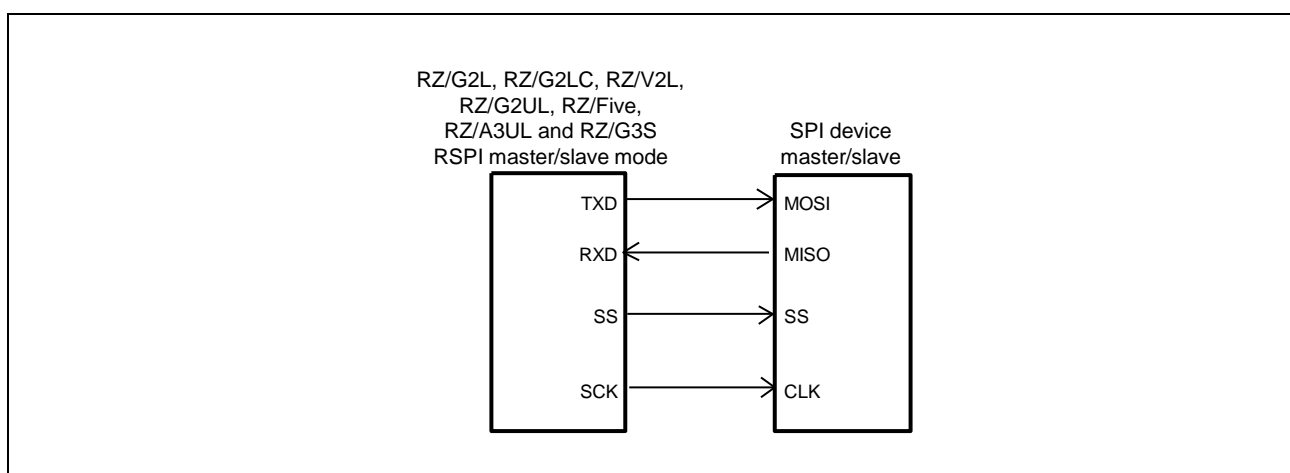
Figure 5.11   Connection of SPI and RSPI

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

- Datasheets or technical documents for the individual peripheral devices

5.20 External Input Clock for the SCIF

Points
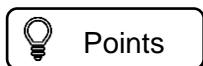
ALL

- Either external clock or internal clock can be selected as the SCIF clock source.

- If there is no possibility of changing the internal clock, and the error rate of the SCIF (UART) bit rate generated from the internal clock is within an allowable range, it is not always necessary to use an external clock.

Documents for Reference

- Circuit diagrams of individual evaluation board kits

- Datasheets or technical documents for the individual peripheral devices

5.21 Coupling Capacitors for Audio Output Circuits

💡 Points

ALL

- Pay attention to the polarity if you will be using aluminum electrolytic capacitors as coupling capacitors for the audio circuits.

- Please refer to the datasheet of the peripheral devices to be used.
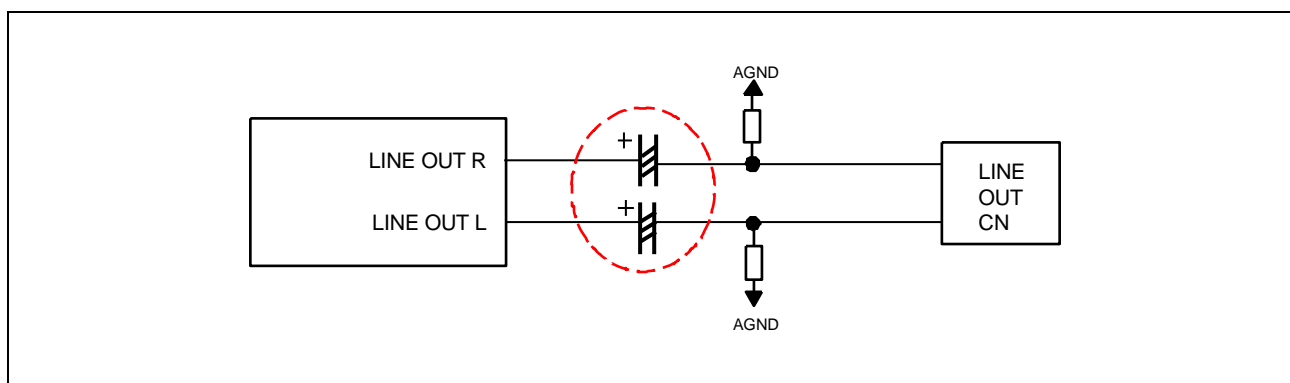
Figure 5.12   Polarity of Electrolytic Capacitors for Audio Output Circuits

Documents for Reference

- Circuit diagrams of individual evaluation board kits

5.22 Polarity of Electrolytic Capacitors

Points

ALL

- Incorrect polarity of the power supply capacitor may cause a serious accident such as generation of toxic gas.

- To make it easy to detect errors in implementation when designing a circuit in addition to paying attention to correct polarity of the power supply capacitor, observe the following.

  − Silk-screen markings to highlight the point

  − Devising the layout and component arrangement for uniform orientation

Prevent errors by silk-screen printing of shapes.

Devise the layout and component placement such that orientation is uniform both vertically and horizontally to reduce the possibility of errors in implementation.
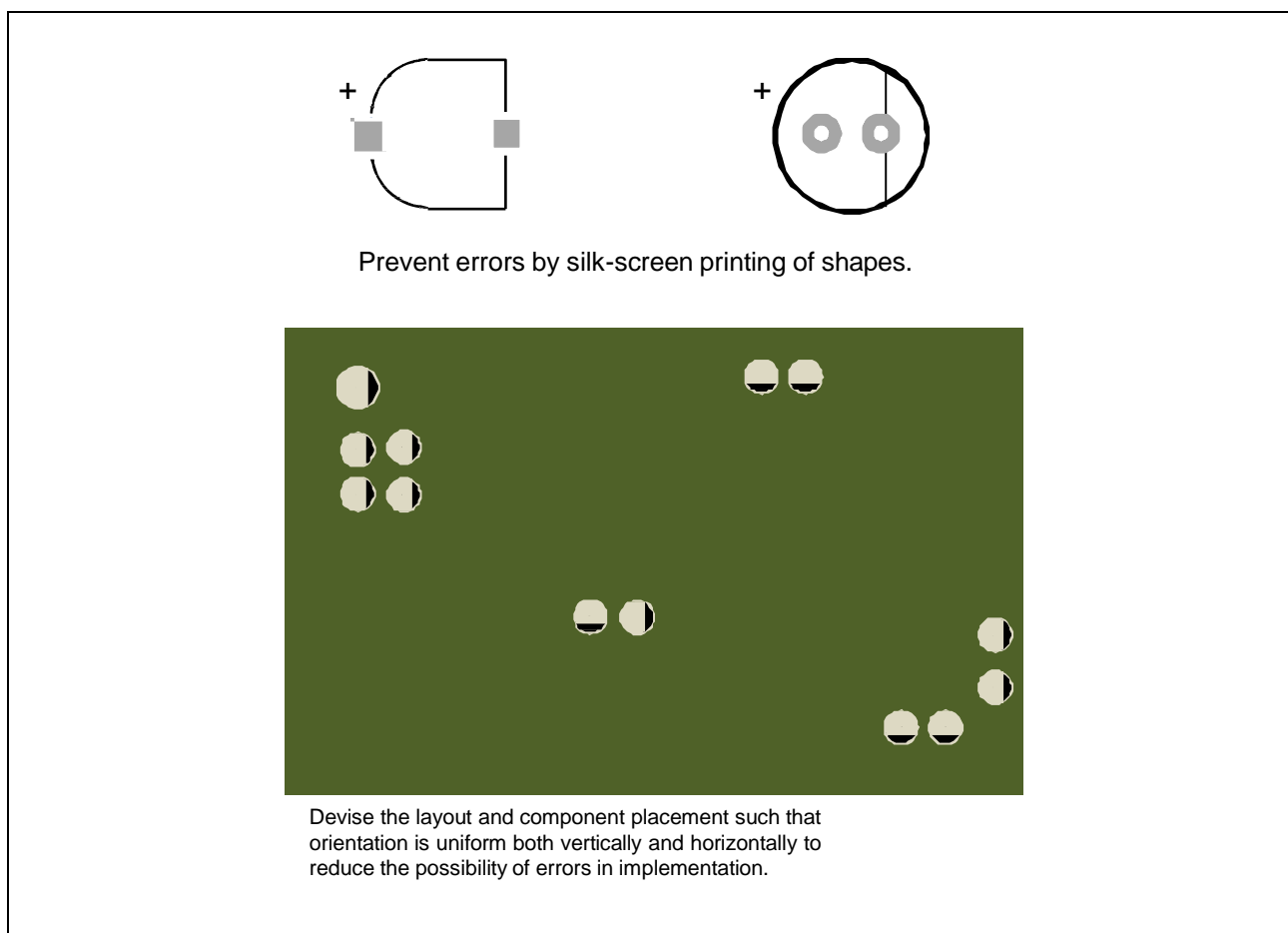
Figure 5.13   Silk-Screen Printing and Orientation of Electrolytic Capacitors

5.23 Programming the On-Board EEPROM

Points

ALL

- A system configuration in which on-board EEPROM is installed for the writing and reading of configuration information such as for the system power supply (PMIC), an FPGA or CPLD, MAC address, and board ID via the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S or a separate on-board controller might be useful in terms of evaluation and debugging.

- Accessing the internal SPI or EEPROM on the I2C bus when RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S are not powered on violates the absolute maximum rating. In such a situation, the circuit must be configured so that the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S are isolated and protected.

- In particular, you need to pay attention to devices that are not powered on, including RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, when programming an FPGA/CPLD that includes the system power supply (PMIC) and power control circuit.
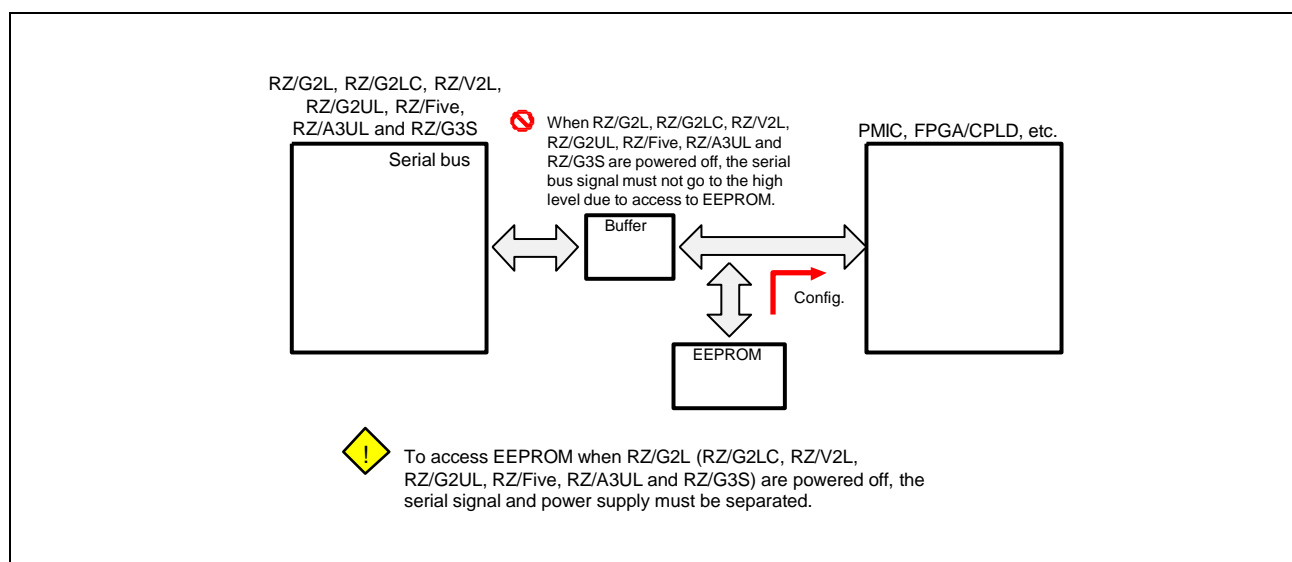
Figure 5.14   Example of a Circuit to Program the On-Board EEPROM

Document for Reference

- Circuit diagrams of individual evaluation board kits

5.24 Notes on Connecting Connectors

Points

ALL

- Note the following points when installing board-to-board connectors for peripheral devices and the expansion of memory.

    - Is there any consistency in the connector pin arrangement between the main board and the expansion board?

    - Is the connector pin arrangement designed so that noise such as crosstalk is likely to be applied?

    - Is there no problem with the allowable current per connector pin when power is supplied through the connector?

    - Do the connectors have a sufficient number of GND pins in terms of the allowable current and reducing noise?

    - Is the power supply on the main board designed to use expansion boards?

    - Are the values of capacitors on the connector's boundary plane sufficient?

    - When power to the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S and peripheral devices on the main board is off, will the expansion board circuit not produce a high-level output?

    - Are measures such as against the reverse insertion of connectors taken?

    - Are the heights of the connectors sufficient for those of the components on the main board and expansion boards?

    - Are safeguards against the connection of extension boards that might render the board inoperable sufficient?

Documents for Reference

- Circuit diagrams of individual evaluation board kits

- Datasheets or technical documents for the individual connectors and connected devices

5.25   Checking the Revision Number of Mounted Targeted Devices

Points

ALL

- Make sure that the MD pin settings suit the revision of the device.

    – For optional products such as for security, the MD pins (details are not disclosed) may need to be set to the side designated as "prohibited".

- Please confirm Part Number (P/N) of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S.

Document for Reference

- Hardware user's manuals for individual target devices

5.26   Reconfirming the Operation of Adapted Circuits

Points

ALL

- Although using circuits designed and evaluated for past hardware as design assets is common practice, assuming that a circuit is proven may delay the detection of defects and problems with the circuit.

- Confirming that points of change such as the conditions applicable to peripheral circuits and changes to the specifications of the ICs used do not raise problems is important, even for a circuit with a proven track record.

  - Have new restrictions not been added?

  - Has the revision number of the device to be used not changed?

  - Are the adapted circuits appropriate compared to application circuits described in the technical documentation?

  - Is the power connection and signal connection inconsistent due to careless copy and paste?

5.27 Handling the NC pin

Points

G2UL   Five

- In general, a pin being labeled NC means that the pin is not connected to the silicon die inside the LSI.

  - NC: Non-connection (or no connection)

- Although the NC pin is basically not connected to anything, the recommended pin handling such as connection to the GND or power supply might be provided depending on the product.

- Be sure to check whether the recommended pin handling is described in the technical documentation of each LSI, rather than assuming that a pin labeled NC is not connected to anything from its name.

- If the handling method is not described, we recommend that you contact the chip's vendor.

- Additionally, pay attention to the LSI test pins and internal regulator power output.

Documents for Reference

- RZ/G2UL Group User's Manual: Hardware

- RZ/Five Group User's Manual: Hardware

- Lists of pin functions for RZ/G2UL and RZ/Five

- Manuals, datasheets, or technical documents for the peripheral LSI chip

5.28   Notes on SCIF0 Signal Connection

Points

G2L   G2LC   V2L

G2UL   Five   G3S

- SCIF0_RXD/TXD must be assigned so that it can be used as a SCIF download.

- It is recommended that SCIF0_RXD/TXD be ready to be connected to a console for debugging.

- The following circuit configuration is recommended to output to a console when power is turned on.
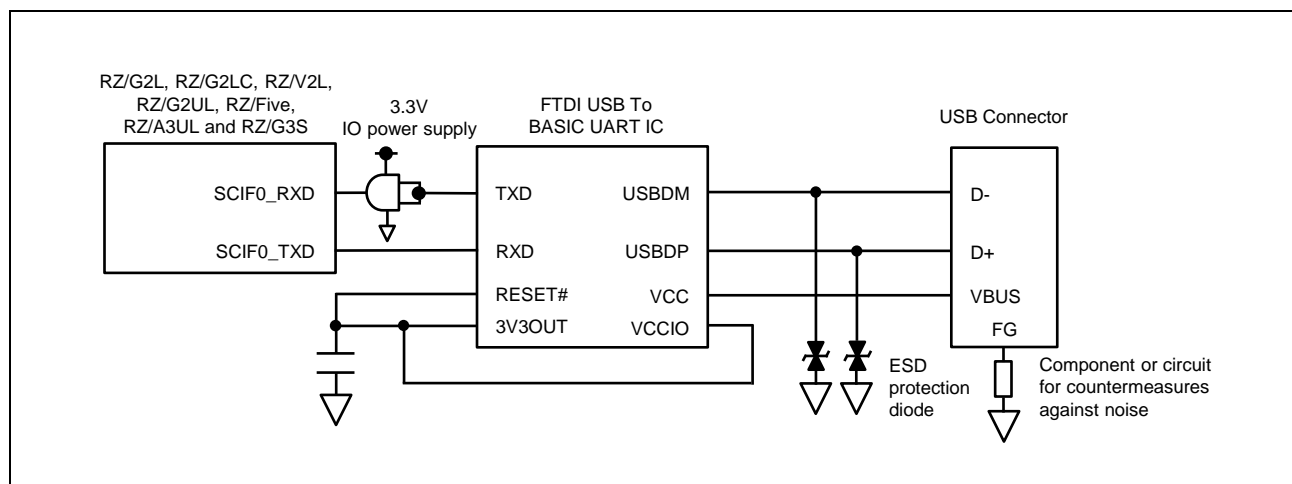
Figure 5.15   Example of a Circuit Configuration for SCIF0 Signal

Documents for Reference

- Hardware user's manuals for individual target devices

- Circuit diagrams of individual evaluation board kits

5.29 Octa Memory Controller

Points

A3UL   G3S

- When using an OctaFlash as boot memory connect the QSPI_RESET# pin to the OctaFlash RESET# pin. An OctaFlash can be only connected to the Octa Memory Controller, not to the SPI Multi I/O Bus Controller. **Figure 5.16** shows examples of an OctaFlash and controller connection.
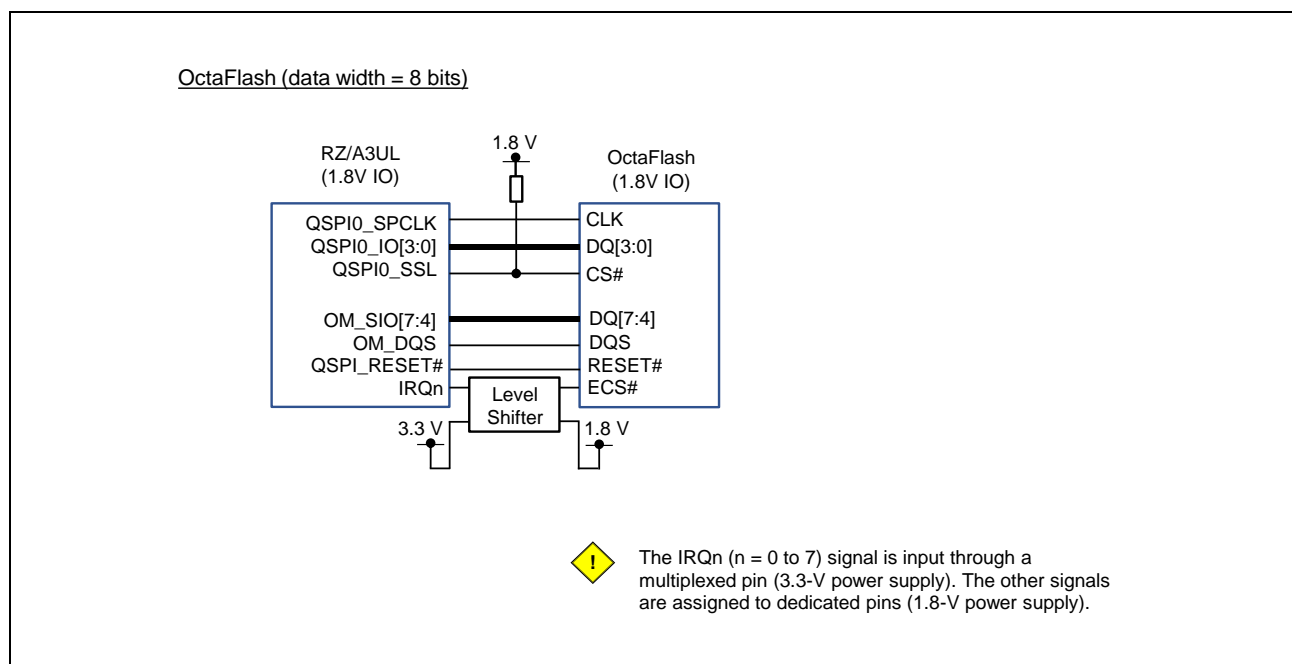
Figure 5.16(a) Connection of OctaFlash
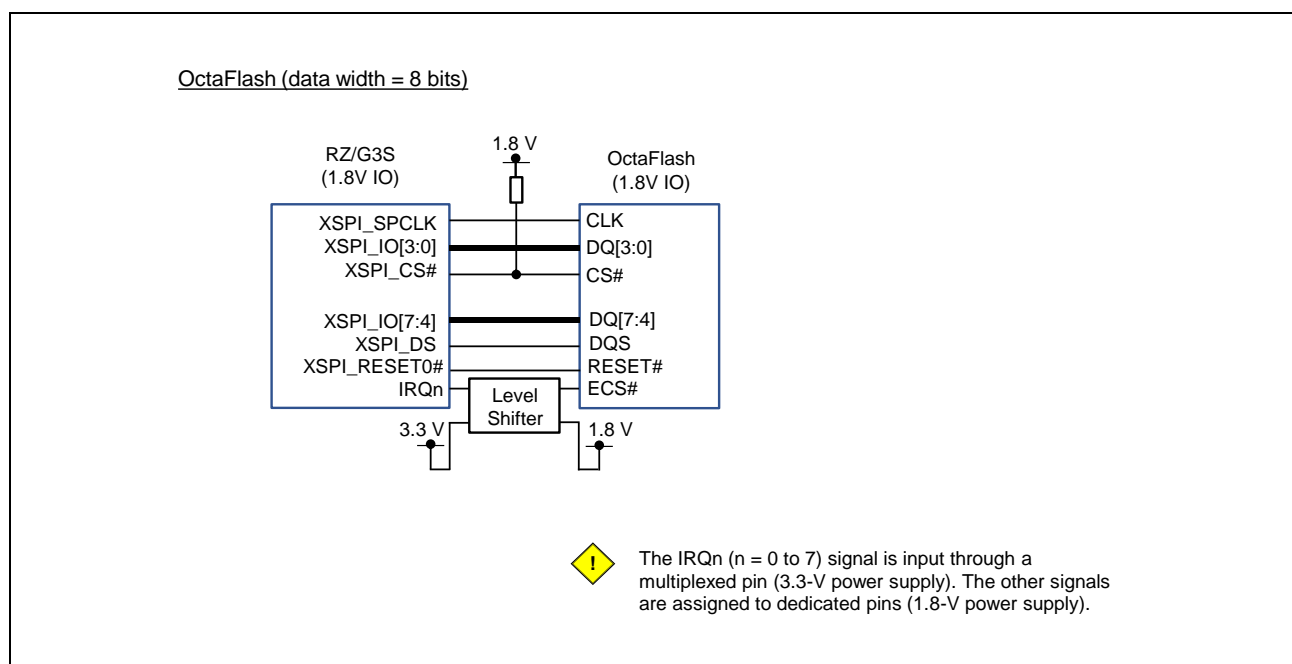
Figure 5.16(b) Connection of OctaFlash

Figure 5.17 shows an example of an OctaRAM connection.
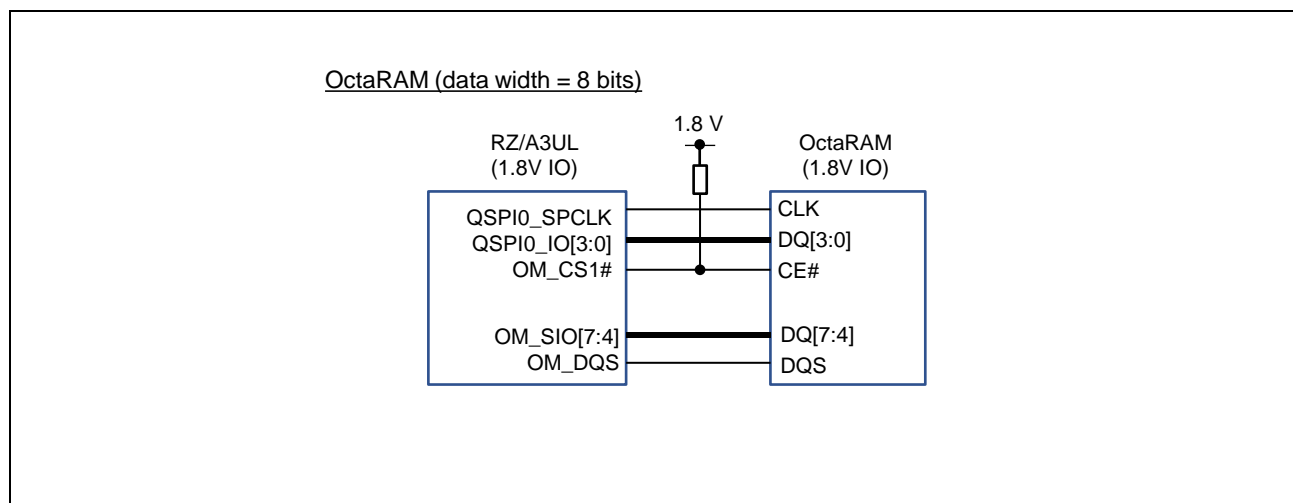
Figure 5.17(a)   Connection of OctaRAM
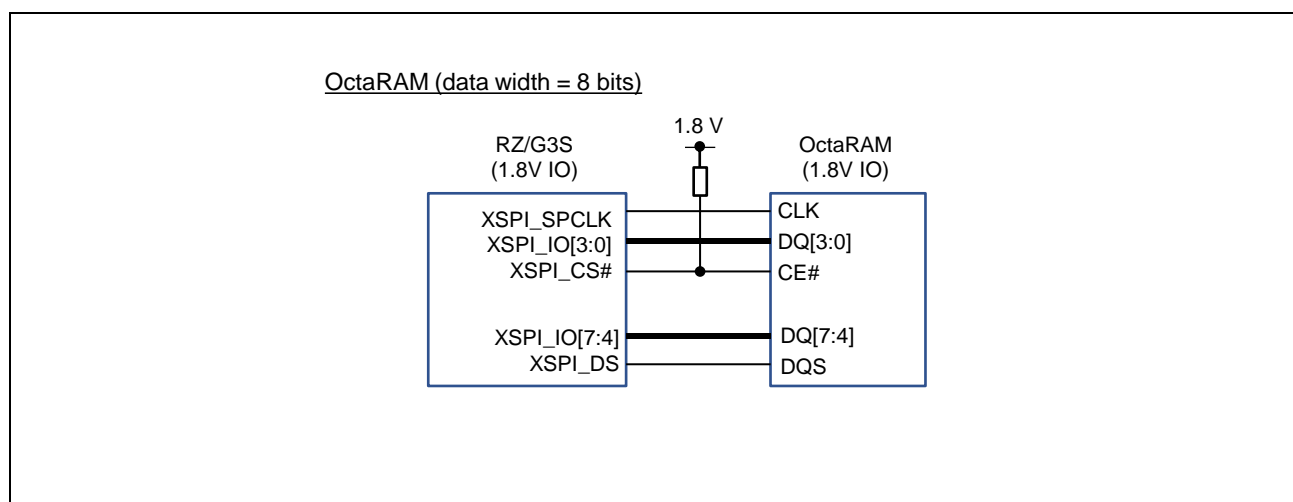
Figure 5.17(b)   Connection of OctaRAM

Documents for Reference

- RZ/A3UL Group User's Manual: Hardware

- RZ/G3S Group User's Manual: Hardware

- Circuit diagram of RZ/A3UL Evaluation board Kit Octal Edition

- Datasheets or technical documents for OctaFlash or OctaRAM memory

5.30 IO Voltage Level available for power domain "PVDD182533"

Points
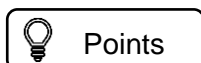
ALL

There are the following unused GPIO pins on the Evaluation board Kits.

These pins belong to the power domains "PVDD182533_0" or "PVDD182533_1" and 1.8 V, 2.5 V, and 3.3 V are selectable when used as Ethernet function. If using these pins as GPIO, these power domains should be 3.3 V.

Table 5.9   Supported IO Voltage Levels by Each Function

Power Domain	RZ/G2L, RZ/G2LC, RZ/V2L Pin Name	RZ/G2UL, RZ/A3UL, RZ/Five RZ/G3S Pin Name	Pin Function	Supported IO Voltage Level when Used as Ethernet	Supported IO Voltage Level when Used as GPIO
PVDD182533_0	P22_1	P2_1	ET0_TX_ERR	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_0	P23_0	P2_2	ET0_TX_COL	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_0	P23_1	P2_3	ET0_TX_CRS	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_0	P27_0	P4_2	ET0_RX_ERR	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_1	P32_0	P8_1	ET1_TX_ERR	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_1	P32_1	P8_2	ET1_TX_COL	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_1	P33_0	P8_3	ET1_TX_CRS	1.8 V/2.5 V/3.3 V	3.3 V
PVDD182533_1	P36_1	P10_1	ET1_RX_ERR	1.8 V/2.5 V/3.3 V	3.3 V

Documents for Reference

- Hardware user's manuals for individual target devices

- Lists of pin functions for individual target devices

- Circuit diagrams of individual evaluation board kits

5.31　Selection of QSPI flash memory

Points
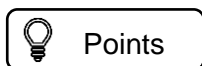
ALL

Using a QPSI flash memory with RESET pin is recommended.

When accessing over 16MB memory area, following changes are needed.

(1)　change from 3-BYTE address access to 4-BYTE address access (ENTER 4-BYTE ADDRESSING, Address: B7h)

(2)　switch to a BANK other than the first 16MB (READ EXTENDED ADDRESS REGISTER, Address: C8h)

When a reset occurs after these changes, the SoC will be reset, but the flash memory will not be reset. Then changes on the flash memory will remain. The boot ROM code on the SoC will try to read first 16MB of the flash memory with "3-BYTE address", however, the flash memory cannot accept that request. Therefore, the SoC will fail to reboot.

With a QSPI flash memory less than 16MB capacity, this issue will not be occurred because the changes (1) and (2) for 4-BYTE address read are not needed.

Besides the software reset, following events should be considered.

- A watchdog timer reset
- A physical reset button

If an over 16MB QSPI flash memory without RESET pin is used, it is needed to take some measures by hardware and/or software for this issue.

This is why using a QPSI flash memory with RESET pin is recommended.

6.   Points to Note in Designing PCB Wiring Patterns

6.1   Target Impedances of Wiring Patterns for Power Supplies

⚕ Points
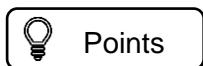
ALL

- Target inductance or impedance values are given for some power supply systems of an LSI.

- The target values are desired values in the design of patterns for power supplies rather than guaranteed values to avoid malfunctions. However, actual values greatly differing from the target values make malfunctions more likely. Therefore, we recommend designing wiring patterns within the range of target values.

- Some peripheral LSI chips may also have estimated target impedance values for their power supply pins. Contact peripheral LSI vendors regarding whether they provide such target values.

Table 6.1   Guidelines Covering Target Impedance and Inductance Values for Power Supply Systems

Power Supply	Related Guideline	Target Item
Logic power supplies (VDD)	PCB verification guide for Core	Target impedance
DRAM I/O power supplies (DDR_VDDQ)	PCB verification guide for DDR4/DD3L	Target impedance
USB 2.0	PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2	Target impedance
MIPI-CSI		Target impedance
MIPI-DSI		Target impedance
PCIe		Target impedance

6.2   Width of Wiring Patterns for Power Supplies

Points

ALL

- For RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, a current of approx. several amperes may be drawn through power supply pins. For such power supplies, take care with the widths of wiring patterns between the power supplies and the LSI.

  − The recommended width of power supply patterns is generally 2 mm per A to take the DC resistance of copper and the generation of heat into account. Even if a pattern width alone cannot satisfy the above recommendation, ensure no more than 2 A per mm as a minimum requirement. In cases where sufficient pattern width cannot be ensured, consider countermeasures such as sharing the pattern for the same power supply between 2 layers.

  − When the wiring patterns for power supplies are such that wiring runs are drawn from a power supply IC to multiple layers through via holes, take the maximum current into account in ensuring a sufficient number of via holes.

  − On RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S, logic power supply pins which draw relatively large amounts of current are arranged around the center of the package. Take care that the wiring patterns for the power supplies are not narrowed or divided into parts due to clearance for via holes to be used in bringing signal lines out from the pins on the periphery of the package. Examine the widths of power supply patterns in terms of the clearance for via holes being removed from the conductor widths.

  − Narrow wiring patterns for power supplies lead to the generation of heat on the board itself. The combination of the generation of heat by an RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S itself and narrow patterns leads to further lowering of the power supply voltage due to the DC resistance vs. temperature characteristic of copper. This also makes countermeasures for heat more expensive.

  − When a power supply IC you are using has a remote-sensing pin, placing the sensing pin closest to the RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S (the source of the power consumption) is advantageous from the viewpoint of cancelling the voltage-dropping effect of the power supply pattern.

Pattern width:

The per-square resistance of copper foil with a thickness t of 35 μm at 20°C is approx. 0.5mΩ. When such a wiring pattern for a power supply is 20-mm long, the DC resistance of the pattern is approx. 10mΩ. In this case, if a 5-A current is drawn, the voltage drops by approx. 50 mV.

The resistance of copper has a positive temperature coefficient. The temperature of the wiring pattern for a power supply changing from 20°C to 100°C will increase the resistance by approx. 1.35 times.

When t = 35 μm, rough estimates of the allowable currents for limiting the rise in temperature to 10°C and 20°C are 1 A and 3 A, respectively, per mm of width.

Via hole:

The thickness of the plating metal of a standard via hole is from 10 μm to 20 μm. A via hole must be suitable for the current that flows through it according to the same considerations as described for pattern width above. A rough estimate of the allowable current is 0.5 A for a via hole 0.5 mm in diameter and 0.3 A for a via hole 0.3 mm in diameter.

When the width of a power supply pattern is reduced to bring signal lines out as shown in the figure at right, examine the width of the power supply pattern with the parts occupied by the via holes and the clearance between them removed.

Ensure sufficiently wide paths for the flow of current from each power supply through countermeasures such as taking the placement of via holes into account, as in the example at right. If doing so is impossible, consider other measures such as using two layers of wiring for the power supply or exchanging the PCB design for a build-up board that has no via holes.

Power supply pattern

Power supply pattern

Via holes for bringing signal lines out

Placing via holes in a row horizontally makes the flow paths extremely narrow.

Ensure sufficiently wide flow paths by placing the via holes in a staggered arrangement or through other countermeasures.
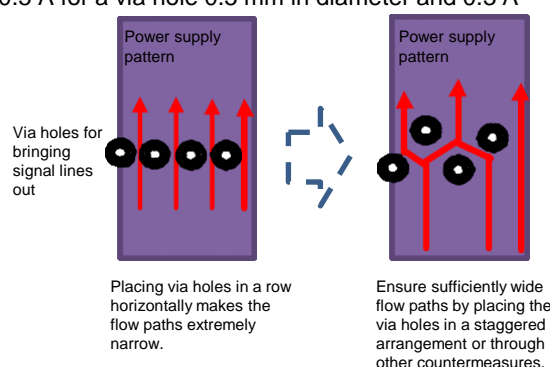
Figure 6.1   Width of Wiring Patterns and Via Holes for Power Supplies

6.3   Connecting Digital and Signal Grounds to Other Grounds

Points

ALL

- Analog grounds are sensitive to noise, so take particular care to avoid the application of noise from digital or signal grounds, which are relatively noisy. This is why separating analog grounds from digital and signal grounds and only connecting them at a single point are recommended in most cases. Avoid the analog ground not being connected or being connected to multiple points in the layout of patterns on a PCB by stating the one-point connection as a note on the circuit diagram.

- As the ground around a switching power supply IC draws a large amount of current in many cases, the ground is usually separated as a power ground. Most power supply IC makers provide a recommended layout of patterns on PCBs. Clearly state that the recommended layout is present on the circuit diagram.

- When connecting a frame ground for USB memory or an SD card, etc. with a digital or signal ground, take appropriate measures such as a one-point connection through noise-suppressing components. If a connector vendor provides a recommended layout of patterns on PCBs, follow the vendor's recommendation.

- When connecting a chassis ground and a PCB, take the application of external noise such as electro-static discharge (ESD) into account in the pattern design. Though the way of connecting a chassis ground and digital or signal ground differs from case to case, including non-connection, ensure the following points: noise must run through paths with relatively low impedance and be earthed; and the above paths do not include digital or signal grounds for the LSI chip that is the main component.

Making a note on the circuit diagram.

PCB layout

Clearly state the connection of digital and analog grounds on the circuit diagram.

Insert a virtual component or 0-Ω resistor that indicates the one-point connection.

Digital ground

Analog ground

Analog ground

Digital ground

One-point connection in layout of patterns on the PCB

Power ground

Power ground   Digital ground

Clearly state the presence of a recommended PCB layout on the circuit diagram.

CN

FG
FG

Frame ground

Frame ground   Digital ground

through noise-suppressing components.

Clearly state the presence of a recommended PCB layout on the circuit diagram.

Figure 6.2   Connecting Digital Grounds to Other Grounds

6.4   Handling Exposed Pads

Points

ALL

- Some ICs such as power supply ICs have exposed pads to improve heat dissipation.

- The exposed pad may not be defined as an LSI pin in some cases. To avoid forgetting the need for connection to the specified destination such as the ground or a power supply, apply countermeasures such as adding pin names for exposed pads to the circuit diagram.

- The majority of exposed pads are intended for the dissipation of heat. So that the generated heat is propagated to the inner layer along paths with low thermal resistances, apply countermeasures such as using more via holes leading to grounds in the inner layer than would be usual.

- If a recommended wiring pattern for the LSI chip covers the wiring pattern around an exposed pad, follow the recommendation.
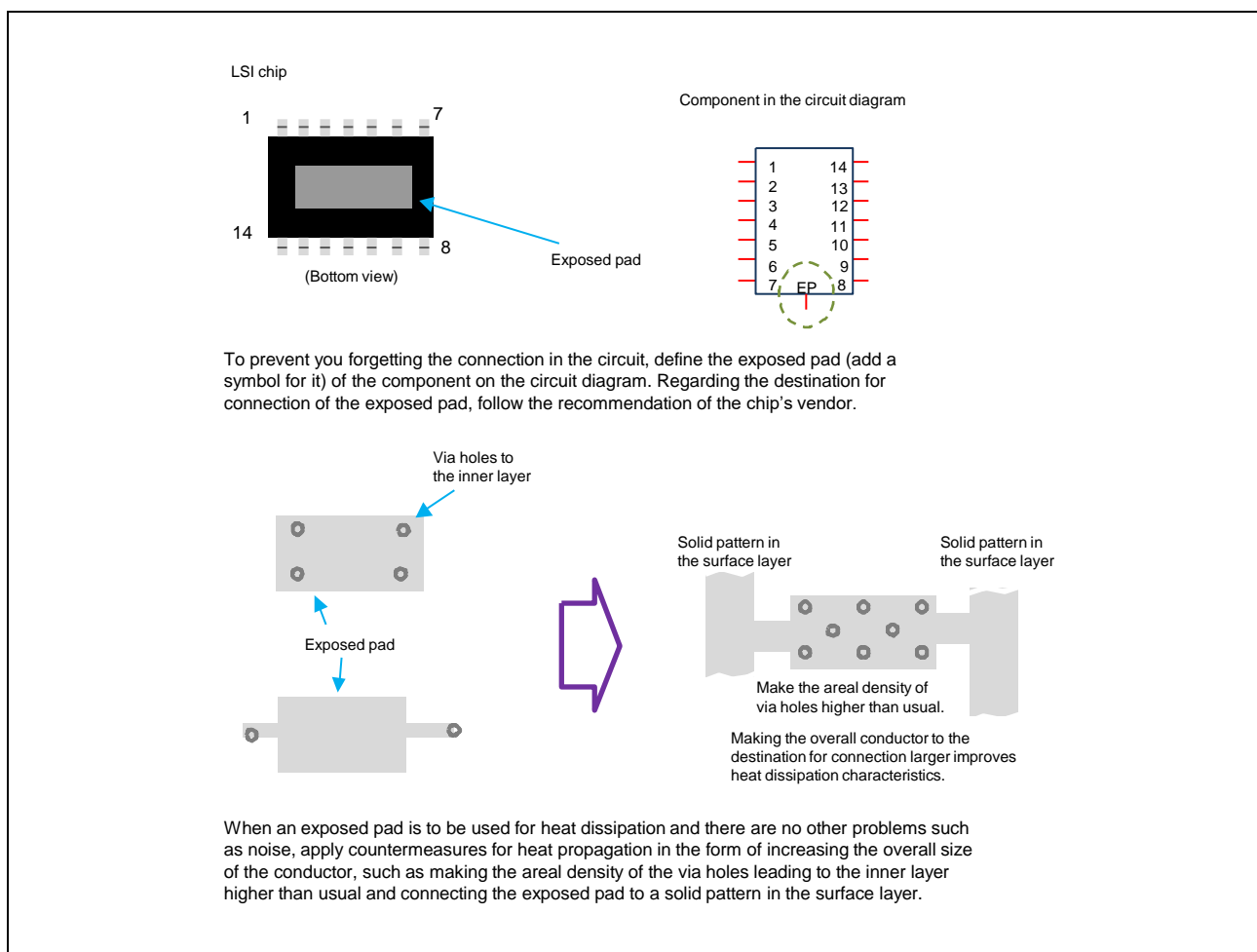
Figure 6.3   Handling Exposed Pads

6.5 Designing Wiring Patterns that Include Ground Shields/Guards

💡 Points

ALL

- Applying ground shields to clock, reset, or faint analog signals may be desirable or necessary in many cases.

- Ground shields are only effective if the wiring is appropriate. Inappropriate wiring may lead to the ground shields having the opposite effect to that which was intended.

  – Be sure to connect both sides of a ground shield to the ground plane in the inner layer to prevent their being left open-circuit.

  – When the ground shield wiring runs are long, as well as a single via hole leading to the ground layer from both sides, place a via hole every 5 to 10 mm.

  – The width of the ground shield lines must be at least the same as that of the signal line, and ideally at least as wide as the diameter of the via holes leading to the ground plane.

- Care is also required in the placement of solid patterns of ground in unused areas of the PCB.

  – If this prevents the preparation of via holes leading to the inner ground, do not proceed with the application of a solid pattern of ground.

  – For a large solid pattern of ground, place one via hole leading to the ground layer roughly every 10 mm.

- Especially in the case of applying ground shields to high-speed signals, take care with regard to the uniformity of the shields.

  – When applying a ground shield to a high-speed signal, take care on the following points: do not change the spacing between the signal and ground shield along their paths; do not divide the ground shield into parts due to via holes; and as far as possible, do not allow variation in the wiring widths of a ground shield.

- When applying ground shields to differential wiring, take care with regard to the point that the ground shields being too close to the differential wiring is likely to have a strong effect on the differential combination.

  – In the wiring of a ground shield, its clearance must be at least twice the spacing of the wiring for the differential signals.

Connect long ground shield wiring runs to the ground layer at multiple points.

Via hole leading to the ground layer

Ground shield
Signal line
Ground shield

The width of the ground shield lines must be at least the same as that of the signal line.

Be sure to connect both sides of a ground shield to the ground layer.

When applying ground shields to differential signals, the spacing between the ground shield and signal must be at least twice that between the differential signal lines.

Differential signal lines

Ground shield

Allow at least twice the spacing between the differential signal lines.

When applying ground shields to high-speed signals, as far as possible avoid creating points at which the impedance changes.

Do not divide the ground shield into segments due to via holes.

X

High-speed signal line

X: No good

X

Do not change the spacing between the signal and ground shield.

Connect ground shield wiring runs to the ground layer at multiple points.

Do not leave a porti on of a solid ground pattern open-circuit.

X

Figure 6.4   Ground Shields/Guards

6.6   Ensuring Return Paths

Points   ALL

- A single-ended signal is propagated from a driver to a receiver through signal wiring, and a return current flows from the receiver to the driver at the same time. In such cases, the path along which the return current flows is referred to as a return path. The ground or power supply layer placed closest to the signal wiring serves as the return path in most cases. To retain signal quality and prevent problems before they arise, take the return paths into account in pattern design.

    - In most cases, return paths are just below the signal wiring.

    - The higher the speed of a signal, the more important taking return paths into account in pattern design to retain the signal quality becomes.

    - Take care that arranging via holes to change bus signal wiring runs from one layer to another does not create slits along the return paths.

    - Take care slits in the ground layer or clearance for use with via holes arranged horizontally do not divide the return paths into parts.

    - When a reference layer (ground layer) for use as a return path is changed, place a ground via hole in an appropriate location to avoid a detour from the original return path.

    - If insufficient via holes leading to the reference layer (ground layer) are present near locations where LSI signals are brought out or bus signals are propagated from one layer to another, etc., the flow of the return currents will be concentrated in a particular via hole, leading to the generation of noise such as crosstalk from the return paths. To avoid this, place a ground via hole in every one of several signal wiring runs near locations where signals are propagated from one layer to another.

    - For wiring patterns for circuits that are sensitive to noise such as crystal oscillation circuits, pay attention to the return paths of signals as well as the wiring patterns in the circuit diagram, such as in terms of parallel runs of signal wiring.

Return path

Signal wiring

Return path

Reference layer (ground layer)

The return path is through the reference layer (ground layer) just below the signal wiring.

Slit

Via holes + clearance (for a build-up board)

The return path crossing slits or via holes that have clearance forces it to make a detour. Such detours lower the quality of highspeed signals. If you cannot arrange the slits etc. in other locations, however, do apply a countermeasure such as having the signal wiring run make a detour.

Signal layer
Ground layer

Ground layer
Signal layer

When a signal is propagated from one layer to another and this leads to a change of the signal in the reference layer, the return current flows across layers through the ground via hole in the vicinity. Place a ground via hole near the location where the signal is propagated from one layer to another to avoid the return current having to make a long detour.

Flow of the return currents is concentrated in a single via hole.

Ground via hole

When there are many bus and other signals for which the reference layers are changed in wiring patterns and the number of ground via holes is insufficient, the flow of the return currents is concentrated in a single via hole. Place a ground via hole for each one of the several individual wiring runs in such patterns to balance the return currents.

Ground layer

When the wiring for a signal that is sensitive to noise is immediately above or below the return path, takecaree with regard to noise that the return current may apply to the signal.

Figure 6.5   Ensuring Return Paths

6.7 Designing Wiring Patterns when Using a Chip 3-Terminal Capacitor with a "Non-feedthrough" Connection

Points

ALL

- When a chip 3-terminal capacitor that does not have a feedthrough connection is used for its structural advantages, consideration of pattern design is important in bringing out its performance.

- For details, refer to the Web page of Murata Manufacturing Co., Ltd. and TDK Corporation.
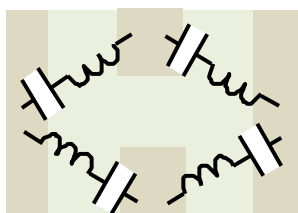
Equivalent structure of a chip 3-terminal capacitor

Via hole leading to the power supply plane

Via hole located nearest to a power supply ball of the LSI

Via hole leading to the ground plane

Via hole located nearest to a ground ball of the LSI

Via hole leading to the ground plane

Chip 3-terminal capacitor

Via hole located nearest to a power supply ball of the LSI

Via hole leading to the power supply plane
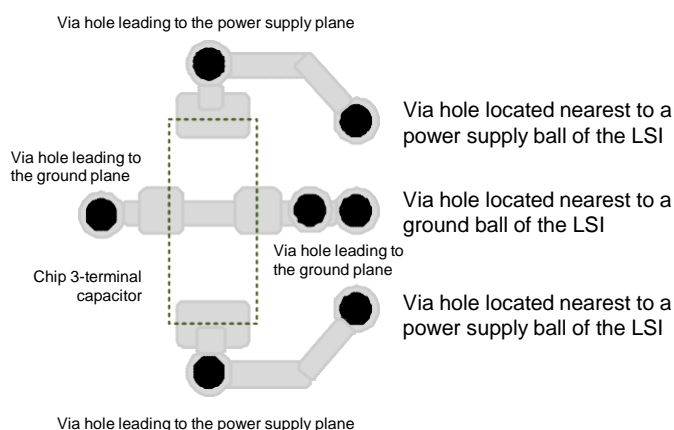
When using a chip 3-terminal capacitor that does not have a feedthrough connection, use a pair of ground via holes for both ground pins in the center to make more effective use of the four capacitors that are equivalently generated as bypass capacitors in terms of the internal structure.

Figure 6.6   Designing Wiring Patterns when Using a Chip 3-Terminal Capacitor with a "Non-feedthrough" Connection

6.8　Designing Wiring Patterns for High-Speed Interfaces

🔖 Points

ALL

- Guidelines for board development with regard to the DDR4/DDR3L, USB 2.0, CSI, and DSI are separately available and listed in the table below.

- Each guideline covers constraints, instructions, and guidance on the design of the related patterns on a PCB.

- Refer to these guidelines in pattern design.

- The guidelines also state reference documents from vendors other than Renesas and recommend referring to them. As these documents may also cover constraints, instructions, and guidance, refer to them together with the guidelines from Renesas.

Table 6.2　　　Guidelines Covering Descriptions Related to the Design of Wiring Patterns for High-Speed Interfaces

Interface	Guideline
DDR4, DDR3L	PCB design guideline for DDR4/DDR3L
	PCB verification guide for DDR4/DDR3L
LPDDR4, DDR4	PCB design guideline for LPDDR4/DDR4
	PCB verification guide for LPDDR4/DDR4
USB 2.0	PCB design guidelines for MIPI-CSI, MIPI-DSI, USB2.0, and PCI Express Gen2
CSI	
DSI	
PCIe	

6.9　Designing Wiring Patterns for Differential Signals

💡 Points	ALL

- RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, and RZ/A3UL products have several high-speed differential signal interfaces such as the USB modules.

- In differential interfaces in general, positive and negative signals are paired. This allows reduction of the signal amplitude and increases the immunity to common mode noise, thus allowing for higher-speed transfer.

- Wiring patterns for pairs of differential signals are required to make the best use of differential transfer.

- To avoid any problems arising later, consider modelling interface components such as components to be inserted and connectors in advance, and confirming the signal quality such as in terms of the deterioration of open eye patterns through simulation.

    1.   Wiring of differential pairs

- Design the wiring patterns for pairs of differential signals while basically maintaining the required isometry and parallelism without changes in the width and spacing of the wiring.

- As far as possible, that is, unless this presents a difficulty in terms of bringing the signal lines out or inserting any components for use as countermeasures for noise, place the wiring pairs for differential signals in the same layer.

- When the locations where the signal lines are brought out lead to differences in electrical length, as far as possible adjust the lengths by a measure before the location. Methods of adjustment include changing the direction in which the signals are brought out. Do not use meandering wiring.

- When a bend in a signal wiring run leads to a difference in electrical length, adjust the lengths to remove the difference by a measure as close as possible to the location where the difference was produced.

- Place components such as those for use as countermeasures for noise, via holes for use in interlayer routing, and ground shields as close to symmetrically as possible relative to the wiring runs of differential pairs.

- When you cannot avoid using meandering wiring to adjust the timing relative to that of other signals, ensure enough spacing of the meandering wiring relative to that of the other wiring for the differential pair.

    2.   Differential impedance

- Adjust the differential impedance to be roughly estimated as ±10% relative to the characteristic impedance specific to the given interface unless otherwise specified in the guideline or other documents for the given interface.

- Remove the ground layer immediately under the wiring for differential pairs as required to adjust the impedance. Take care that the wiring runs of differential pairs do not cross slits in the ground plane for use as the reference layer.

- When running the wiring for a differential pair from one layer to another, place a ground via hole near the via hole for the differential pair to suppress the generation of uneven impedances.

    3.   Taking peripheral wiring patterns into account

- When ground shields are not to be applied, the wiring for a differential pair and another signal must be separated from each other by at least five times the width of the signal wiring.

- When ground shields are to be applied, the wiring for a differential pair and for the ground shield must be separated from each other by at least twice the width of the signal wiring.

- When bending signal wiring runs, do not bend them through right angles but by no more than 45° (or at least 135°).

- When you cannot avoid using wiring patterns that lead to deterioration of the signal integrity (SI) of differential signals such as for test points, use as few as is possible.
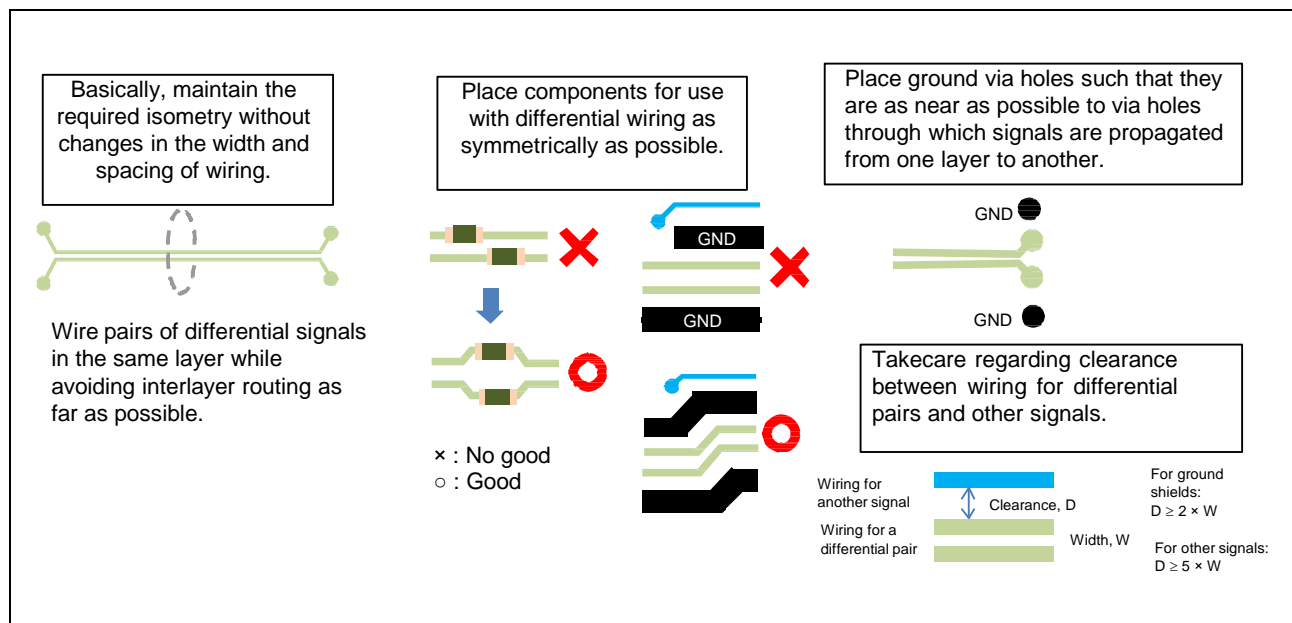
Figure 6.7   Designing Wiring Patterns for Differential Signals

6.10 Taking Suppression of Crosstalk into Account in the Design of Wiring Patterns

💡 Points

ALL
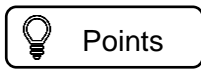
Especially in the case of wiring patterns for high-speed signals, deterioration of signal quality due to crosstalk affects timing design, and may also strongly affect signals that are sensitive to noise such as analog signals. Typical countermeasures for crosstalk are given below.

- For wiring patterns for single-ended signals, make the spacing between wiring runs as wide as possible, and take care not to arrange multiple wiring runs in parallel over long stretches.

- When multiple signal wiring runs are arranged in parallel over a long stretch in the case of the routing of buses or otherwise, apply countermeasures for crosstalk such as inserting ground signal wiring once every few wiring runs.

- Also, take care not to arrange wiring runs in parallel over long stretches in layers just above or below the wiring for high-speed signals.

- When using meandering wiring to adjust timing, take care that the meandering wiring itself is arranged correctly in terms of, e.g., the spacing.

- In pattern design where major adjustments of timing are required, verify how crosstalk affects the timing with the resulting wiring patterns through simulation to confirm that the patterns do not create a problem.

- When guidelines define constraints regarding wiring patterns such as spacing, follow the guidelines.

- When adjacent wiring is for signals that are sensitive to noise, ensure sufficient spacing, including for the respective return paths. Moreover, apply countermeasures such as the use of ground guards.

Signal wiring

Signal wiring

Spacing of wiring

Signal layer

Reference layer

Distance between layers, d

Spacing of wiring > d × 3

The reference spacing of signal wiring is set according to the distance from the solid ground layer or other layer that is just below the signal layer and serves as the reference layer and to the frequencies of the signals. For wiring patterns for high-speed signals, the standard spacing is at least three times the distance from the reference plane in most cases.

Signal layer

Signal layer

Reference layer

Spacing of wiring
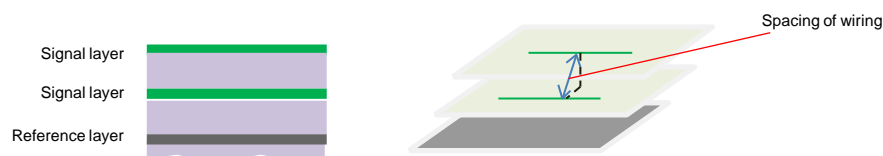
The reference spacing of signal wiring is set according to the distance from the solid ground layer or other layer that is just below the signal layer and serves as the reference layer and to the frequencies of the signals. For wiring patterns for high-speed signals, the standard spacing is at least three times the distance from the reference plane in most cases.

Spacing of wiring

The concept mentioned above also applies to wiring patterns using meandering wiring for timing adjustment. Ensure that spacing between adjacent wiring runs is sufficient.

Figure 6.8   Taking Suppression of Crosstalk into Account in the Design of Wiring Patterns

6.11 Designing Wiring Patterns for Use in Monitoring High-Speed Signals

⟨ Points ⟩
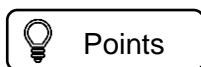
ALL

Separate design guidelines are available regarding wiring patterns for use in connection with DDR4-SDRAM and for interfaces such as USB2.0, CSI, DSI, and PCIe. In such cases, basically follow the respective guidelines for pattern design. When placing pads for monitoring high-speed signals, take care on the following points.

- Place one side of the pad on the signal line so that the stub lengths are as short as possible.

- Place a ground pad near the monitoring point if this is possible. When placing a ground pad in a ground shield, take care that slits in the shield and so on do not change the impedance.

- When the target for monitoring is a pair of differential signals, place the components including ground pads for use in monitoring symmetrically relative to the wiring runs of the differential pair.

- For monitoring a high-speed signal, select a monitoring point that suits the aims of the monitoring, such as close to the receiving terminal.

- When you proceed with simulation to check signal integrity (SI), do so with the inclusion of a pad for use in monitoring. Note that the signals monitored from the pad and at the receiving terminal will not perfectly match. The simulation of monitoring waveforms on the pad may be used to extrapolate those at the receiving terminal in later evaluation of the waveforms.
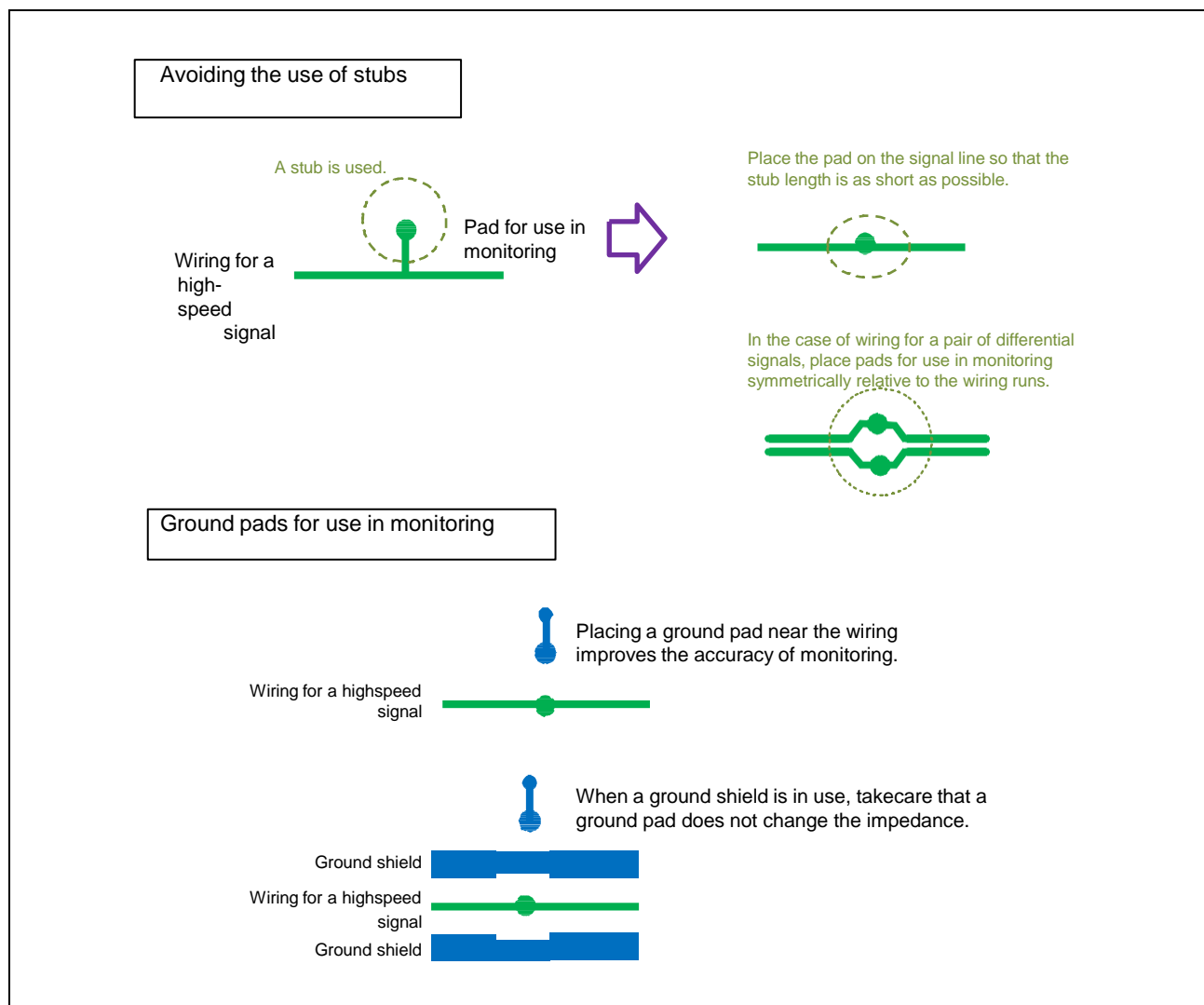
Figure 6.9   Wiring Patterns for Use in Monitoring High-Speed Signals

6.12   Designing Wiring Patterns for Signals (General Notes)

Points

ALL

- General notes on designing wiring patterns for signals are given below.
  When the wiring patterns for a circuit can be predicted to have a relatively strong effect on the signal quality, we recommend stating this as a note on the circuit diagram to aid in avoiding wiring patterns that are not as intended.

  - For wiring patterns for relatively high-speed signals, avoid the use of stubs or branching of the wiring and make the wiring lengths as short as possible.

  - For wiring patterns for clock signals, take care that elements such as reflections due to stubs or branches of the wiring and waveform rounding on rising or falling edges due to long wiring runs do not lead to excessive deterioration in the quality of the clock signals.

  - When stubs are used in wiring of circuits for mode settings, external pulling up or pulling down, and filtering, make the stubs as short as possible.

  - When bending wiring runs is not avoidable, do not bend them through a right angle but through 45° to avoid sudden changes in the impedance of the wiring. Especially for wiring patterns for high-speed signals, apply countermeasures such as rounding the wiring runs at the corners or using curved wiring to retain the signal quality.

  - As far as possible, bring signal lines out near an LSI chip to take reflections of the signals at via holes into account. Moreover, keep the main wiring in the same layer.

  - For wiring patterns for parallel synchronous signals such as in routing for a bus, use the same layer and employ isometric wiring.

  - When using different layers for wiring patterns for parallel synchronous signals such as in routing for a bus is not avoidable, especially when an inner layer and the surface layer are used, simulate signal propagation and confirm that the delay times are the same on the bus as a whole. Adjust the wiring if this is not the case.

  - For a circuit that has a record of unsuccessful operation, we recommend applying countermeasures for improving the monitoring performance in confirming its operation such as mainly using the surface layer for wiring patterns or the setting of test points.

  - For wiring patterns for a crystal oscillation circuit, take care on the following points in general:
    place the wiring patterns such that they are as near as possible to the LSI chip;
    place the wiring patterns such that they are not too close to other patterns, including the digital ground, in the layer where the wiring patterns are placed and those above and below it;
    as far as possible, remove the ground layer just below wiring patterns;
    place the wiring patterns such that they are not too near to wiring for input or output; and apply load capacitance with the connection to the same ground.

  - For wiring patterns for a crystal oscillation circuit, if the LSI vendor provides a recommended layout of patterns on a PCB, follow the recommendation.

6.13 Placing Components that Serve as Countermeasures for Noise

💡 Points

ALL

- The inappropriate placement of components that serve as countermeasures for noise may prevent them being sufficiently effective and may even lead to their having the opposite effect to that which was intended.

- Even if the connection information such as for parallel circuits is the same as that in the net list, take care in terms of the order of connection and the method of connection to other circuits with grounds or power supplies possibly being important.

- State constraints and conditions on pattern design as notes on the circuit diagram as far as possible to avoid wiring patterns that are not as intended.

- Reference documents such as datasheets or design guidelines for the given LSI chip cover the recommended layout of patterns and constraints on the methods of connection. Follow the recommendations and apply the constraints.

Examples

- Place a common mode noise filter or component that serves as a countermeasure for electro-static discharge (ESD) nearest to its potential entry point, that is, the connector for use in connecting an external device.

- Place a damping resistor such that the resistor is as near as possible to the sending terminal, while placing a parallel terminating resistor such that the resistor is as near as possible to the receiving terminal.

- Connect a parallel or differential terminator after a wiring run passes through an input point to the IC to avoid the use of stubs as far as possible.

- Place a current reference resistor adjacent to the LSI chip to avoid lengthening the wiring run.

- Place bypass capacitors with a smaller capacitance nearer the given LSI power supply.

- Connect wiring runs for the reference voltage and remote sensing for a switched-mode power supply through a smoothing capacitor to a location where the ripple generated in the power supply line will be sufficiently small.

- For wiring patterns for filter circuits such as resistor–capacitor (RC) filters, connect the components in the order that provides the greatest effectiveness. Specifically, in a case where an RC filter is used to reduce noise in an IC input, connect the wiring run to the IC input pin through a resistor and capacitor, in that order.

- Connect a filter circuit to ground at one point if doing so makes it more effective.

7. Check List

Table 7.1   Check List

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
										Section in the Application Note for Reference		**Link**
1	PRST#	Is a 3.3-V signal applied to the PRST# signal?	Y	Y	Y	Y	Y	Y	Y	1	1.1	
2	PRST#	Is the logic of signals (such as JTAG) used in generating PRST# for the RZ/G2L correct?	Y	Y	Y	Y	Y	Y	Y	1	1.1	
3	PRST#	Did you neglect pulling up the open drain output in the PRST# generation circuit?	Y	Y	Y	Y	Y	Y	Y	1	1.1	
4	PRST#	For the value of the pull-up resistor for the PRST# signal, we recommend the use of a pull-up resistor with a value no greater than 10kΩ.	Y	Y	Y	Y	Y	Y	Y	1	1.1	
5	PRST#	When using an open-drain wired OR connection configuration in the PRST# generation circuit, is the pull-up resistor immediately before input to targeted devices only connected to 1.8 V?	Y	Y	Y	Y	Y	Y	Y	1	1.6	
6	PRST#	When PRST# is used to reset a peripheral device, is a Schmitt trigger input used on the receiving side?	Y	Y	Y	Y	Y	Y	Y	1	1.1 1.6	
7	PRST#	Did you confirm that there is no problem with the voltage, active sense, and external or internal pulling up and down of the signals used in producing PRST#?	Y	Y	Y	Y	Y	Y	Y	1	1.6	
8	PRST#	Have you taken sufficient measures such as the use of ground shields for PRST# and the signals used in producing PRST#?	Y	Y	Y	Y	Y	Y	Y	1	1.6	
9	PRST#	In the power-on sequence, is the PRST# signal kept at the low level for at least a further 100 ns after all power supplies have been turned on?	Y	Y	Y	Y	Y	Y	Y	1	1.2	
10	PRST#	In the power-off sequence, is the PRST# signal at the low level before the first power supply is turned off?	Y	Y	Y	Y	Y	Y	Y	1	1.2	
11	PRST#	When a cold reset is applied by a reset switch during operation, will the PRST# signal always be asserted for at least 1 ms?	Y	Y	Y	Y	Y	Y	Y	1	1.2	
12	Others related to reset	When PRST#, QSPI_RESET#, DDR_RESET# or SD0_RST# are used to reset a peripheral device, is the target peripheral device turned on?	Y	Y	Y	Y	Y	Y	Y	1	1.4	
13	Others related to reset	When PRST#, QSPI_RESET#, DDR_RESET# or SD0 _RST# are used to reset a peripheral device, are the voltage and active sense of reset input for the target peripheral device correct?	Y	Y	Y	Y	Y	Y	Y	1	1.4	

#	Item	Point to Check	Section in the Application Note for Reference							Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	
14	Others related to reset	When PRST#, QSPI_RESET#, DDR_RESET# or SD0_RST# are used to reset a peripheral device, is the reset input for the target peripheral device set in consideration of the possible presence of an internal pull-up or pull-down resistor?	Y	Y	Y	Y	Y	Y	Y	1	1.4	
15	Others related to reset	When PRST#, QSPI_RESET#, DDR_RESET# or SD0_RST# are used to reset peripheral devices, is the driving ability of the reset signal sufficient?	Y	Y	Y	Y	Y	Y	Y	1	1.4	
16	Others related to reset	Is PRST# connected to specific peripheral devices for which targeted devices have dedicated reset pins (such as QSPI_RESET#, DDR_RESET#, and SD0_RST#)?	Y	Y	Y	Y	Y	Y	Y	1	1.4	
17	Others related to reset	When a GPIO output is used to reset a peripheral device, is the circuit configured in consideration of the GPIO outputs of the RZ/G2L being Hi-Z from startup until setting of the PFC?	Y	Y	Y	Y	Y	Y	Y	1	1.4	
18	Others related to reset	Is the JTAG reset such as TRST# level-shifted to 1.8 V to get the logical AND for PRST#?	Y	Y	Y	Y	Y	Y	Y	1	1.5	
19	Others related to reset	Did you include resets in the time chart of the power-on and -off sequences for the entire power tree, and then confirm that there were no problems with the timing of the resets?	Y	Y	Y	Y	Y	Y	Y	3	3.3	
20	MD pin setting	Did you check whether the connected device has an internal pull-up or pull-down resistor to maintain correct operation when the MD pin signal returns to its primary function?	Y	Y	Y	Y	Y	Y	Y	1	1.7	
21	MD pin setting	Are the external pull-up and pull-down resistance values for setting the MD pin selected in consideration of the internal pull-up and pull-down resistors of targeted devices and peripheral devices?	Y	Y	Y	Y	Y	Y	Y	1	1.7	
22	MD pin setting	Does the peripheral device malfunction due to external pull-up or pull-down for setting the MD pin?	Y	Y	Y	Y	Y	Y	Y	1	1.7	
23	MD pin setting	Is the MD pin setting confirmed to keep the level for 100 ns or less after PRST # = H change?	Y	Y	Y	Y	Y	Y	Y	1	1.7	
24	EXCLK	When inputting external oscillation clock to EXCLK, release PRST# Is the oscillation stable?	Y	Y	Y	Y	Y	Y	—	2	2.5	
25	EXCLK	"When the IO voltage level of the external clock input to EXCLK is Exceeds 3.3V IO power supply voltage level during power supply ON / OFF sequence Isn't it?"	Y	Y	Y	Y	Y	Y	—	2	2.5	
26	EXCLK	When an external clock is input to EXCLK, its voltage level is 3.3 V?	Y	Y	Y	Y	Y	Y	—	2	2.5	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
			Section in the Application Note for Reference							Link		
27	EXCLK	If an external clock signal is to be input to the EXCLK pin is the XOUT pin open-circuit? Is the XIN pin pull-down?	Y	Y	Y	Y	Y	Y	—	2	2.5	
28	XIN/EXCLK	If targeted devices are the XIN/EXCLK frequency correct? That is, the allowable values is only 24 MHz.	Y	Y	Y	Y	Y	Y	Y	2	2.2	
29	AUDIO_CLK1/2	If an external clock signal is being input to the AUDIO_CLK1/2 pin of targeted devices is the voltage 3.3 V?	Y	Y	Y	Y	Y	Y	Y	2	2.1	
30	Clock input	Is the clock frequency input to the RZ/G2L appropriate for the purpose?	Y	Y	Y	Y	Y	Y	Y	2	2.2	
31	Clock input	Do the accuracy and deviation of the clock input to the RZ/G2L conform to the electrical characteristics?	Y	Y	Y	Y	Y	Y	Y	2	2.3	
32	Clock input	Do the accuracy and deviation of the clock input to targeted devices conform to the recommended values stated in the guidelines?	Y	Y	Y	Y	Y	Y	Y	2	2.3	
33	High-speed serial clock	Is the clock input signal for the high-speed serial interface from a non-SSC type oscillator?	Y	Y	Y	Y	Y	Y	Y	4	4.15	
34	X'tal circuit	Do you include patterns for a damping resistor or feedback resistor that might be necessary for evaluating the oscillation of a crystal resonator?	Y	Y	Y	Y	Y	Y	Y	2	2.4	
35	X'tal circuit	Do the circuit constants for the crystal resonator match the constants of the crystal resonator in use?	Y	Y	Y	Y	Y	Y	Y	2	2.4	
36	X'tal circuit	Have you considered the notes in the circuit design guideline for the crystal resonator in use?	Y	Y	Y	Y	Y	Y	Y	2	2.4	
37	X'tal circuit	Is the crystal resonator free of oscillation in the unwanted overtone mode?	Y	Y	Y	Y	Y	Y	Y	2	2.4	
38	X'tal circuit	Have you confirmed that the selected crystal resonator manufacturer supports the evaluation of oscillation?	Y	Y	Y	Y	Y	Y	Y	2	2.4	
39	Others related to clock	Did you pay equal attention to the clock input to peripheral devices and targeted devices?	Y	Y	Y	Y	Y	Y	Y	2	2.8	
40	Others related to clock	Did you pay equal attention to the connection of crystal resonators to peripheral devices and targeted devices?	Y	Y	Y	Y	Y	Y	Y	2	2.8	
41	Others related to clock	Did you follow the general notes in the guidelines for the connection of clocks to targeted devices and peripheral devices?	Y	Y	Y	Y	Y	Y	Y	2	2.8	
42	Others related to clock	Did you include instructions on ground shielding, such as in the wiring layers for PCB pattern design, in the circuit diagram for clock connections and clock wiring?	Y	Y	Y	Y	Y	Y	Y	2	2.8	
43	Power supply	Did you check the power tree for the required power consumption and whether the power supply circuit has sufficient capacity?	Y	Y	Y	Y	Y	Y	Y	3	3.1	

| # | Item | Point to Check | Section in the Application Note for Reference | | | | | | | Link | | Check |
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	
44	Power supply	When using targeted devices in the development phase, are you designing the power supply capacity with a margin in consideration of possible increase in current drawn?	Y	Y	Y	Y	Y	Y	Y	3	3.1 3.2	
45	Power supply	For the logic power supply, have you considered the likely average current drawn in terms of the electrical characteristics? Additionally, does the limit on current of the power supply IC allow a sufficient margin to provide the estimated current?	Y	Y	Y	Y	Y	Y	Y	3	3.1 3.2	
46	Power supply	When lowering the estimated current for the logic power supply according to a use case, have you confirmed that the use case is reasonable?	Y	Y	Y	Y	Y	Y	Y	3	3.1 3.2	
47	Power supply	Have you placed a sufficient number of 0.1 to 10 µF capacitors in the power supply circuit to handle sudden surges in the logic power supply?	Y	Y	Y	Y	Y	Y	Y	3	3.2	
48	Power supply	If you are using a switched-mode power supply for the logic power supply, have you confirmed that the switching frequency is capable of following the variations in load?	Y	Y	Y	Y	Y	Y	Y	3	3.8	
49	Power supply	Does the circuit configuration conform to the power-on and -off sequences?	Y	Y	Y	Y	Y	Y	Y	3	3.3	
50	Power supply	Did you create a time chart of the power-on and -off sequences for the entire power tree, and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	3	3.3	
51	Power supply	Did you create a time chart of special conditions, such as the time of the first power-on, for the power-on and -off sequences of the entire power tree, and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	3	3.3	
52	Power supply	Is there any circuit that may cause damage when the power of targeted devices is being switched on or off, such as pulling up at the power supplies of peripheral devices?	Y	Y	Y	Y	Y	Y	Y	3	3.3	
53	Power supply	Are there enough discharge circuits for power-off to conform to the power supply sequence?	Y	Y	Y	Y	Y	Y	Y	3	3.3	
54	Power line filter	Have you selected and installed filters as recommended in the guidelines for power supply filter circuits to take account of the noise-sensitivity of dedicated power supplies?	Y	Y	Y	Y	Y	Y	Y	3	3.4	
55	Power line filter	Is the noise filter for the CPG PLL power supply one provided in the guidelines?	Y	Y	Y	Y	Y	Y	Y	3	3.4	
56	Power line filter	Have the noise filters for individual power supplies not been merged?	Y	Y	Y	Y	Y	Y	Y	3	3.4	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
			Section in the Application Note for Reference							Link		
57	Power line filter	As well as targeted devices, have you selected and installed filter circuits as recommended in the datasheet or technical documentation for peripheral devices?	Y	Y	Y	Y	Y	Y	Y	3	3.4	
58	Power circuit	Did you analyze the impedances of the VDD power supplies by applying the method stated in the guidelines and confirmed that there were no problems?	Y	Y	Y	Y	Y	Y	Y	3	3.5	
59	Power circuit	Did you analyze the impedance of the DRAM IO power supply by applying the method stated in the guidelines and confirmed that there were no problems?	Y	Y	Y	Y	Y	Y	Y	3	3.5	
60	Power circuit	Have multiple DRAM IO power supply systems not been merged to act as a single power supply?	Y	Y	Y	Y	Y	Y	Y	3	3.5	
61	Power circuit	Did you analyze the inductance of the dedicated power supply for high-speed serial interfaces and IO power supply by applying the method stated in the guidelines and confirmed that there were no problems?	Y	Y	Y	Y	Y	Y	Y	3	3.5	
62	Power circuit	As well as targeted devices, did you analyze the power supply impedances of peripheral devices that came with recommendations on this point, and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	3	3.5	
63	Bypass capacitor	Did you install the appropriate number and capacity of bypass capacitors for the IO power supply?	Y	Y	Y	Y	Y	Y	Y	3	3.6	
64	Bypass capacitor	Did you install bypass capacitors in consideration of simultaneous-switching output noise SSO, such as placing capacitors with large capacitances of about 10 μF at the end of the IO power supply pattern?	Y	Y	Y	Y	Y	Y	Y	3	3.6	
65	Bypass capacitor	Did you include instructions regarding the PCB pattern in the circuit diagram, such as the placement of capacitors with small capacitances near the device?	Y	Y	Y	Y	Y	Y	Y	3	3.6	
66	Bypass capacitor	Did you consider bypass capacitors for peripheral devices as well as for targeted devices?	Y	Y	Y	Y	Y	Y	Y	3	3.6	
67	Bypass capacitor	Do the bypass capacitors have sufficient capacity in consideration of the decrease in the effective capacitance due to variations in DC bias and temperature?	Y	Y	Y	Y	Y	Y	Y	3	3.7	
68	Bypass capacitor	Is the value of the bypass capacitor for the power supply circuit of the high-speed serial interface as recommended in the guide?	Y	Y	Y	Y	Y	Y	Y	4	4.18	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
			Section in the Application Note for Reference							**Link**		
69	Bypass capacitor	If aluminum electrolytic capacitors are to be used as bypass capacitors, have you taken measures in the silk-screened markings or pattern design to prevent insertion with reverse polarity?	Y	Y	Y	Y	Y	Y	Y	5	5.25	
70	Power-IC circuit	Does the design conform to the recommended circuit provided in the datasheet or technical documentation of the power supply IC in use?	Y	Y	Y	Y	Y	Y	Y	3	3.8	
71	Power-IC circuit	Do the components for the selected power supply circuit, such as coils, FETs, and diodes, correspond to the power supply specifications?	Y	Y	Y	Y	Y	Y	Y	3	3.8	
72	Power-IC circuit	Did you include typical characteristics regarding the selection of peripheral components for the power supply IC in the circuit diagram?	Y	Y	Y	Y	Y	Y	Y	3	3.8	
73	Power-IC circuit	Does the design take the allowable losses and heat dissipation into account?	Y	Y	Y	Y	Y	Y	Y	3	3.8	
74	Power-IC circuit	Have you confirmed that the phase margin and gain margin of the power supply sufficient?	Y	Y	Y	Y	Y	Y	Y	3	3.8	
75	Power-IC circuit	Did you place the remote sensing pin of the power supply IC in the vicinity of the load? Additionally, did you include instructions on PCB pattern design in the circuit diagram to avoid degradation of the power quality due to noise?	Y	Y	Y	Y	Y	Y	Y	3	3.9	
76	Power pin on CN	Do the numbers of power pins and FGND pins allow margins for the maximum current when power is being supplied via a connector?	Y	Y	Y	Y	Y	Y	Y	3	3.1	
77	Power pin on CN	Is a capacitor with a relatively large capacitance installed near the connector when power is being supplied via a connector?	Y	Y	Y	Y	Y	Y	Y	3	3.1	
78	SDHI power circuit	Did you take care to prevent the SD card power supply adversely affecting other power supplies when it is turned on or off?	Y	Y	Y	Y	Y	Y	Y	3	3.11	
79	SDHI power circuit	When the SD card power supply is controlled by the pin of targeted devices, does the configuration take into account the fact that the pin becomes Hi-Z when the power pin on the targeted devices side is initially turned on?	Y	Y	Y	Y	Y	Y	Y	3	3.11	
80	SDHI power circuit	Does the bypass capacitor for the SD card interface have a proven capacitance?	Y	Y	Y	Y	Y	Y	Y	3	3.11	
81	SDHI power circuit	Did you check that the SD card power supply being turned on while the power of targeted devices is off and IO pins are being pulled up does not violate the ratings?	Y	Y	Y	Y	Y	Y	Y	3	3.11	
82	SDHI power circuit	Is a discharge circuit prepared for the SD card power supply?	Y	Y	Y	Y	Y	Y	Y	3	3.11	

#	Item	Point to Check	Section in the Application Note for Reference							Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	
83	SDHI power circuit	Have you confirmed that no excessive voltage occurs when the voltage is changed in the SDHI IO power supply switching circuit?	Y	Y	Y	Y	Y	Y	Y	3	3.12	
84	LPDDR4/DDR4/ DDR3L SDRAM	Is the connected DRAM supported by targeted devices?	Y	Y	Y	Y	Y	Y	Y	4	4.1	
85	LPDDR4/DDR4/ DDR3L SDRAM	Did you perform SI verification, timing verification, and PI verification for the connection between targeted devices and DRAM according to the guidelines?	Y	Y	Y	Y	Y	Y	Y	4	4.2	
86	LPDDR4/DDR4/ DDR3L SDRAM	Is the DRAM to be used a product type (model) for which SI verification, timing verification, and PI verification have been completed?	Y	Y	Y	Y	Y	Y	Y	4	4.3	
87	LPDDR4/DDR4/ DDR3L SDRAM	Do the circuits for signal termination and ZQ pin handling follow the recommendations in the guidelines?	Y	Y	Y	Y	Y	Y	Y	4	4.5	
88	LPDDR4/DDR4/ DDR3L SDRAM	Have you confirmed the selection of an appropriate DRAM connection topology?	Y	Y	Y	Y	Y	Y	Y	4	4.4	
89	DDR4/DDR3L SDRAM	Is the configuration of the VREF circuit for DDR4 or DDR3L SDRAM appropriate?	Y	Y	Y	Y	Y	Y	Y	4	4.6 4.7	
90	DDR4/DDR3L SDRAM	In designing the resistive division circuit to obtain VREF for DDR4 or DDR3L SDRAM, was the input current of the IC taken into consideration when selecting the resistor values?	Y	Y	Y	Y	Y	Y	Y	4	4.6 4.7	
91	DDR4/DDR3L SDRAM	In designing the resistive division circuit to obtain VREF for DDR4 or DDR3L SDRAM, is VREF generated independently for each VREF pin?	Y	Y	Y	Y	Y	Y	Y	4	4.6 4.7	
92	DDR4/DDR3L SDRAM	Is there any error in the tolerance of the resistor connected to the ZQ pin of the RZ/G2L and DRAM, and in the destination for connection (power supply or GND)?	Y	Y	Y	Y	Y	Y	Y	4	4.8	
93	DDR3L SDRAM	Have the restrictions described in this guideline been applied to pin swapping of the CA and DQ pins when targeted devices are connected to DDR3L SDRAM?	Y	Y	Y	Y	Y	Y	—	4	4.9	
94	DDR4 SDRAM	Have the restrictions described in this guideline been applied to pin swapping of the CA and DQ pins when targeted devices are connected to DDR4 SDRAM?	Y	Y	Y	Y	Y	Y	Y	4	4.10	
95	LPDDR4 SDRAM	Have the restrictions described in this guideline been applied to pin swapping of the CA and DQ pins when targeted devices are connected to LPDDR4 SDRAM?	—	—	—	—	—	—	Y	4	4.11	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
						Section in the Application Note for Reference					Link	
96	LPDDR4/DDR4/ DDR3L SDRAM	Have the DDR3L, DDR4 or LPDDR4 power supply sequence been applied when targeted devices are connected to DDR3L, DDR4 or LPDDR4 SDRAM?	Y	Y	Y	Y	Y	Y	Y	4	4.1	
97	High-speed serial IF	Does the design of the high-speed serial interface follow the restrictions and recommendations described in the guidelines?	Y	Y	Y	Y	Y	Y	Y	4	4.13	
98	High-speed serial IF	Did you check the +E118 accuracy and temperature coefficients of the components for connection to the high-speed serial interface?	Y	Y	Y	Y	Y	Y	Y	4	4.13	
99	High-speed serial IF	Is a coupling capacitor inserted for the transmission-side signal line of the high-speed serial interface?	—	—	—	—	—	—	Y	4	4.16	
100	High-speed serial IF	Did you include the restrictions and recommendations for the high-speed serial interface signal described in the guidelines in the circuit diagram?	Y	Y	Y	Y	Y	Y	Y	4	4.15	
101	High-speed serial IF	When you prepare a pad for observing signals, is the circuit configured such that doing so does not degrade the signal quality?	Y	Y				Y	Y	4	4.16	
102	High-speed serial IF	If the signal observation point is different from the end point for specifying the signal quality, have you performed the required simulation to examine the difference to prepare for later evaluation?	Y	Y	Y	Y	Y	Y	Y	4	4.16	
103	High-speed serial IF	Did you take appropriate measures against signal ESD and noise? Additionally, did you include instructions for the placement of these countermeasure components on the PCB in the circuit diagram?	Y	Y	Y	Y	Y	Y	Y	4	4.18	
104	USB	Is the USBn_OVRCUR# (n = 0, 1) input level-shifted to 3.3-V signal?	Y	Y	Y	Y	Y	Y	Y	4	4.19	
105	USB	Is a 1-kΩ series resistor inserted in the VBUS input?	Y	Y	Y	Y	Y	Y	Y	4	4.19	
106	USB	Is USBn_VBUSEN (n = 0, 1) for the USB power circuit active high?	Y	Y	Y	Y	Y	Y	Y	4	4.20	
107	eMMC	Did you check the speed grade of the eMMC to be connected?	Y	Y	Y	Y	Y	Y	Y	5	5.9	
108	eMMC	Did you confirm that the external pulling up and down of the eMMC signal lines does not violate the eMMC standard?	Y	Y	Y	Y	Y	Y	Y	5	5.10	
109	eMMC	If the eMMC is set as the boot device, did you confirm that resetting of the eMMC was released before the start of booting up the targeted devices?	Y	Y	Y	Y	Y	Y	Y	5	5.10	
110	SPI Multi I/O I/F	Did you confirm that the connection of the QSPI flash memory and HyperFlash memory (Target: RZ/G2L, RZ/G2LC, and RZ/V2L) is correct?	Y	Y	Y	Y	Y	Y	Y	5	5.11	
111	SPI Multi I/O I/F	Is the QSPI CS# signal being pulled up to the 1.8 or 3.3-V supply?	Y	Y	Y	Y	Y	Y	Y	5	5.11	
112	SPI Multi I/O I/F	Are the CS#, INT#, and RESET# signals of HyperFlash memory being pulled up to the 1.8-V supply?	Y	Y	Y	—	—	—	—	5	5.11	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
			Section in the Application Note for Reference								Link	
113	xSPI	Did you confirm that the connection of the QSPI flash memory and OctaRAM is correct?	—	—	—	—	—	—	Y	5	5.12	
114	xSPI	Is the QSPI CS# signal being pulled up to the 1.8 or 3.3-V supply?	—	—	—	—	—	—	Y	5	5.12	
115	SDHI IF	Did you confirm that the destination for pulling up the CD and WP signals of the SD card interface is the system power supply (3.3 V)?	Y	Y	Y	Y	Y	Y	Y	5	5.13	
116	SDHI IF	Did you confirm that the destination for pulling up the signals (other than CD and WP) of the SD card interface is the SDHI IO power supply?	Y	Y	Y	Y	Y	Y	Y	5	5.14	
117	JTAG	Did you confirm the pull-up/pull-down processing of each signal?	Y	Y	Y	Y	Y	Y	Y	5	5.16	
118	RGMII, MII	Is the connection to the Ethernet PHY properly performed with reference to the contents of the application notes?	Y	Y	Y	Y	Y	Y	Y	5	5.15	
119	I2C	Is the internal pull-up of the LSI being used to pull the I2C signal lines up?	Y	Y	Y	Y	Y	Y	Y	5	5.17	
120	I2C	Did you confirm that the I2C with an LVTTL-type buffer being pulled up when 5.0-V is applied?	Y	Y	Y	Y	Y	Y	Y	5	5.17	
121	I2C	Is the I2C of an open-drain type buffer is being pulled up with 3.3-V?	Y	Y	Y	Y	Y	Y	Y	5	5.17	
122	I2C	When the IO power for targeted devices is not turned on, has the power supply for the destination for pulling the I2C signal lines up being turned on been avoided?	Y	Y	Y	Y	Y	Y	Y	5	5.17	
123	I2C	Has any slave address conflict between the I2C device been avoided? Did you include the slave addresses in the circuit diagram as a supplement for software design and so on?	Y	Y	Y	Y	Y	Y	Y	5	5.18	
124	SPI/RSPI	Is the signal connection between targeted devices and SPI device correct?	Y	Y	Y	Y	Y	Y	Y	5	5.19	
125	SCIF	Have you decided whether to use an external or internal SCIF clock? If you chose to use an external SCIF clock, is the clock at an appropriate frequency input?	Y	Y	Y	Y	Y	Y	Y	5	5.20	
126	AUDIO AOUT	If you will be using aluminum electrolytic capacitors as coupling capacitors for audio analog output, is the polarity correct?	Y	Y	Y	Y	Y	Y	Y	5	5.2	
127	Others	Is the handling of unused pins of targeted devices in accord with the statements on the handling of unused pins in the hardware manual?	Y	Y	Y	—	—	—	—	5	5.1	
128	Others	As well as targeted devices, is the handling of unused pins of peripheral devices in accord with the statements on the handling of unused pins in the hardware manual?	Y	Y	Y	—	—	—	—	5	5.1	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
			Section in the Application Note for Reference							Link		
129	Others	Did you provide circuits, such as damping and parallel termination, as countermeasures on circuits for interfaces where signals may undershoot or overshoot?	Y	Y	Y	Y	Y	Y	Y	5	5.2	
130	Others	Did you consider the risk of interfaces where signals may undershoot or overshoot by checking the component specifications and simulating transmission?	Y	Y	Y	Y	Y	Y	Y	5	5.2	
131	Others	Did you confirm that there is no problem with the voltage of all the signals connected to targeted devices?	Y	Y	Y	Y	Y	Y	Y	5	5.3	
132	Others	Did you confirm sufficient AC and DC margins for the connections between targeted devices and peripheral devices?	Y	Y	Y	Y	Y	Y	Y	5	5.4	
133	Others	Did you provide circuits as countermeasures on connections between targeted devices and peripheral devices for which AC and DC margins may be insufficient?	Y	Y	Y	Y	Y	Y	Y	5	5.4	
134	Others	Did you check all internal pull-up and pull-down resistors of targeted devices and peripheral devices, and apply measures in the form of external circuits to prevent the generation of intermediate potentials due to contention between pulling up and down?	Y	Y	Y	Y	Y	Y	Y	5	5.5	
135	Others	For relatively high-speed parallel IO interfaces such as QSPI and VIN/VOUT, did you include instructions on pattern design in the circuit diagram, such as instructions regarding equal lengths and delays, and stating the wiring layers?	Y	Y	Y	Y	Y	Y	Y	5	5.6	
136	Others	For relatively high-speed parallel IO interfaces such as QSPI and VIN/VOUT, did you confirm that there is no problem with the signal quality by simulating transmission?	Y	Y	Y	Y	Y	Y	Y	5	5.6	
137	Others	When connecting a relatively high-speed parallel IO interfaces such as QSPI and VIN/VOUT through a connector, did you prepare a sufficient number of ground pins to secure the return path?	Y	Y	Y	Y	Y	Y	Y	5	5.6	
138	Others	When targeted devices and peripheral devices are connected, did you confirm that Hi-Z input does not occur even in specific situations such as resets, and that there will be no problems even if Hi-Z input does occur?	Y	Y	Y	Y	Y	Y	Y	5	5.7	
139	Others	When targeted devices and peripheral devices are connected, did you confirm that output signals are not directly connected even in specific situations such as resets?	Y	Y	Y	Y	Y	Y	Y	5	5.7	
140	Others	Is the polarity of the aluminum electrolytic capacitors used in the power supply circuits and peripheral circuits correct?	Y	Y	Y	Y	Y	Y	Y	5	5.22	

#	Item	Point to Check	G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	Section	Sub section	Check
										Section in the Application Note for Reference		Link
141	Others	In a circuit configuration where power is partially turned on to operate the board, such as EEPROM programming, has application of the high level to devices that are not turned on, such as targeted devices, been avoided?	Y	Y	Y	Y	Y	Y	Y	5	5.23	
142	Others	Are the connectors correctly arranged in terms of male and female matching?	Y	Y	Y	Y	Y	Y	Y	5	5.24	
143	Others	Are the pin 1 positions of the connectors correct?	Y	Y	Y	Y	Y	Y	Y	5	5.24	
144	Others	Did you include a pattern diagram in the circuit diagram to specify the positions and arrangements of pin 1 of each of the connectors?	Y	Y	Y	Y	Y	Y	Y	6	5.24	
145	Others	When the RZ/G2L is turned off, have you ensured that an expansion board device connected through a connector does not output a high-level signal, and that pull-up resistors are not connected?	Y	Y	Y	Y	Y	Y	Y	5	5.24	
146	Others	Did you provide fail safes to prevent the reverse insertion of connectors?	Y	Y	Y	Y	Y	Y	Y	5	5.24	
147	Others	Does the circuit that has been created match the revision of targeted devices to be installed?	Y	Y	Y	Y	Y	Y	Y	5	5.25	
148	Others	If the circuit is an adaptation of a previous design, did you review the circuit configuration and the revision of the installed device, and confirm which parts of the circuit raise no problem in being used as is?	Y	Y	Y	Y	Y	Y	Y	5	5.26	
149	Others	Is the NC pin of targeted devices and peripheral devices properly handled?	—	—	—	Y	Y	—	—	5	5.27	
150	SCIF	Did you assign SCIF0_TXD and SCIF0_RXD signals to be used as SCIF download?	Y	Y	Y	Y	Y	—	Y	5	5.28	
151	Octa Memory Controller	Did you confirm that the connection of the OctaFlash and OctaRAM is correct?	—	—	—	—	—	Y	Y	5	5.29	
152	Power supply	Did you confirm that power domain "PVDD182533" is at 3.3 V when using pins belonging to power domain "PVDD182533" as GPIO?	Y	Y	Y	Y	Y	Y	Y	5	5.30	
153	SPI Multi I/O I/F	Did you understand that using a QSPI flash memory with RESET pin was recommended?	Y	Y	Y	Y	Y	Y	Y	5	5.31	
154	Others	Did you understand the contents of this circuit design guideline, including restrictions and recommendations, before designing the PCB patterns?	Y	Y	Y	Y	Y	Y	Y	6	6.1 to 6.13	

REVISION HISTORY	Check List for Designing RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, and RZ/G3S Circuit Boards

		Description	
Rev.	Date	Page	Summary
1.00	Sep 30, 2021	—	First edition issued
1.01	Jan 07, 2022	All	RZ/G2UL product is added. Chapter titles are updated.
		5 to 7	Figure 1.1 is updated.
		12	Figure 1.5 is modified.
		13	Figure 1.6 is modified.
		15	Figure 1.7 is modified.
		18	Table 2.2 is modified.
		39	Table 4.1 is modified.
		42	Figure 4.1 is modified.
		47	Figure 4.4 is modified.
		48	Figure 4.5 is modified.
		57	PRST_N is changed to PRST#.
		58	Figure name of Figure 5.1 is added.
		74	Table 5.6 is modified.
		75	Table 5.7 is modified.
		87	Section 5.26 is added.
		88	Section 5.27 is added.
		109 to 118	Section 7 is updated.
1.02	Feb 25, 2022	All	RZ/Five product is added.
1.03	Apr 26, 2022	All	For Section 4.1 through 4.7, the topologies correspond to "2Rank" for DRAM rank or "2" for the number of DRAM connections are available
		14	For Figure 1.6, the DRAM connection is modified from 1 to 2.
		39	For Table 4.1, the maximum Number of Ranks is modified from 1 to 2.
		42	For Figure 4.1, the number of address terminal is modified.
		46	For Figure 4.4, the DRAM connection is modified from 1 to 2.
		48	For Figure 4.5, the DRAM connection is modified from 1 to 2.
		63	For Section 5.5, the description involved in pull-up or -down resistor values is modified.
1.04	Jun 10, 2022	All	RZ/A3UL product is added.
		All	RZ/G2UL Group User's Manual: Hardware was added as a reference.
		All	RZ/A3UL Group User's Manual: Hardware was added as a reference.
		72	Figure 5.3 is modified for the connection of a SPI flash memory (data width = 8bits).
		73	Figure 5.4 is modified for the connection of a HyperFlash memory (data width = 8bits).
		91	Section 5.28 "Octa Memory Controller" is added.
		112 to 122	Section 7 is updated.
1.10	Dec 21, 2022	5 to 7	For Figure 1.1 (a), Figure 1.1 (b) and Figure 1.1 (c), the pin name of JTAG ICE are modified from "TRST#" to "nRESET".
		57	For Section 4.16, pin handling is added for "USBn_OVRCUR (n = 0, 1)" pin when not in use. For Figure 4.7, overcurrent input of the USB is modified.
		71	For Section 5.10, pull-up connection of CLK signal is not required for eMMC interface circuit.
		77	For Section 5.15, pin handling is added for "DEBUGEN" pin for JTAG circuit.

		Description	
Rev.	Date	Page	Summary
1.10	Dec 21, 2022	89	For Section 5.26, pin handling is removed for "IC" pin. Target products are restricted to RZ/G2UL and RZ/Five.
		92	For Section 5.28, document is added for reference.
		93	Section 5.29 "IO voltage level available for power domain "PVDD182533"" is added.
		114 to 124	Section 7 is updated.
1.11	Apr 06, 2023	57	For Section 4.16 "Voltage for the overcurrent or VBUS Input of the USB", pin handling is updated for "USBn_OVRCUR (n = 0, 1)" pin when not in use.
		94	Section 5.30 "Selection of QSPI flash memory" is added
		115 to 125	Section 7 "Check List" is updated.
1.12	Oct 31, 2023	16	For Section 2.1 "Voltage for Clock Input", the input voltage of the ET0/1_TXC/TX_CLK pin is changed from 1.8 V to 1.8/2.5/3.3 V for all products.
1.20	Nov 06, 2023	All	RZ/G3S product is added.
		7	For Figure 1.1 (b) of Section 1.1 "Circuits for Generating PRST# Inputs", the part name of a PMIC is modified from "PMIC" to "RAA215300A2GNP#HA0".
		17	For Figure 1.6 of Section 1.6 "Making Reset Signals Open-Drain Output", the buffer types of the QSPI_RESET# and the SD0_RST# are modified from "3.3V output, open drain" to "3.3/1.8V output, open drain". For Figure 1.6 of Section 1.6 "Making Reset Signals Open-Drain Output", the buffer type of the DDR_RESET# is modified from "3.3V CMOS output" to "1.2/1.35V CMOS output".
		20	For Section 2.1 "Voltage for Clock Input", a crystal oscillator is added.
		22	For Table 2.2 of Section 2.3 "Accuracy and Deviation of the Input Clocks", the XIN is added for the clock input.
		35	For Section 3.4 "Noise Filter Circuits for Power Supplies", the description "Although the hardware manuals or guidelines do not include recommended circuits for the CPG PLL power supply circuit, this circuits indicate that the circuit is noise-sensitive." is removed. description and added a crystal oscillator. The description "filters are recommended in the guidelines" changed to "filters are recommended in the evaluation board kits or guidelines"
		48	For Section 4.4 "Command and Address Wiring Topologies for Connecting with DRAM", the section name is changed to "Wiring Topologies for Connecting with DRAM", The description "Command and Address wiring connection between target device and DRAM is under below." is changed to "Command and address wiring connection between a target device and DRAM is only supported point-to-point on our reference board.". The description "Data wiring connection between a target device and DRAM is shown below." is added. The description "If you support wiring connection other than that of our reference board, please refer to the PCB verification guide for DRAM and perform simulation by yourself. Even if you support wiring connection of our reference board, it is strongly recommended to perform simulation because a PCB structure, material, and target DRAM are not exactly the same" is added.
		61	For Table 4.3 of Section 4.14 "PCB Design Guide for High-Speed Serial Interfaces", the guideline name is changed from "PCB design guidelines for MIPI-CSI, NIPI-DSI, and USB2.0" to "PCB design guidelines for MIPI-CSI, NIPI-DSI, USB2.0, and PCI Express Gen2".
		68	For Section 4.21 "USB VBUSEN", the description "refer to Figure 4.7 to make the connection" is removed. The description "It is shown a design example of an evaluation board manufactured by Renesas Electronics." is added.
		77	For Section 5.8 "Interrupt Signals", the description "Partially shared" is changed to "Dedicated" for Table 5.1 Specification of the NMI Signal.
		82	For Section 5.11 "SPI Multi I/O Interface", the description "serial flash, OctaFlash™" is changed to "Quad/Octal-SPI flash memory". Figure "Connection of SPI Flash Memory" is modified.
		93	For Section 5.19 "Master and Slave Settings of SPI", section name is modified.

Rev.	Date	Description	
		Page	Summary
1.20	Nov 06, 2023	127 to 137	Section 7 "Check List" is updated.
1.21	Mar 18, 2024	6	For Figure 1.1 (a) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		7	For Figure 1.1 (b) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		8	For Figure 1.1 (c) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		9	For Figure 1.1 (d) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		14	For Figure 1.5 (a) of Section 1.5 "Circuits for Generating TRST# from JTAG-ICE", the diagram is modified.
		102	For Section 5.28 "Notes on SCIF0 Signal Connection", it is not mandatory to be supported for RZ/A3UL product
		137	For Section 7 "Check List", the support for #150 SCIF is not mandatory for RZ/A3UL product.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
    "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
    "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
    Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1   October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.