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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Block transfer by using DMAC

1.0 Abstract

The following are steps for changing both source address and destination address to transfer data from memory to another. The DMA transfer utilizes the workings that assign a higher transfer priority to the DMA that has the highest priority if transfer requests simultaneously occur in two DMA channels.
Use the following peripheral functions:
• Timer mode of timer A
• Two DMAC channels
• One-byte temporary RAM (address 0800_{16})

2.0 Introduction

Specifications

(1) Transfer the content of memory extending over 128 bytes from address $FFA000_{16}$ to a 128-byte area starting from address $C00_{16}$. Transfer 1-byte of data every time a timer A0 interrupt request occurs.

(2) Use DMA0 for a transfer from the source to built-in memory, and DMA1 for a transfer from built-in memory to the destination.

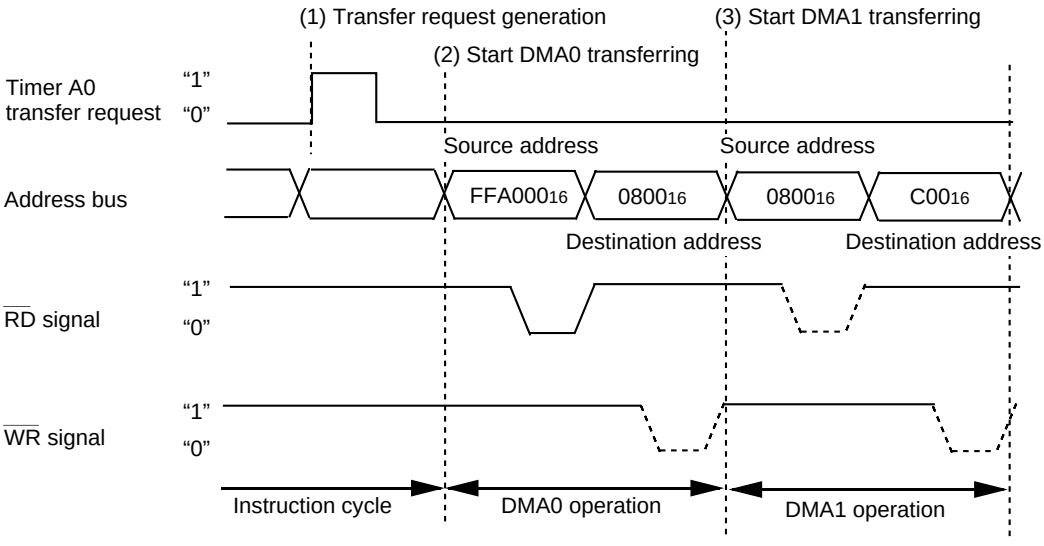
Operation

(1) A timer A interrupt request occurs. Though both a DMA0 transfer request and a DMA1 transfer request occur simultaneously, the former is executed first.

(2) DMA0 receives a transfer request and transfers data from the source to the built-in memory. At this time, the source address is incremented.

(3) Next, DMA1 receives a transfer request and transfers data involved from built-in memory to the destination. At this time, the destination address is incremented.

Figure 1 shows the operation timing.



Note 1: The DMA0 operation and DMA1 operation are not necessarily executed in succession due to the a cycle steal operation.
Note 2: The instruction cycle varies from instruction to instruction.
Note 3: Since the parts of the $\overline{RD}$ and $\overline{WR}$ signals shown in short-dash lines vary in step with writing to the internal RAM, waveforms are not output to the $\overline{RD}$ and $\overline{WR}$ pins.

Figure 1. Operation timing of Block transfer by using DMAC

Figure 2 shows the connection diagram of Block transfer by using DMAC.

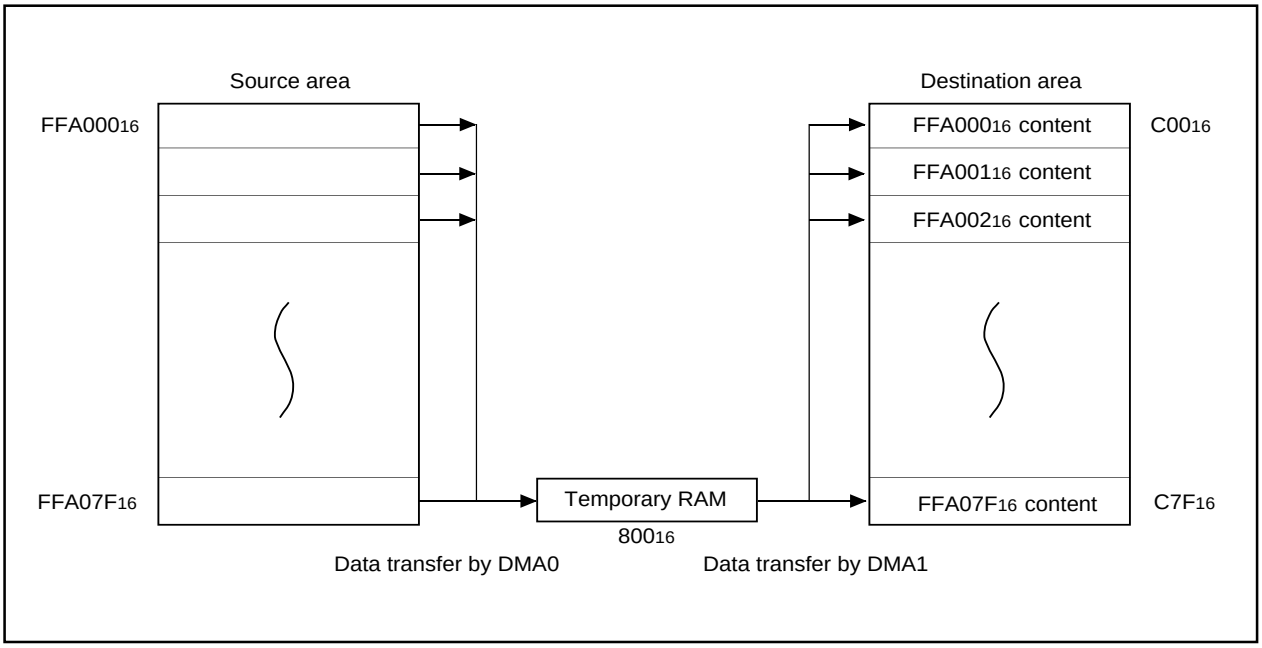
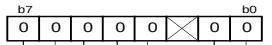


Figure 2. Connection diagram of Block transfer by using DMAC

3.0 Set-up procedure

Initialization of timer A0



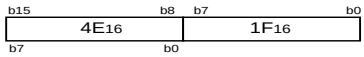
Timer A0 mode register
TA0MR [Address 035616]
0 0 : Selection of timer mode

Gate function select bit
b4 b3
0 0 : Gate function not available (TA0IN pin is a normal port pin)

0 (Must always be fixed to "0" in timer mode)

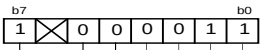
Count source select bit
b7 b6
0 0 : f1

b7	b6	Count source	Count source period f(XIN) : 20MHz f(XCIN) : 32.768kHz
0	0	f1	50ns
0	1	f8	400ns
1	0	f32	1.6µs
1	1	fC32	976.56µs



Timer A0 register
TA0 [Address 0347, 034616]

Initialization of DMA0

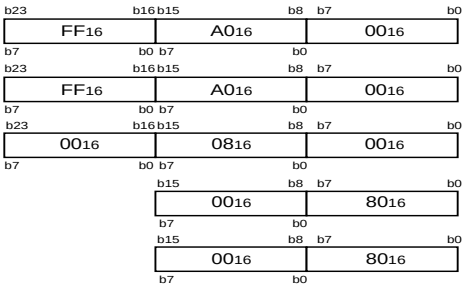


DMA0 request cause select register
DM0SL [Address 037816]

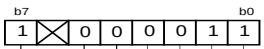
DMA request cause select bit
0 0 0 1 1 : Timer A0

Software DMA request bit
0 : Software trigger is not generated

DMA request bit
Must write "1" to this bit



Initialization of DMA1

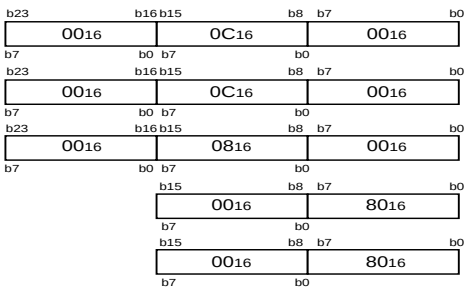


DMA1 request cause select register
DM1SL [Address 037916]

DMA request cause select bit
0 0 0 1 1 : Timer A0

Software DMA request bit
0 : Software trigger is not generated

DMA request bit
Must write "1" to this bit



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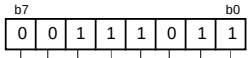
Setting DMA mode register



DMA mode register 0
DMD0 [CPU internal memory]

Channel 0 transfer mode select bit
1 1 : Repeat transfer

Channel 0 transfer unit select bit
0 : 8 bits

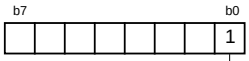
Channel 0 transfer direction select bit
1 : Memory (forward direction) to fixed address

Channel 1 transfer mode select bit
1 1 : Repeat transfer

Channel 1 transfer unit select bit
0 : 8 bits

Channel 1 transfer direction select bit
0 : Fixed address to memory (forward direction)

Setting count start flag



Count start flag [Address 0340_{16}]
TABSR

Timer A0 count start flag
1 : Starts counting

4.0 Programming Code

```
;*****************************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0510_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : DMAC Applications
;               (Block transfer by using DMAC)
;   HISTORY   : 2004.03.15  Ver 1.00
;
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;
;*****************************************************************************************
;*****************************************************************************************
;       Include
;*****************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;*****************************************************************************************
;       Symbol definition
;*****************************************************************************************
RAM_TOP          .EQU    000400H    ;Start address of RAM
RAM_END          .EQU    002BFFH    ;End address of RAM
ROM_TOP          .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP   .EQU    0FFFFDCH   ;Start address of fixed vector
;
A_SRC_MEM        .EQU    0FFA000H   ;Top address of source area (Block 1)
A_TMP_MEM        .EQU       0800H   ;Address of temporary area
A_DST_MEM        .EQU       0C00H   ;Top address of destination area
C_CNT_DMA        .EQU    128        ;DMA transfer counter
;
;*****************************************************************************************
;       Allocation of work RAM area
;*****************************************************************************************
        .SECTION    WORKRAM, DATA
        .ORG        RAM_TOP
;
        .ORG        A_TMP_MEM          ;Temporary RAM area
v_Tmp_mem:     .BLKB   1
;
        .SECTION    DMA_DST, DATA      ;Destination area
        .ORG        A_DST_MEM
v_Dst_mem:     .BLKB   (C_CNT_DMA*1)
;
;*****************************************************************************************
;       Program area
;*****************************************************************************************
;=========================================================================
;       Start up
;=========================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        LDC      #RAM_END+1, ISP   ;Sets initial value in stack pointer
```

```
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr         ;Removes protect
        MOV.B    #10000000B, pm0    ; Single-chip mode
        MOV.B    #11000000B, pm1    ; Flash memory version
        MOV.B    #00001000B, cm0    ; Xcin-Xcout High
        MOV.B    #00100000B, cm1    ; Xin-Xout High
        MOV.B    #00010010B, mcd    ; No division mode
        MOV.B    #00H, prcr         ;Protects all registers
;
;=============================================================================
;       DMAC (Block transfer by using DMAC)
;=============================================================================
        ; Disable the corresponding channel DMAi (DMA0 & DMA1)
        STC      dmd0, R0           ;Read DMA mode register
        AND.B    #11001100B, R0L
;                  ||  ++---------;Channel 0 transfer mode select bit (00:DMA0 inhibit)
;                  ++-------------;Channel 1 transfer mode select bit (00:DMA1 inhibit)
        LDC      R0, dmd0           ;Disable DMA0 & DMA1
;
;-----------------------------------------------------------------------------
;       Initialization of Timer A0
;-----------------------------------------------------------------------------
        ; Set up the peripheral used as the source of the DMA transfer
        ; (Note) At this time, the peripheral should remain disabled.
        ; Stop Timer A0 counting
        BCLR     ta0s
        ; Selecting timer mode and functions
        MOV.B    #00000000B, ta0mr
;                 ||||||++---------;Selection of timer mode
;                 |||||+-----------;This bit is invalid in M16C/80 series
;                 |||++------------;Gate function select bit
;                 |||               (00 or 01:Gate function not available)
;                 ||+--------------;Must always be "0" in timer mode
;                 ++---------------;Count source select bit (00:f1)
        ; Clearing interrupt request bit and interrupt disabled
        MOV.B    #00000000B, ta0ic
        ; Setting divide ratio
        MOV.W    #04E1FH, ta0       ;(1ms @20MHz, f1)
;
```

```
;-------------------------------------------------------------------------
;       Initialization of DMA0
;-------------------------------------------------------------------------
        ; Setting DMA0 request cause select register
        MOV.B    #10000011B, dm0sl
;                 | |+++++---------;DMA request cause select bit (00011:Timer A0)
;                 | +--------------;Software DMA request bit (0:Software trigger is not generated)
;                 +----------------;DMA request bit (Must write "1" to this bit)
        ; Setting DMA0 memory address register (Setting source memory address)
        LDC      #(A_SRC_MEM & 0FFFFFFh), dma0  ;DMA0 memory address
        LDC      #(A_SRC_MEM & 0FFFFFFh), dra0  ;DMA0 memory address reload
        ; Setting DMA0 SFR address register (Setting destination fixed address)
        LDC      #(v_Tmp_mem & 0FFFFFFh), dsa0  ;DMA0 SFR address
        ; Setting DMA0 transfer count register
        LDC      #(C_CNT_DMA & 0FFFFh), dct0    ;DMA0 transfer count
        LDC      #(C_CNT_DMA & 0FFFFh), drc0    ;DMA0 transfer count reload
;
;-------------------------------------------------------------------------
;       Initialization of DMA1
;-------------------------------------------------------------------------
        ; Setting DMA1 request cause select register
        MOV.B    #10000011B, dm1sl
;                 | |+++++---------;DMA request cause select bit (00011:Timer A0)
;                 | +--------------;Software DMA request bit (0:Software trigger is not generated)
;                 +----------------;DMA request bit (Must write "1" to this bit)
        ; Setting DMA1 memory address register (Setting destination memory address)
        LDC      #(A_DST_MEM & 0FFFFFFh), dma1  ;DMA1 memory address
        LDC      #(A_DST_MEM & 0FFFFFFh), dra1  ;DMA1 memory address reload
        ; Setting DMA1 SFR address register (Setting source fixed address)
        LDC      #(v_Tmp_mem & 0FFFFFFh), dsa1  ;DMA1 SFR address
        ; Setting DMA0 transfer count register
        LDC      #(C_CNT_DMA & 0FFFFh), dct1    ;DMA1 transfer count
        LDC      #(C_CNT_DMA & 0FFFFh), drc1    ;DMA1 transfer count reload
;
        ; Selecting DMA mode register
        OR.B     #00111011B, R0L
;                 ||||||++---------;Channel 0 transfer mode select bit (11:Repeat transfer)
;                 |||||+-----------;Channel 0 transfer unit select bit (0:8bits)
;                 ||||+------------;Channel 0 transfer direction select bit (1:Memory to Fixed address)
;                 ||++-------------;Channel 1 transfer mode select bit (11:Repeat transfer)
;                 |+---------------;Channel 1 transfer unit select bit (0:8bits)
;                 +----------------;Channel 1 transfer mode select bit (0:Fixed address to Memory)
;
        ; Enable DMA0 & DMA1
        ; (Note1)
        ;    At this point, if the number of elapsed cycles are less than 26, add code
        ;    (NOP's or other processing) to make up some time.
        ; (Note2)
        ;    After writing to the DMAi request cause select register, wait at least 8+6N BCLK cycles
        ;    before enabling DMA.
        ;    Where N is the number of other DMA channels that may generate a DMA request.
        LDC      R0, dmd0
;
        ; Setting count start flag
        MOV.B    #00000001B, tabsr
;                        +---------;Timer A0 count start flag
MAIN:
        JMP      MAIN
;
```

```
;======================================================================
;       Dummy interrupt processing program
;======================================================================
dummy:
        REIT
;
;***************************************************************************************
;
;       DMA source area
;***************************************************************************************
;
        .SECTION    SRC_DMA, ROMDATA
        .ORG        A_SRC_MEM
        ; DMA transmission data
        .BYTE   01h,    02h,    03h,    04h,    05h,    06h,    07h,    08h
        .BYTE   09h,    0Ah,    0Bh,    0Ch,    0Dh,    0Eh,    0Fh,    10h
        .BYTE   11h,    12h,    13h,    14h,    15h,    16h,    17h,    18h
        .BYTE   19h,    1Ah,    1Bh,    1Ch,    1Dh,    1Eh,    1Fh,    20h
        .BYTE   21h,    22h,    23h,    24h,    25h,    26h,    27h,    28h
        .BYTE   29h,    2Ah,    2Bh,    2Ch,    2Dh,    2Eh,    2Fh,    30h
        .BYTE   31h,    32h,    33h,    34h,    35h,    36h,    37h,    38h
        .BYTE   39h,    3Ah,    3Bh,    3Ch,    3Dh,    3Eh,    3Fh,    40h
        .BYTE   41h,    42h,    43h,    44h,    45h,    46h,    47h,    48h
        .BYTE   49h,    4Ah,    4Bh,    4Ch,    4Dh,    4Eh,    4Fh,    50h
        .BYTE   51h,    52h,    53h,    54h,    55h,    56h,    57h,    58h
        .BYTE   59h,    5Ah,    5Bh,    5Ch,    5Dh,    5Eh,    5Fh,    60h
        .BYTE   61h,    62h,    63h,    64h,    65h,    66h,    67h,    68h
        .BYTE   69h,    6Ah,    6Bh,    6Ch,    6Dh,    6Eh,    6Fh,    70h
        .BYTE   71h,    72h,    73h,    74h,    75h,    76h,    77h,    78h
        .BYTE   79h,    7Ah,    7Bh,    7Ch,    7Dh,    7Eh,    7Fh,    80h
;
;***************************************************************************************
;
;       Setting of fixed vector
;***************************************************************************************
;
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

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Data Sheet

M16C/80 group Rev. E3
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