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H8/300H Tiny Series

Application Examples for Reading from/Writing to Serial EEPROM

Introduction

This application note gives examples of reading from/writing to two-wire serial (I²C bus) EEPROM via the on-chip I²C module 2 (I²C) of the H8/3694 or H8/3687.

Target Device

H8/3694, H8/3687

Contents

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1. Specifications

This application is for the H8/3694 and H8/3687.

From now on in this text, the H8/3694 is used as a representative target product name.

This application note introduces specific application examples for reading from/writing to two-wire serial (I²C bus) EEPROM using the on-chip I²C module 2 (IIC2) of the H8/3694 (here, the H8/3694 is assumed as the master, and EEPROM as a slave).

Please make use of this application note as a reference in addition to the hardware manual for programming with the I²C module 2 (IIC2).

The sample programs for this application note are written in C language.

The functions in the sample programs are those typically required for using I²C module 2 (IIC2) and have been created for versatile use; so they can be reused as service modules.

It is assumed that the serial (I²C bus) EEPROM in this application requires its memory address to be specified in two bytes.

The operation of this application has been confirmed with the EEPROM products shown in table 1.1.1.

Since a standard bus format is employed, it is considered that this application may run with other I²C bus-compliant products.

Figure 1.1.1 shows the operating environment (connection diagram) for this application.

Table 1.1.1 Operation-Confirmed EEPROM Products with This Application

No.	Operation-Confirmed Products	Manufacturer	Capacity [byte]	Page Size [byte]
1	H8/3694N on-chip EEPROM	RENESAS	512	8
2	H8/3687N on-chip EEPROM	RENESAS	512	8
3	HN58X2432I	RENESAS	4,096	32
4	HN58X2464I	RENESAS	8,192	32

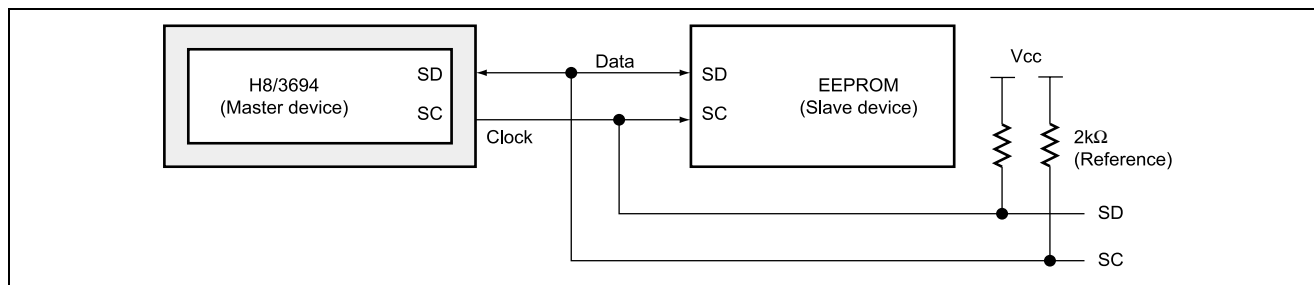


Figure 1.1.1 Operating Environment for this Application (Connection Diagram)

2. Bus Specifications

1. On-chip I²C bus interface 2 (IIC2)

The on-chip I²C bus interface (IIC2) of the H8/3694 conforms to the I²C bus (inter IC bus) interface method propounded by Philips, and embeds sub-set functions.
 For details, refer to I²C Bus Interface 2 (IIC2) section in the Hardware Manual.
2. I²C bus interface of EEPROM

For the I²C bus interface of EEPROM, refer to the Hardware Manual of the EEPROM.
3. Bus mode

This application performs communications through the I²C bus with the configuration of one master device (H8/3694), on which this application program runs, and one slave device (EEPROM) (see figure 1.1.1).
 Among transmission/reception modes of the I²C bus interface 2, only the master transmission/reception mode is used in this application.

3. EEPROM Basic Specifications

For the I²C bus interface specifications of the on-chip EEPROM of the H8/3694N, refer to the Hardware Manual of the product.

According to the I²C bus interface specifications, there are following four types of standard specifications (read/write specifications) for accessing to EEPROM having an I²C bus interface.

This application note describes operations of the four types of basic specifications (read/write specifications) through functionalization with versatility.

1. Read specifications
 - A. Random read (1-byte read)

Data is read out from a given address.
 - B. Sequential read (N-byte read)

N-byte data is sequentially read out starting from a given address.
2. Write specifications
 - A. Byte write (1-byte write)

Data is written to a given address.
 - B. Page write (N-byte write)

One page of (N-byte) data is sequentially written to starting from a given address.
 In writing, after confirming the completion of the writing operation by acknowledgement polling, the next data write is performed.

4. Software Specifications

4.1 Software Specifications

The software specifications of this application are described below.

4.1.1 Basic functions

The basic functions listed in table 4.1.1 have been provided for reading from/writing to serial EEPROM via the I²C bus interface 2 (IIC2) embedded in the H8/3694.

Table 4.1.1 Basic Functions for Read/Write Access to Serial EEPROM

No.	Function	Function Name
1	1-byte write	Master_byte_write(Device_id, Addr, Data)
2	1-byte read	Master_read_byte_random(Device_id, Addr)
3	1-page write (N-byte write)	Master_page_write(Device_id, Addr, Length, *buff_ptr)
4	Sequential read (N-byte read)	Master_read_sequential(Device_id, Addr, Length, *buff_ptr)

4.1.2 Functional policy of this application

To perform data communications via the I²C bus interface 2 (IIC2), processing is done through reading/writing of flags and data in the internal registers by software.

In this application, read/write processing of flags and data of internal registers is grouped into functional units and made into functions for each functional unit to describe the operation of the I²C bus interface 2 (IIC2).

4.1.3 Slave address of the EEPROM

The slave address (7 bits) of the EEPROM to be connected as a slave device is assigned to be 0xa0 (upper 7 bits are used). For details, see table 4.1.2.

Table 4.1.2 Slave Address (7 Bits) Assignment of the EEPROM to be Connected

Bit	Bit Name	Setting
7	Device code D3	1
6	Device code D2	0
5	Device code D1	1
4	Device code D0	0
3	Slave address code A2	0
2	Slave address code A1	0
1	Slave address code A0	0

Note: Bit 0 is used as a R/W code.

4.1.4 Transfer method

Data transfer through the I²C bus is carried out by performing communications while confirming the transfer through an acknowledgement for every one-byte transmission/reception.

Alternatively, transfer processing can be performed using interrupts. For details, see table 4.1.4 and the Hardware Manual of the target product.

4.1.5 Timeout processing for individual control flags

In the control of I²C bus interface 2 (IIC2), it is necessary to check individual control flags repeatedly until they become active.

In this application, a timeout function is added as part of control flag checking functionality.

When the flag check count exceeds the limit value, it is regarded that a timeout error has occurred, so that the process exits from the flag check loop and error processing is performed.

When returning to the upper function, a timeout error code should be returned.

For details on the timeout limit counter value and error code, see table 4.3.2, Constants 2. and 3. .

In the checking of respective control flags, the minimum time for the flag becoming active is determined by the internal logic.

The minimum time until a timeout occurs for each flag is shown in table 4.1.3 for reference. When performing timeout processing, the limit count (retry count) values should be set referring to these minimum times as a guide and then be adjusted.

Note that the minimum time is a value when the transfer clock does not go rusty. When the transfer clock dulls, the value may be larger. Therefore, a margin should be taken according to the environment for use.

In this application, the values shown in table 4.3.2, Constants 2., are used as assumed values for explanation.

Table 4.1.3 Minimum Time till Timeout of Each Processing (when transfer clock does not dull)

No.	Control Flag Check	Target Control Flag Name where Timeout Processing is Required	Minimum Time till Timeout (Transfer Clock Count)
1	Timeout of bus busy check	IIC2.ICCR2.BIT.BBSY	2
2	Timeout of ACK check	IIC2.ICIER.BIT.ACKBR	21
3	Timeout of TEND check	IIC2.ICSR.BIT.TEND	21
4	Timeout of RDRF check	IIC2.ICSR.BIT.RDRF	21
5	Timeout of STOP check	IIC2.ICSR.BIT.STOP	2

Note: One transfer clock cycle = (1/transfer clock frequency) [time](When transfer clock frequency = 400 kHz, one transfer clock cycle = 2.5 μs)

4.1.6 Main processing

To present usage examples of basic functions, a simple main processing that uses the four basic functions (see table 4.1.1) have been created.

The following processing 1. and 2. are performed in the main processing.

Note that it is assumed that the on-chip EEPROM of the H8/3694N is used as a slave device.

1. Test data (the lower 8 bits of an EEPROM address) is written to EEPROM by using "1-byte write" function (byte write); the data that has been written is then read by "1-byte read" function (byte read), and the write/read operation is checked by verification. This processing is repeated for all addresses in a 512-byte area in the EEPROM. The result of the processing is output to port 1 (P12, P11, and P10).
2. To all addresses in a 512-byte area of EEPROM, test data (the lower 8 bits of the EEPROM address + 1) is written using "1-page write" function; the block of data that has been written is then read by using "sequential read" function, and the write/read operations are checked by verification. The result of the processing is output to port 1 (P12, P11, and P10).

For details on main processing, see the module configuration diagram, flowchart, and program.

4.1.7 Language used in this application

In this application, C language is used for programming.

The program-developing processes from the source program creation to the object code generation is carried out by using the integrated development environment HEW2 (product of Renesas Technology Corp.).

4.1.8 Representation of I²C bus transmission/reception formats

In this application note, the I²C bus transmission/reception formats are described using the representation shown in figure 4.1.1.

Applicable EEPROM types are those for which the memory address is specified in two bytes.

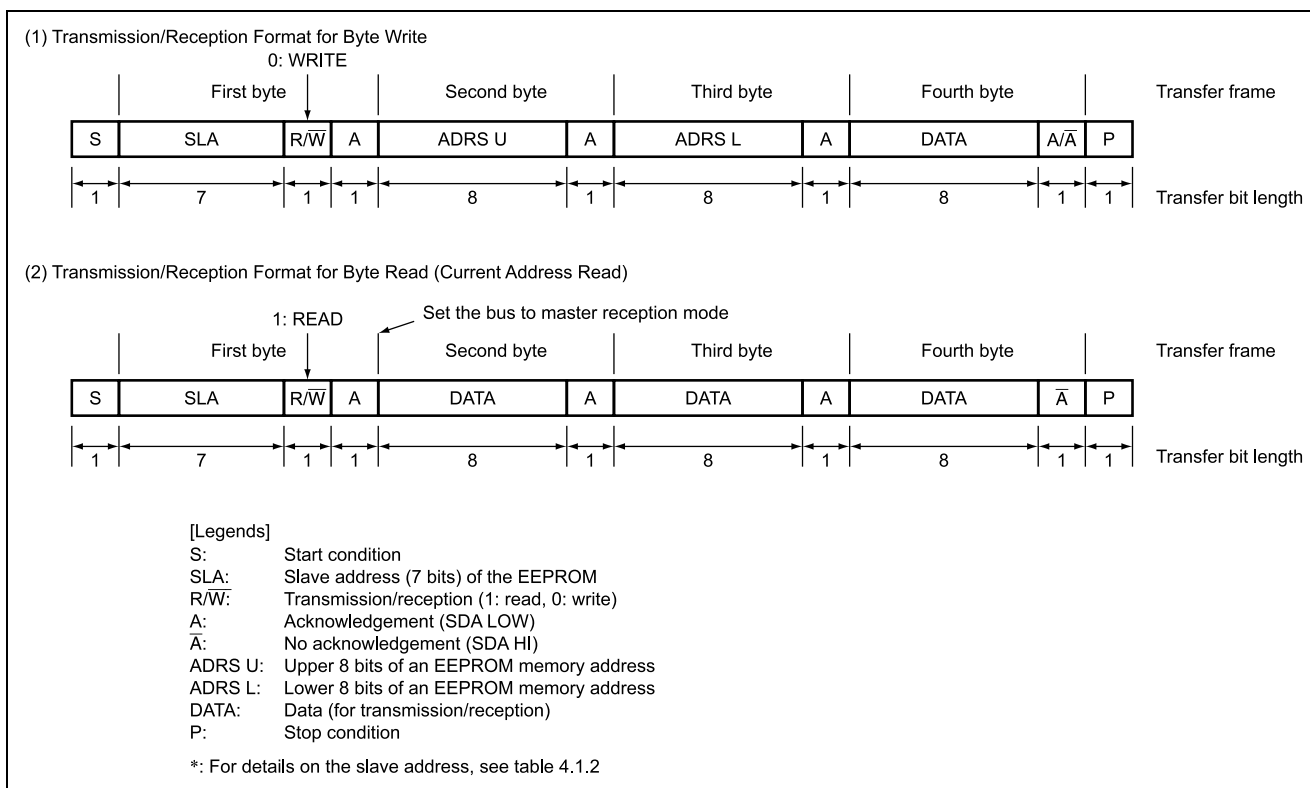


Figure 4.1.1 Representation of I²C Bus Transmission/Reception Format

4.1.9 Functions of control flags and registers used in this application

Table 4.1.4 summarizes the functions of the control flags and registers used in this application.

Table 4.1.4 Functions of Control Flags and Registers

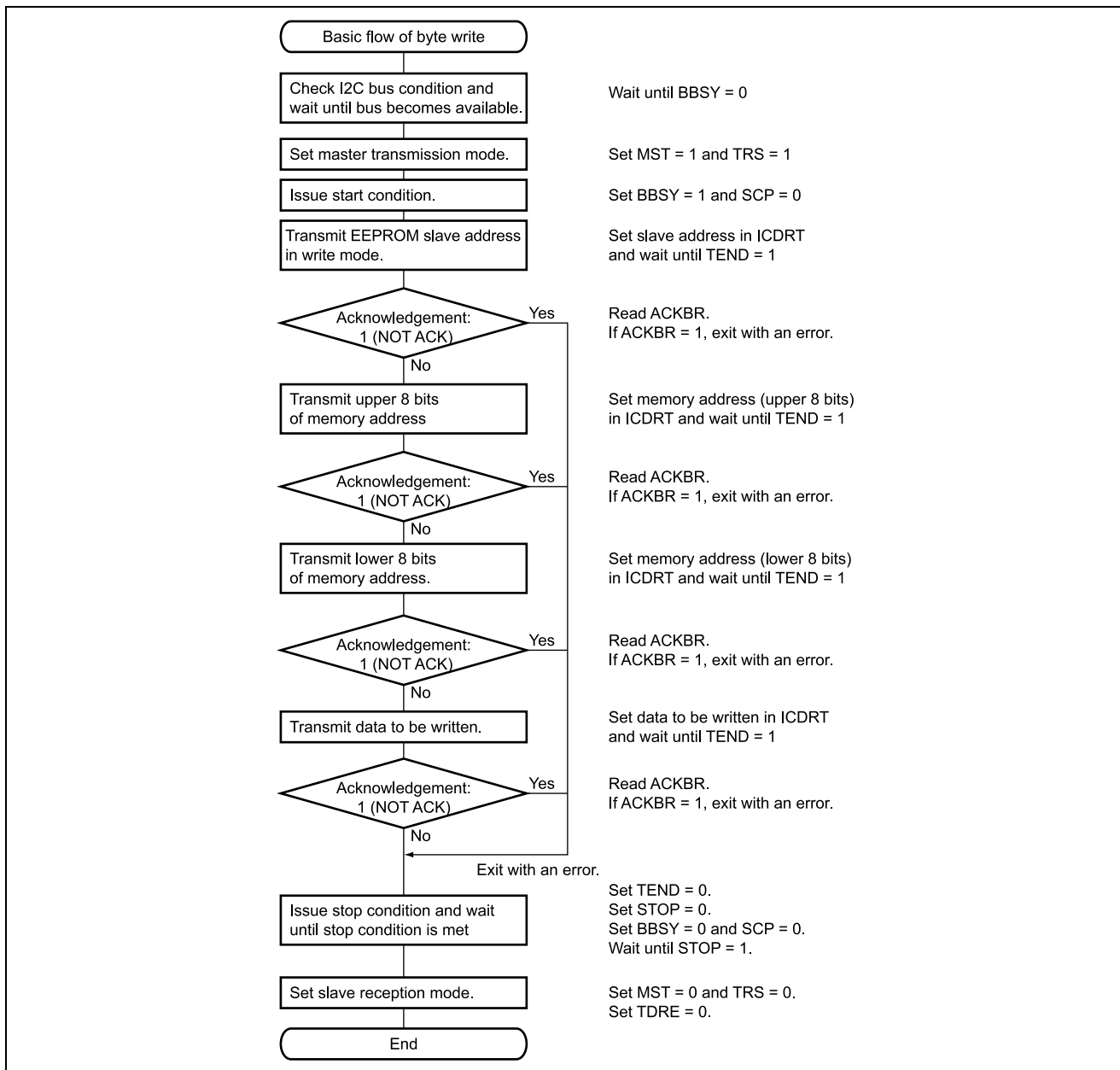
No.	Control Flag/Register Name	Description
1	ICDRR	Receive data register When read, the next reception is performed (the clock output is started).
2	RDRF	Receive data register full This flag is set when data is placed in ICDRR after completion of reception. If the receive-data-full interrupt is enabled (RIE = 1), an RXI interrupt is generated.
4	RCVD	Receive disable 0: Enables subsequent reception operation. (When ICDDR is read, clock for subsequent reception is output.) 1: Disables subsequent reception operation. (When ICDDR is read, clock for subsequent reception is not output.) RCVD should be set prior to reading of ICDRR.
5	ACKBT	Transmission acknowledgement Sets the acknowledgment to be transmitted in reception mode. 0: ACK 1: NOT ACK ACKBT should be set prior to reading of ICDRR.
6	ICDRT	Transmit data register Data transmission is started when data is written to this register and the data is transferred to the shift register (ICDRS). Sequential transmission is possible by writing the subsequent data to ICDRT during data
7	TEND	Transmit end This flag is set on the rising edge of the ninth clock of SCL when TDRE = 1. When TDRE = 1, transmission has been completed and acknowledgement is being received. The TEND flag can be used if data should be transferred while confirming the acknowledgement. (TEND is used in this application.) After transmission of a slave address or final data, completion of transmission can be securely detected by using the TEND flag. If the transmit-end interrupt is enabled (TEIE = 1), a TEI interrupt is generated.
8	TDRE	Transmit data empty This flag is set when data is transferred from ICDRT to ICDRS. The TDRE flag can be used when data transfer is done without confirming the acknowledgement. (Detection of an acknowledgement error in this case can be performed by means of NACK receive interrupts (NACKI). If the transmit data empty interrupt is enabled (TIE = 1), a TXI interrupt is generated.
9	ACKBR	Reception acknowledgement In transmission mode, an acknowledgement from a receiving device is stored to this bit. 0: ACK, 1: NOT ACK

4.1.10 Basic Flow of the EEPROM Write/Read Processing

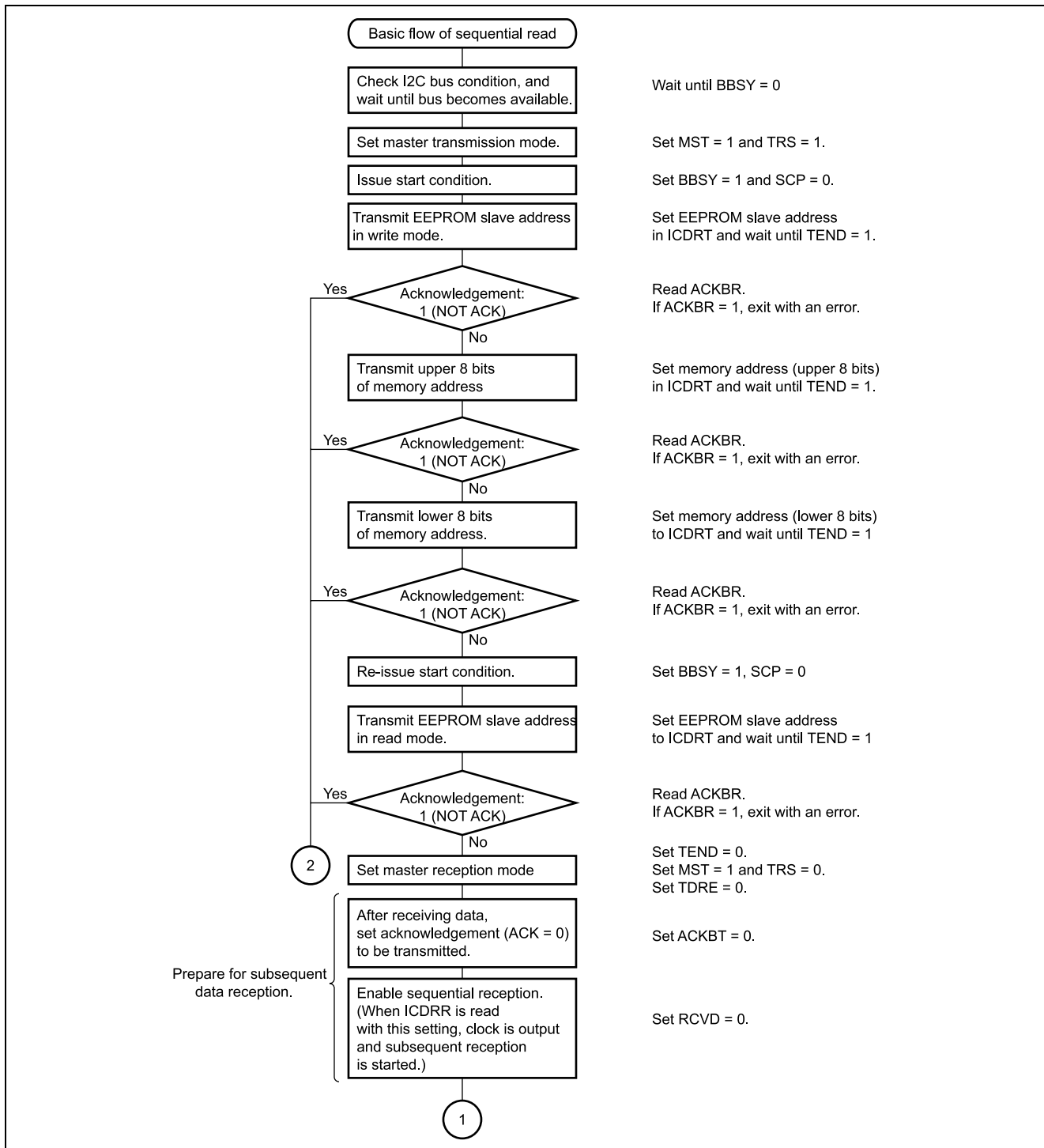
The basic flow of EEPROM write/read processing via the I²C bus interface 2 (IIC2) are described below with reference to the examples: 1. byte write and 2. sequential read.

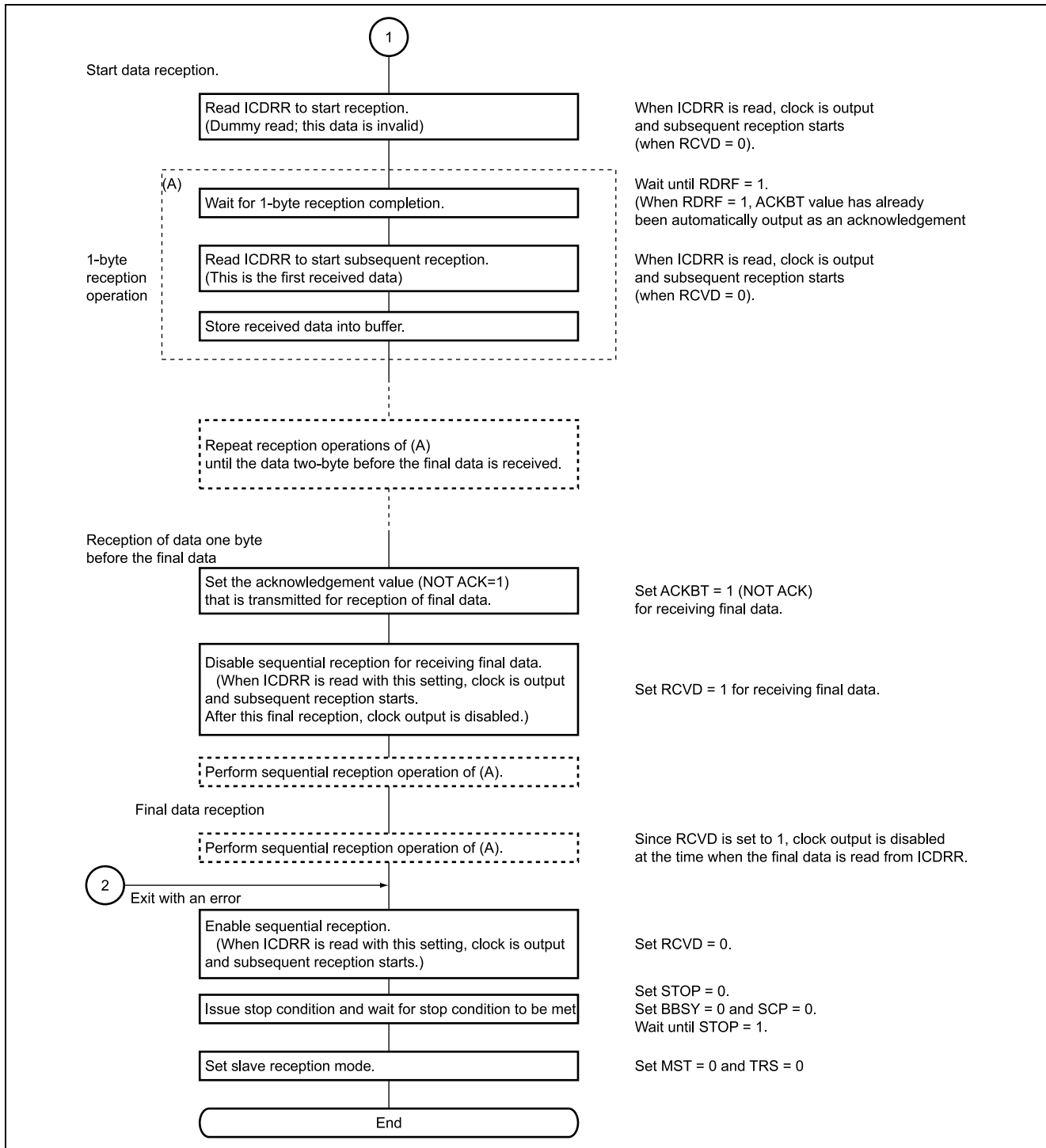
Since these flows are only for describing the basic flow of processing, they might not be consistent with the sample application program at some minor points. Thus, please use this flow in addition to the Hardware Manual as a reference for dealing with the flags and registers.

1. Standard write processing flow for EEPROM (Byte write)



2. Standard read processing flow for EEPROM (Sequential read)





4.2 Function list

The functions created for this application and their functionalities are shown in tables 4.2.1 to 4.2.5.

Table 4.2.1 IIC2 Main Function

No.	Function Name	Description
0	Main(void)	Functions No. 1 to No. 4 are called to show their usage examples.
1	Master_byte_write(Device_id, Addr, Data)	1-byte write
2	Master_read_byte_random(Device_id, Addr)	1-byte read
3	Master_page_write(Device_id, Addr, Length, *buff_ptr)	1-page write (N-byte write)
4	Master_read_sequential(Device_id, Addr, Length, *buff_ptr)	Sequential read (N-byte read)

Table 4.2.2 IIC2 Sub Function

No.	Function Name	Description
5	Master_address_set(Device_id, Addr)	Transmits slave address and memory address.
6	Check_bus_condition(void)	Checks bus condition.
7	Send_start_condition(void)	Issues start condition.
8	Send_stop_condition(void)	Issues stop condition.
9	Send_byte_data(Byte_data)	Transmits 1-byte data.
10	Receive_byte_data(void)	Receives 1-byte data.
11	Receive_byte_data_fin(void)	Receives final 1-byte data
12	Receive_byte_data_many(Length, *buff_ptr)	Receives byte data sequentially (for read byte length).
13	Set_slave_read_mode(Device_id)	Transmits slave address (read mode).
14	Set_slave_write_mode(Device_id)	Transmits slave address (write mode).
15	Set_receive_mode(Ackbt_flag, Rcvd_flag)	Sets ACKBT and RCVD flags.

Table 4.2.3 IIC2 Initialization Function

No.	Function Name	Description
16	Init_iic2 (void)	Initializes IIC2 I/F.
17	Set_iic_bus_mode(MLS, WAIT, BC210)	Sets master device bus mode.
18	Set_iic_mode(MODE)	Sets master device transmission/reception mode.
19	Set_iic_rate(RATE)	Sets master device transfer rate.
20	Set_iic2_if_enable(ICE)	Sets IIC2 I/F module operation status.

Table 4.2.4 EEPROM Initialization Function (Controls IIC Bus through Port Processing and Initializes EEPROM)

No.	Function Name	Description
21	Init_eeprom(void)	Initializes EEPROM bus condition.
22	I2c_start (void)	Issues start condition to IIC device. (port processing)
23	I2c_stop (void)	Issues stop condition to IIC device. (port processing)
24	I2c_set (Scl, Sda)	Outputs SCL and SDA to IIC device. (port processing)
25	I2c_bytesend (Tx_data)	Transmits byte data to IIC device. (port processing)
26	I2c_bit send (Tx_data, Ckbit)	Transmits bit data to IIC device. (port processing)
27	I2c_send (Bit_data)	Transmits bit data synchronized with a clock from IIC port. (port processing)
28	I2c_ackck (void)	Obtains acknowledgements from IIC device. (port processing)
29	I2c_sda_in (void)	Sets SDA (P56) of IIC port as input and SCL (P57) as output.
30	I2c_sda_out (Data)	Sets SDA (P56) and SCL (P57) of IIC port as output and outputs data.
31	Wait_timer (Wait_cnt)	Wait for the specified time (countdown until the wait count reaches 0).

Note: The EEPROM initialization functions are used to forcibly bring the SDA bus of EEPROM into input mode when the SDA bus of EEPROM still remains in output mode (this might be caused when, for example, communication is halted during data reception from EEPROM) and reception processing from the master device cannot be performed. These functions are only for reference and do not have direct relation to the main function.

Table 4.2.5 Initialization (Startup) Function

No	Function Name	Description
32	INIT(void)	Initialization (startup) routine (created in INIT.SRC file)

4.3 Global variables and constants

Tables 4.3.1 and 4.3.2 show the global variable and constants (defined using #define directives) used in this application program.

Table 4.3.1 Global Variable

No.	Variable Name	Type	Size	Application
1	eeeprom_buf	unsigned char	513	EEPROM read/write data storage buffer

Table 4.3.2 Constants

1. Device code definition

No.	Variable Name	Type	Size	Application
1	DEVICE_CODE	unsigned char	0xa0	EEPROM device code: 1010 (D3, D2, D1, D0)
2	SLAVE_ADRS	unsigned char	0x00	Slave address code: 000 (A2, A1, A0)
3	RW_CODE_W	unsigned char	0x00	R/W code: 0 (data write)
4	RW_CODE_R	unsigned char	0x01	R/W code: 1 (data read)
5	DEVICE_ADDRESS_WORD_W	unsigned char	See right. (DEVICE_CODE SLAVE_ADRS RW_CODE_W)	Slave address (for writing)
6	DEVICE_ADDRESS_WORD_R	unsigned char	See right. (DEVICE_CODE SLAVE_ADRS RW_CODE_R)	Slave address (for reading)

Note: For slave address, see table 4.1.2.

2. Definition of timeout limit counts (number of times for terminating respective flag check processings: assumed value)

No.	Variable Name	Type	Size	Application
1	TIMEOUT_LIMIT_BBSY	unsigned char	1000	Bus busy check timeout limit
2	TIMEOUT_LIMIT_ACK	unsigned char	1000	ACK check timeout limit
3	TIMEOUT_LIMIT_TEND	unsigned char	1000	TEND check timeout limit
4	TIMEOUT_LIMIT_RDRF	unsigned char	1000	RDRF check timeout limit
5	TIMEOUT_LIMIT_STOP	unsigned char	1000	STOP check timeout limit

3. Definition of error codes

No.	Variable Name	Type	Size	Application
1	IMEOUT_ERR_BUS_BUSY	unsigned char	200	Bus busy timeout error
2	TIMEOUT_ERR_ACK	unsigned char	201	Acknowledgement polling timeout error
3	TIMEOUT_ERR_TEND	unsigned char	202	Transmit end timeout error
4	TIMEOUT_ERR_RDRF	unsigned char	203	Receive end timeout error
5	TIMEOUT_ERR_STOP	unsigned char	204	Stop condition issue timeout error
6	ERR_ACK	unsigned char	205	Acknowledgement error

4. Other definition

No.	Variable Name	Type	Size	Application
1	TM	unsigned char	100 (assumed value)	Wait count for the wait timer (Used for clock output of EEPROM initialization function)

4.4 Section definitions

Table 4.4.1 shows section (memory allocation address) definitions of this application program.

Table 4.4.1 Section Definitions

Allocated Address	Section name	Allocated as
H'0000	C	Vector area
H'1000	P	Program area
H'FB80	B	RAM area

4.5 Description of Functions

Description of the major functions are provided in sections 4.5.1 through 4.5.7.

The major functions described are listed in table 4.5.1. (Section numbers 4.5.1 through 4.5.7 correspond to the major function numbers in this table.)

Table 4.5.1 Major Functions Described in This Section

No.	Function Name	Description
1	Master_byte_write(Device_id, Addr, Data)	1-byte write
2	Master_read_byte_random(Device_id, Addr)	1-byte read
3	Master_page_write(Device_id, Addr, Length, *buff_ptr)	1-page write
4	Master_read_sequential(Device_id, Addr, Length, *buff_ptr)	Sequential read
5	Master_address_set (Device_id, Addr)	Transmission of slave address and memory address
6	Receive_byte_data_many (Length, *buff_ptr)	Sequential data reception
7	Init_eeprom(void)	Initialization of EEPROM bus condition

4.5.1 1-byte write

1. Function Name

Master_byte_write(Device_id, Addr, Data)

1-byte write

2. Argument

A. Entry

(1) Device_id (unsigned char) ; Slave address code: 0 to 7 (A2, A1, A0)

(2) Addr (unsigned short) ; Memory address (2 bytes)

(3) Data (unsigned char) ; Write data (1 byte)

B. Return

(1) Err_code (unsigned char); Error code

0: Normal termination

2: Second byte acknowledgement error (upper 8 bits of memory address)

3: Third byte acknowledgement error (lower 8 bits of memory address)

4: Fourth byte acknowledgement error (data)

TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error

TIMEOUT_ERR_ACK: Acknowledgement polling timeout error

TIMEOUT_ERR_STOP: Stop condition detection timeout error

Note: The transmit end timeout error is returned as 2 to 4 of Err_code.

3. Processing

Transmits to the slave device the slave address (1 byte), memory address (2 bytes), and write data (1 byte) according to the transmission/reception format, and writes the write data to the memory address.

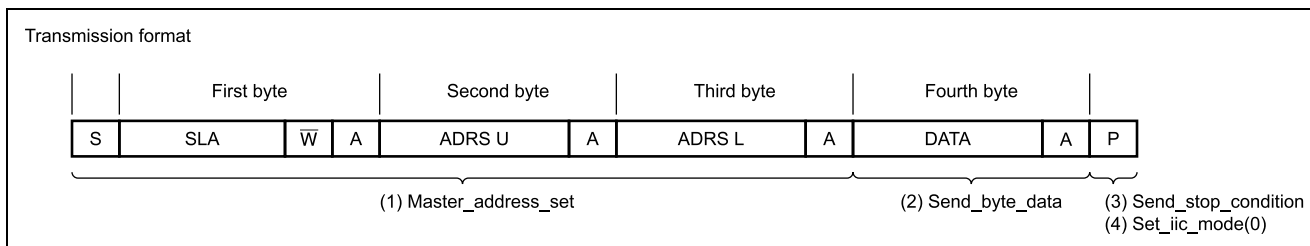
4. Functions used

(1) Master_address_set(Device_id, Addr); Transmits slave address and memory address.

(2) Send_byte_data(Data); Transmits data.

(3) Send_stop_condition(); Issues stop condition.

(4) Set_iic_mode(0); Sets slave reception mode.



4.5.2 1-byte read

1. Function Name

Master_read_byte_random(Device_id, Addr)

1-byte read

2. Arguments

A. Entry

(1) Device_id (unsigned char) ; slave address code: 0 to 7 (A2,A1,A0)

(2) Addr (unsigned short) ; memory address (2 bytes)

B. Return

(1) Err_code (unsigned char); error code (upper 8 bits)

0: Normal termination

2: Second byte acknowledgement error (upper 8 bits of memory address)

3: Third byte acknowledgement error (lower 8 bits of memory address)

ERR_ACK: Slave address (read) acknowledgement error

TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error

TIMEOUT_ERR_ACK: Acknowledgement polling timeout error

TIMEOUT_ERR_RDRF: Receive end timeout error

TIMEOUT_ERR_STOP: Stop condition detection timeout error

Note: The transmit end timeout error is returned as 2 to 3 of Err_code.

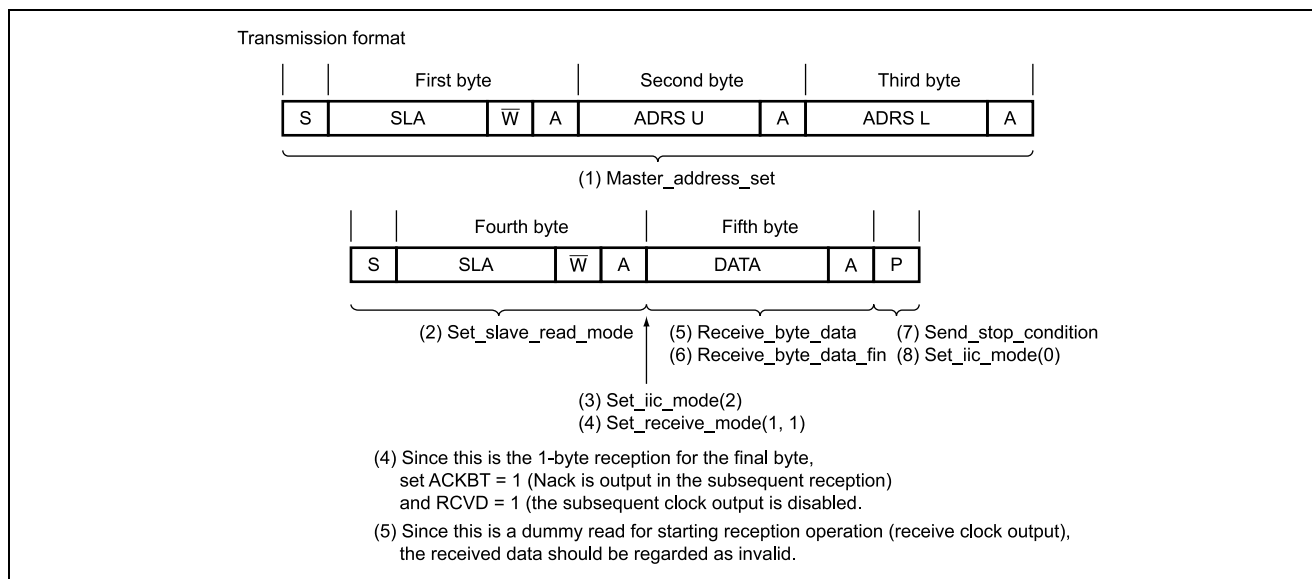
(2) Data (unsigned char) ; received data (lower 8 bits)

3. Processing

Transmits to the slave device the slave address (1 byte) and memory address (2 bytes) according to the transmission/reception format, retransmits the slave address (1 byte) in read mode, and reads the data (1 byte) from the memory address in master reception mode.

4. Functions used

- (1) Master_address_set(Device_id, Addr); Transmits slave address and memory address.
- (2) Set_slave_read_mode(Device_id); Retransmits slave address in read mode.
- (3) Set_iic_mode(2); Sets master reception mode.
- (4) Set_receive_mode(1, 1); Sets reception mode (ACKBT = 1, RCVD = 1).
- (5) Receive_byte_data(); Receives data
- (6) Receive_byte_data_fin(); Gets the finally received data.
- (7) Send_stop_condition(); Issues stop condition.
- (8) Set_iic_mode(0); Sets slave reception mode.



4.5.3 1-page write (N-byte write)

1. Function Name

Master_page_write(Device_id, Addr, Length, *buff_ptr)

1-page write (N-byte write)

2. Arguments

A. Entry

- (1) Device_id (unsigned char); Slave address code: 0 to 7 (A2, A1, A0)
- (2) Addr (unsigned short); Write start memory address (2 bytes)
- (3) Length (unsigned char); Write byte length N (specify within 1 page)
- (4) *buff_ptr (unsigned char); First address of the write data storage buffer

B. Return

- (1) Err_code (unsigned char); error code
 - 0: Normal termination
 - 2: Second byte acknowledgement error (upper 8 bits of memory address)
 - 3: Third byte acknowledgement error (lower 8 bits of memory address)
 - 4 to 131 (number of transmitted bytes + 3): Transmission acknowledgement error for the fourth and following bytes (data)
 - TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error
 - TIMEOUT_ERR_ACK: Acknowledgement polling timeout error
 - TIMEOUT_ERR_STOP: Stop condition detection timeout error

Note: The transmit end timeout error is returned as 2 to 131 of Err_code.

3. Processing

Transmits to the slave device the slave address (1 byte) and memory address (2 bytes) according to the transmission/reception format; after that, sequentially transmits the write data of the size specified by Length (N bytes), and writes the data through page writing.

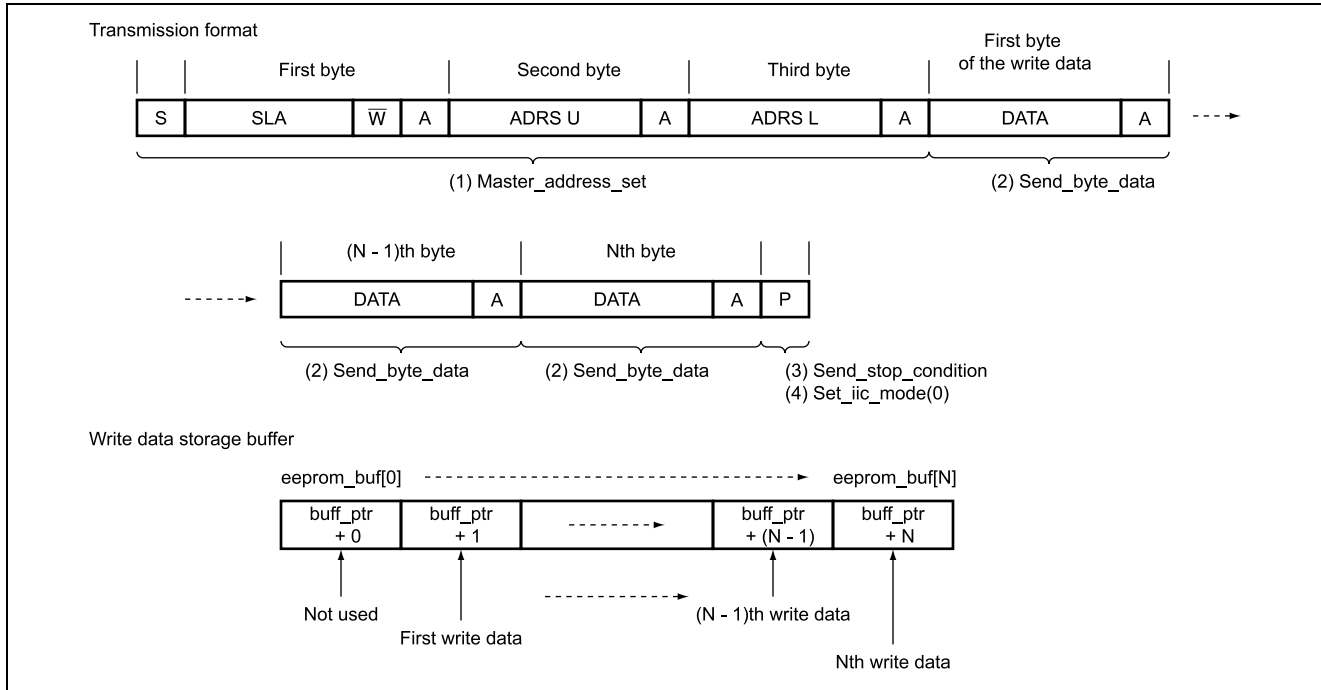
— Write start memory address (Addr) and write byte length (Length) should be set so that the write addresses fall within a page during writing process.

When the address exceeds the range of a page, the write address pointer for EEPROM is rollovers, and overwriting occurs from the first address of the page.

— Write data of the size specified by Length (N bytes) should be written in advance to the write data storage buffer, from its first address + 1 to the first address + N. (The location at the first address of the buffer is not used.)

4. Functions used

- (1) Master_address_set(Device_id, Addr); Transmits slave address and memory address.
- (2) Send_byte_data(Data); Transmits data.
- (3) Send_stop_condition(); Issues stop condition.
- (4) Set_iic_mode(0); Sets slave reception mode.



4.5.4 Sequential read (N-byte read)

1. Function Name

Master_read_sequential(Device_id, Addr, Length, *buff_ptr)

Sequential read (N-byte read)

2. Arguments

A. Entry

- (1) Device_id (unsigned char) ; Slave address code: 0 to 7 (A2, A1, A0)
- (2) Addr (unsigned short) ; Read start memory address (2 bytes)
- (3) Length (unsigned short) ; Read byte length N (more than 2 bytes)
- (4) *buff_ptr (unsigned char) ; First address of the read data storage buffer

B. Return

- (a) Err_code (unsigned char); error code
 - 0: Normal termination
 - 2: Second byte acknowledgement error (upper 8 bits of memory address)
 - 3: Third byte acknowledgement error (lower 8 bits of memory address)
 - ERR_ACK: Slave address (read) acknowledgement error
 - TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error
 - TIMEOUT_ERR_ACK: Acknowledgement polling timeout error
 - TIMEOUT_ERR_RDRF: Data receive end timeout error
 - TIMEOUT_ERR_STOP: Stop condition detection timeout error

3. Processing

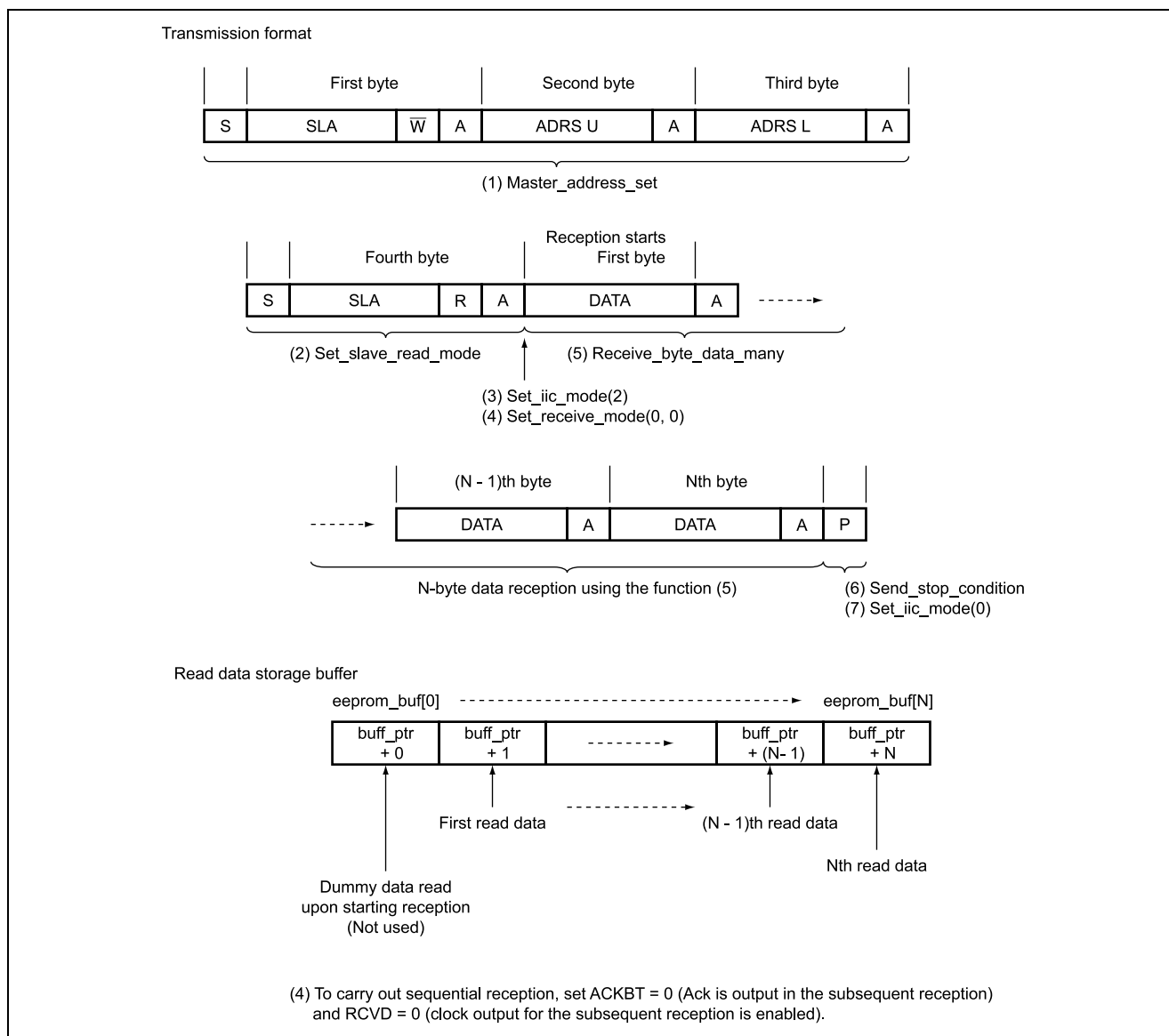
Transmits to the slave device the slave address (1 byte) and memory address (2 bytes) according to the transmission/reception format; after that, retransmits the slave address (1 byte) in read mode, and sequentially reads data (N bytes) from the memory address in master reception mode.

— The read data is sequentially stored in the read data storage buffer from its first address.

In the location at the first address of the buffer, dummy data which has been read upon starting reception is stored. Therefore, valid received data is stored to the addresses from (first address of the buffer + 1) to (first address of the buffer + N).

4. Functions used

- (1) Master_address_set(Device_id, Addr; Transmits slave address and memory address.
- (2) Set_slave_read_mode(Device_id); Retransmits slave address in read mode.
- (3) Set_iic_mode(2); Sets master reception mode.
- (4) Set_receive_mode(0, 0); Sets reception mode (ACKBT = 0, RCVD = 0).
- (5) Receive_byte_data_many(Length, buff_ptr); Receives data (N bytes).
- (6) Send_stop_condition(); Issues stop condition.
- (7) Set_iic_mode(0); Sets slave reception mode.



4.5.5 Transmits slave address and memory address

1. Function Name

Master_address_set (Device_id, Addr)

Transmits slave address and memory address

2. Arguments

A. Entry

(1) Device_id (unsigned char); Slave address code: 0 to 7 (A2, A1, A0)

(2) Addr (unsigned short) ; Memory address (2 bytes)

B. Return

(1) Err_code (unsigned char); error code

0: Normal termination

2: Second byte acknowledgement error (upper 8 bits of memory address)

3: Third byte acknowledgement error (lower 8 bits of memory address)

TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error

TIMEOUT_ERR_ACK: Acknowledgement polling timeout error

3. Processing

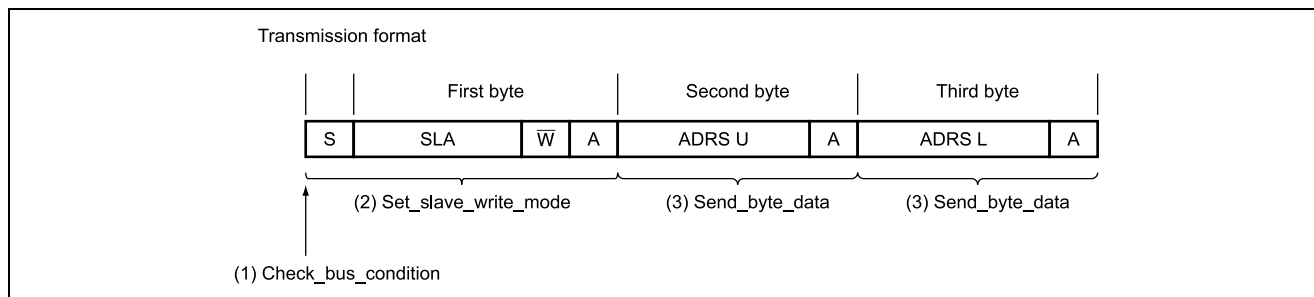
Transmits to the slave device the slave address (1 byte) and memory address (2 byte) according to the transmission/reception format.

4. Functions used

(1) Check_bus_condition(); Checks bus condition.

(2) Set_slave_write_mode(Device_id); Transmits slave address (write mode).

(3) Send_byte_data(Data); Transmits data.



4.5.6 Sequential data reception (for N bytes)

1. Function Name

Receive_byte_data_many (Length, *buff_ptr)

Sequential data reception (for N bytes)

2. Arguments

A. Entry

(1) Length (unsigned short); Read byte length N (2 bytes or more)

(2) *buff_ptr (unsigned char); First address of read data storage buffer

Since dummy data, which is read upon start of reception, is stored to the first address (buff_ptr), valid data of the size specified by Length is stored to (buff_ptr + 1) and following addresses.

B. Return

(1) Err_code (unsigned char); error code

0: Normal termination

TIMEOUT_ERR_RDRF: Data receive end timeout error

3. Processing

Reads data (N bytes) from the slave device sequentially according to the transmission/reception format.

— The read data is sequentially stored in the read data storage buffer from its first address.

In the location at the first address of the buffer, dummy data which has been read upon starting reception is stored. Therefore, valid received data is stored to the addresses from (first address of the buffer + 1) to (first address of the buffer + N).

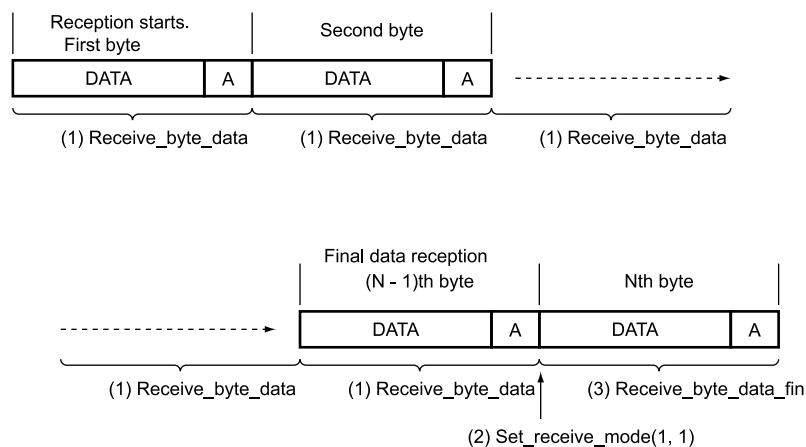
4. Functions used

(1) Receive_byte_data(); Receives 1-byte data.

(2) Set_receive_mode(1, 1); Sets reception mode (ACKBT = 1, RCVD = 1).

(3) Receive_byte_data_fin(); Receives final 1-byte data.

Transmission format



(1) The first data read (first byte) is dummy read for starting reception operation (receive clock output). This invalid received data is stored in eeprombuf[0].

(2) Since this is the final reception for the N-th byte, set ACKBT = 1 (Nack is output in the subsequent reception) and RCVD = 1 (the subsequent clock output is disabled).

4.5.7 Initializes EEPROM bus condition

1. Function Name

Init_eeprom(void)

Initializes EEPROM bus condition

2. Arguments

A. Entry

None; None

B. Return

None; None

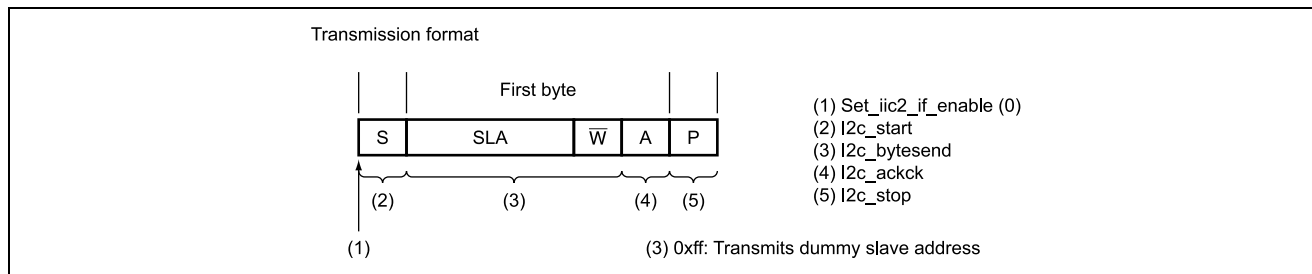
3. Processing

Forcibly initializes EEPROM bus condition by first issuing start condition according to the transmission/reception format via a port, transmitting dummy slave address (0xff), then issuing stop condition.

(This initialization processing is used to forcibly set the SDA bus of the EEPROM in input mode when reception processing from the master device cannot be performed because of the SDA bus of the EEPROM still remaining in output mode due to communication disconnection during data reception from EEPROM.)

4. Functions used

- (1) Set_iic2_if_enable (0); Sets IIC2 I/F module to a halt state.; (SCL/SDA pin to port function)
- (2) I2c_start (); Issues start condition to the IIC device (port processing).
- (3) I2c_bytesend (Tx_data); Transmits byte data to the IIC device (port processing).
- (4) I2c_ackck (); Obtains acknowledgement from the IIC device (port processing).
- (5) I2c_stop (); Issues stop condition to the IIC device (port processing).
- (6) Wait_timer (); Waits for the specified time (countdown until the wait count reaches 0).



4.6 Program Files

Table 4.6.1 shows the program files involved in this application.

Table 4.6.1 Program Files Involved in This Application

No.	Function Name	Description
1	H8_3694_IIC2.H	Register map definitions
2	INIT.SRC	Initialization routine (start up)
3	eeprom.c	Main routine
4	iic2_eeprom.c	Processing functions

4.7 Module configuration diagram

Module configuration of this application program is shown in section 4.7 1. through 7. .

In the following module configuration diagrams, a function is represented as a box (figure 4.7.1) and the hierarchical structure of functions is depicted.

The function numbers correspond to the item numbers in the function lists (table 4.2.1 through 4.2.4). A function number containing a dot indicates that there is any functions called in that function.

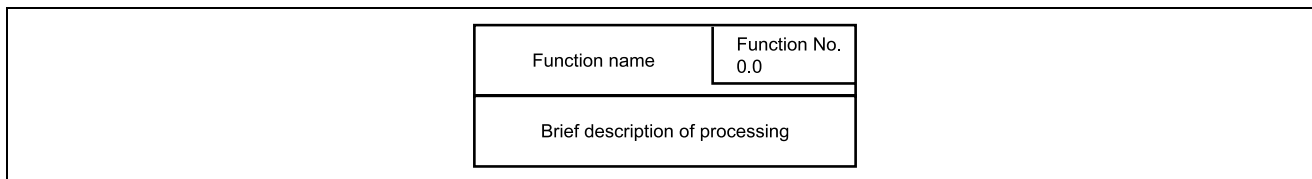
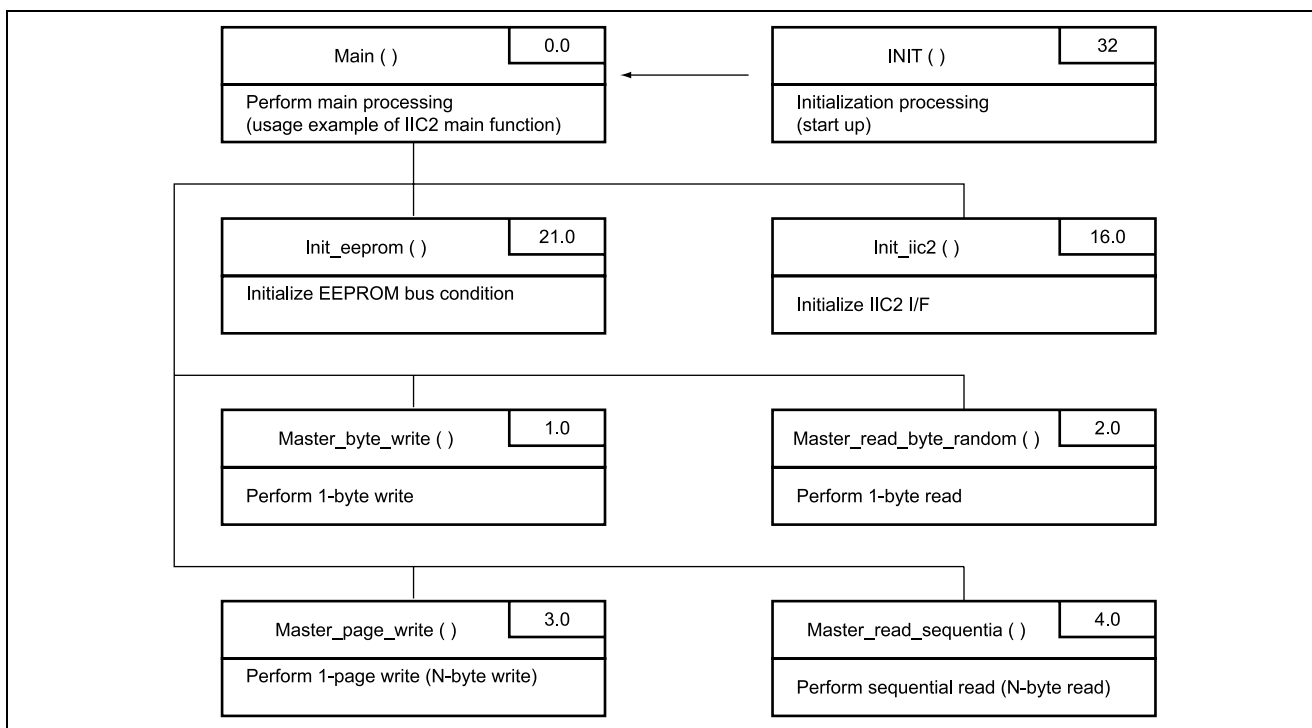
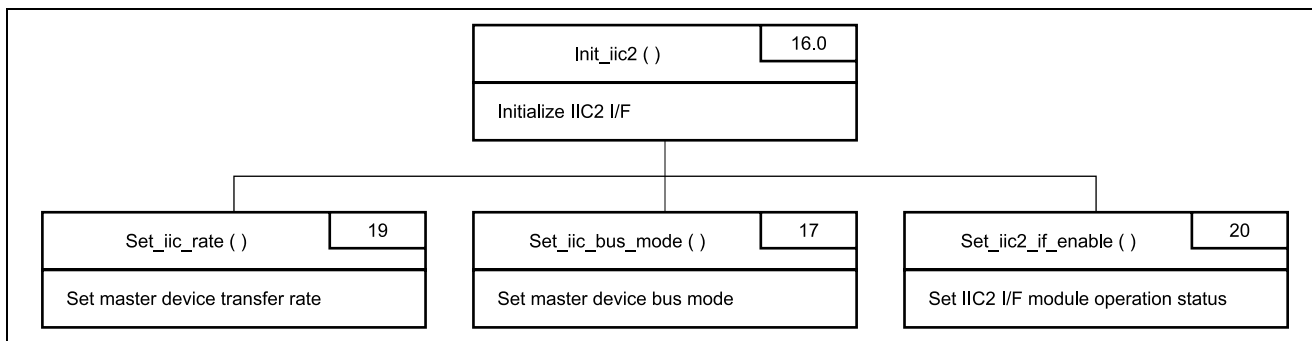


Figure 4.7.1 Representation of a Function

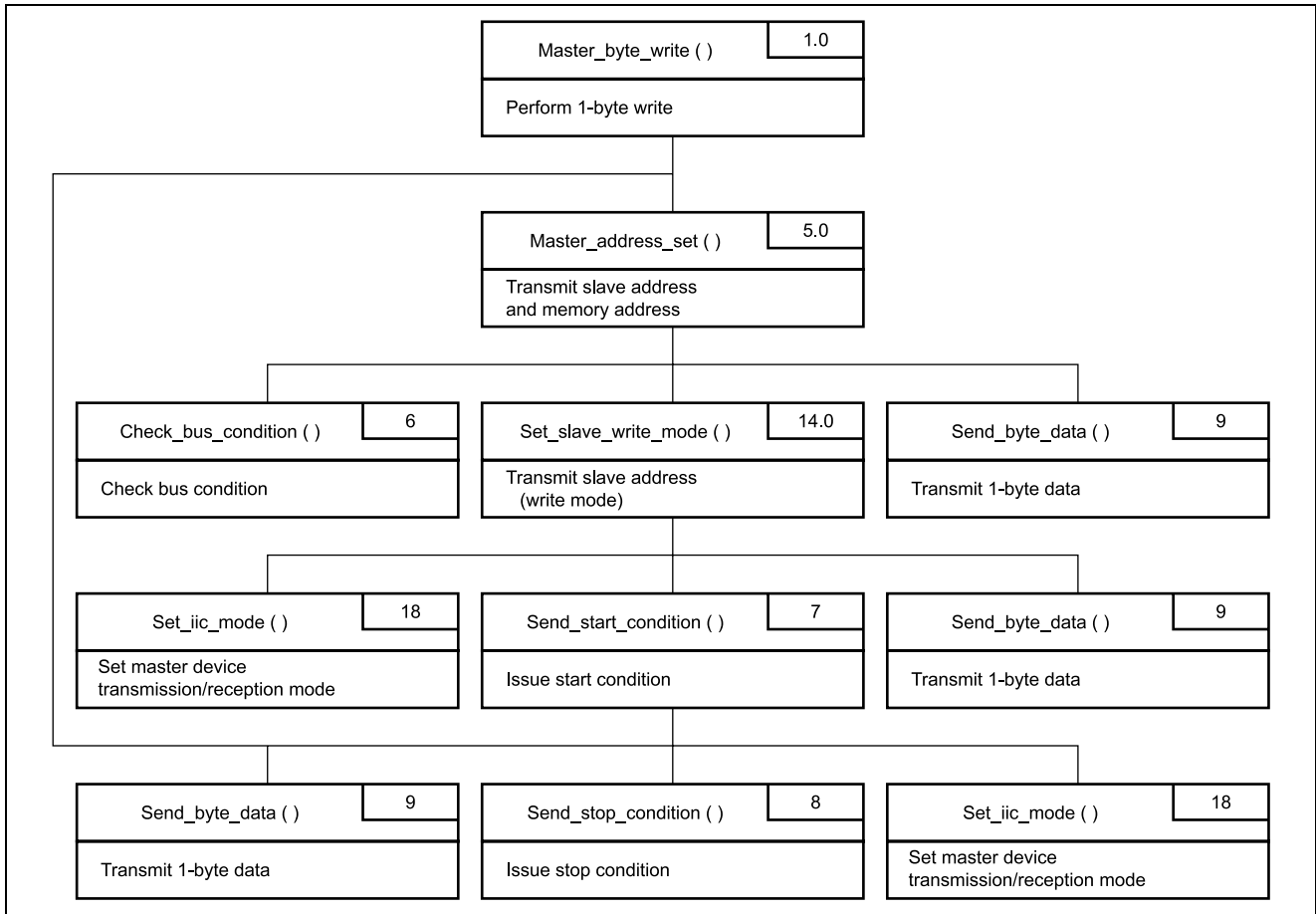
1. Main ()



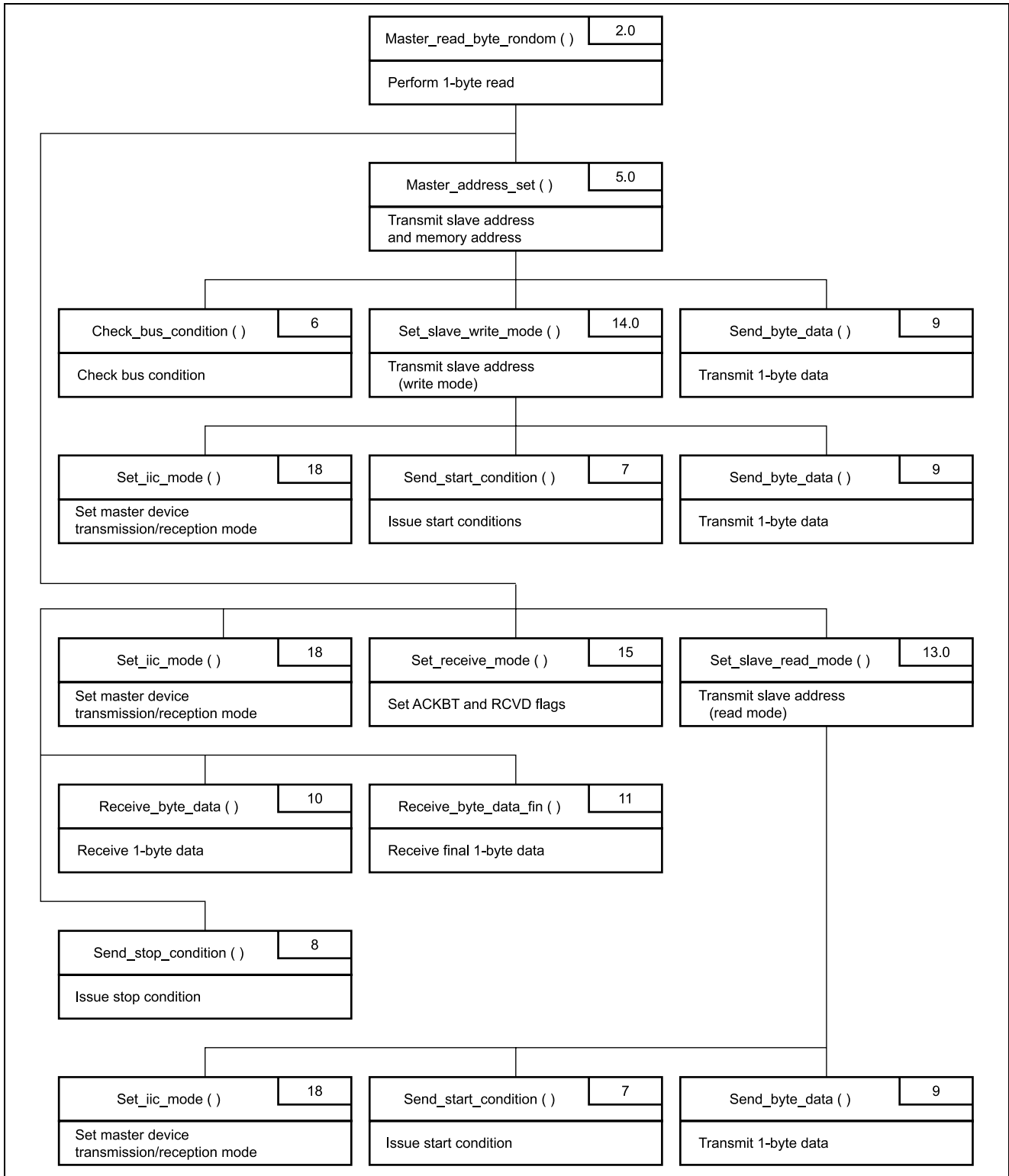
2. Init_iic2 ()



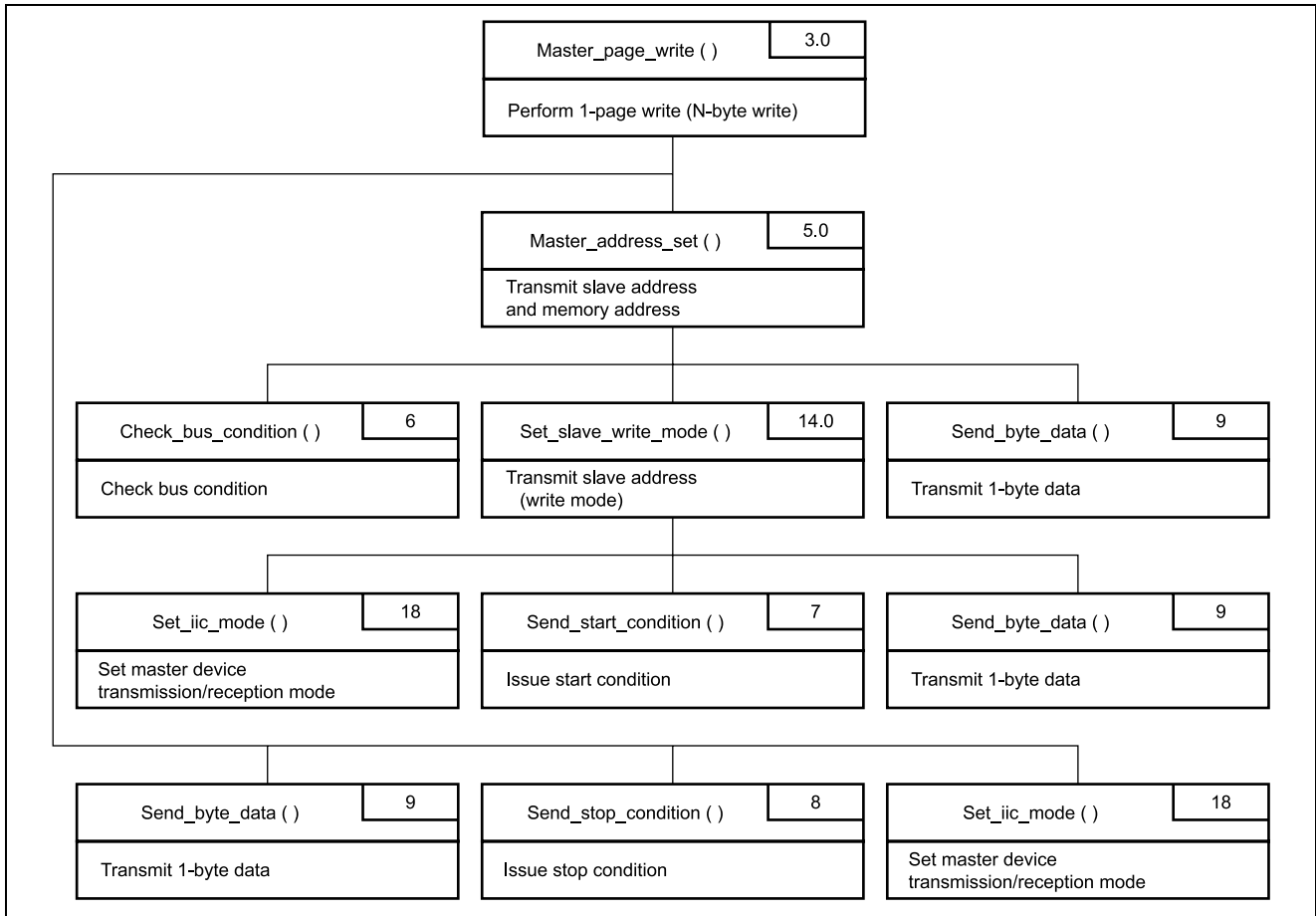
3. Master_byte_write ()



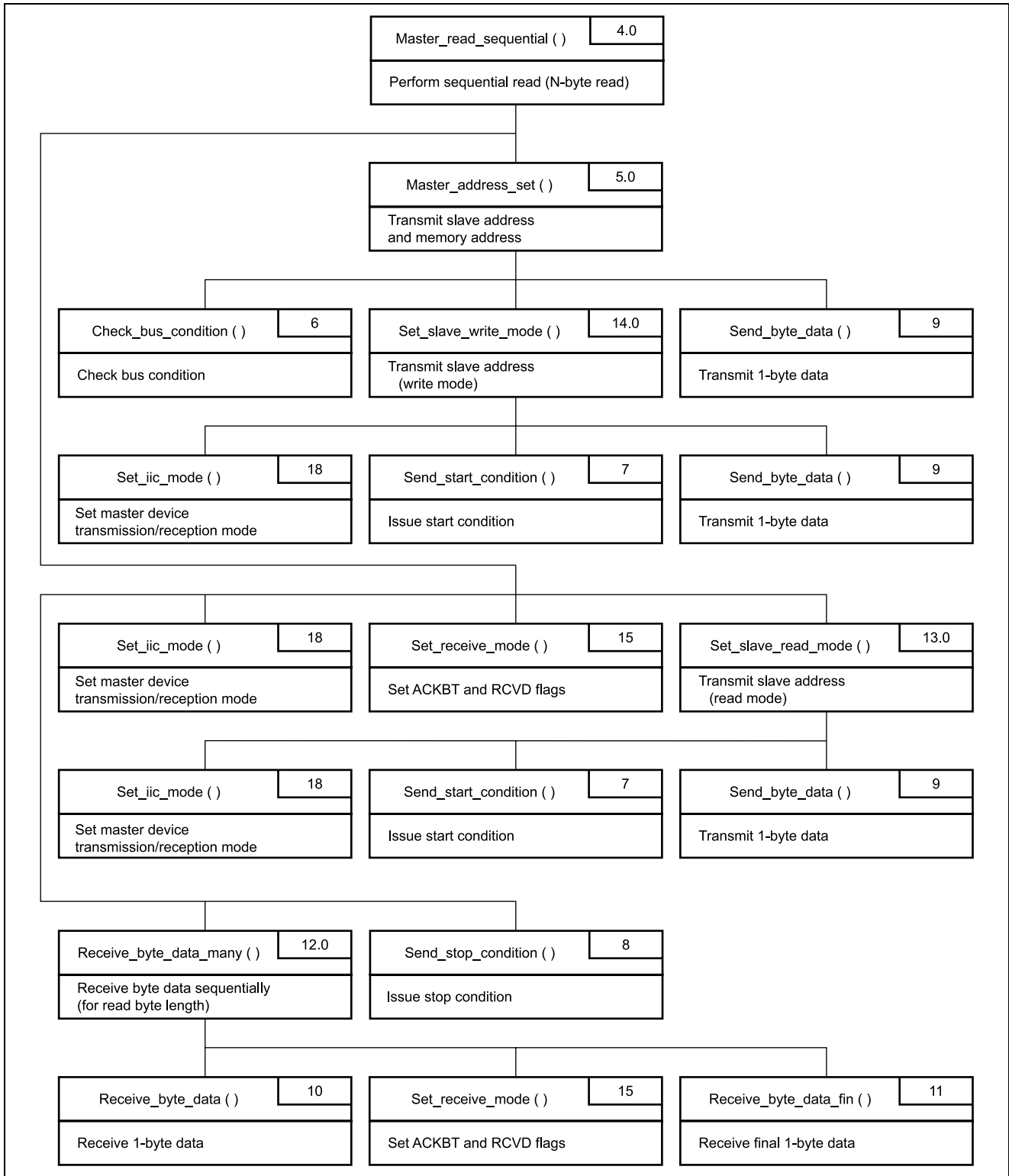
4. Master_read_byte_random ()



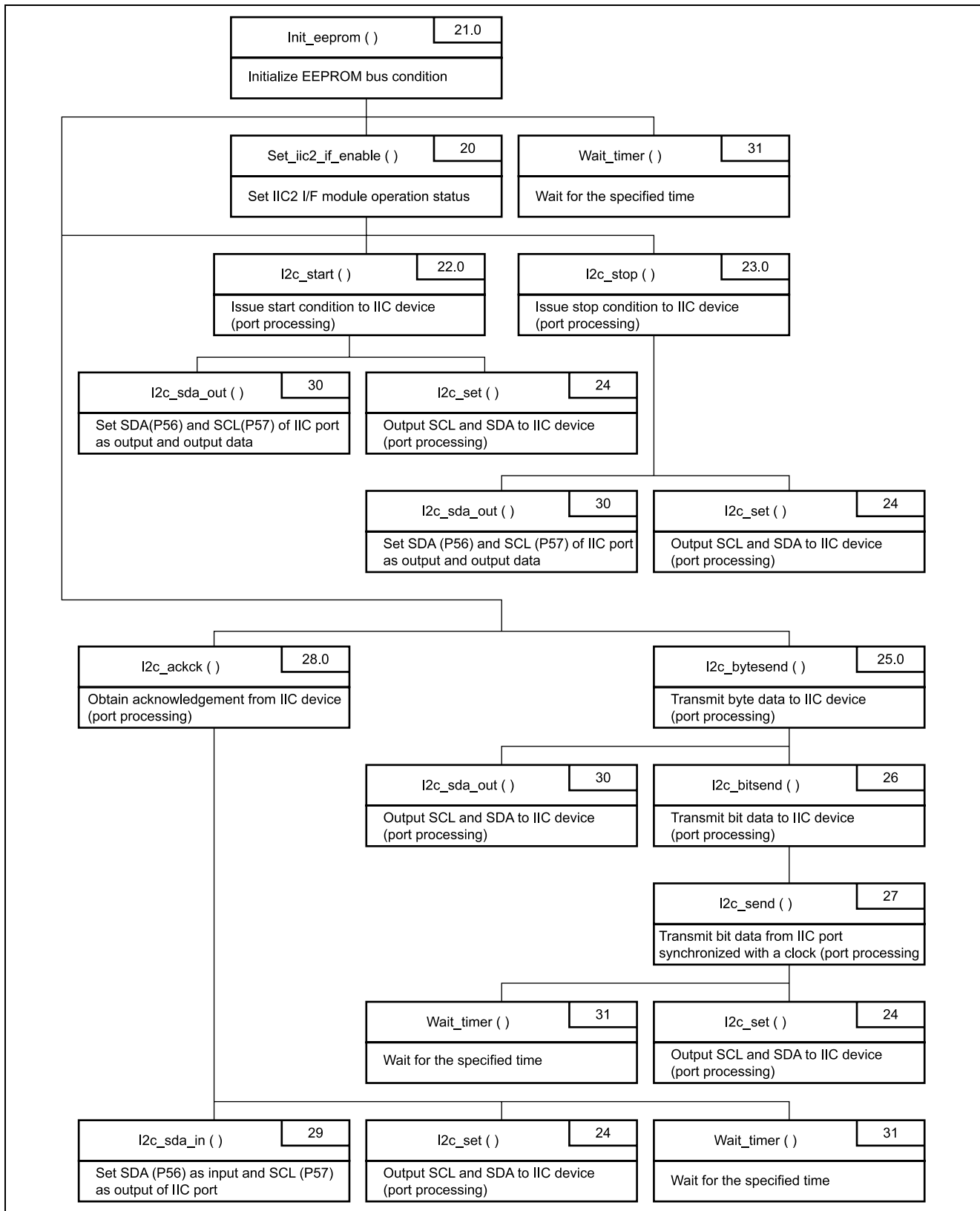
5. Master_page_write()



6. Master_read_sequential ()



7. Init_eeprom ()

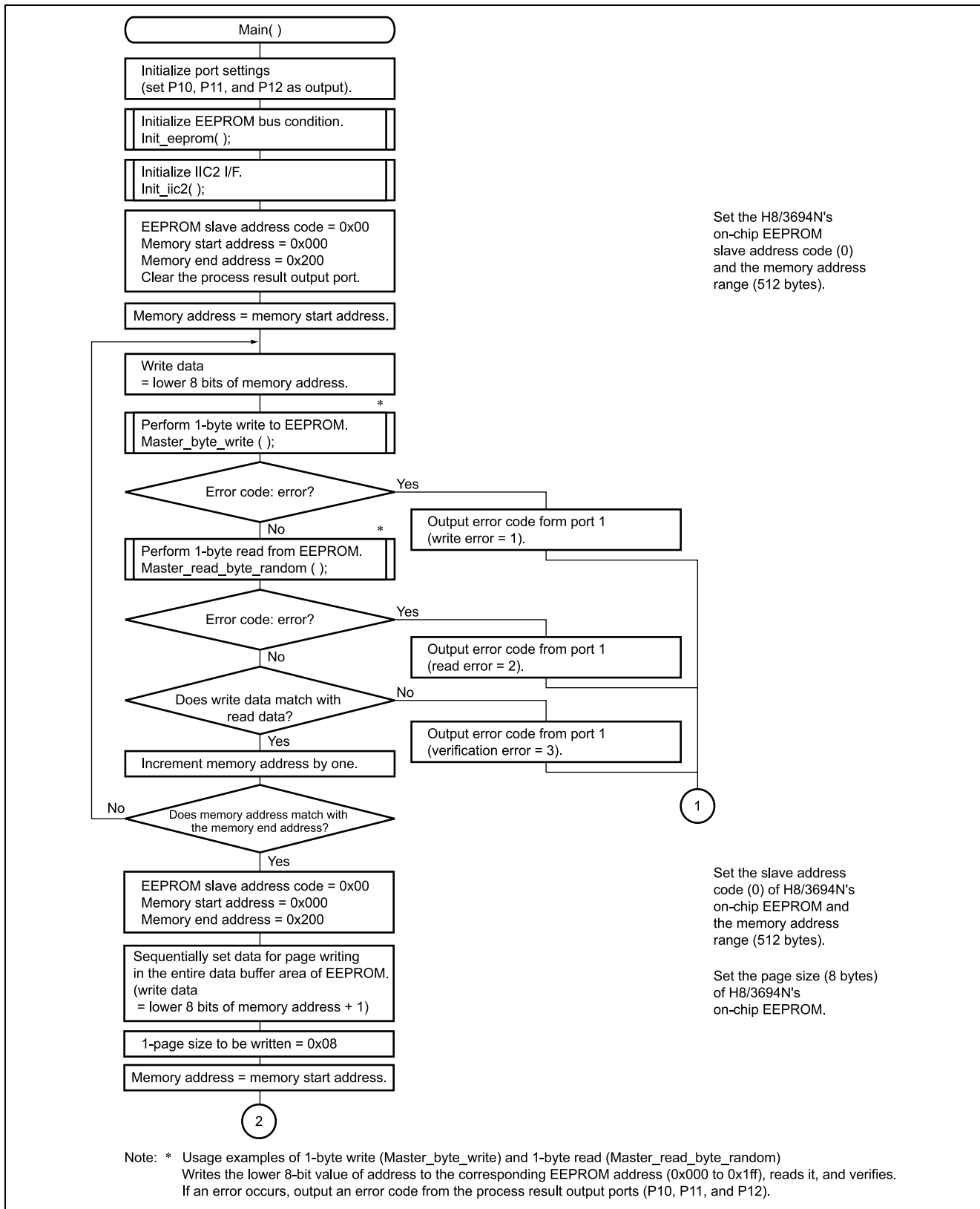


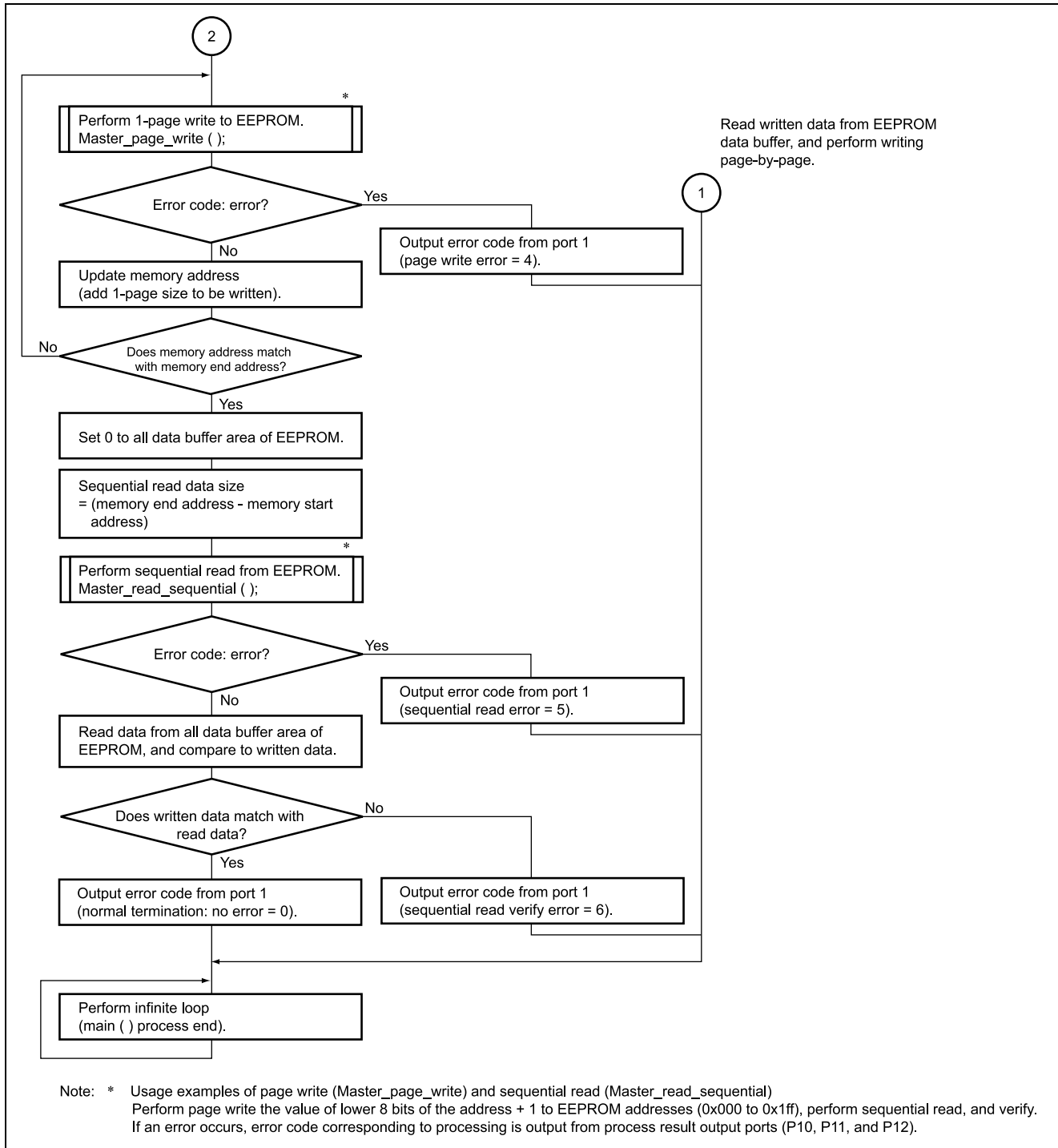
5. Flowchart

Flowcharts of this application program are shown in [0] to [21] and [32].

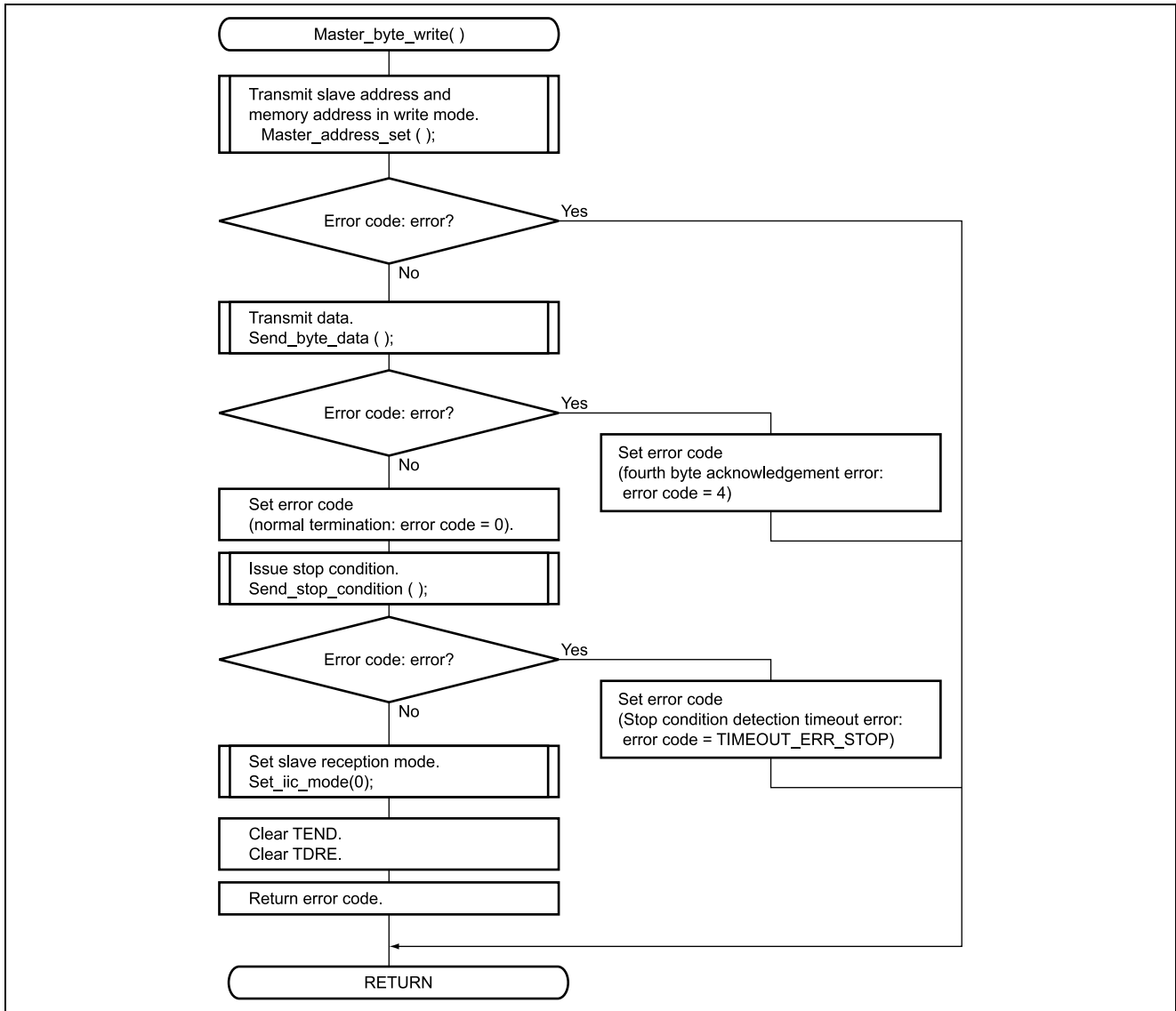
Note that the numbers [0] to [21] and [32] correspond to function number shown in section 4.2, Function Lists (tables 4.2.1 to 4.2.5).

[0] Main () Function: Main processing

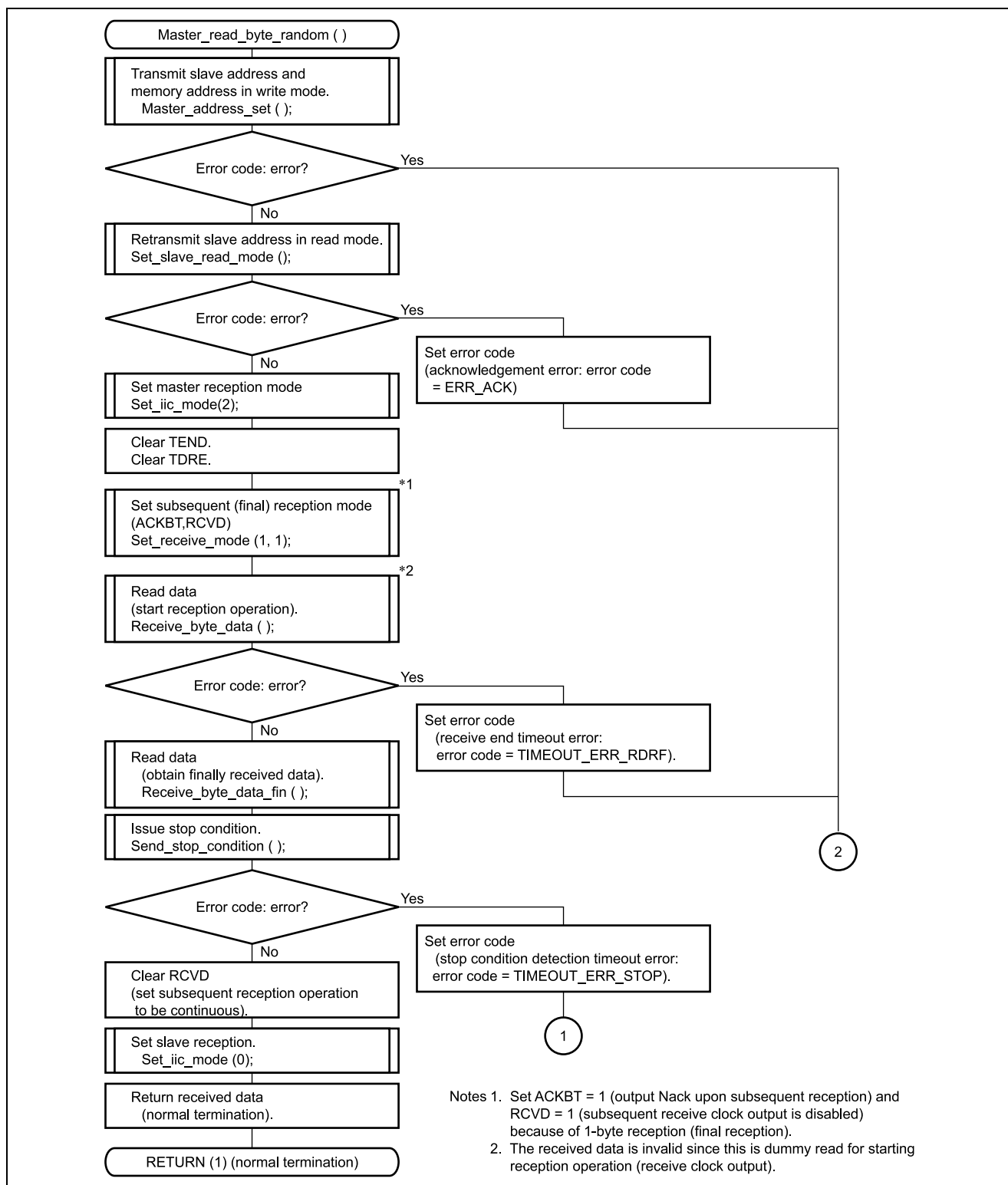


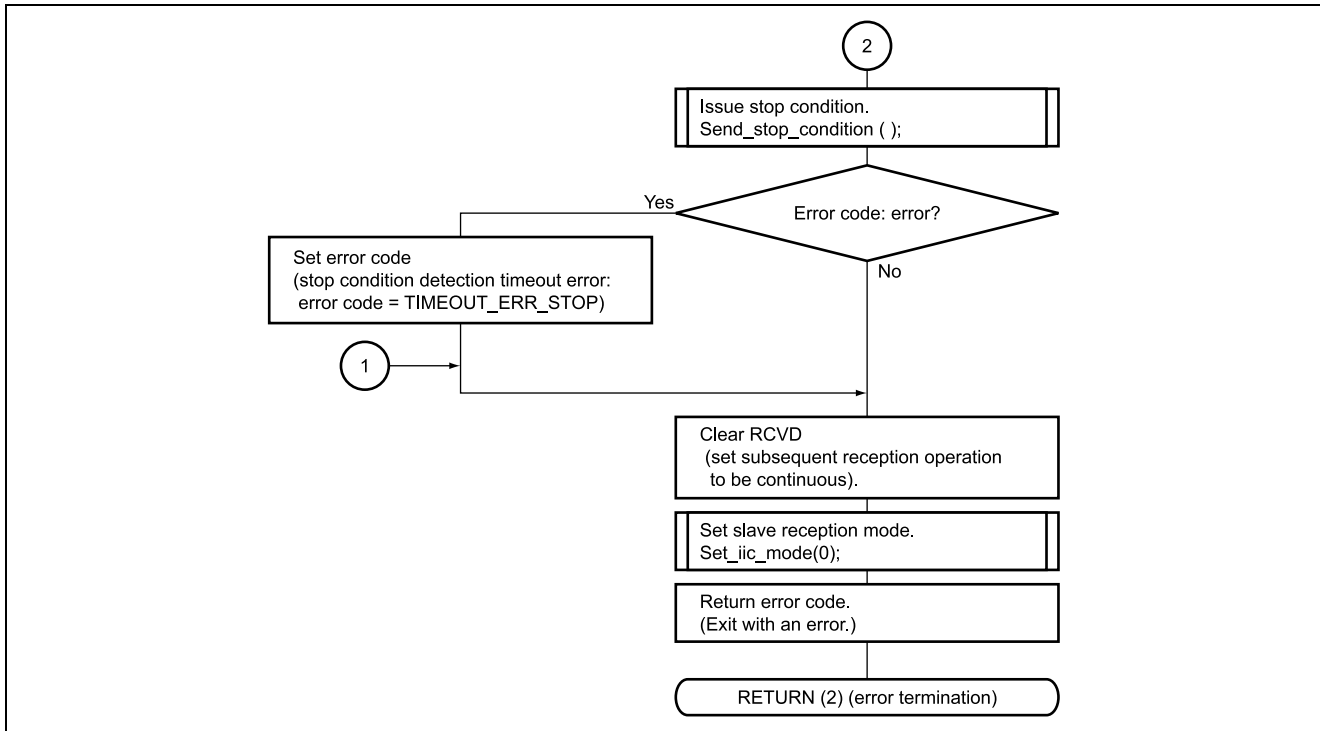


[1] Master_byte_write () Function: 1-byte write

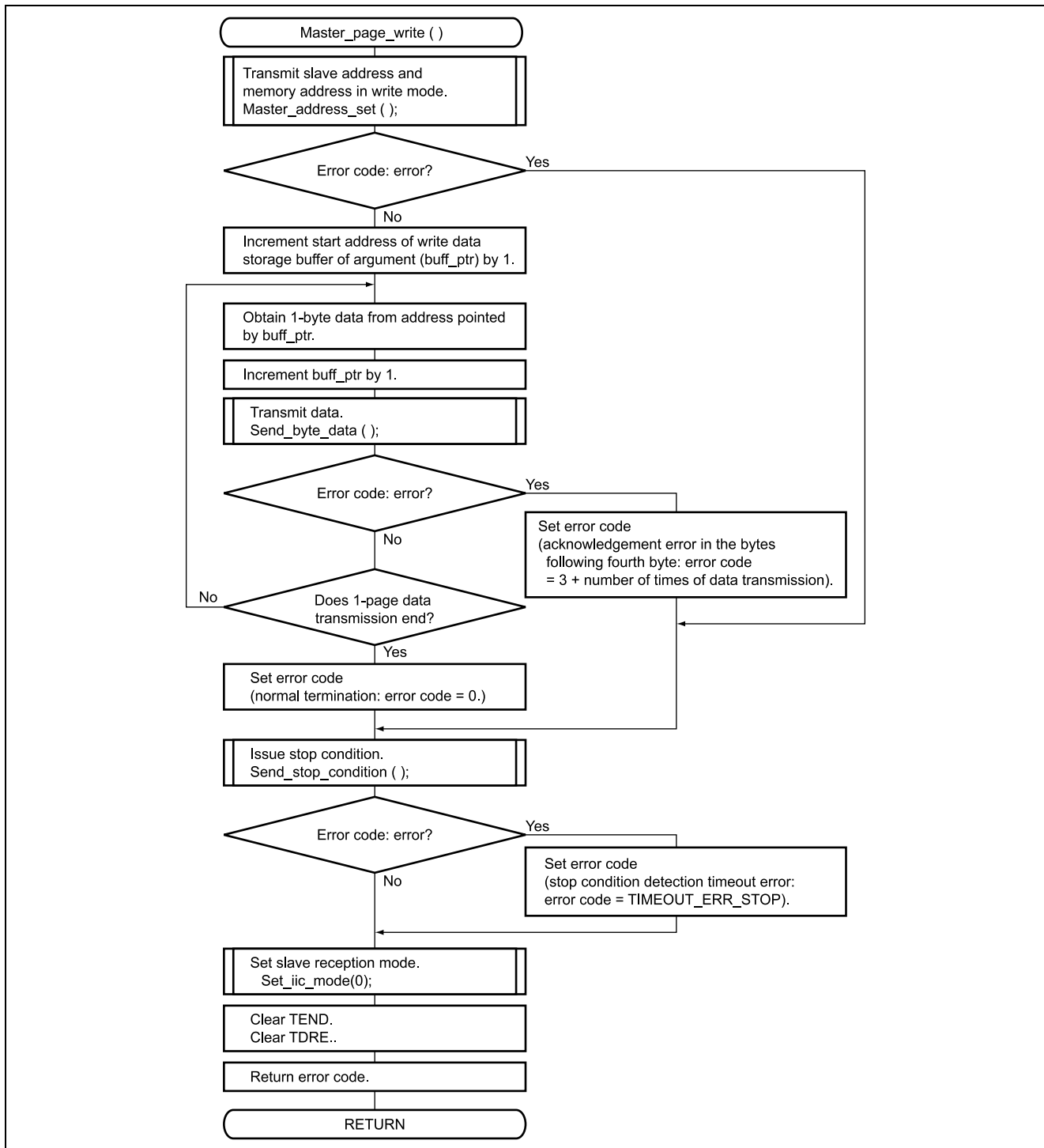


[2] Master_read_byte_random () Function: 1-byte read

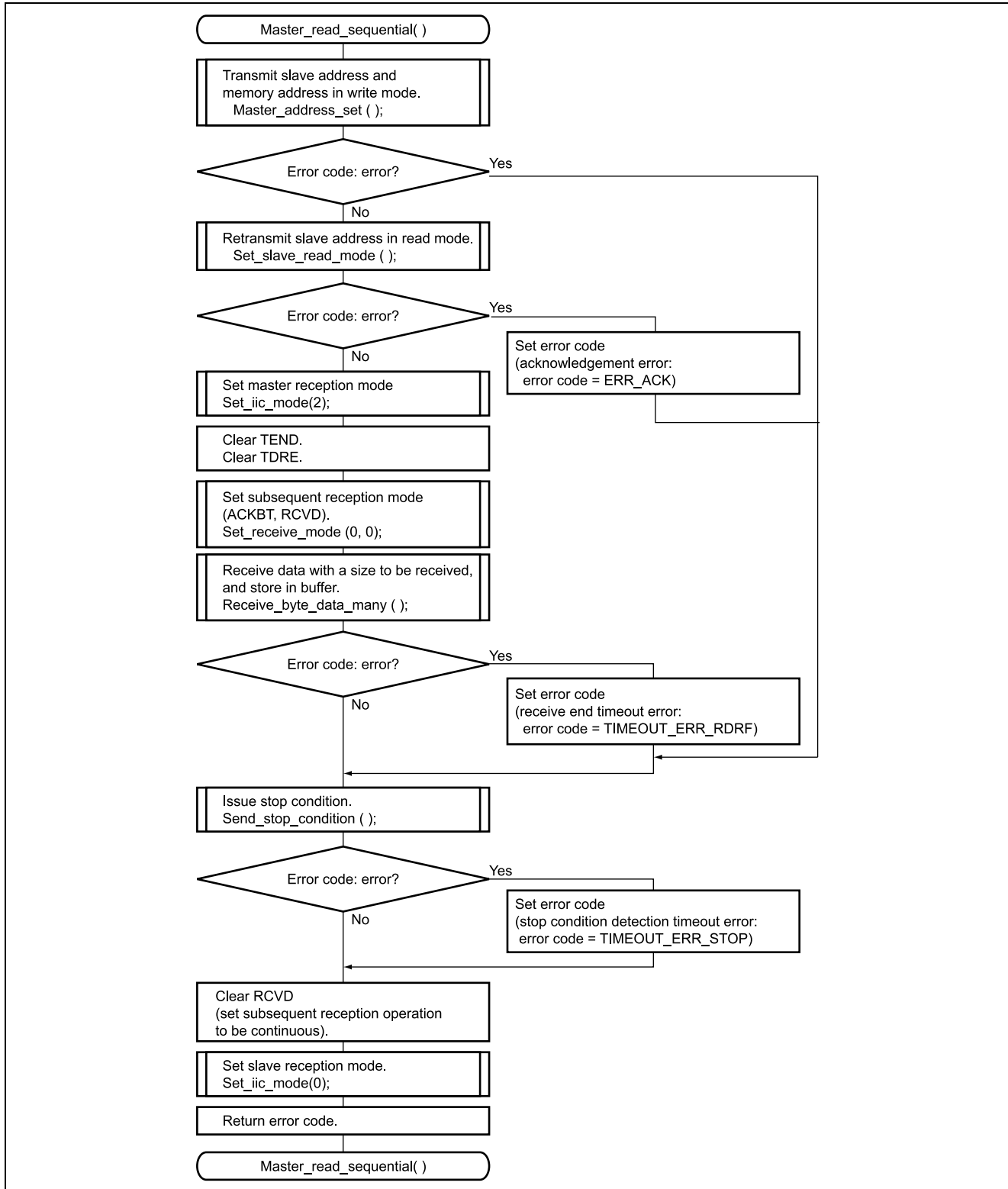




[3] Master_page_write () Function: 1-page write

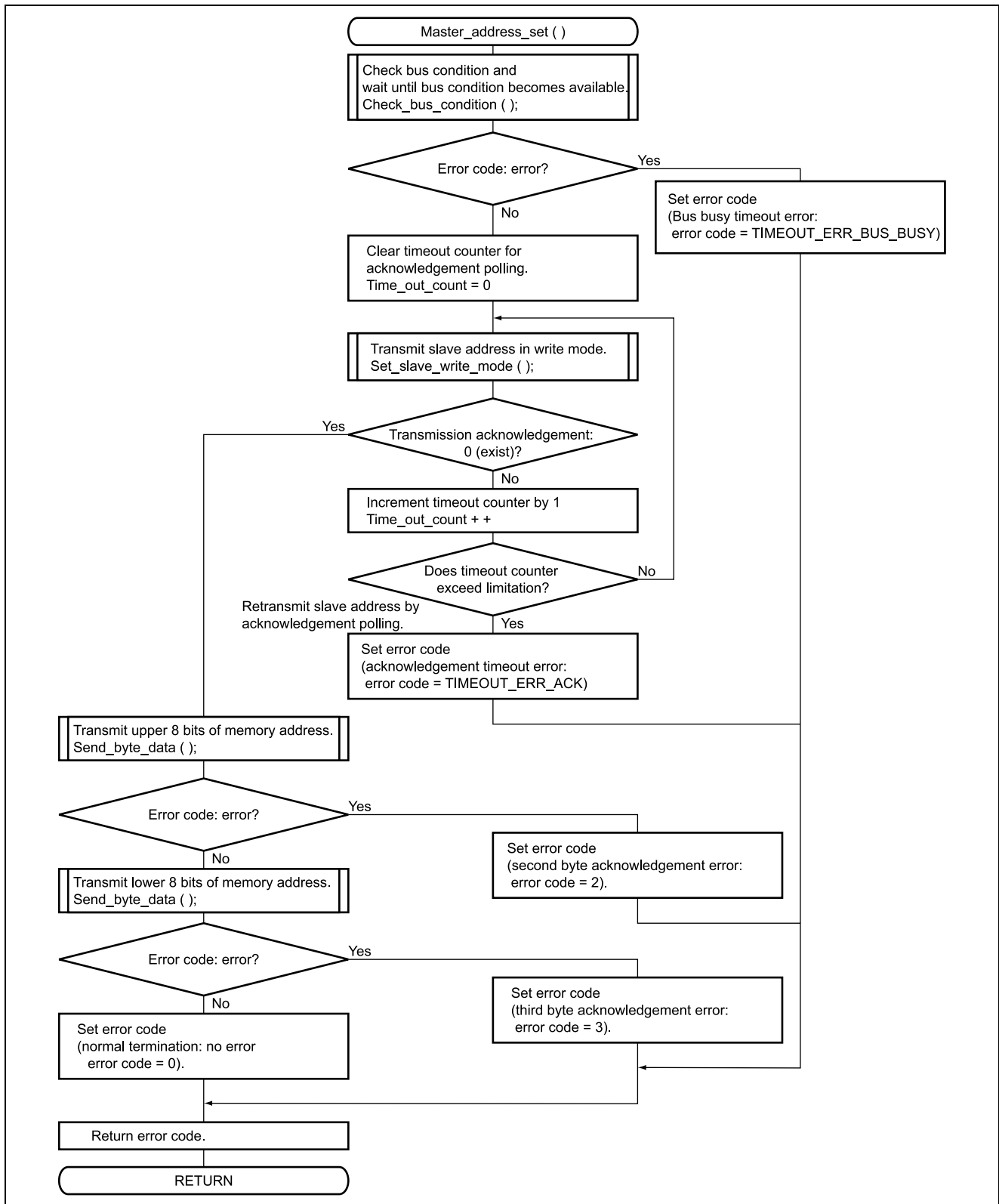


[4] Master_read_sequential() Function: sequential read

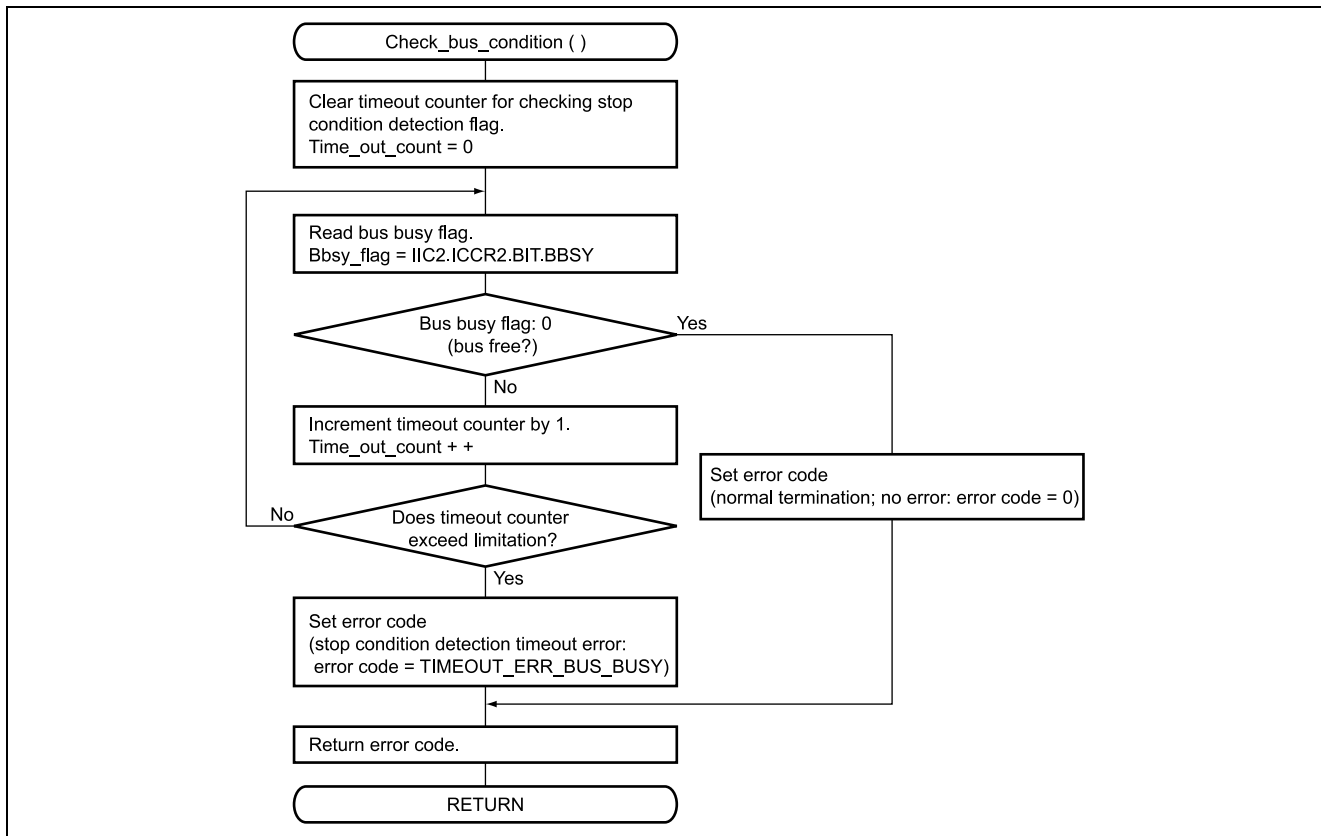


[5] Master_address_set ()

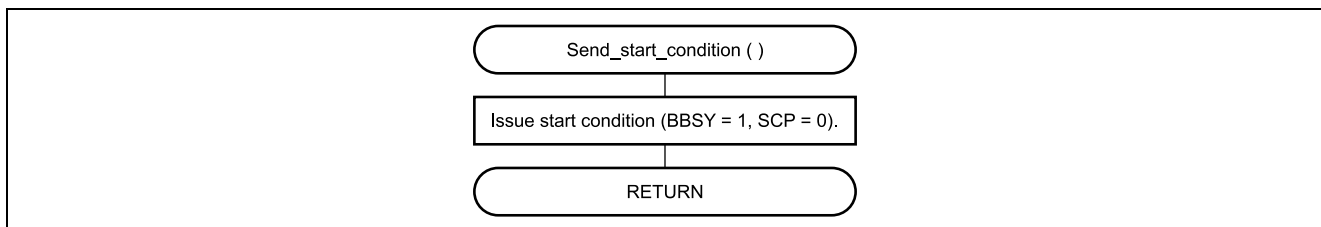
Function: Transmit slave address and memory address



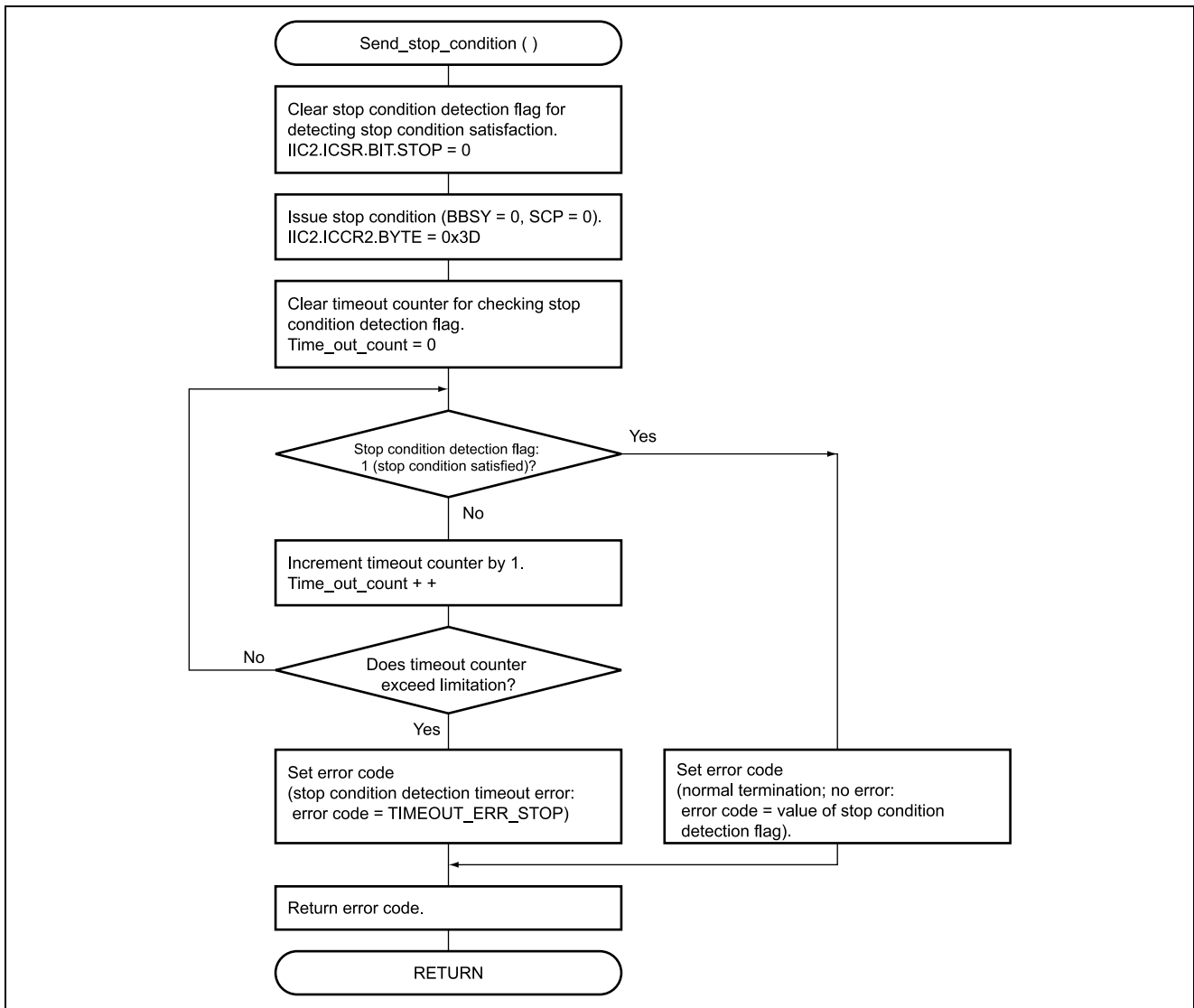
[6] Check_bus_condition () Function: Check IIC bus condition and wait until bus becomes available



[7] Send_start_condition () Function: Issue start condition

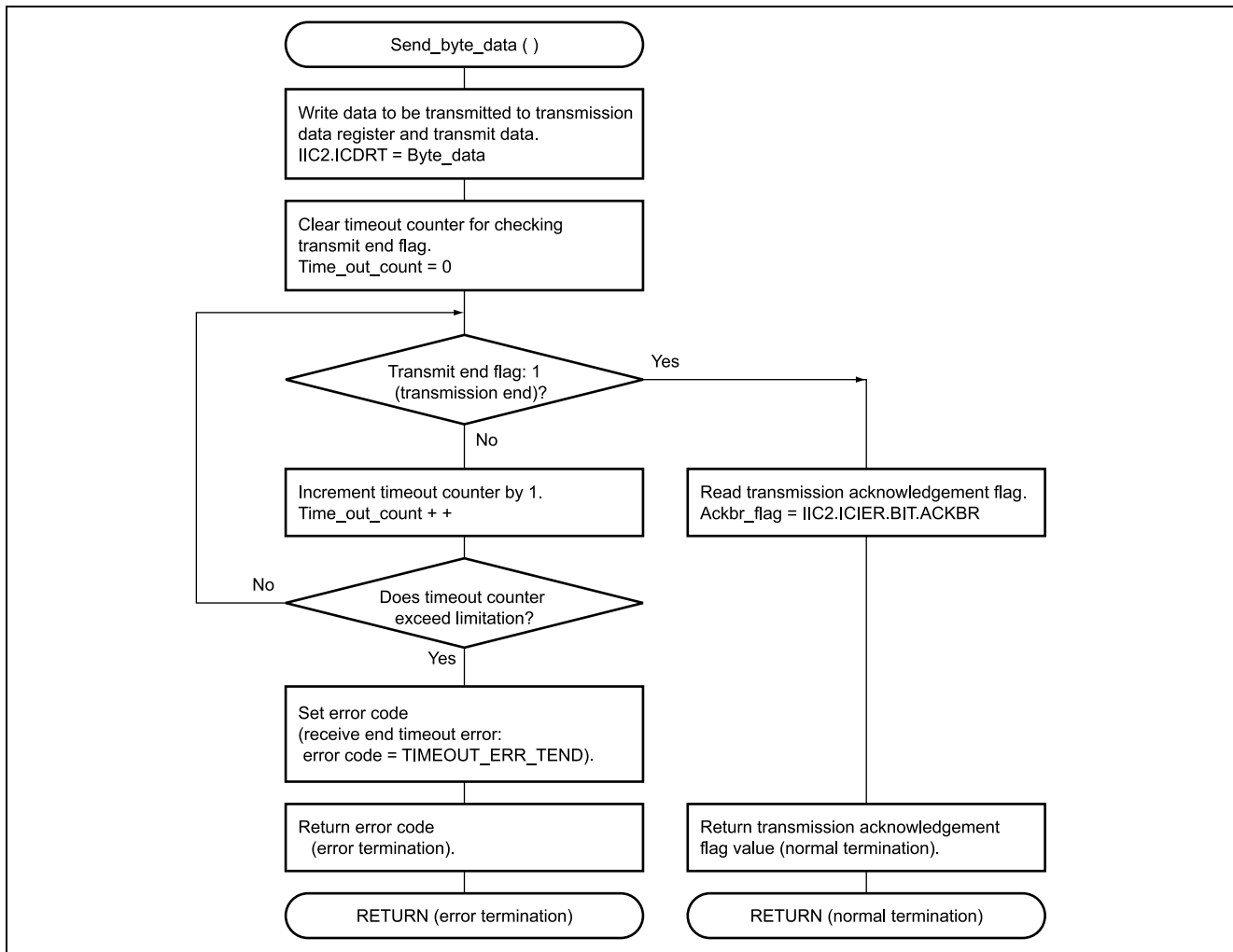


[8] Send_stop_condition () Function: Issue stop condition

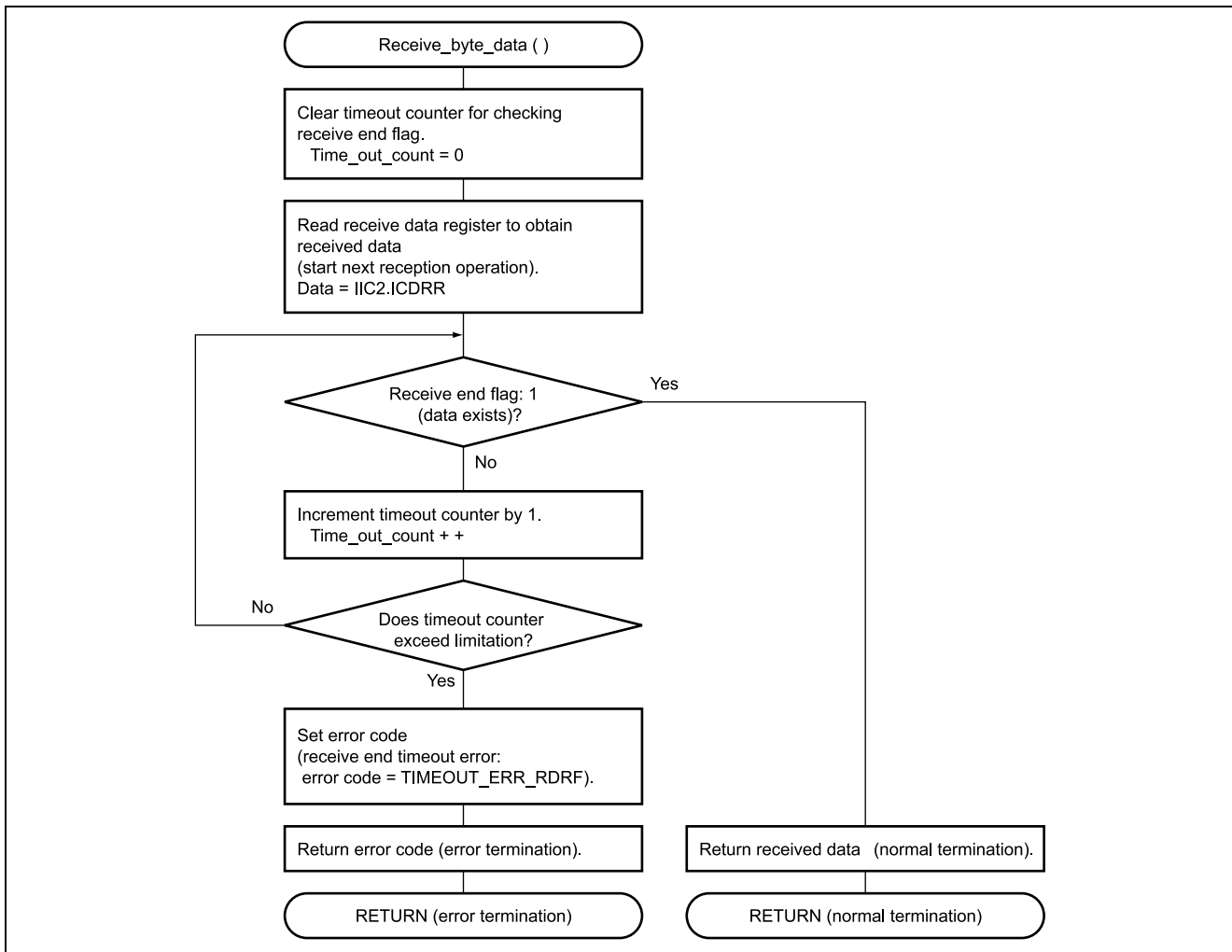


[9] Send_byte_data ()

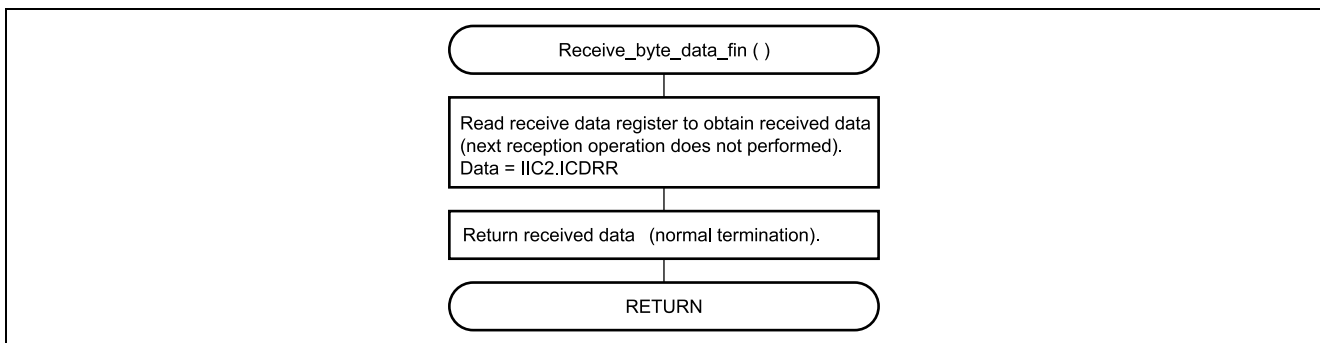
Function: Perform 1-byte data transmission



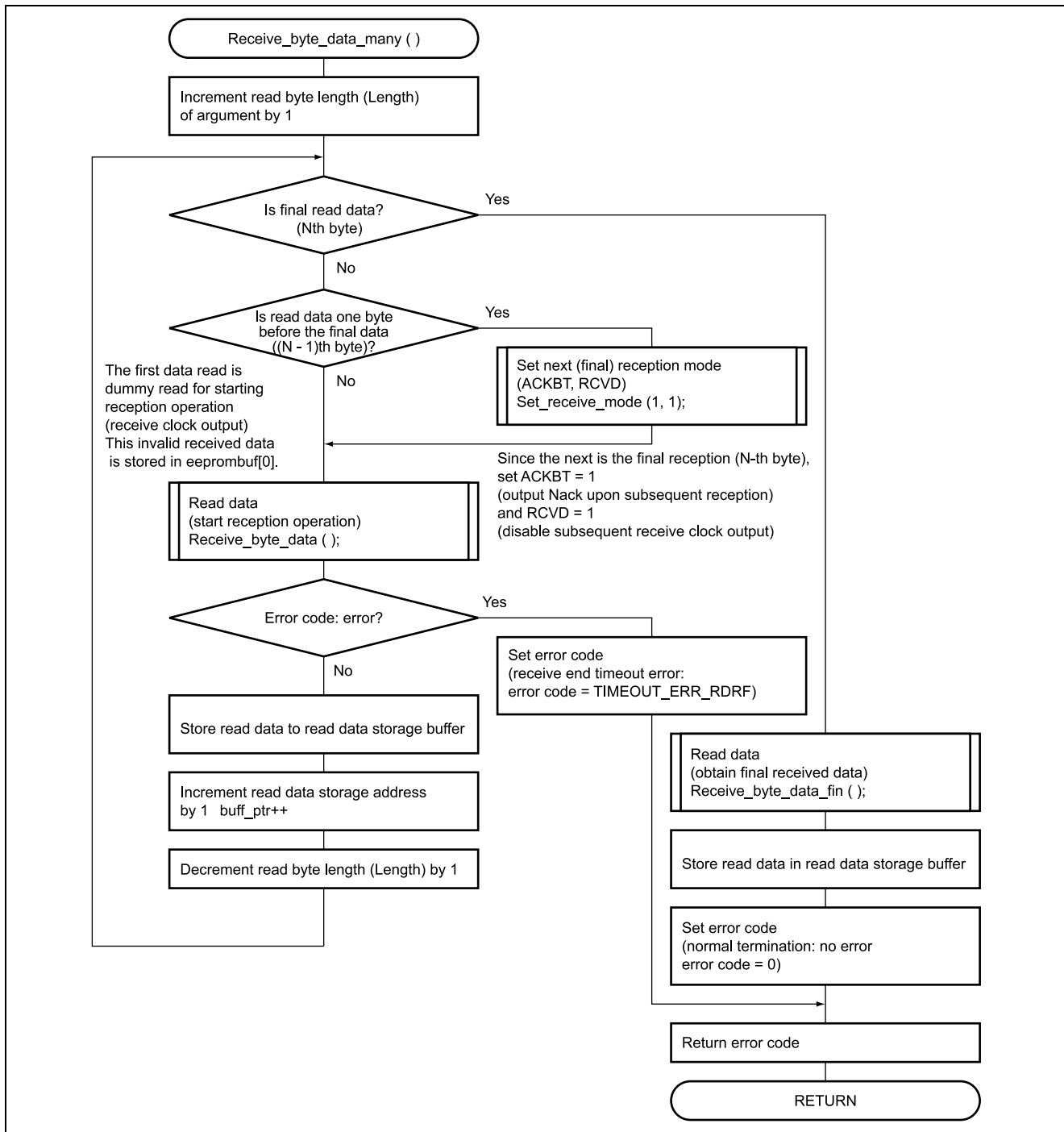
[10] Receive_byte_data () Function: 1-byte data reception



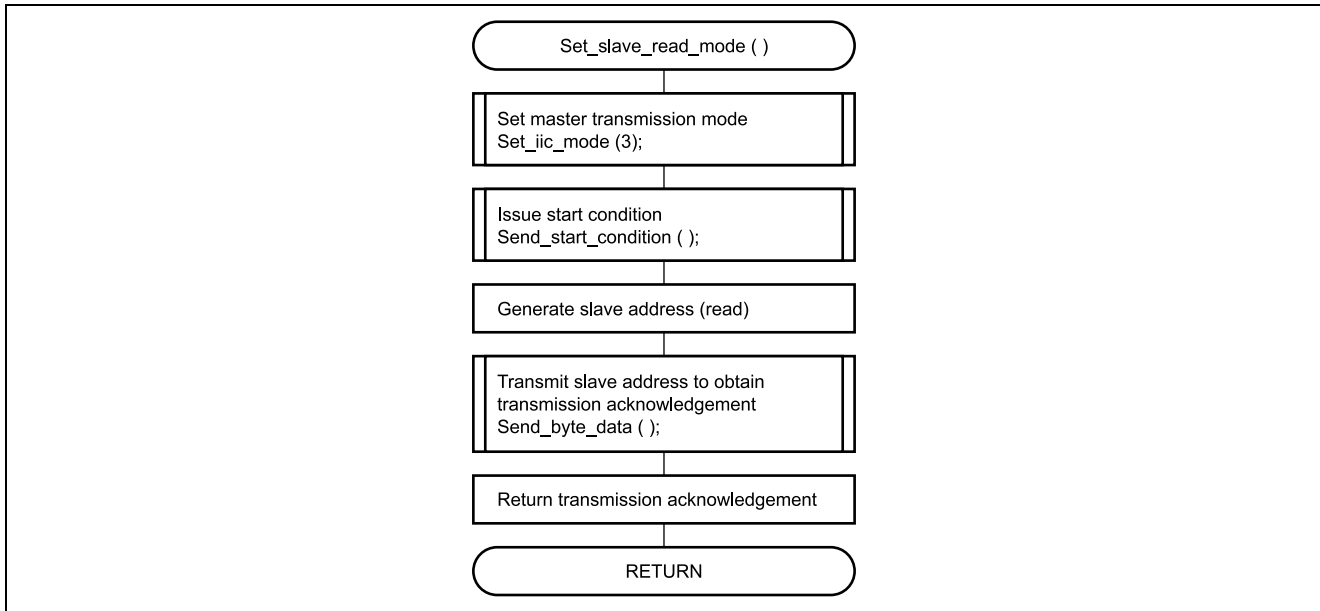
[11] Receive_byte_data_fin () Function: Perform final 1-byte data reception



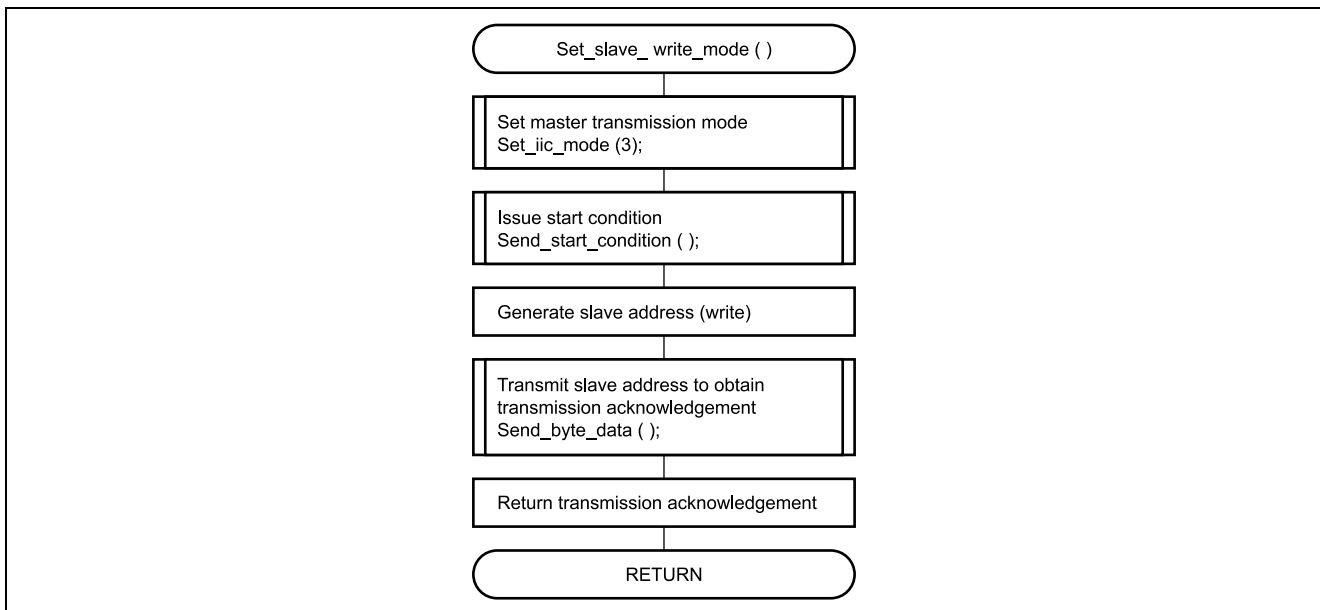
[12] Receive_byte_data_many () (1) Function: Receive byte data sequentially



[13] Set_slave_read_mode () Function: Transmit slave address (read mode)

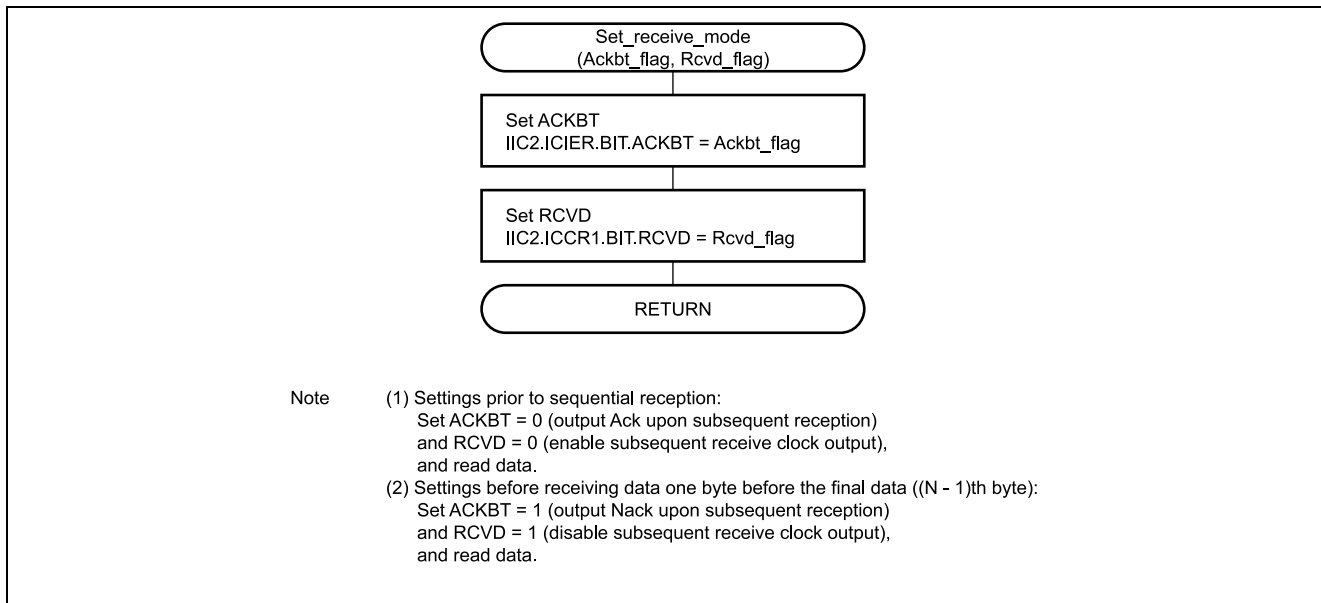


[14] Set_slave_write_mode() Function: Transmit slave address (write mode)



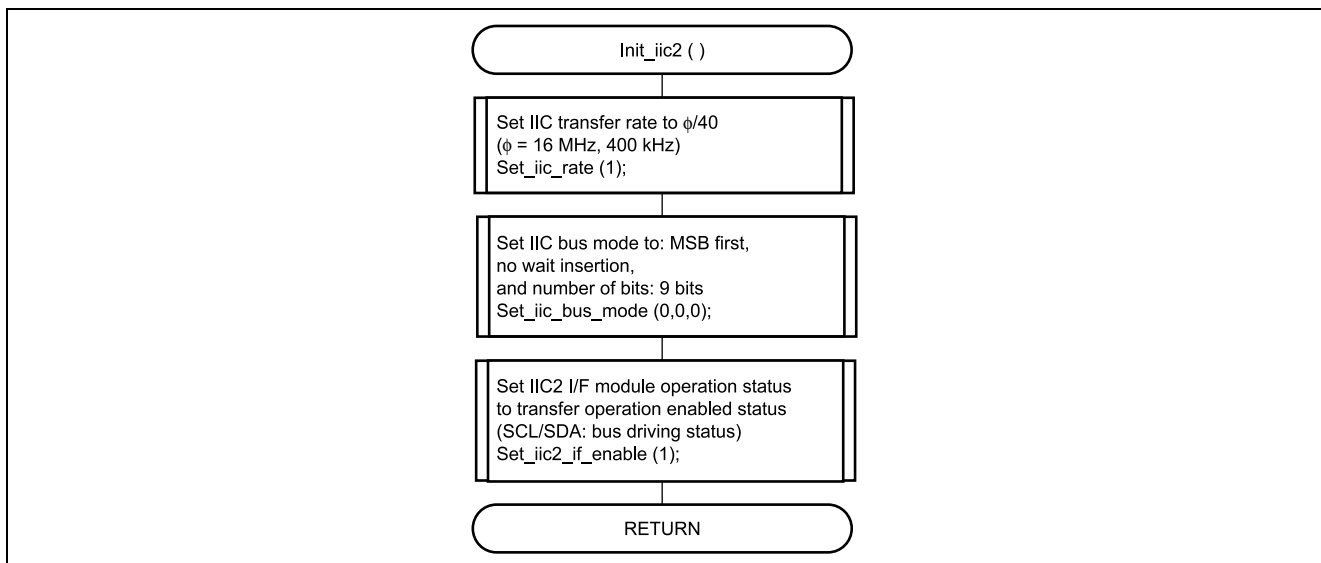
[15] Set_receive_mode ()

Function: Set ACKBT and RCVD flags for receiving data



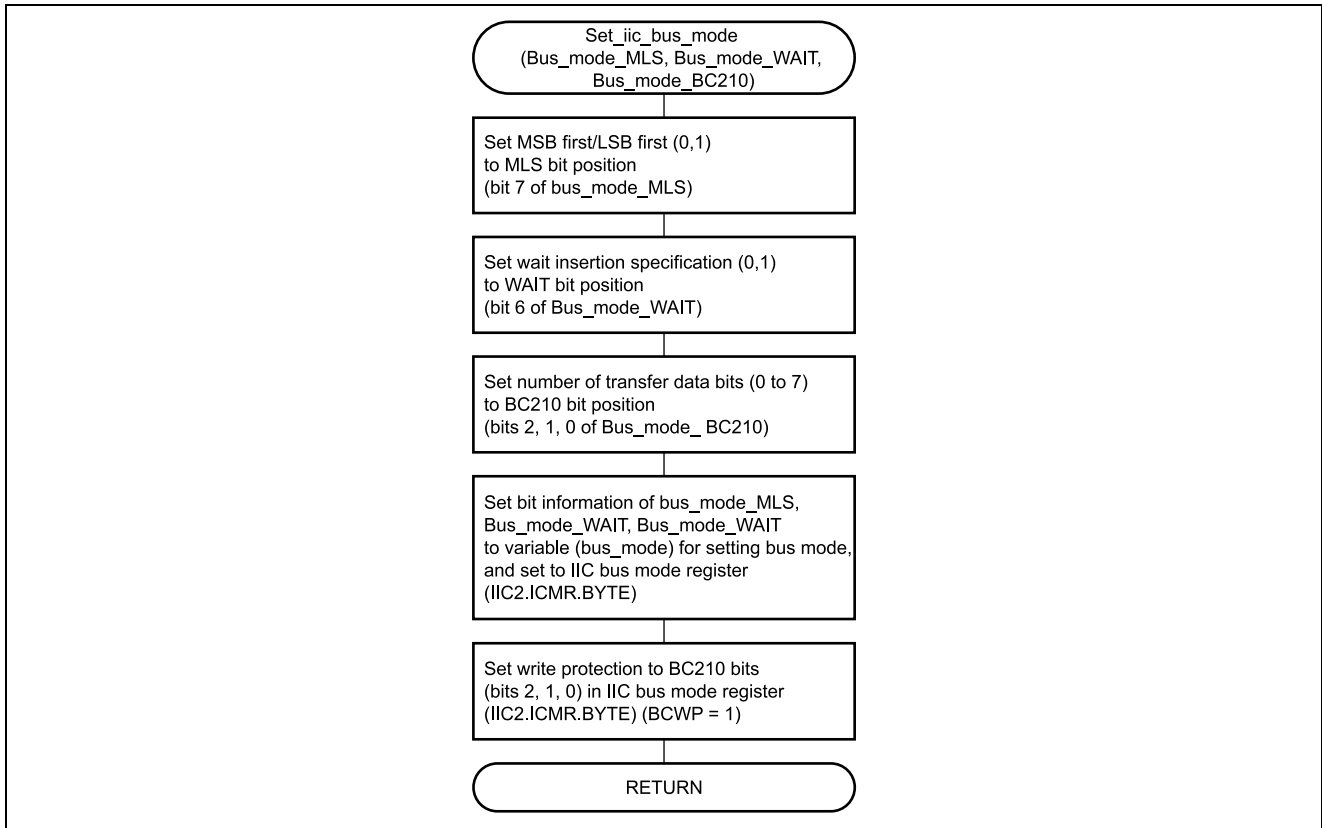
[16] Init_iic2 ()

Function: Initialize IIC2 I/F



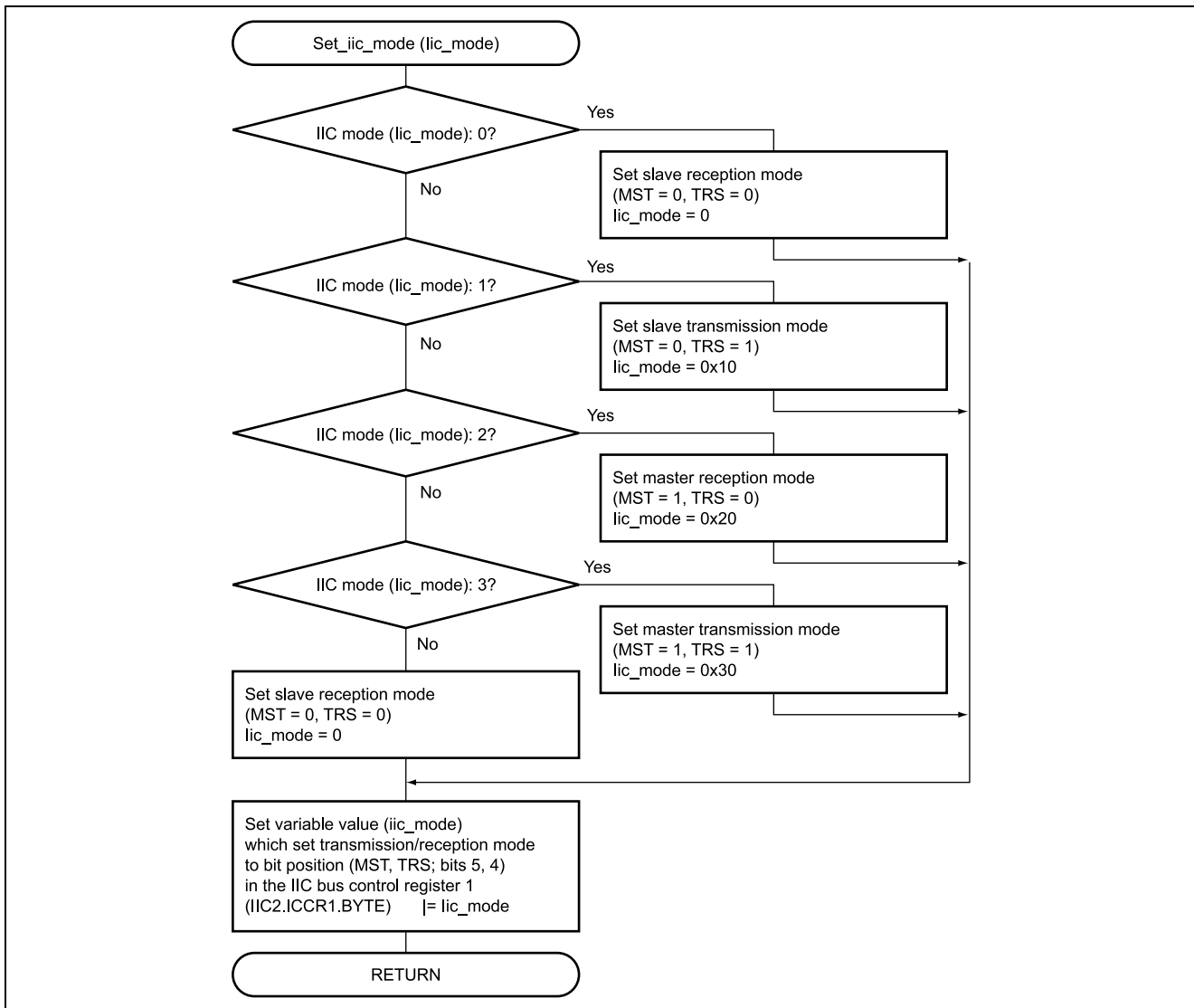
[17] Set_iic_bus_mode ()

Function: Set master device bus mode (MLS, WAIT, BC210)



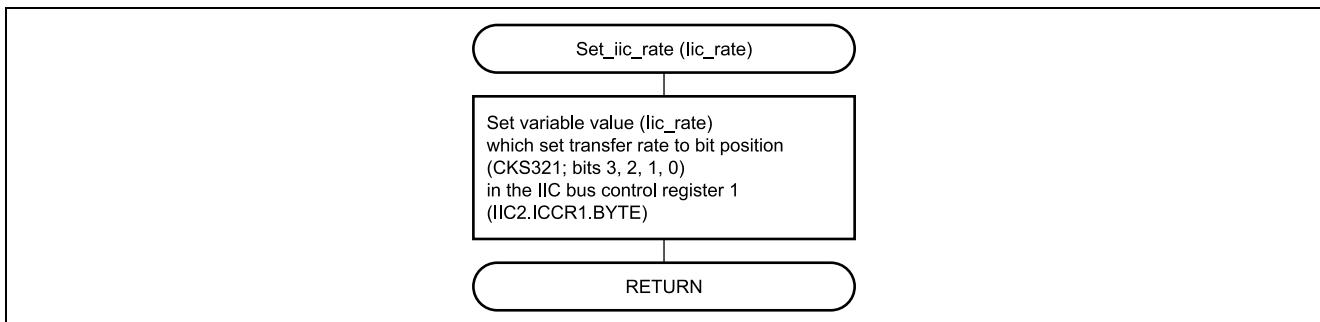
[18] Set_iic_mode ()

Function: Set master device transmission/reception mode (MST, TRS)



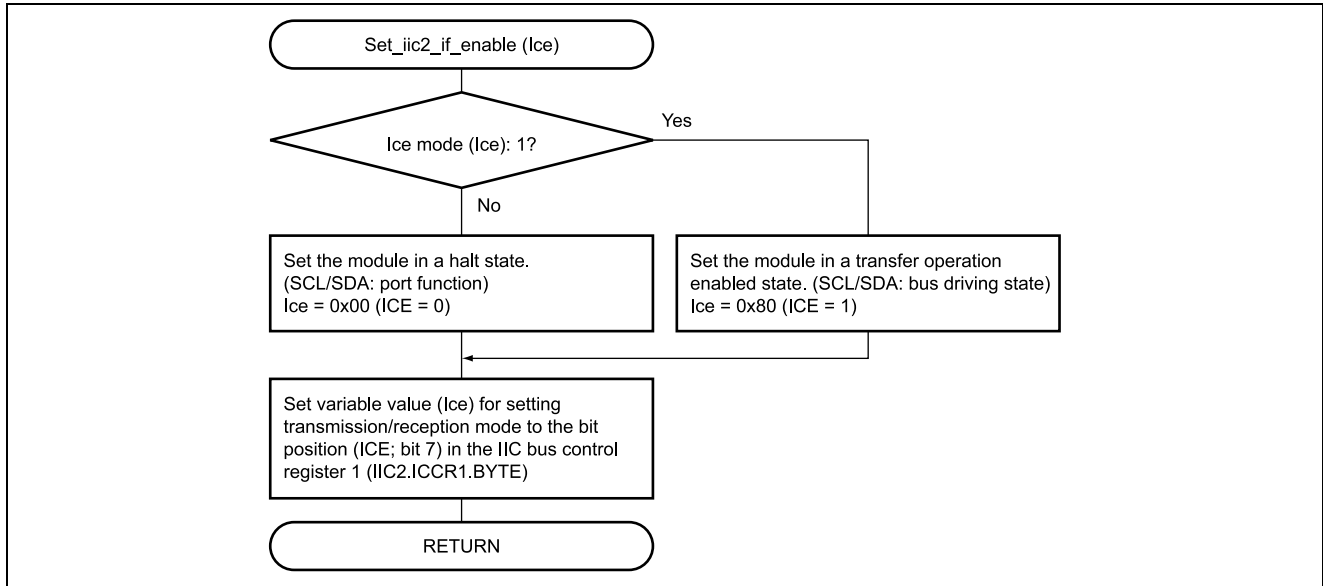
[19] Set_iic_rate ()

Function: Set master device transfer rate (CKS3, 2, 1, 0)



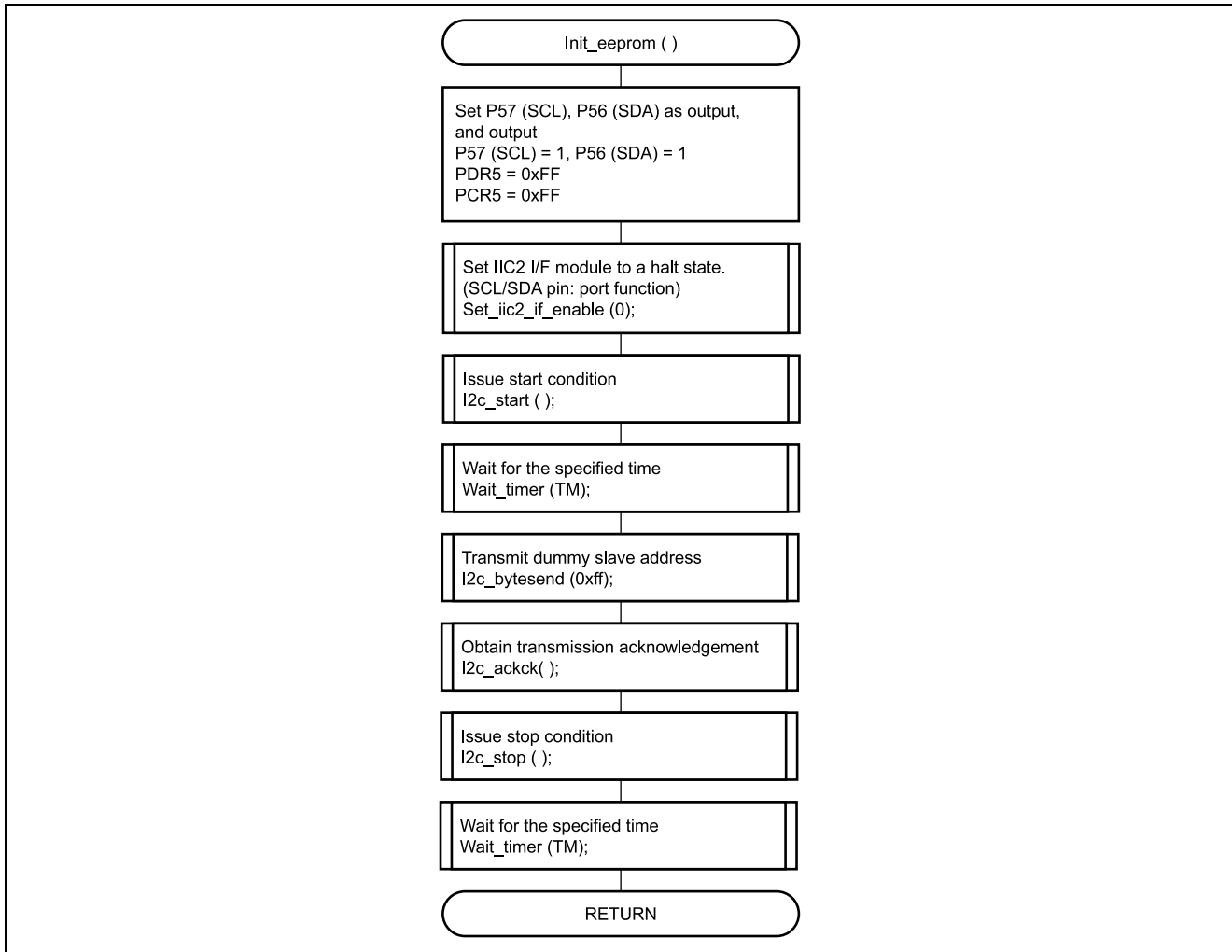
[20] Set_iic2_if_enable ()

Function: Set the IIC2 I/F module's operation status bit (ICE)



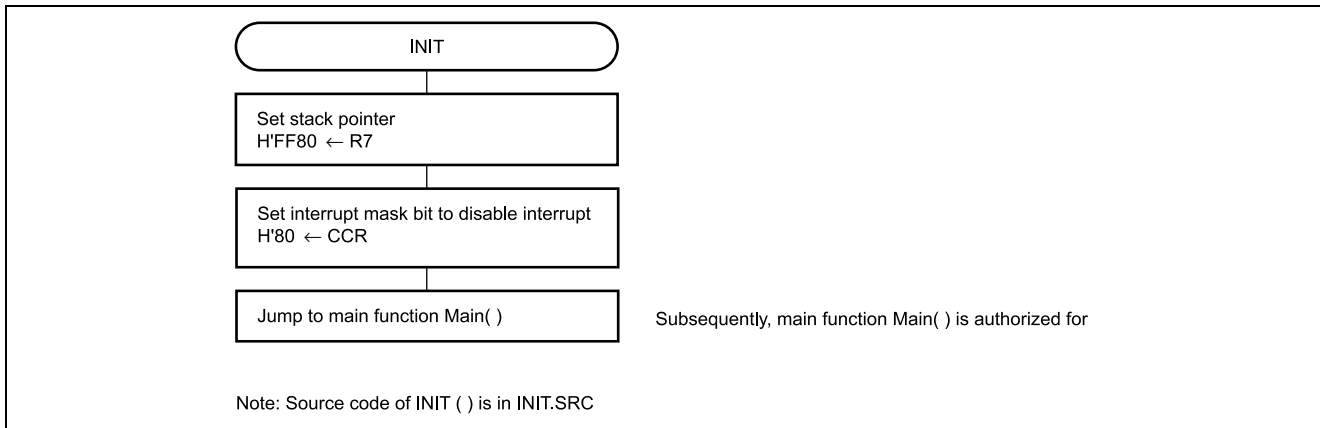
[21] Init_eeprom ()

Function: Initialize EEPROM bus condition



[32] INIT()

Function: Initialization (start up)



6. Program Listing

Program list of this application program is shown in section 6, [1] to [4].

```

/*****
/* H8/3694, H8/3687 IIC2 Include File Ver 1.1
*****/
struct st_iic2 {
    union {
        unsigned char BYTE;
        struct {
            unsigned char ICE :1;
            unsigned char RCVD:1;
            unsigned char MST :1;
            unsigned char TRS :1;
            unsigned char CKS3:1;
            unsigned char CKS2:1;
            unsigned char CKS1:1;
            unsigned char CKS0:1;
        } BIT;
    } ICCR1;
    union {
        unsigned char BYTE;
        struct {
            unsigned char BBSY :1;
            unsigned char SCP :1;
            unsigned char SDAO :1;
            unsigned char SDAOP :1;
            unsigned char SCLO :1;
            unsigned char :1;
            unsigned char IICRST:1;
            unsigned char :1;
        } BIT;
    } ICCR2;
    union {
        unsigned char BYTE;
        struct {
            unsigned char MLS :1;
            unsigned char WAIT :1;
            unsigned char :2;
            unsigned char BCWP :1;
            unsigned char BC2 :1;
            unsigned char BC1 :1;
            unsigned char BC0 :1;
        } BIT;
    } ICMR;
}

```

```

union {
    unsigned char BYTE;
    struct {
        unsigned char TIE :1;
        unsigned char TEIE :1;
        unsigned char RIE :1;
        unsigned char NAKIE :1;
        unsigned char STIE :1;
        unsigned char ACKE :1;
        unsigned char ACKBR :1;
        unsigned char ACKBT :1;
    } BIT;
} ICIER;

union {
    unsigned char BYTE;
    struct {
        unsigned char TDRE :1;
        unsigned char TEND :1;
        unsigned char RDRF :1;
        unsigned char NACKF:1;
        unsigned char STOP :1;
        unsigned char AL_OVE :1;
        unsigned char AAS :1;
        unsigned char ADZ :1;
    } BIT;
} ICSR;

union {
    unsigned char BYTE;
    struct {
        unsigned char SVAX:7;
        unsigned char FS :1;
    } BIT;
} SAR;

unsigned char ICDRT;
unsigned char ICDRR;
};

#define IIC2 (*(volatile struct st_iic2 *)0xF748)

```

[2] File name: INIT.SRC Function: Initialization (start up)

```

;*****
;* H8/3694, H8/3687 IIC2 APPLICATION NOTE STARTUP ROUTINE Ver 1.1 *
;*****
;
EXPORT _INIT
IMPORT _main
;
SECTION P, CODE
_INIT:
MOV.W #H'FF80, R7
LDC.B #B'10000000, CCR
JMP @_main
;
.END

/*-----*/
/* H8/3694, H8/3687 on-chip I2Cbus interface 2 (IIC2) Application note */
/* Application examples for reading from/writing to serial EEPROM (main program) */
/* */
/* 1. Target EEPROM: EEPROM for which memory address is specified in two bytes */
/* 2. Operation confirmed products: */
/* (1) H8/3687N, H8/3694N (512B) with on-chip EEPROM (manufactured by RENESAS TECHNOLOGY) */
/* (2) HN58X2432I (4kB), HN58X2464I (8kB) EEPROM (manufactured by RENESAS TECHNOLOGY) */
/* */
/* Ver 1.1 2003.5.9 */
/* */
/* Copyright (C) RENESAS TECHNOLOGY 2003 */
/*-----*/
/* Header Definition */
/*-----*/
#include <machine.h>

/*-----*/
/* Function Prototype declarations */
/*-----*/

extern void INIT( void );

extern unsigned short Master_read_byte_random( unsigned char Device_id, unsigned short Addr );
extern unsigned char Master_read_sequential( unsigned char Device_id, unsigned short Addr, unsigned short Length, unsigned char *buff_ptr );
extern unsigned char Master_byte_write( unsigned char Device_id, unsigned short Addr, unsigned char Data );
extern unsigned char Master_page_write( unsigned char Device_id, unsigned short Addr, unsigned char Length, unsigned char *buff_ptr );

extern void Init_eeprom( void );

void main ( void );

```

[3] File name: eeprom.c (2)

Function: Main processing

```

/*****
/*  Vector address definition
/*****
#pragma section          /* VECTOR SECTOIN SET
void (*const VEC_TBL1[])(void) = {
    INIT,
};

#ifdef __cplusplus
extern "C" {
#endif
void abort(void);
#ifdef __cplusplus
}
#endif

/*****
/*  RAM allocated section definition
/*****
#pragma section          /* section:B
unsigned char  eeprom_buf[513];

/*****
/*  ROM allocated section definition
/*****
#pragma section          /* section:P

/*****
/*  Main program
/*****
#pragma option nooptimize

/*-----*/
/*  Process result output port address definition
/*-----*/
#define PCR1  (*(volatile unsigned char *)0xFFE4)    /* Port control register 1
#define PDR1  (*(volatile unsigned char *)0xFFD4)    /* Port data register 1

/*-----*/
/*  IIC2 port address definition
/*-----*/
#define PCR5  (*(volatile unsigned char *)0xFFE8)    /* Port control register 5
#define PDR5  (*(volatile unsigned char *)0xFFD8)    /* Port data register 5
void main(void){

unsigned char  Device_id;
unsigned short Address;
unsigned short Address_start;
unsigned short Address_end;

unsigned short Result_code;
unsigned char  Err_code;
unsigned char  Data_w;
unsigned char  Data_r;
unsigned short Length;

```



```

PDR1 = 0x00; /* Port1 = 0 */
PCR1 = 0x07; /* Set P10, P11, P12 as output */
/* (used for process result output) */

Init_eeeprom(); /* Initialize EEPROM bus condition */
Init_iic2(); /* Initialize IIC2 I/F */

/*-----*/
/* Usage examples of 1-byte write (Master_byte_write) and 1-byte read (Master_read_byte_random) */
/*
/* Write lower 8-bit value of address to EEPROM address (0x000 to 0x1fff), read, and verify */
/* When an error occurs, output error code corresponding to process from process result output port (P10, P11, P12) */
/*-----*/
Device_id = 0x00; /* Set EEPROM slave address code: 0 (A2,A1,A0) */
Address_start = 0x000; /* Set EEPROM memory start address */
Address_end = 0x200; /* Set EEPROM memory end address */
PDR1 = 0x00; /* Clear process result output port */

for (Address = Address_start; Address < Address_end; Address++){
    Data_w = (unsigned char) (Address & 0x00FF); /* Obtain lower 8-bit value of address */
    Err_code = Master_byte_write (Device_id, Address, Data_w); /* Perform 1-byte write to EEPROM */
    if (Err_code != 0){ /* Check error code, and if an error occurs, */
        PDR1 = 0x01; /* set error code (write error = 1), and */
        goto Exit_err; /* exit with an error */
    }

    Result_code = Master_read_byte_random (Device_id, Address); /* Perform 1-byte read from EEPROM */
    Err_code = Result_code >> 8; /* Obtain error code (upper 8 bits) */
    Data_r = (unsigned char) (Result_code & 0x00FF); /* Obtain read data (lower 8 bits) */
    if (Err_code != 0){ /* Check error code, and if an error occurs, */
        PDR1 = 0x02; /* set error code (read error = 2), and */
        goto Exit_err; /* exit with an error */
    }

    if (Data_w != Data_r){ /* Compare write data to read data, */
        /* and if an error occurs, */
        PDR1 = 0x03; /* set error code (verify error = 3), and */
        goto Exit_err; /* exit with an error */
    }
}

/*-----*/
/* Usage examples of page write (Master_page_write) and sequential read (Master_read_sequential) */
/*
/* Perform page write to EEPROM address (0x000 to 0x1fff) lower 8-bit value of address, perform sequential read, and verify. */
/* If an error occurs, output error code corresponding to process from process result output ports (P10, P11, P12). */
/*-----*/
Device_id = 0x00; /* Set EEPROM slave address code: 0 (A2, A1, A0) */
Address_start = 0x000; /* Set EEPROM memory start address */
Address_end = 0x200; /* Set EEPROM memory end address */

/*-----*/
/* Set data to be performed page writing to EEPROM data buffer */
/*-----*/
for (Address = Address_start; Address < Address_end; Address++){
    Data_w = (unsigned char) ((Address + 1) & 0x00FF); /* Obtain lower 8-bit value of address */
    eeeprom_buf[Address+1] = Data_w; /* Store lower 8 bits of address */
    /* to EEPROM data buffer */
}

```

```

/*-----*/
/* Perform page write from data buffer to EEPROM */
/*-----*/
Length = 0x08; /* Set 1-page size to be written */
/* (3687N, 3694N; 8 bytes/page) */
/* Length = 0x20; */ /* Set 1-page size to be written */
/* (HN58X2432I, HN58X2464I; 32 bytes/page) */

for (Address = Address_start; Address < Address_end; Address+= Length){
    /* Perform writing all pages */
    Err_code = Master_page_write(Device_id, Address, Length, (eeprom_buf+Address));
    /* Perform writing 1 page to EEPROM */
    if (Err_code != 0){ /* Check error code, and if an error occurs, */
        PDR1 = 0x04; /* set error code (page write error = 4), and */
        goto Exit_err; /* exit with an error. */
    }
}

/*-----*/
/* Clear EEPROM data buffer to 0 */
/*-----*/
for (Address = Address_start; Address < Address_end; Address++){
    eeprom_buf[Address+1] = 0;
}

/*-----*/
/* Perform sequential read from EEPROM to data buffer */
/*-----*/
Length = Address_end - Address_start; /* Set data size to be performed sequential reading */

Err_code = Master_read_sequential(Device_id, Address_start, Length, eeprom_buf);
/* Perform sequential read for data size */
/* from EEPROM to data buffer */
if (Err_code != 0){ /* Check error code, and if an error occurs, */
    PDR1 = 0x05; /* set error code (sequential read error = 5), and */
    goto Exit_err; /* exit with an error. */
}

for (Address = Address_start; Address < Address_end; Address++){
    Data_w = (unsigned char)((Address + 1) & 0x00FF); /* Obtain written data (lower 8 bits of address) */
    Data_r = eeprom_buf[Address+1]; /* Obtain sequentially read data from data buffer */

    if (Data_w != Data_r){ /* Compare written data to read data, */
        /* and if an error occurs, set error code */
        PDR1 = 0x06; /* (sequential verify error = 6), and */
        goto Exit_err; /* exit with an error. */
    }
}

PDR1 = 0x00; /* Normal termination: set normal termination code */
/* to process result output port */

/*-----*/
/* Exit test */
/*-----*/
Exit_err: /* Exit test */
    while(1) /* Stop program */
        ; /*
}

#pragma option
void abort(void){

}

```

[4] File name: iic2_eeprom.c (1)

Function: Sub processing (function group)

```

/*-----*/
/* H8/3694, H8/3687 on-chip I2C bus interface 2 (IIC2) Application note */
/* Application examples for reading from/writing to serial EEPROM (sub program) */
/* */
/* 1. Target EEPROM: EEPROM which specifies memory address in two bytes */
/* 2. Operation confirmed product types: */
/* (1) H8/3687N, H8/3694N(512B) on-chip EEPROM (manufactured by RENESAS TECHNOLOGY) */
/* (2) HN58X2432I(4kB), HN58X2464I(8kB) EEPROM (manufactured by RENESAS TECHNOLOGY) */
/* Ver 1.1 2003.5.9 */
/* */
/* Copyright (C) RENESAS TECHNOLOGY 2003 */
/*-----*/
/*****
/* Header definition */
/*****
#include <machine.h>
#include "H8_3694_IIC2.h" /* Definition file of IIC2 module register map */

/*****
/* EEPROM device code definition */
/*****
#define DEVICE_CODE 0xa0 /* EEPROM device code: 1010 (D3,D2,D1,D0) */
#define SLAVE_ADDR 0x00 /* Slave address code: 000 (A2,A1,A0) */
#define RW_CODE_W 0x00 /* R/W code: 0 (data write) */
#define RW_CODE_R 0x01 /* R/W code: 1 (data read) */
#define DEVICE_ADDRESS_WORD_W (DEVICE_CODE | SLAVE_ADDR | RW_CODE_W) /* Slave address (for writing) */
#define DEVICE_ADDRESS_WORD_R (DEVICE_CODE | SLAVE_ADDR | RW_CODE_R) /* Slave address (for reading) */

/*****
/* Timeout limit count value definition */
/*****
#define TIMEOUT_LIMIT_BBSY 1000 /* Timeout limit for bus busy check */
#define TIMEOUT_LIMIT_ACK 1000 /* Timeout limit for ACK check */
#define TIMEOUT_LIMIT_TEND 1000 /* Timeout limit for TEND check */
#define TIMEOUT_LIMIT_RDRF 1000 /* Timeout limit for RDRF check */
#define TIMEOUT_LIMIT_STOP 1000 /* Timeout limit for STOP check */

/*****
/* Error code definition */
/*****
#define TIMEOUT_ERR_BUS_BUSY 200 /* Error code: Bus busy timeout */
#define TIMEOUT_ERR_ACK 201 /* Error code: Acknowledgement polling timeout */
#define TIMEOUT_ERR_TEND 202 /* Error code: Transmit end timeout */
#define TIMEOUT_ERR_RDRF 203 /* Error code: Receive end timeout */
#define TIMEOUT_ERR_STOP 204 /* Error code: Stop condition issue timeout */
#define ERR_ACK 205 /* Error code: Acknowledgement error */

```

```

/*****
/*   Port address definition
*****/
#define PCR5    (*(volatile unsigned char *)0xFFE8)          /* Port control register 5
#define PDR5    (*(volatile unsigned char *)0xFFD8)          /* Port data register 5

/*****
/*   Other constant definition
*****/
#define   TM           100                                  /* Wait for the specified time wait counts

/*****
/*   Prototype declaration for functions to be used
*****/
unsigned char Check_bus_condition ( void );
unsigned char Master_address_set (unsigned char Device_id, unsigned short Addr );
unsigned short Master_read_byte_random (unsigned char Device_id, unsigned short Addr );
unsigned char Master_read_sequential ( unsigned char Device_id, unsigned short Addr, unsigned short Length, unsigned char
*buff_ptr );
unsigned char Master_byte_write (unsigned char Device_id, unsigned short Addr, unsigned char Data);
unsigned char Master_page_write (unsigned char Device_id, unsigned short Addr, unsigned char Length, unsigned char *buff_ptr);
unsigned char Send_byte_data ( unsigned char Byte_data );
void Send_start_condition ( void );
void Set_iic_bus_mode ( unsigned char Bus_mode_MLS, unsigned char Bus_mode_WAIT, unsigned char Bus_mode_BC210);
void Set_iic_mode ( unsigned char Iic_mode );
void Set_iic_rate ( unsigned char Iic_rate );
unsigned char Send_stop_condition ( void );
void Set_iic2_if_enable ( unsigned char Ice );
unsigned char Set_slave_read_mode ( unsigned char Device_id );
unsigned char Set_slave_write_mode ( unsigned char Device_id );
unsigned short Receive_byte_data ( void );
void Set_receive_mode ( unsigned char Ackbt_flag, unsigned char Rcvd_flag );
unsigned char Receive_byte_data_many ( unsigned short Length, unsigned char *buff_ptr );
unsigned short Receive_byte_data_fin ( void );

void Init_eeprom ( void );
void I2c_start ( void );
void I2c_stop ( void );
void I2c_set ( unsigned char Scl , unsigned char Sda );
void I2c_bytesend ( unsigned char Tx_data );
void I2c_bitsend ( unsigned char Tx_data , unsigned char Ckbit );
void I2c_send ( unsigned char Bit_data );
unsigned char I2c_ackck ( void );
void I2c_sda_in ( void );
void I2c_sda_out ( unsigned char Data );
void Wait_timer ( unsigned short Wait_cnt );

```

```

/*=====*/
/* Check IIC bus condition, and wait until bus becomes available */
/* */
/* Entry:  None ; None */
/* Return: Bbsy_flag (unsigned char); Bus condition flag */
/* 0: Bus free */
/* 1: Bus busy */
/* TIMEOUT_ERR_BUS_BUSY: Timeout */
/* */
/*=====*/
unsigned char Check_bus_condition ( void ){

    unsigned char    Bbsy_flag;
    unsigned short   Time_out_count;

    Time_out_count = 0;                               /* Clear timeout counter */

    while (1) {                                       /*
        Bbsy_flag = IIC2.ICCR2.BIT.BBSY;             /* Read BBSY to obtain bus condition
        if (Bbsy_flag== 0){                           /* Wait until bus condition becomes available
            break;
        }

        Time_out_count++;                             /* Check timeout
        if (Time_out_count > TIMEOUT_LIMIT_BBSY){     /* If timeout occurs,
            Bbsy_flag = (unsigned char) TIMEOUT_ERR_BUS_BUSY; /* set bus condition code = TIMEOUT_ERR_BUS_BUSY
            break;                                       /* and exit
        }
    }                                                 /* Wait until bus condition becomes available

    return( Bbsy_flag );                             /* Return bus condition code
}

```

```

/*=====*/
/* Transmit slave address and memory address to IIC device */
/* */
/* Entry: Device_id (unsigned char) ; Slave address code: 0 to 7 (A2, A1, A0) */
/* Addr (unsigned short) ; Memory address */
/* Return: Err_code (unsigned char) ; ; Error code */
/* 0: Normal termination */
/* 2: Second byte transmission acknowledgement error (upper 8 bits of memory address) */
/* 3: Third byte transmission acknowledgement error (lower 8 bits of memory address) */
/* TIMEOUT_ERR_BUS_BUSY: Bus busy timeout */
/* TIMEOUT_ERR_ACK: Acknowledgement polling timeout */
/* Note: Transmit end timeout error is returned as 2 to 3 of Err_code. */
/*=====*/
unsigned char Master_address_set ( unsigned char Device_id, unsigned short Addr ){

    unsigned char Bbsy_flag;
    unsigned char Ack_flag;

    unsigned char Addr_msb;
    unsigned char Addr_lsb;
    unsigned char Err_code;
    unsigned short Time_out_count;
    Bbsy_flag = Check_bus_condition(); /* Check bus condition */
    /* and wait until bus becomes available */
    if( Bbsy_flag != 0 ){ /* If bus busy timeout occurs, */
        Err_code = (unsigned char)TIMEOUT_ERR_BUS_BUSY; /* set error code = TIMEOUT_ERR_BUS_BUSY */
        goto Exit_err; /* and exit */
    } /*

    Time_out_count = 0; /* Clear timeout counter

    while (1) { /*
        Ack_flag = Set_slave_write_mode ( Device_id ); /* Transmit slave address (write)
        /* (Transmit first byte)

        if ( Ack_flag == 0 ) {
            break;
        }

        Time_out_count++; /* Check acknowledgement timeout
        if (Time_out_count > TIMEOUT_LIMIT_ACK){ /* If timeout occurs,
            Err_code = (unsigned char)TIMEOUT_ERR_ACK; /* set error code = TIMEOUT_ERR_ACK
            goto Exit_err; /* and exit
        }
    } /* Perform acknowledgement polling
    /* until acknowledgement is obtained

    while (1) {
        Addr_msb = (unsigned char)( Addr >> 8 ); /* Obtain upper (MSB) address
        Ack_flag = Send_byte_data( Addr_msb ); /* Transmit upper (MSB) memory address
        /* (second byte) and check acknowledgements
        if (Ack_flag != 0) { /* If the acknowledgement value is 1,
            /* acknowledgement error occurs
            Err_code = 2; /* Set error code (second byte: error)
            break; /* and exit
        }
    }

```

```
Addr_lsb = (unsigned char)( Addr & 0x00ff );          /* Obtain lower (LSB) address          */
Ack_flag = Send_byte_data( Addr_lsb );              /* Transmit lower (LSB) memory address (third byte) */
                                                    /* and check acknowledgement          */
if (Ack_flag != 0) {                                /* If the acknowledgement value is 1,  */
                                                    /* acknowledgement error occurs      */
    Err_code = 3;                                   /* Set error code (third byte: error)  */
    break;                                          /* and exit                            */
}

Err_code = 0;                                       /* Since this is normal termination,   */
                                                    /* clear error code                    */
break;                                              /* Exit                                 */
}

Exit_err:
    return( Err_code );                             /* Return error code                  */
}
```

```

/*=====*/
/* Random address read (byte read) from IIC device */
/* */
/* Entry: Device_id (unsigned char); Slave address code: 0 to 7 (A2, A1, A0) */
/* Addr (unsigned short) ; Memory address */
/* Return: Normal termination : Data_s (unsigned short) ; Received data (lower 8 bits)□ */
/* Error termination : Err_code_s (unsigned short) ; Error code (upper 8 bits) */
/* */
/* Error code; */
/* 0: Normal termination */
/* 2: Second byte transmission acknowledgement error (upper 8 bits of memory address) */
/* 3: Third byte transmission acknowledgement error (lower 8 bits of memory address) */
/* ERR_ACK: Slave address (read) acknowledgement error */
/* TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error */
/* TIMEOUT_ERR_ACK: Acknowledgement polling timeout error */
/* TIMEOUT_ERR_RDRF: Receive end timeout error */
/* TIMEOUT_ERR_STOP: Stop condition detection timeout error */
/* Note: Transmit end timeout error is returned as 2 to 3 of Err_code. */
/* */
/*=====*/
unsigned short Master_read_byte_random ( unsigned char Device_id, unsigned short Addr ){

    unsigned char Ack_flag;
    unsigned char Stop_flag;
    unsigned char Data;
    unsigned short Data_s;
    unsigned char Err_code;
    unsigned short Err_code_s;

    Err_code = Master_address_set ( Device_id, Addr ); /* Transmit slave address and memroy address */
                                                    /* in write mode */
    if (Err_code != 0){ /* If an error occurs, abort processing, */
                        /* and issue stop condition */
        goto Exit_err; /* Perform error processing */
    } /*

    Ack_flag = Set_slave_read_mode ( Device_id ); /* Retransmit slave address in read mode */
    if (Ack_flag != 0){ /* If there is no acknowledgement, */
                        /* abort processing, and issue stop condition */
        Err_code = ERR_ACK ; /* Set acknowledgement error code */
        goto Exit_err; /* Perform error processing */
    }

    Set_iic_mode(2); /* Set master reception mode (MST = 1, TRS = 0) */

    IIC2.ICSR.BIT.TEND = 0; /* Clear TEND */
    IIC2.ICSR.BIT.TDRE = 0; /* Clear TDRE */

    Set_receive_mode ( 1, 1 ); /* Set subsequent reception mode (ACKBT, RCVD). */
                                /* ACKBT=1 (because of only 1-byte reception, */
                                /* set the acknowledgement value to No (ACK = 1) */
                                /* as final data.) */
                                /* RCVD =1 (disable subsequent reception operation) */

```



```

Data_s = Receive_byte_data ();                               /* Read data (start reception operation) */
if ((Data_s & 0xff00) != 0){                                  /* If an error occurs */
                                                            /* (when upper 8 bits are not 0), */
                                                            /* abort processing and issue stop condition */
    Err_code = (unsigned char)TIMEOUT_ERR_RDRF;              /* Set receive end timeout error code */
    goto Exit_err;                                          /* Perform error processing */
}                                                            /*

Data_s = Receive_byte_data_fin (); □□                       /* Read data (obtain final received data) */

Stop_flag = Send_stop_condition();                          /* Issue stop condition (BBSY = 0, SCP = 0) */
if (Stop_flag != 1){                                        /* If an error occurs, abort processing */
                                                            /* and issue stop condition */
    Err_code = (unsigned char)TIMEOUT_ERR_STOP;              /* Set stop condition detection timeout error code */
    goto Exit_err_2;                                        /* Perform error processing */
}                                                            /*

IIC2.ICCR1.BIT.RCVD = 0;                                    /* Clear RCVD(set subsequent reception operation as */
                                                            /* to be continuous) */
Set_iic_mode(0);                                           /* Set slave reception mode (MST = 0, TRS = 0) */

return ( Data_s );                                         /* Normal termination; return received data */
                                                            /* (lower 8 bits: data, */
                                                            /* upper 8 bits: error code = 0) */

Exit_err:
    Stop_flag = Send_stop_condition();                      /* Issue stop condition (BBSY = 0, SCP = 0) */
    if (Stop_flag != 1){                                    /* If an error occurs, set error code */
        Err_code = (unsigned char)TIMEOUT_ERR_STOP;          /* Set stop condition detection timeout error code */
    }

Exit_err_2:
    IIC2.ICCR1.BIT.RCVD = 0;                                /* Clear RCVD(set subsequent reception operation */
                                                            /* as to be continuous) */
    Set_iic_mode(0);                                       /* Set slave reception mode (MST = 0, TRS = 0) */

    Err_code_s = ((unsigned short) Err_code << 8);          /* Shift error code to upper 8 bits */
    return ( Err_code_s );                                  /* Error termination; return error code */
                                                            /* (upper 8 bits) */
}

```

```

/*=====*/
/* Sequential address read from IIC device */
/* */
/* Entry: Device_id (unsigned char) ; Slave address code: 0 to 7 (A2, A1, A0) */
/* Addr (unsigned short) ; Read start memory address */
/* Length (unsigned short) ; Length of read bytes (more than 2 bytes) */
/* *buff_ptr (unsigned char) ; Read data storage buffer start address */
/* Return: Err_code (unsigned char) ; Error code */
/* 0: Normal termination */
/* 2: Second byte acknowledgement error (upper 8 bits of memory address) */
/* 3: Third byte acknowledgement error (lower 8 bits of memory address) */
/* ERR_ACK: Slave address (read) acknowledgement error */
/* TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error */
/* TIMEOUT_ERR_ACK: Acknowledgement polling timeout error */
/* TIMEOUT_ERR_RDRF: Data receive end timeout error */
/* TIMEOUT_ERR_STOP: Stop condition detection timeout error */
/* Note: Transmit end timeout error is returned as 2 to 3 of Err_code. */
/* */
/*=====*/
unsigned char Master_read_sequential ( unsigned char Device_id, unsigned short Addr, unsigned short Length, unsigned char
*buff_ptr ){

    unsigned char Ack_flag;
    unsigned char Stop_flag;
    unsigned char Err_code;

    Err_code = Master_address_set ( Device_id, Addr ); /* Transmit slave address and memory address */
                                                    /* in write mode */
    if (Err_code != 0){ /* If an error occurs, abort processing, */
                        /* and issue stop condition */
        goto Exit_err; /* Perform error processing */
    } /*

    Ack_flag = Set_slave_read_mode ( Device_id ); /* Retransmit slave address in read mode */
    if (Ack_flag != 0){ /* If there is no acknowledgement, abort processing */
                        /* and issue stop condition */
        Err_code = ERR_ACK ; /* Set acknowledgement error code */
        goto Exit_err; /* Perform error processing */
    } /*

    Set_iic_mode(2); /* Set master reception mode (MST = 1, TRS = 0) */

    IIC2.ICSR.BIT.TEND = 0; /* Clear TEND */
    IIC2.ICSR.BIT.TDRE = 0; /* Clear TDRE

    Set_receive_mode ( 0, 0 ); /* Set subsequent reception mode */
                                /* (ACKBT = 0, RCVD = 0) */
                                /* ACKBT = 0 (set acknowledgement (ACK = 0)) */
                                /* RCVD = 0 (set subsequent reception operation */
                                /* as to be continuous) */

```

```

Err_code = Receive_byte_data_many( Length, buff_ptr );          /* Receive data with a size to be received */
                                                                /* and store it in buffer */
                                                                /* If an error occurs, abort processing */
                                                                /* and issue stop condition */
                                                                /* Set receive end timeout error code */
                                                                /*
if (Err_code != 0){
                                                                /*
    Err_code = (unsigned char)TIMEOUT_ERR_RDRF;                /*
}                                                                /*
Exit_err:
Stop_flag = Send_stop_condition();                             /* Issue stop condition (BBSY = 0, SCP = 0) */
if (Stop_flag != 1){                                          /* If an error occurs, */
    Err_code = (unsigned char)TIMEOUT_ERR_STOP;                /* set stop condition detection timeout error code */
}                                                                /*
                                                                /*
IIC2.ICCR1.BIT.RCVD = 0;                                       /* Clear RCVD (set subsequent reception operation */
                                                                /* as to be continuous) */
Set_iic_mode(0);                                              /* MST = 0, TRS = 0 (set slave reception mode) */
                                                                /*
return ( Err_code );                                          /* Return error code */
                                                                /* (in normal operation, error code = 0) */
}

```

```

/*=====*/
/* Byte data write to IIC device (byte write) */
/* */
/* Entry: Device_id (unsigned char) ; Slave address code: 0 to 7 (A2,A1,A0) */
/* Addr (unsigned short) ; Memory address */
/* Data (unsigned char) ; Write data */
/* Return: Err_code (unsigned char) ; Error code */
/* 0: Normal termination */
/* 2: Second byte acknowledgement error (upper 8 bits of memory address) */
/* 3: Third byte acknowledgement error (lower 8 bits of memory address) */
/* 4: Fourth byte acknowledgement error (data) */
/* TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error */
/* TIMEOUT_ERR_ACK: Acknowledgement polling timeout error */
/* TIMEOUT_ERR_STOP: Stop condition detection timeout error */
/* Note: Transmit end timeout error is returned as 2 to 3 of Err_code. */
/*=====*/
unsigned char Master_byte_write ( unsigned char Device_id, unsigned short Addr, unsigned char Data ){

    unsigned char Ack_flag;
    unsigned char Err_code;
    unsigned char Stop_flag;

    while (1) {
        Err_code = Master_address_set( Device_id, Addr ); /* Transmit slave address */
        /* and memory address in write mode */
        if (Err_code != 0){ /* If an error occurs, abort processing */
            /* and issue stop condition */
            break; /*
        } /*

        Ack_flag = Send_byte_data( Data ); /* Transmit data */
        if (Ack_flag != 0) { /* If the acknowledgement value is 1, */
            /* an acknowledgement error occurs */
            Err_code = 4; /* Set error code (fourth byte: error) and */
            break; /* issue stop condition */
        }

        Err_code = 0; /* Because of normal termination, clear error code, */
        break; /* and issue stop condition */
    }

    Stop_flag = Send_stop_condition(); /* Issue stop condition (BBSY=0, SCP=0) */
    if (Stop_flag != 1){ /* If an error occurs, */
        Err_code = (unsigned char)TIMEOUT_ERR_STOP; /* set stop condition detection timeout error code */
    } /*

    Set_iic_mode( 0 ); /* MST=0, TRS=0 (set slave reception mode) */

    IIC2.ICSR.BIT.TEND = 0; /* Clear TEND */
    IIC2.ICSR.BIT.TDRE = 0; /* Clear TDRE */

    return( Err_code ); /* Return error code */
}

```

```

/*=====*/
/* Page data write to IIC device (page write) */
/* */
/* Entry: Device_id (unsigned char) ; Slave address code: 0 to 7 (A2,A1,A0) */
/* Addr (unsigned short) ; write start memory address */
/* Length (unsigned char) ; Write byte length (within 1 page) */
/* buff_ptr (unsigned char) ; Written data storage buffer start address */
/* Return: Err_code (unsigned char) ; Error code */
/* 0: Normal termination */
/* 2: Second byte acknowledgement error (upper 8 bits of address) */
/* 2: Second byte acknowledgement error (upper 8 bits of address) */
/* 4 to 131 (transmitted byte length + 3): */
/* Transmission acknowledgement error in the bytes following fourth byte (data) */
/* TIMEOUT_ERR_BUS_BUSY: Bus busy timeout error */
/* TIMEOUT_ERR_ACK: Acknowledgement polling timeout error */
/* TIMEOUT_ERR_STOP: Stop condition detection timeout error */
/* Note: Transmit end timeout error is returned as 2 to 131 of Err_code. */
/*=====*/
unsigned char Master_page_write ( unsigned char Device_id, unsigned short Addr, unsigned char Length, unsigned char *buff_ptr ){

    unsigned char Ack_flag;
    unsigned char Err_code;
    unsigned char Data;
    unsigned char Cnt;
    unsigned char Stop_flag;

    Err_code = Master_address_set ( Device_id, Addr ); /* Transmit slave address and memory address */
    /* in write mode */
    if (Err_code != 0){ /* If an error occurs, abort processing */
        goto Exit_err; /* and issue stop condition */
        /* Error termination */
    }

    buff_ptr++; /* Increment written data storage address */
    /* by 1 to set head of data by 1 */

    for ( Cnt = 1; Cnt <= Length; Cnt++ ){ /* Transmit data equaling the size */
        /* of the written byte length value */
        Data = *buff_ptr; /* Obtain written data */
        /* from written data storage address */
        buff_ptr++; /* Increment written data storage address */

        Ack_flag = Send_byte_data( Data ); /* Transmit data */
        if (Ack_flag != 0) { /* If the acknowledgement value is not 0, */
            /* acknowledgement error occurs */
            Err_code = 3 + Cnt; /* Set error code (following fourth byte: error) */
            goto Exit_err; /* Error termination; */
            /*abort processing and issue stop condition */
        } /* Error code is 3 + transmitted data length */
    }

    Err_code = 0; /* Because of normal termination, clear error code */

Exit_err:
    Stop_flag = Send_stop_condition(); /* Issue stop condition (BBSY=0, SCP=0) */
    if (Stop_flag != 1){ /* If an error occurs, */
        Err_code = (unsigned char)TIMEOUT_ERR_STOP; /* set stop condition detection timeout error code */
    }

    Set_iic_mode( 0 ); /* MST=0, TRS=0 (set slave reception mode) */

    IIC2.ICSR.BIT.TEND = 0; /* Clear TEND */
    IIC2.ICSR.BIT.TDRE = 0; /* Clear TDRE */

    return( Err_code ); /* Return error code */
}

```

```

/*=====*/
/* Transmit data (1 byte) to IIC device */
/* */
/* Entry:   Byte_data      (unsigned char) ; Transmitted data */
/* Return:  Ackbr_flag     (unsigned char) ; Acknowledgement flag */
/*         0: Normal termination */
/*         1: Abnormal termination */
/*         TIMEOUT_ERR_TEND: Transmit end timeout */
/* */
/*=====*/
unsigned char Send_byte_data ( unsigned char Byte_data ){

    unsigned char Tend_flag;
    unsigned char Ackbr_flag;
    unsigned short Time_out_count;

    IIC2.ICDRT = Byte_data;                               /* Transmit data */

    Time_out_count = 0;                                   /* Clear timeout count */

    while(1) {
        Tend_flag = IIC2.ICSR.BIT.TEND;                  /* Check TEND and */
        if ( Tend_flag == 1 ){                            /* wait for transmission completion */
            break;                                        /* */
        }                                                 /* */

        Time_out_count++;                                 /* Check transmit end timeout */
        if (Time_out_count > TIMEOUT_LIMIT_TEND){        /* If timeout occurs, */
            Ackbr_flag = (unsigned char)TIMEOUT_ERR_TEND; /* set Ackbr_flag = TIMEOUT_ERR_TEND and */
            goto Exit_err;                               /* exit */
        }                                               /* */
    }

    Ackbr_flag = IIC2.ICIER.BIT.ACKBR;                   /* When transmission completed, */
                                                       /* obtain acknowledgement */

Exit_err:
    return( Ackbr_flag );                               /* Return acknowledgement */
}

/*=====*/
/* Issue start condition to IIC device */
/* */
/* Entry:   None ; None */
/* Return:  None ; None */
/* */
/*=====*/
void Send_start_condition ( void ){

    IIC2.ICCR2.BYTE = 0xBD;                             /* Issue start condition (BBSY=1, SCP=0) */
}

```

```

/*=====*/
/* Issue stop condition to IIC device */
/* */
/* Entry:  None ; None */
/* Return:  Stop_flag (unsigned char); Stop condition detection flag */
/*          1: Stop condition detected */
/*          TIMEOUT_ERR_STOP: Stop condition detection timeout (stop condition not detected) */
/* =====*/
unsigned char  Send_stop_condition ( void ){

    unsigned char  Stop_flag;
    unsigned short Time_out_count;

    IIC2.ICSR.BIT.STOP = 0;          /* Clear STOP */
    IIC2.ICCR2.BYTE = 0x3D;         /* Issue stop condition (BBSY=0, SCP=0) */

    Time_out_count = 0;            /* Clear timeout counter */

    while (1) {
        Stop_flag = IIC2.ICSR.BIT.STOP;
        if ( Stop_flag == 1 ){
            break;
        }

        Time_out_count++;
        if (Time_out_count > TIMEOUT_LIMIT_STOP){
            Stop_flag = (unsigned char)TIMEOUT_ERR_STOP;
            goto Exit_err;
        }
    }
Exit_err:
    return ( Stop_flag );
}

/*=====*/
/* Retransmit slave address (read) to IIC device and set read mode */
/* */
/* Entry:  Device_id (unsigned char) ; Slave address code: 0 to 7 (A2,A1,A0) */
/* Return:  Ack_flag (unsigned char) ; Reception acknowledgement flag */
/*          0: Normal, 1: Error */
/* =====*/
unsigned char  Set_slave_read_mode ( unsigned char Device_id ){

    unsigned char  Slave_address;
    unsigned char  Ack_flag;

    Set_iic_mode(3);
    Send_start_condition();

    Slave_address = (unsigned char)DEVICE_ADDRESS_WORD_R | (Device_id << 1);

    Ack_flag = Send_byte_data( Slave_address );

    return( Ack_flag );
}

```

```

/*=====*/
/* Retransmit slave address (read) to IIC device, and set write mode */
/* */
/* Entry: Device_id (unsigned char) ; Slave address code: 0 to 7 (A2,A1,A0) */
/* Return: Ack_flag (unsigned char) ; Receive acknowledgement flag */
/* 0: Normal, 1: Error */
/* */
/*=====*/
unsigned char Set_slave_write_mode ( unsigned char Device_id ){

    unsigned char Slave_address;
    unsigned char Ack_flag;

    Set_iic_mode(3); /* Set master transmission mode (MST=1, TRS=1) */
    Send_start_condition(); /* Issue start condition (BBSY=1, SCP=0) */

    Slave_address = (unsigned char)DEVICE_ADDRESS_WORD_W | (Device_id << 1); /* Generate slave address (write) */
    Ack_flag = Send_byte_data( Slave_address ); /* Transmit slave address */

    return( Ack_flag ); /* Return reception acknowledgement */
}

/*=====*/
/* Receive data from IIC device (start reception operation simultaneously with data read) */
/* Start reception operation and perform RDRF check */
/* */
/* Entry: None ; None */
/* Return: Err_code_s (unsigned short) ; Error code (upper 8 bits) */
/* Data_s (unsigned short) ; Received data (lower 8 bits) */
/* */
/* Error code; */
/* 0: Normal termination */
/* TIMEOUT_ERR_RDRF:Receive end timeout error */
/* */
/*=====*/
unsigned short Receive_byte_data ( void ){

    unsigned char Rdrf_flag;
    unsigned char Data;
    unsigned short Data_s;
    unsigned short Err_code_s;
    unsigned short Time_out_count;

    Time_out_count = 0; /* Clear timeout counter */

    Data = IIC2.ICDRR; /* Read data */
    /* (start subsequent reception when ICDRR is read) */

    while(1) { /* */
        Rdrf_flag = IIC2.ICSR.BIT.RDRF; /* */
        if ( Rdrf_flag == 1 ){ /* Wait for all data */
            break; /* */
        } /* */
    } /* */

    Time_out_count++; /* Check receive end timeout */
    if (Time_out_count > TIMEOUT_LIMIT_RDRF){ /* If timeout occurs, */
        Err_code_s = (unsigned short) TIMEOUT_ERR_RDRF; /* set Err_code = TIMEOUT_ERR_RDRF and */
        goto Exit_err; /* exit */
    } /* */
} /* Normal termination */

```



```

Data_s = (unsigned short) Data;          /* Extend data to 2 bytes          */
return ( Data_s );                      /* Return data                    */

Exit_err:                               /* Error termination              */
Err_code_s = (Err_code_s << 8);        /* Shift error code to upper 8 bits */
return ( Err_code_s );                  /* Return error code              */
/* (set upper 8 bits as error code)      */
}

/*=====*/
/* Receive data from IIC device (read final data) Since subsequent reception operation is not performed
/* because of it is final data, RDRF check is not performed
/*
/* Entry:  None ; None
/* Return: Data_s (unsigned short); Received data (lower 8 bits)
/* (upper 8 bits are 0)
/*
*/
/*
/*=====*/
unsigned short Receive_byte_data_fin ( void ){

    unsigned char  Data;
    unsigned short Data_s;

    Data = IIC2.ICDRR;                  /* Read final data                */
    Data_s = (unsigned short) Data;     /* Extend data to 2 bytes          */

    return( Data_s );                  /* Return read data                */
}

/*=====*/
/* Set ACKBT and RCVD flags for receiving data
/*
/* Entry:  Ackbt_flag (unsigned char) ; Flag to be set as ACKBT (0,1)
/*         Rcvd_flag (unsigned char) ; Flag to be set as RCVD (0,1)
/* Entry:  None ; None
/*
/*=====*/
void Set_receive_mode ( unsigned char Ackbt_flag, unsigned char Rcvd_flag ){

    IIC2.ICIER.BIT.ACKBT = Ackbt_flag; /* Set ACKBT                      */
    IIC2.ICCR1.BIT.RCVD = Rcvd_flag;   /* Set RCVD                       */
}

```

```

/*=====*/
/* Receive byte data from IIC device sequentially(for read byte length) */
/* */
/* Entry: Length (unsigned short) ; Read byte length (more than 2 bytes) */
/* *buff_ptr (unsigned char) ; Read data storage buffer start address */
/* Since dummy data upon starting reception is stored in the start address (buff_ptr), */
/* valid data is stored with a size specified by Length from (buff_ptr + 1) */
/* Return: Err_code (unsigned char) ; Error code */
/* 0: Normal termination */
/* TIMEOUT_ERR_RDRF:Receive end timeout error */
/* */
/*=====*/
unsigned char Receive_byte_data_many ( unsigned short Length, unsigned char *buff_ptr ){

    unsigned char Err_code;
    unsigned short Data_s;
    unsigned char Data;
    Length++;

    /* Since the data first received is dummy data */
    /* (invalid), actual received size must be */
    /* incremented by 1. */

    while( Length > 1 ) {

        /* Receive data equalling the size */
        /* of data byte length value to be received */
        if ( Length == 2 ){

            /* Check whether the received data is one byte */
            /* before the final data */
            Set_receive_mode ( 1, 1 );

            /* Set subsequent reception mode (ACBT=1,RCVD=1) */
            /* Set ACKBT (for receiving final data, */
            /* set the acknowledgement value to No (ACK=1) */
            /* Set RCVD */
            /* (disable subsequent reception operation) */

        }

        Data_s = Receive_byte_data ();
        if ((Data_s & 0xff00) != 0){

            /* Read received data (start reception operation) */
            /* If an error occurs, abort processing, */
            /* and issue stop condition */
            Err_code = (unsigned char) TIMEOUT_ERR_RDRF;
            goto Exit_err;

            /* Set receive end timeout error code */
            /* Perform error processing */

        }

        Data = (unsigned char)(Data_s & 0x00ff);
        *buff_ptr = Data;

        /* Obtain lower 8 bits of received data */
        /* Store received data in buffer */

        buff_ptr++;
        Length--;

        /* Increment storage buffer address */
        /* Decrement received data length */

    }

    Data_s = Receive_byte_data_fin ();

    /* Read received data (obtain final received data) */

    Data = (unsigned char)(Data_s & 0x00ff);
    *buff_ptr = Data;

    /* Obtain lower 8 bits of received data */
    /* Store received data in buffer */

    Err_code = 0;

    /* Normal termination; set error code as 0 */

Exit_err:
    return ( Err_code );

    /* Return error code */

}

/*=====*/
/* Initialize IIC2 I/F */
/* */
/* Entry: None ; None */
/* Return: None ; None */
/* */
/*=====*/
void Init_iic2 ( void ){

    Set_iic_rate (1);
    Set_iic_bus_mode (0,0,0);

    /* Set IIC transfer rate as  $\phi/40$  ( $\phi = 16\text{MHz}$ , 400 kHz), */
    /* IIC bus mode as MSB first, no wait insertion, */
    /* and,bit length:9 bits */

    Set_iic2_if_enable (1);

    /* Set IIC2 I/F module to a transfer operation */
    /* enabled state (SCL/SDA: bus driving status) */

}

```

```

/*=====*/
/* Set master device bus mode (MLS, WAIT, BC210) */
/* */
/* Entry: Bus_mode_MLS (unsigned char) ; MSB first/LSB first */
/* 0(MLS=0): MSB first (When IIC is used, set to 0) */
/* 1(MLS=1): LSB first */
/* Bus_mode_WAIT (unsigned char) ; Wait insertion specification */
/* 0(WAIT=0): Not insert wait */
/* 1(WAIT=1): Insert wait */
/* Bus_mode_BC210 (unsigned char) ; Transfer data bit length specification */
/* 0(BC210=000): 9-bit mode */
/* 1(BC210=001): 2-bit mode */
/* 2(BC210=010): 3-bit mode */
/* 3(BC210=011): 4-bit mode */
/* 4(BC210=100): 5-bit mode */
/* 5(BC210=101): 6-bit mode */
/* 6(BC210=110): 7-bit mode */
/* 7(BC210=111): 8-bit mode */
/* Return: None ; None */
/* Note: Call as SCL = 1, except for setting the transfer data bit length to 0. */
/* */
/*=====*/
void Set_iic_bus_mode ( unsigned char Bus_mode_MLS, unsigned char Bus_mode_WAIT, unsigned char Bus_mode_BC210){

    unsigned char bus_mode;

    Bus_mode_MLS &= 0x01; /* t MSB first/LSB first to MLS */
    if (Bus_mode_MLS == 1){ /*
        Bus_mode_MLS = 0x80; /* MLS = bit7
    } /*

    Bus_mode_WAIT &= 0x01; /* Set wait insertion specification as WAIT */
    if (Bus_mode_WAIT == 1){ /*
        Bus_mode_WAIT = 0x40; /* WAIT = bit6
    } /*

    Bus_mode_BC210 &= 0x03; /* Set transfer data bit length as BC210 */

    bus_mode = 0; /* Generate bus mode setting value */
    bus_mode = (Bus_mode_MLS | Bus_mode_WAIT | Bus_mode_BC210); /*

    IIC2.ICMR.BYTE = bus_mode; /* Set bus mode to register */
    IIC2.ICMR.BYTE = (bus_mode | 0x08); /* Set write protect for BC210 (BCWP=1) */
}

```

```

/*=====*/
/* Set master device transmission/reception mode (MST, TRS) */
/* */
/* Entry: Iic_mode (unsigned char) ; Transmission/reception mode */
/* 0(MST=0, TRS=0): Slave reception mode */
/* 1(MST=0, TRS=1): Slave transmission mode */
/* 2(MST=1, TRS=0): Master reception mode */
/* 3(MST=1, TRS=1): Master transmission mode */
/* Return: None ; None */
/* */
/*=====*/
void Set_iic_mode ( unsigned char Iic_mode ){

    Iic_mode &= 0x03; /* Mask argument range between 0 and 3 */

    switch ( Iic_mode ){ /* Generate data to be set */
        case 0: Iic_mode = 0; /* MST=0, TRS=0 */
            break;
        case 1: Iic_mode = 0x10; /* MST=0, TRS=1 */
            break;
        case 2: Iic_mode = 0x20; /* MST=1, TRS=0 */
            break;
        case 3: Iic_mode = 0x30; /* MST=1, TRS=1 */
            break;
        default: Iic_mode = 0; /* MST=0, TRS=0 */
    }

    IIC2.ICCR1.BYTE = ((IIC2.ICCR1.BYTE & 0xcf) | Iic_mode); /* Set transmission/reception mode to register */
}

/*=====*/
/* Set master device transfer rate (CKS3, 2, 1, 0) */
/* */
/* Entry: Iic_rate (unsigned char) ; Transfer rate */
/* 0(CKS3210=0000): c clock;Φ/28 mode */
/* 1(CKS3210=0001): c clock;Φ/40 mode */
/* 2(CKS3210=0010): c clock;Φ/48 mode */
/* 3(CKS3210=0011): c clock;Φ/64 mode */
/* 4(CKS3210=0100): c clock;Φ/80 mode */
/* 5(CKS3210=0101): c clock;Φ/100 mode */
/* 6(CKS3210=0110): c clock;Φ/112 mode */
/* 7(CKS3210=0111): c clock;Φ/128 mode */
/* 8(CKS3210=1000): c clock;Φ/56 mode */
/* 9(CKS3210=1001): c clock;Φ/80 mode */
/* 10(CKS3210=1010): c clock;Φ/96 mode */
/* 11(CKS3210=1011): c clock;Φ/128 mode */
/* 12(CKS3210=1100): c clock;Φ/160 mode */
/* 13(CKS3210=1101): c clock;Φ/200 mode */
/* 14(CKS3210=1110): c clock;Φ/224 mode */
/* 15(CKS3210=1111): c clock;Φ/256 mode */
/* Return: None ; None */
/* */
/*=====*/
void Set_iic_rate ( unsigned char Iic_rate ){

    Iic_rate &= 0x0f; /* et master device transfer rate as CKS3210 */
    IIC2.ICCR1.BYTE = ((IIC2.ICCR1.BYTE & 0xf0) | Iic_rate); /* Set transfer rate to register */
}

```

```

/*=====*/
/* Set IIC2 I/F module operation status (ICE) */
/* */
/* Entry: Ice (unsigned char) ; Operation status */
/*          0 (ICE=0): Halt state (SCL/SDA: port function) */
/*          1 (ICE=1): Transfer-operation-enabled state (SCL/SDA: bus driving status) */
/* Return:  None ; None */
/* */
/*=====*/
void Set_iic2_if_enable ( unsigned char Ice ){

    Ice &= 0x01;

    if ( Ice == 1 ){
        Ice = 0x80; /* Check Ice, and */
    }else{ /* 1: Set ICE (7th bit) */
        Ice = 0x00; /* 0: Reset ICE (7th bit) */
    }

    IIC2.ICCR1.BYTE = ((IIC2.ICCR1.BYTE & 0x7f) | Ice); /* Set operation status to register */
}

/*=====*/
/* Initialize EEPROM bus condition */
/* */
/* Issue start condition using port, transmit dummy slave address (0xff), and issue a stop condition */
/* to forcibly initialize the EEPROM bus condition */
/* (This initialization process is used for forcibly making EEPROM SDA bus input state */
/* when reception processing from the master device cannot be performed since EEPROM */
/* SDA bus still remains in output status due to communication termination during receiving data from EEPROM) */
/* Entry:  None ; None */
/* Return: None ; None */
/* */
/*=====*/
void Init_eeeprom ( void ){

    unsigned char Ack_flg;

    PDR5 = 0xFF; /* Set P57 (SCL), P56 (SDA) as output and */
    PCR5 = 0xFF; /* output P57 (SCL) = 1, P56 (SDA) = 1 */

    Set_iic2_if_enable ( 0 ); /* Set IIC2 I/F module in a halt state */
                             /* (SCL/SDA pin: port function) */

    I2c_start (); /* Issue start condition */
    Wait_timer (TM); /* Wait tiemr */

    I2c_bytesend ( 0xff ); /* Transmit dummy slave address, and */
    Ack_flg = I2c_ackck(); /* then obtain acknowledgement */

    I2c_stop (); /* Issue stop condition */
    Wait_timer (TM); /* Wait for the specified time */
}

```

```

/*=====*/
/* Issue start condition to IIC device (through port processing) */
/* */
/* Entry:   None ; None */
/* Return:  None ; None */
/* */
/*=====*/
void I2c_start ( void ){

    I2c_sda_out( 0xC0 );          /* Set P57 (SCL), P56 (SDA) as output, */
                                /* and output P57 (SCL) = 1, P56 (SDA) = 1 */

    I2c_set (1,1);              /* Set SCL = 1, SDA = 1 and output from port */
    I2c_set (1,0);              /* Set SCL = 1, SDA = 0 and output from port */
    I2c_set (0,0);              /* Set SCL = 0, SDA = 0 and output from port */
}

/*=====*/
/* Issue stop condition to IIC device(through port processing) */
/* */
/* Entry:   None ; None */
/* Return:  None ; None */
/* */
/*=====*/
void I2c_stop ( void ){

    I2c_sda_out( 0x00 );          /* Set P57 (SCL), P56 (SDA) as output, */
                                /* and output P57 (SCL) = 0, P56 (SDA) = 0 */

    I2c_set (0,0);              /* Set SCL = 0, SDA = 0 and output from port */
    I2c_set (1,0);              /* Set SCL = 1, SDA = 0 and output from port */
    I2c_set (1,1);              /* Set SCL = 1, SDA = 1 and output from port */
}

/*=====*/
/* Output SCL, SDA to IIC device (through port processing) */
/* */
/* Entry:   Scl (unsigned char) ; Clock (SCL) output value */
/*           0: SCL(P57) = 0, 1: SCL(P57) = 1 */
/*           Sda (unsigned char) ; Data (SDA) output value */
/*           0: SDA(P56) = 0, 1: SDA(P56) = 1 */
/* Return:  None ; None */
/* */
/*=====*/
void I2c_set ( unsigned char Scl , unsigned char Sda ){

    unsigned char  Data;

    Data = 0;                  /* Initialize data to output */
                                /* to P57 (SCL), P56 (SDA) */

    if ( Scl == 1 ){          /* If SCL = 1, set P57 = 1 */
        Data = 0x80;         /* */
    }                          /* */

    if ( Sda == 1 ){          /* If SDA = 1, set P56 = 1 */
        Data |= 0x40;        /* */
    }                          /* */

    PDR5 = ((PDR5 & 0x3F) | Data); /* Output data to P57 (SCL), P56 (SDA) */
}

```

```

/*=====*/
/* Transmit byte data to IIC device (through port processing) */
/* */
/* Entry: Tx_data (unsigned char) ; Byte data to be transmitted */
/* Return: None ; None */
/* */
/*=====*/
void I2c_bytesend ( unsigned char Tx_data ){

    unsigned char Ckbit;

    I2c_sda_out( 0x00 ); /* Set P57 (SCL), P56 (SDA) as output, */
                        /* and output P57 (SCL) = 0, P56 (SDA) = 0 */

    for (Ckbit = 0x80; Ckbit > 0; Ckbit >>= 1){ /* Transmit 8-bit data */
        I2c_bitsend ( Tx_data , Ckbit ); /* from MSB sequentially */
    } /* */
}

/*=====*/
/* Transmit bit data to IIC device (through port processing) */
/* */
/* Entry: Tx_data (unsigned char) ; Byte data to be transmitted */
/* Ckbit (unsigned char) ; Bit position of bit data to be transmitted (value setting 1 to bit position) */
/* Return: None ; None */
/* */
/*=====*/
void I2c_bitsend ( unsigned char Tx_data , unsigned char Ckbit ){

    unsigned char Bit_data;

    Bit_data = ( Tx_data & Ckbit ); /* Obtain bit information */
                                    /* from a bit position to be transmitted */

    if ( Bit_data != 0 ){ /* Check bit information, and generate bit data */
        Bit_data = 1; /* Bit data = 1, */
    } /* */
    else { /* */
        Bit_data = 0; /* Bit data = 0, */
    } /* */

    I2c_send ( Bit_data ); /* Transmit generated bit data */
}

/*=====*/
/* Transmit bit data from IIC port synchronized with a clock (through port processing) */
/* */
/* Entry: Bit_data (unsigned char) ; Bit data to be transmitted */
/* Return: None ; None */
/* */
/*=====*/
void I2c_send ( unsigned char Bit_data ){

    I2c_set (0,Bit_data); /* Output SCL = 0, SDA = bit_dat from port */
    Wait_timer (TM); /* Wait for the specified time */

    I2c_set (1,Bit_data); /* Output SCL = 1, SDA = bit_dat from port */
    Wait_timer (TM); /* Wait for the specified time */

    I2c_set (0,Bit_data); /* Output SCL = 0, SDA = bit_dat from port */
    Wait_timer (TM); /* Wait for the specified time */
}

```

```

/*=====*/
/* Obtain acknowledgement from IIC device (through port processing) */
/* (read data at ninth clock) */
/* */
/* Entry:   Bit_data (unsigned char) ; Bit data to be transmitted */
/* Return:  Ack_flag (unsigned char) ; Acknowledgement */
/*         0: Normal, 1: Error */
/* =====*/
unsigned char I2c_ackck ( void ){

    unsigned char Ack_flag;

    I2c_sda_in();                               /* Set P57 (SCL) as output and P56 (SDA) as input */
                                               /* */
    I2c_set (0,0);                               /* Output SCL = 0, SDA = 1 from port */
    Wait_timer (TM);                             /* Wait tiemr */
                                               /* */

    I2c_set (1,0);                               /* Output SCL = 1, SDA = from port */
    Wait_timer (TM);                             /* Wait for the specified time */
                                               /* */

    Ack_flag = PDR5 & 0x40;                     /* Obtain acknowledgement (SDA: P56) */
    Wait_timer (TM);                             /* Wait for the specified time */
                                               /* */

    I2c_set (0,0);                               /* Output SCL = 0, SDA = 1 from port */
    Wait_timer (TM);                             /* Wait for the specified time */
                                               /* */

    if (Ack_flag != 0){                          /* If the acknowledgement value */
                                                /* (SDA: P56) is 1, set 1 */
            Ack_flag = 1;                        /* */
        }                                       /* */
                                               /* */

    return (Ack_flag);                           /* Return acknowledgement */
}

/*=====*/
/* Set SDA (P56) as input, and SCL (P57) as output of IIC port */
/* */
/* Entry:   None ; None */
/* Return:  None ; None */
/* =====*/
void I2c_sda_in ( void ){

    PCR5 = 0x80;                               /* Set SDA (P56)as input, andSCL (P57) as output */
}

/*=====*/
/* Set SDA (P56), SCL (P57) of IIC port as output, and output data */
/* */
/* Entry:   Data (unsigned char) ; Output data (bit 7 = SCL, bit 6 = SDA) */
/* Return:  None ; None */
/* =====*/
void I2c_sda_out ( unsigned char Data ){

    PDR5 = Data;                               /* Set Data to PDR5 */
    PCR5 = 0xC0;                               /* Set P57 (SCL), P56 (SDA) as output, */
                                               /* and output Data */
}

```



```
/*=====*/
/* Wait for the specified time (decrement wait counts until the count becomes 0) */
/* */
/* Entry:   Wait_cnt (unsigned char) ; Wait counts */
/* Return:  None ; None */
/* */
/*=====*/
void Wait_timer ( unsigned short Wait_cnt ){

    unsigned short    cnt;

    for (cnt = 0; cnt < Wait_cnt; cnt ++){
        }
    }
}
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Revision Record

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Keep safety first in your circuit designs!

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