

Introduction

The most popular DC-DC converter topologies are also the simplest - the flyback converter and the forward converter. Much of their simplicity is because they employ a single power transistor referenced to the primary-side return. Though these topologies are straightforward, they do have some significant drawbacks in many applications. In these situations, designers turn to more elegant topologies, such as the full-bridge and half-bridge converters. These topologies are complicated mainly by having to drive multiple power transistors, where one or more of the transistors is not referenced to the primary-side return. These converters require either a pulse transformer or an IC driver that can level-shift the ground-referenced pulse-width modulator (PWM) signal to the half-bridge node.

The Intersil HIP2100 driver IC simplifies the task of driving two MOSFETs connected in a half-bridge configuration. This small, fast, and low-cost driver is a better alternative to a pulse transformer or other driver ICs for most applications (up to 100V) requiring both a low-side and a high-side driver [1]. It enables higher switching frequencies in isolated DC-DC converters while maintaining high efficiency.

This Application Note describes the design issues associated with a 50W two-switch forward converter featuring the HIP2100. This surface-mount DC/DC converter accepts a 48V_{DC} input and provides 5V_{DC} output. The full-load efficiency of the converter is 83% and the power density is 11W/in³. The HIP2100's fast propagation delay times and 2A drive capability enables converter switching frequencies of 500kHz or higher without an exotic resonant or resonant-transition topology. The two-switch forward converter referenced design runs at 500kHz.

This Application Note first introduces the HIP2100 and some of its innovative features and characteristics. The two-switch converter topology and the architecture of the design are then discussed. The detailed design is presented, including semiconductor selection, magnetics design, and control loop issues. An evaluation board built to this design (HIP2100EVAL2) is available. Predicted versus measured performance of this converter is compared where appropriate.

The converter design details are presented for two main reasons. The principal reason is to highlight the operation and performance of the evaluation board and display the benefits of the HIP2100. The second reason is to make it easier to customize the referenced design for a broader base of applications.

HIP2100 Half-Bridge Driver

The HIP2100 is a high-speed, 100V half-bridge MOSFET driver. Figure 1 shows a simple block diagram of the HIP2100. It integrates a 115V, 1Ω Schottky bootstrap diode, two independent 2A output drive stages, and the necessary control and logic into an 8-pin SOIC. The input-to-output propagation delays of the HIP2100 are typically 20ns. This allows the HIP2100 to be implemented into applications with switching frequencies exceeding 1MHz. Power dissipation is not compromised to achieve this high-speed operation. The quiescent supply current is typically 100μA and the operating current is about 1.5mA when operated at 500kHz [2].

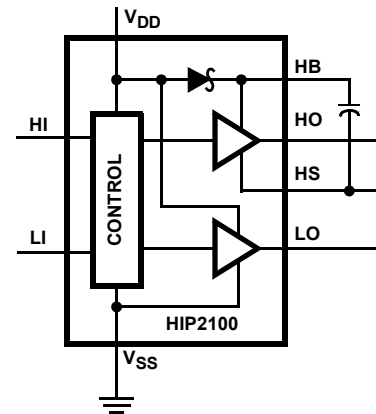


FIGURE 1. HIP2100 BLOCK DIAGRAM WITH EXTERNAL BOOTSTRAP CAPACITOR

One of the innovative features of the HIP2100 is its self-correcting logic. The HIP2100 uses a pulsed, latching level-shifter because it is faster and more efficient than a DC level-shifter. Historically, the problem with the latching method was that it could latch to the wrong state, given some noise or other perturbation. The HIP2100 has built-in logic to correct for such events. A potential catastrophic problem is avoided while still maintaining the benefits of a pulsing level-shifter.

The HIP2100 has undervoltage lockout (UVLO) on both the low-side bias and the high-side bias. The high-side bias is developed via the internal bootstrap diode and an external bootstrap capacitor. The UVLO features on both bias supplies, along with the self-correcting level-shifter, make the HIP2100 a very safe part to use. Output signal integrity is maintained in start-up, normal operation, and power-down situations.

Two-Switch Forward Topology

The HIP2100 is an ideal building block for many DC-DC converters with input voltage requirements under $100V_{DC}$, including telecommunications and other distributed power applications. There are many choices of buck-derived converter topologies. We chose the two-switch forward converter as a vehicle to illustrate the benefits of the HIP2100. A block diagram of this topology is depicted in Figure 2. It is beyond the context of this Application Note to detail all the advantages and disadvantages of this topology in comparison to other topologies. However, it is important to show the relative merits of the two-switch forward in comparison to the standard single-switch forward converter. The standard forward serves as a benchmark since it is one of the most popular converter topologies.

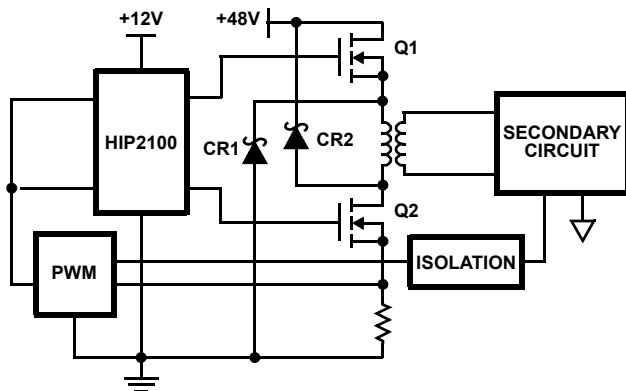


FIGURE 2. TWO-SWITCH FORWARD CONVERTER

The two-switch forward topology is very similar to the standard forward converter in both architecture and design complexity. In fact, the two-switch forward may be easier to design than the forward because of its simple transformer reset method. Rectifiers CR1 and CR2 clamp the reverse voltage of the primary to the input source.

There are two principal benefits of the two-switch forward in comparison to the standard, single-switch forward converter. The two-switch forward topology allows MOSFETs with a voltage rating greater than $V_{IN(MAX)}$ to be used. In contrast, the standard forward topology requires a MOSFET with a voltage rating greater than twice $V_{IN(MAX)}$. Using the typical telecommunications input voltage range of -36V to -72V, 100V MOSFETs could be used in the two-switch forward converter while the forward converter would require 200V MOSFETs. For a given die size, two 100V MOSFETs have lower combined on-resistance ($r_{DS(ON)}$) than does one 200V MOSFET. The other advantage the two-switch forward converter has is that it distributes the MOSFET losses over two devices. This allows a higher power converter or less elaborate and costly heatsinks.

Architecture Issues

Primary Versus Secondary Referenced Control

Galvanic isolation requirements between input supply and output load complicates the converter design in a number of ways. The best isolation method for the power delivery circuitry requires a transformer, with its own set of

complications. Other difficulties arise depending upon the location of the pulse-width modulator (PWM) control circuitry. We choose to reference the PWM control to the input, or primary side of the isolation boundary. This is the method shown in Figure 2. In addition to the main power transformer, the only other isolation boundary crossing is in the voltage feedback loop. An opto-isolator is the most popular method for handling this isolation boundary crossing, although a magnetic element could also be used. Care must be taken in designing this feedback loop to achieve the desired regulation and small-signal response.

Secondary referenced control locates the PWM control on the output side of the isolation boundary. The number of isolation boundary crossings is typically greater with this referencing scheme, in comparison to primary referenced control. The power transformer accounts for one boundary crossing, regardless of where the control is referenced. Instead of the output voltage having to be fed back to the primary side, the second crossing with secondary referenced control is typically a transformer to communicate the MOSFET drive signals across the boundary. A third isolation boundary crossing is required to develop a secondary-referenced bias voltage, typically a separate flyback converter off the input voltage. A fourth possible isolation boundary crossing uses a current-sense transformer for current-mode control. These numerous isolation boundary crossings make primary referenced control more appealing than secondary referenced control in many instances. For this reason, we implement primary referenced control in this design, using an opto-isolator to provide the necessary isolation in the voltage feedback loop.

Voltage-Mode Versus Current-Mode Control

The best control topology is very application dependent, and in many situations a strong case could be made for either voltage-mode or current-mode control. Reference [3] details the relative merits and drawbacks of the two topologies. Current-mode control inherently provides pulse-by-pulse current limiting. However, it requires either a lossy resistor or a transformer to sense the current. Therefore, a solid argument can be made for current-mode control if the converter requires overcurrent protection. In this case, some mechanism for current sense will be required regardless of control method. Since this application protects against output overloads, we select current-mode control. We will sense the primary current with a resistor, as shown in Figure 2.

Converter Design

With the selection of a two-switch forward converter with primary-referenced, current-mode control, we now discuss the design details of this converter for a 50W power level.

Power MOSFET Selection

The power switches require 100V rated MOSFETs for this application. Cost, size, and efficiency are the main criteria in selecting a MOSFET for a given application. This converter is a completely surface-mount solution, which has definite limitations thermally. For this reason, the most critical parameter for MOSFET selection in this application is power losses. The MOSFET losses consist of conduction,

switching, and gate drive terms. Equations 1 through 4 define the MOSFET loss expressions, with the switching losses split into two terms (Equations 2 and 3). The terms used in the equations are itemized in the Appendix.

$$P_{COND} = I_{PRI}^2 \cdot r_{DS(ON)} \cdot D \quad (EQ. 1)$$

$$P_{SW1} = \frac{1}{2} \cdot I_{PRI} \cdot \frac{V_{IN}}{2} \cdot t_{SW} \cdot F_S \quad (EQ. 2)$$

$$P_{SW2} = \frac{2}{3} C_{OSS} \cdot \sqrt{V_{DS}} \cdot \left(\frac{V_{IN}}{2}\right)^{\frac{3}{2}} \cdot F_S \quad (EQ. 3)$$

$$P_{GDR} = Q_G \cdot V_{CC} \cdot F_S \quad (EQ. 4)$$

In most applications, the conduction losses (Equation 1) dominate. The temptation is to select very low $r_{DS(ON)}$ MOSFETs to reduce the conduction losses. However, switching losses can more than negate the conduction loss benefits when going to lower $r_{DS(ON)}$ FETs. This is because the switching transition time (t_{SW}) increases due to the larger MOSFET gate charge inherent in larger (lower $r_{DS(ON)}$) MOSFETs. Complicating the analysis further is the fact that the $r_{DS(ON)}$ varies greatly with temperature. The thermal characteristics of the MOSFET package can therefore have a great impact on the overall converter efficiency.

We use a MathCAD® program to calculate the MOSFET losses at any converter line, load, and ambient temperature condition.

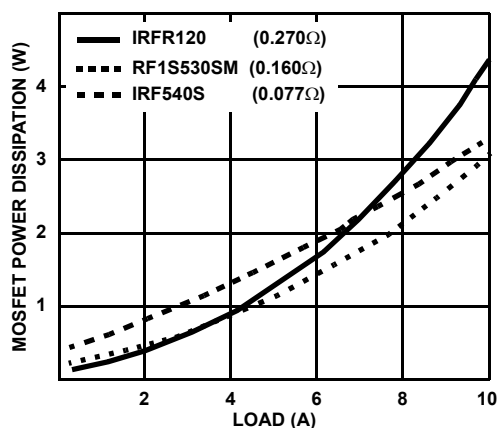


FIGURE 3. PREDICTED MOSFET POWER DISSIPATION FOR THREE DIFFERENT SIZE DIE IN THE TWO-SWITCH FORWARD APPLICATION

The program includes Equations 1 through 4 and the most significant converter losses. We utilize MathCAD's solve function to calculate thermal equilibrium for the components with loss terms dependent upon temperature. Figure 3 shows the MathCAD prediction for the total MOSFET losses as a function of load current at a nominal 48V input and 25°C ambient temperature for three different surface-mount MOSFETs. Figure 3 also displays the maximum rated $r_{DS(ON)}$ at a junction temperature of 25°C for each of the three MOSFETs. We select the RF1S530SM based upon this analysis.

Power Transformer Design

Power transformer design is typically an iterative process which requires experience to produce desired results. This section describes a general transformer design procedure as applied to this application. Much of the iterative nature of the process is not presented for simplicity. The design procedure we use is as follows:

1. Select Transformer Geometry.
2. Make Assumption of Transformer Power Losses.
3. Select Transformer Size.
4. Select Transformer Material.
5. Calculate Maximum Allowable Flux Excursion.
6. Calculate Minimum Number of Primary Turns.
7. Calculate Turns Ratio.
8. Select Wire to Complete Design.
9. Verify Power Loss Assumptions.

Step 1: Select Transformer Geometry

The choice of core geometry is daunting and is highly application dependent. For this application, we choose TDK EPC geometry due to its low-profile, surface-mountable structure and because there are core materials available in this geometry (PC44, PC50) that are low-loss, high-frequency ferrites.

Steps 2 and 3: Assume Transformer Power Losses and Select Transformer Size

As a starting point, we assume that the transformer power losses will be approximately 1W. We arrive at this number by equating transformer losses to 2% of the converter output power. This is a reasonable assumption, but again is very application dependent. Most designs are a compromise between efficiency and size.

With this assumption, we narrow the core size down to a couple of choices based upon acceptable temperature rise. From the manufacturer's curves [4], we find that the EPC-19 core size can dissipate about 0.8W and the next larger core, EPC-25, can dissipate approximately 1.1W with a 50°C temperature rise. We do not yet have enough information to decide which is the best size core. We proceed and design with both size cores; after Step 6 we will decide which design seems more feasible.

Total transformer losses consist of both core and winding copper losses. Assume that the copper losses are 0.5W and 0.6W for the EPC-25 and EPC-19 cores respectively. We assume that the copper losses will be greater for the smaller core because a smaller winding area is available. This allows for 0.6W core loss for the EPC-25 and 0.2W core loss for the smaller core (EPC-19).

Steps 4 and 5: Select Transformer Material and Calculate Maximum Allowable Flux Excursion

With core loss goals identified, we then determine the maximum allowable flux excursion (ΔB) via Figure 4, which reproduces manufacturer's data on both PC44 and PC50

material at 500kHz. PC50 material can operate at higher flux densities than PC44 material with equivalent core losses. However, PC50 material is relatively new, and thus, is more expensive and less readily available than PC44 material. We decide to defer material choice until we complete Step 6. This gives us a total of four possible designs; two different core sizes and two different core materials. This extra effort in the initial portion of the transformer design will hopefully prevent numerous iterations of the complete design.

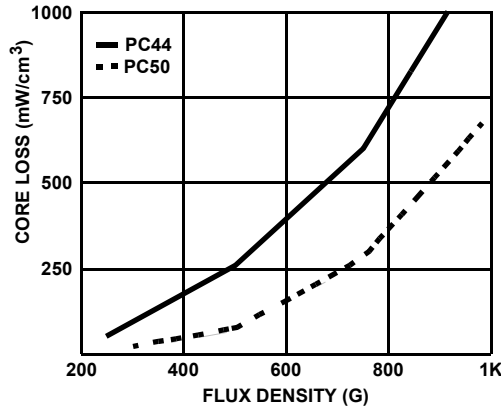


FIGURE 4. MANUFACTURER'S DATA FOR PC44 AND PC50 MATERIAL AT 500kHz

To utilize Figure 4, we first calculate P_C , the core loss in mW/cm^3 . For the EPC-19 size cores:

$$P_{CORE} = 0.2W$$

$$V_E = 1.05 \text{ cm}^3$$

Thus, $P_C = 190 \text{ mW/cm}^3$ and from Figure 4, $\Delta B(\text{MAX})$ is approximately 400 Gauss for PC44 material and 625 Gauss for PC50 material. We also calculate this maximum flux excursion for the larger core (EPC-25) designs. This information is contained in Table 1.

**Step 6:
Calculate Minimum Number of Primary Turns**

Given the maximum flux density (ΔB) found in Step 5, we use Faraday's Law, Equation 5, to calculate the minimum number of primary turns (N_P).

$$\Delta B = \frac{V_{PRI} \cdot \frac{D}{F_S}}{A_E \cdot N_P} \cdot 10^8 \quad (\text{EQ. 5})$$

where

$$V_{PRI} = V_{IN} - 2 \cdot I_{PRI} \cdot (1.5)r_{DS(ON)} - I_{PRI} \cdot R_{PRI} \quad (\text{EQ. 6})$$

$$D = \frac{(V_{OUT} + V_{FWD})}{\left(\frac{N_S}{N_P}\right) \cdot V_{PRI} - I_{OUT} \cdot R_{SEC}} \quad (\text{EQ. 7})$$

The 1.5x multiplying term on $r_{DS(ON)}$ in Equation 6 is to account for its worst-case thermal dependency. Since there are terms in both equations that are dependent upon the

transformer design, some additional assumptions and iterations are necessary. We assume zero winding resistances and a 2.5:1 turns ratio. The primary current when the MOSFETs are on is approximated by the load current divided by the turns ratio. In this case, $I_{PRI} = 4A$ and $V_{PRI} \approx 46V$. Using an output rectifier forward voltage drop (V_{FWD}) of 0.4V yields a duty-cycle factor, D , of approximately 29%. We now calculate the minimum number of primary turns by rearranging Equation 5. For the EPC-19, PC44 core:

$$N_P(\text{MIN}) = \frac{V_{PRI} \cdot \frac{D}{F_S}}{A_E \cdot \Delta B(\text{MAX})} \cdot 10^8 = \frac{(46) \cdot \left(\frac{0.29}{5 \times 10^5}\right)}{0.227 \cdot 400} \cdot 10^8 \approx 30$$

We calculate $N_P(\text{MIN})$ for the other three designs. This information is summarized in Table 1.

TABLE 1. SUMMARY OF INITIAL TRANSFORMER TRADE-OFF ANALYSIS

| | PC44 MATERIAL | | PC50 MATERIAL | |
|------------------------|----------------------|----------------------|----------------------|----------------------|
| | EPC-19 | EPC-25 | EPC-19 | EPC-25 |
| P_{CORE} | 0.2W | 0.6W | 0.2W | 0.6W |
| V_E | 1.05cm ³ | 2.75cm ³ | 1.05cm ³ | 2.75 cm ³ |
| $\Delta B(\text{MAX})$ | 400G | 425G | 625G | 660G |
| A_E | 0.227cm ² | 0.464cm ² | 0.227cm ² | 0.464cm ² |
| $N_P(\text{MIN})$ | 30 Turns | 14 Turns | 19 Turns | 9 Turns |

We can now make a more informed choice for core size and material. We select the EPC-25 size core because it does not seem feasible that we can fit the necessary turns on the smaller core with large enough wire to meet the winding loss assumptions. If, after completing an EPC-25 design, the losses are lower than the assumptions we have made, then we can try the smaller EPC-19 design. PC44 material is selected based on availability and cost. If lower losses are required, we can iterate the following steps with PC50 material to reduce core loss.

**Step 7:
Calculate Turns Ratio**

The next step is to determine the primary-to-secondary turns ratio required. Equation 8 calculates the maximum allowable turns ratio based on the minimum line voltage and maximum load situation. We use 40% as a maximum achievable duty-cycle factor under this minimum line and maximum load condition.

$$\frac{N_P}{N_S} = \frac{V_{PRI}}{V_{SEC}} \quad (\text{EQ. 8})$$

where V_{PRI} is calculated using Equation 6 with the minimum input voltage ($V_{IN} = 36V$) and:

$$V_{SEC} = \frac{V_{OUT}}{D(\text{MAX})} + V_{FWD} + I_{OUT}(\text{MAX}) \cdot R_{SEC} \quad (\text{EQ. 9})$$

Again assuming zero winding resistances and $I_{PRI} = 4A$, we calculate a turns ratio of 2.64:1. We see that we are close to our 2.5:1 turns ratio assumption. A 13:5 turns ratio is equal to

2.6:1 and falls just one primary turn short of meeting the minimum primary turns calculated for the assumed core loss. To allow for some margin at low-line, and taking into account the realities of winding the transformer (Step 8), the actual turns ratio implemented is 12:5 (2.4:1).

**Steps 8 and 9:
Select Wire to Complete The Design and Verify Assumptions**

To complete the design, we must choose a wire size that best fills the available space on the bobbin. This tedious work is not detailed here, but the results are presented in Table 2. We see that the estimated copper and core loss are different than we initially assumed, but the temperature rise is acceptable. The copper loss calculations account for both DC resistive losses and AC losses due to skin effect.

This design incorporates winding practices that are important for high frequency transformers. It is best to interleave the primary and secondary windings to minimize leakage inductance. Excessive leakage inductance lowers the converter's efficiency and adversely affects EMI. For this design, half of the primary is wound first on the bobbin, the secondary winding is wound next, and then the other half of the primary is wound. This design also uses an auxiliary bias winding which is wound last. Another good practice is to have each layer consist of one complete winding (or half winding). Finally, high frequency transformers should use small gauge wire to minimize skin effect (AC copper losses), utilizing multiple wires in parallel when necessary.

TABLE 2. FINAL TRANSFORMER DETAILS

| | |
|---------------------|---------|
| Material | PC44 |
| Core | EPC25 |
| N _P | 12 |
| N _S | 5 |
| N _{AUX} | 14 |
| Pri Wire | (2) #24 |
| Sec Wire | (5) #28 |
| Aux Wire | (1) #28 |
| P _{CORE} | 0.63W |
| P _{COPPER} | 0.63W |
| P _{TOTAL} | 1.26W |
| Temp Rise | 55×°C |

If we change the material to PC50 for this design, core losses would only be about 0.18W, total losses would be 0.81W, and the temperature rise would be about 35°C. PC44 material was selected mainly due to availability at the time. However, either material could be used and could be evaluated on cost and availability criteria for each application. The EPC-19 designs were not pursued further based on the results of the EPC-25 design.

A final detail regarding the power transformer design is its magnetizing inductance. The core used (EPC25, PC44) has an ungapped A_L value of 1560 nH/N² ±25%. This yields a magnetizing inductance (L_{MAG}) of about 225μH and a

magnetizing current of 120mA. This magnetizing current does not provide sufficient energy to turn on the diodes, CR1-2 in Figure 2, to reset the core. An air gap of about 6 mils was introduced into the core. This reduces L_{MAG} to about 40μH and provides enough magnetizing current for the application. If PC50 material is to be substituted, the gap must be adjusted to achieve L_{MAG} = 40μH since the A_L values are not equivalent for the two materials.

Output Filter Design

The output voltage ripple is the most pertinent specification when designing the L-C filter. A maximum peak-to-peak ripple of 100mV is desired for this application. The equivalent series resistance (ESR) of the output capacitors and the amount of ripple current determine the amount of output voltage ripple. Low ESR tantalum capacitors are a good choice for this application. A 150μF, 10V cap with 100mΩ worst-case ESR is selected. We need to decide on the amount of ripple current to determine how many output capacitors are necessary to achieve the voltage ripple goal.

If we allow the inductor ripple current to be 20% of the rated load, then we require two output caps in parallel (with an equivalent ESR of 50mΩ) to meet the ripple requirement. The value of output inductor for 2A p-p ripple current is determined simply by applying $V = L \cdot di/dt$.

$$L_{OUT} = \frac{(V_{SEC} - V_{OUT} - V_{FWD})}{\Delta I} \cdot D \cdot T \quad (EQ. 10)$$

where: $V_{SEC} \cong 19V$ $\Delta I = 2A$
 $V_{OUT} = 5V$ $D = 0.28$
 $V_{FWD} \cong 0.4V$ $T = 2\mu s$

Plugging in these values yields L_{OUT} = 3.81μH.

Inductor Design

The core material selected for the output inductor is iron powder material mix number 8 from Micrometals [5]. It has very low core loss at high frequency operation and maintains a high percentage of its initial permeability with substantial DC magnetizing force applied. Based upon energy storage requirements ($1/2 \cdot LI^2$), the core size can be narrowed down to the T50 and T60 toroids. The determining factor between the two cores will be their temperature rise.

The inductance without DC bias (no load) is determined by $L_{OUT} = N^2 \cdot A_L$, where A_L is the core inductance rating in nH/N² and N is the number of turns. The inductance with load will be less and is determined by using Oersted's equation, Equation 11, and the percent saturation versus DC magnetizing force curve supplied by Micrometals.

$$= \frac{0.4\pi \cdot N \cdot I}{l_{MP}} \quad (EQ. 11)$$

where l_{MP} = mean magnetic path length of core:

H = DC magnetizing force

Next we calculate the inductor losses and estimate the core temperature rise. Faraday's Law (Equation 5) is once again applied to calculate the peak AC flux density. The voltage term

from Equation 10 is used instead of V_{PRI} in Equation 5. The core loss is then estimated with Equation 12, the core loss curve-fit formula provided by Micrometals.

$$P_{CORE} = 4.28 \cdot 10^{-13} \cdot F_S^{1.13} \cdot B_{PK}^{2.41} \cdot A_E \cdot I_{MP} \quad (\text{EQ. 12})$$

The copper losses dominate the power dissipation at the rated load current with this core material. AWG 17 wire is selected for both designs even though larger wire could fit on the cores. This is because a self-leaded surface-mount header is selected and larger wire would make it more difficult to achieve mechanical co-planarity. The core temperature rise is estimated with Equation 13, where P is the inductor power dissipation in mW.

$$\Delta T = \left(\frac{P}{A_S}\right)^{0.833} [5] \quad (\text{EQ. 13})$$

The two designs are summarized in Table 3. The T50 design is acceptable based on the temperature rise and is the design which is implemented.

TABLE 3. SUMMARY OF THE TWO OUTPUT INDUCTOR DESIGNS

| Core | T50 | T60 |
|----------------------------|-------|-------|
| A_L (nH/N ²) | 17.5 | 19 |
| A_E (cm ²) | 0.112 | 0.187 |
| A_S (cm ²) | 6.86 | 9.84 |
| I_{MP} (cm) | 3.19 | 3.74 |
| N | 15 | 14 |
| H (O _E) | 59 | 47 |
| % Sat | 12% | 9% |
| No-load L (μH) | 3.94 | 3.74 |
| Full-load L (μH) | 3.50 | 3.38 |
| B_{PK} (G) | 226 | 145 |
| P_{CORE} (W) | 0.20 | 0.13 |
| P_{COPPER} (W) | 0.65 | 0.75 |
| P_{TOTAL} (W) | 0.85 | 0.88 |
| Temp Rise | 55°C | 43°C |

Control Loop Design

The feedback loop contains an isolation boundary and an opto-isolator communicates the output voltage information back to the primary. A UC39432 analog control IC is selected on the secondary-side for the opto-isolator drive. It integrates the necessary reference, operational amplifier, and transconductance amplifier into a 8-pin SOIC. A block diagram model of the closed-loop system is shown in Figure 5. In essence, there are two operational amplifiers (op amps) used to compensate the loop. We refer to them as primary amplifier and secondary amplifier, based upon which side of the isolation boundary they are located.

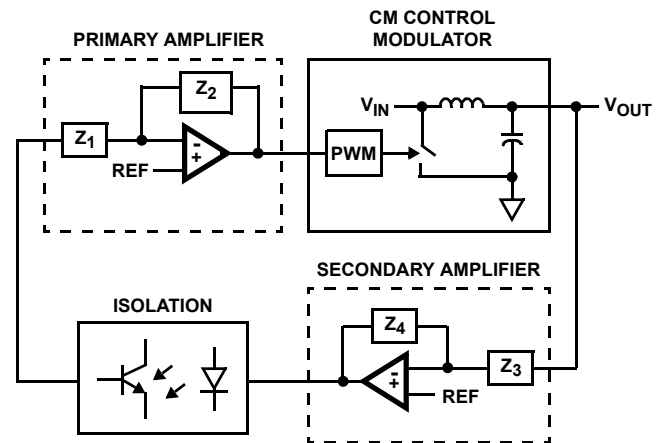


FIGURE 5. BLOCK DIAGRAM OF CONVERTER CONTROL LOOP

The first step in designing a stable control loop is to characterize the modulator response. The topology used is current-mode (CM) control via a primary-side current-sense resistor. The double-pole break normally presented by the LC filter is altered when CM control is employed. The break point becomes a single-pole break at a lower frequency. This normally allows for a higher closed-loop bandwidth. However, modeling the modulator is somewhat more complicated with CM control.

There are many different avenues for attacking the CM control modeling problem. The method that we use is based on a linear representation of the PWM function and is described in Reference [6]. The model was implemented into MathCAD and the modulator gain response for various line/load conditions is shown in Figure 6. Notice how the plots converge in the 10kHz to 100kHz frequency range.

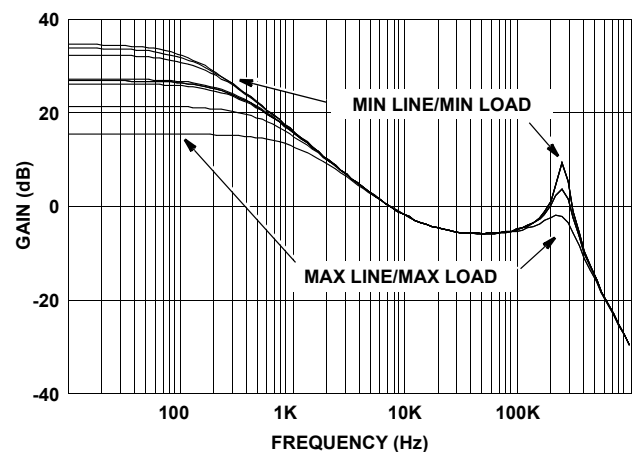


FIGURE 6. OPEN-LOOP MODULATOR GAIN RESPONSE FOR SIXTEEN DIFFERENT COMBINATIONS OF LINE AND LOAD CONDITIONS

The optocoupler and transconductance amplifier frequency responses are also accounted for in the overall loop design. The optocoupler is a NEC PS2701-1, which has a current transfer ratio (CTR) which can vary from 100% to 350% and a unity-gain bandwidth (BW) of about 100kHz. The transconductance amp has a BW of typically 3MHz and a gain

in this application of about -4dB. The opto-isolator and transconductance amp responses are combined and shown in Figure 7 (as "Isolation"), along with a 'worst-case' modulator response and the two op amp compensation responses.

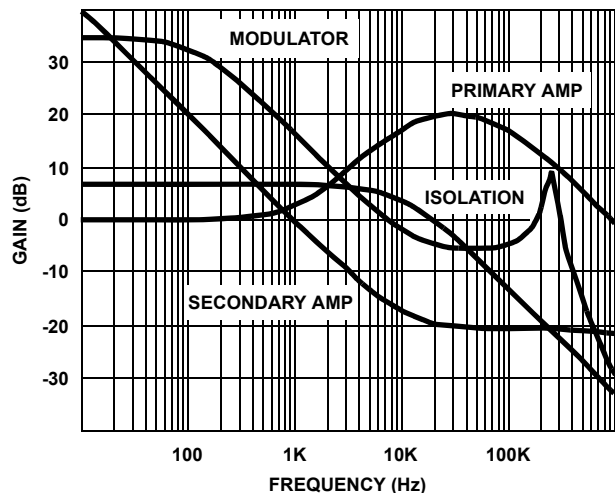


FIGURE 7. GAIN RESPONSE OF THE FOUR DIFFERENT PIECES OF THE CLOSED-LOOP REGULATOR

Our goal for this design is a loop bandwidth of about 10kHz and a phase margin of greater than 60°. The compensation design is straightforward, complicated only by the fact that there are two op amps. For this reason, we present the results of the compensation design without the details. Figure 8 shows both the gain and phase plots of the closed-loop regulator. The closed-loop transfer function is the product of the four different transfer functions which comprise the loop. Pictorially, the gain plot in Figure 8 is the summation of the four different gain responses shown in Figure 7. The unity gain crossover frequency is about 12kHz and the phase margin is 72°.

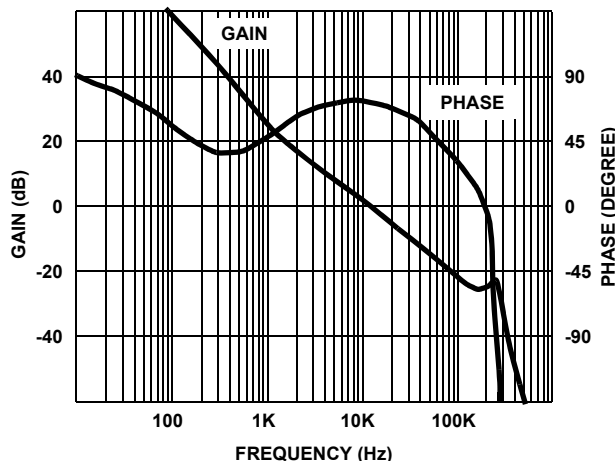


FIGURE 8. CLOSED-LOOP GAIN AND PHASE OF THE CONVERTER

Completing the Design

The choice of output rectifier is critical to the design. Specifically, converter efficiency and thermal performance are very dependent upon the output rectifier. We select a 25A, 35V dual Schottky because of its very low forward voltage

drop. It has about a 0.4V drop at 10A. This translates to 4W of power loss at full load since one of the two legs conducts throughout the entire period. Synchronous rectifiers could substantially reduce the amount of power dissipation. However, the design complexity would increase proportionally.

The PWM controller employed is the UCC3801. It is similar in architecture to the popular UC384x family of controllers, but with numerous enhancements, including lower power operation due to its Bi-CMOS process. It has internal current sense blanking which, in this application, proved to be inadequate. It is necessary to add an external filter to suppress leading-edge switching noise which otherwise interferes with the IC's operation.

The current control loop uses a resistor in series with the power transformer's primary winding. This current sense (CS) resistor converts the primary current waveform to a voltage waveform. This voltage is fed into the 3801's built-in comparators and logic. An overcurrent condition exists when this voltage exceeds 1V. In the event of a very low resistance short on the converter output, the current-sensed voltage could exceed 1.5V. In this case, the controller logic will initiate a soft-start recycle. Designing for an overcurrent level of 12A, we select a 0.2Ω current sense resistor.

The complete DC-DC converter schematic is shown in Figure 13. R1-2, Q1, and VR1 develop a start-up bias voltage for the HIP2100 and UCC3801. Once the converter is running and reaches regulation, the bootstrap winding of the power transformer, CR1-2, and a small LC filter develop a bias voltage of approximately 15V. This voltage effectively turns off Q1 and is a more efficient source of bias power.

Evaluation Board Performance

Figure 9 displays the efficiency of the two-switch forward converter. The predicted curve is generated by the MathCAD program which has been described throughout the Application Note. The predicted and actual data corresponds very well. This lends credence to the design work and allows us to enumerate losses with high accuracy. Table 4 shows the major full-load loss contributors of the converter. The "fixed" losses are the bias, gate drive, and snubber losses.

TABLE 4. FULL LOAD LOSS ANALYSIS

| | |
|-------------------|--------|
| Schottky | 3.72W |
| FET Conduction | 2.07W |
| FET Switching | 1.02W |
| Power Transformer | 1.26W |
| Inductor | 0.85W |
| CS Resistor | 1.20W |
| Fixed | 0.42W |
| Total | 10.54W |

The Schottky rectifier losses, as expected, are the largest loss contributor. A surface-mount heatsink from Wakefield Engineering helps keep the Schottky junction temperature under 125°C at the rated load with about 150-200 linear feet per minute of airflow. Without air flow and at room temperature ambient, the board capability is about 40W with

the board horizontal (lying flat on bench). The heatsink operates more efficiently if the board is oriented vertically with the heatsink fins aligned “north” and “south”. With this board orientation, the converter can safely operate up to approximately 45W maximum output power without airflow.

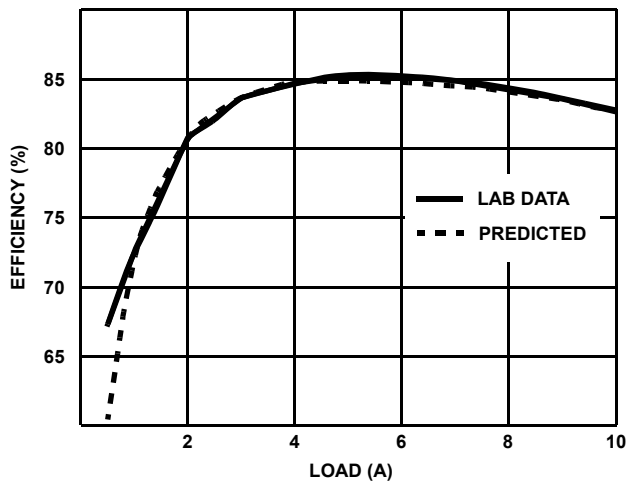


FIGURE 9. EFFICIENCY vs LOAD OF CONVERTER AT 48V_{DC} INPUT, ROOM TEMP, AND 200 LINEAR FEET PER MINUTE OF AIR

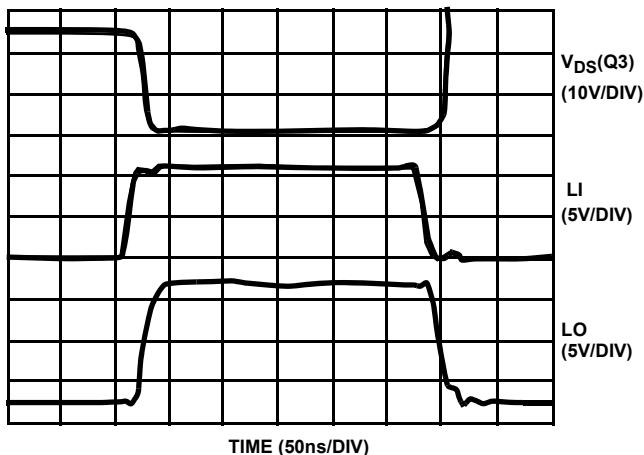


FIGURE 10. LOW-SIDE MOSFET DRIVE TIMING WAVEFORMS

The HIP2100's capability allows high frequency operation and low MOSFET switching losses. Figure 10 shows the LI and LO pins of the 2100 and the drain-to-source voltage across Q3. Notice the fast propagation delay through the 2100 and the short transition time of the FET drain voltage.

The overcurrent limit function of the converter works well. The limit is reached at about 11.5 amps and the converter survives through a short-circuited output. The output voltage returns to regulation when the short is removed. Output voltage regulation is better than $\pm 1\%$ over 36V to 72V line and 0.5A to 10A load conditions. The output response to a step load change from 0.5A to 10A is shown in Figure 11. The load di/dt is 5A/ μ s. The output voltage ripple and noise waveform with an 8A load on the output is shown in Figure 12. The oscilloscope bandwidth is 5MHz for this

measurement.

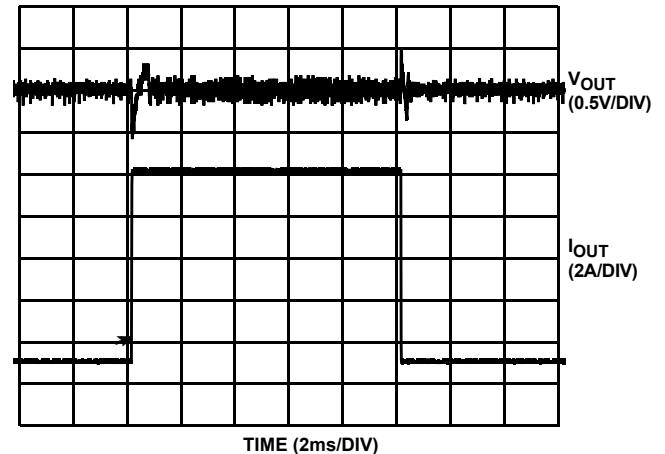


FIGURE 11. OUTPUT TRANSIENT RESPONSE

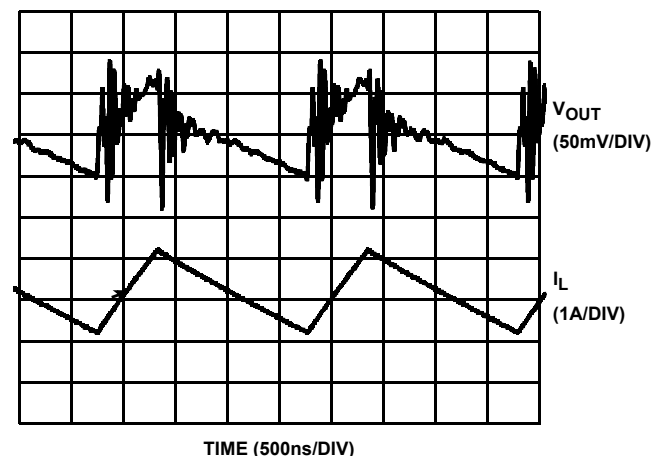


FIGURE 12. OUTPUT VOLTAGE RIPPLE AND INDUCTOR CURRENT

Conclusion

The HIP2100 is an excellent driver for DC-DC converters in distributed power systems. The features of the HIP2100 allowed the design of a high-efficiency, 500kHz, 50W, all surface-mount, two-switch forward converter. This converter achieves 85% efficiency at 30W and 83% at 50W. It uses current-mode control and has overload protection.

The design procedure for this converter was described in sufficient detail to allow for easier customization of this referenced design for a broader base of applications. For instance, one might want to increase the switching frequency in order to reduce the size of the magnetic components. Synchronous rectifiers could be employed to achieve greater output power and higher efficiency. Similarly, a current-sense transformer could be utilized for an efficiency improvement. Thru-hole components and larger heatsinks could be employed for the Schottky rectifier or the MOSFETs to achieve much higher output power. This Application Note attempted to show enough design detail such that the interdependencies of the various parts of the converter design are apparent.

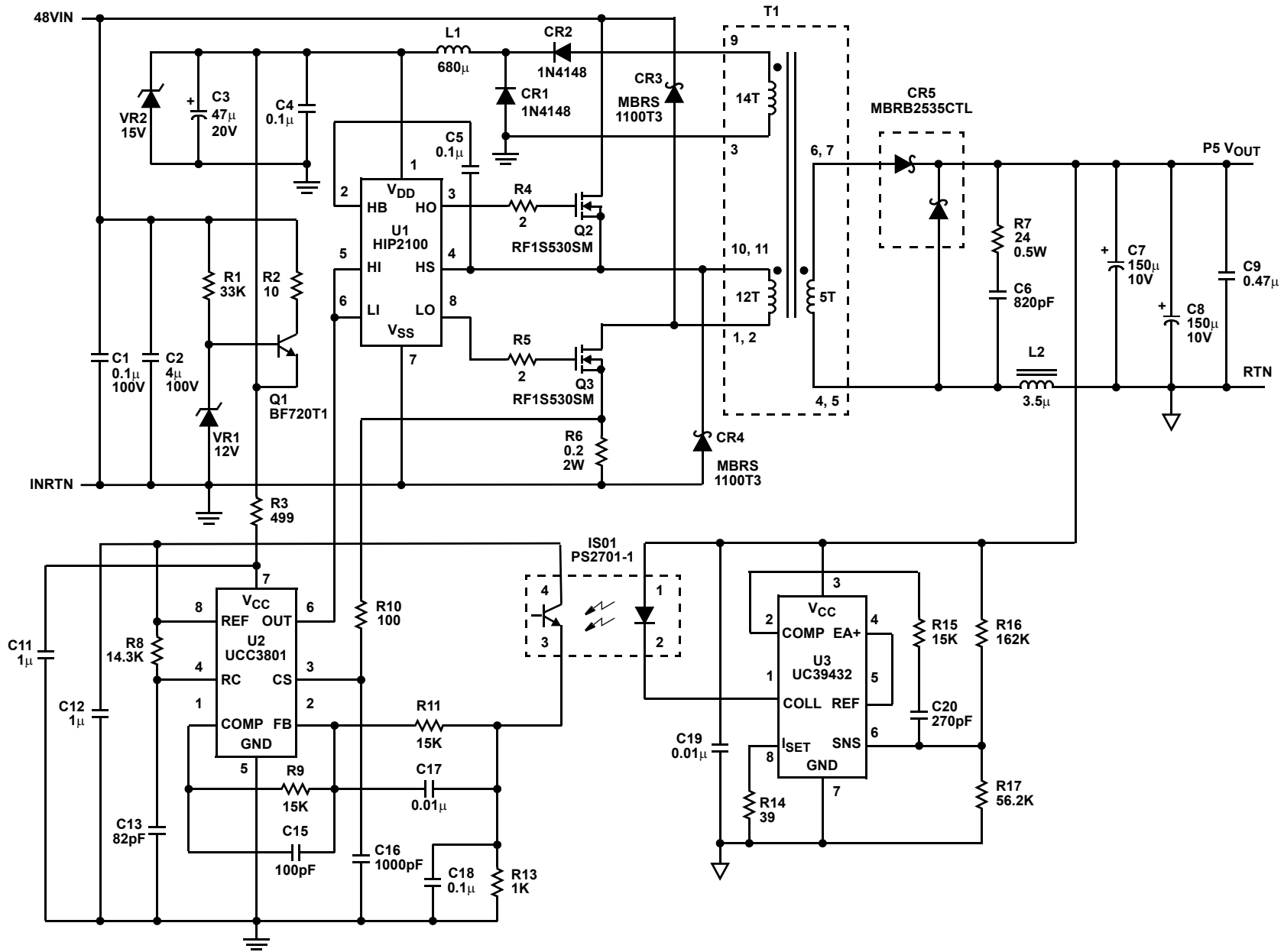


FIGURE 13. SCHEMATIC DIAGRAM OF CONVERTER

Appendix

MATERIAL LIST

| LINE ITEM | REF DESIGN | PART NUMBER | DESCRIPTION | VENDOR(S) |
|-----------|------------|-----------------------------------|-------------------------------------|-------------------------|
| 1 | U1 | HIP2100IB | Half-Bridge Driver | Intersil |
| 2 | U2 | UCC3801DW | PWM | Unitrode |
| 3 | U3 | UC39432D | Analog CNTRLR | Unitrode |
| 4 | Q1 | BF720T1 | NPN, 300V | Motorola |
| 5 | Q2-3 | RF1S530SM | NMOS, 100V | Intersil |
| 6 | CR1-2 | DL4148 | Rectifier, 75V | "Various" |
| 7 | CR3-4 | MBRS1100T3 | Schottky, 100V | Motorola |
| 8 | CR5 | MBRB2535CTL | Schottky, Dual, 35V | Motorola |
| 9 | VR1 | BZX84C12LT1 | Zener, 12V | Motorola |
| 10 | VR2 | BZX84C15LT1 | Zener, 15V | Motorola |
| 11 | ISO1 | PS2701-1 | Optocoupler | NEC |
| 12 | T1 | T7487 2953-H | Power Transformer | TNI GB International |
| 13 | L1 | DT1608C-684 | Inductor | Coilcraft |
| 14 | L2 | T7485 2782-H | Output Choke | TNI GB International |
| 15 | R1 | | 33K, 5%, 0.125W, 1206 | "Various" |
| 16 | R2 | | 10, 5%, 0.125W, 1206 | "Various" |
| 17 | R3 | | 499, 5%, 0.1W, 0805 | "Various" |
| 18 | R4-5 | | 2, 5%, 0.125W, 1206 | "Various" |
| 19 | R6 | CHP2-100-R200-J | 0.2, 5%, 2W, 3610 | IRC |
| 20 | R7 | CHP1/2-100-24R0-J | 24, 5%, 0.5W, 2010 | IRC |
| 21 | R8 | | 14.3K, 5%, 0.1W, 0805 | "Various" |
| 22 | R9, 11, 15 | | 15K, 5%, 0.1W, 0805 | "Various" |
| 23 | R10 | | 100, 5%, 0.1W, 0805 | "Various" |
| 24 | R13 | | 1K, 5%, 0.1W, 0805 | "Various" |
| 25 | R14 | | 39, 5%, 0.1W, 0805 | "Various" |
| 26 | R16 | | 162K, 1%, 0.1W, 0805 | "Various" |
| 27 | R17 | | 56.2K, 1%, 0.1W, 0805 | "Various" |
| 28 | C1 | 12101C104MAT2A | 0.1 μ , 100V, X7R | AVX |
| 29 | C2 | 405K100CS4-AC | 4 μ , 100V | ITW Paktron |
| 30 | C3 | TAZH476M020P | 47 μ , 20V | AVX |
| 31 | C4-5, 18 | 08055E104MATMA | 0.1 μ , 50V, Z5U | AVX |
| 32 | C6 | 08055A821JATMA | 820p, 50V, NPO | AVX |
| 33 | C7-8 | 593D157X0010E2W T495X157K010AS | 150 μ , 10V, 100 m Ω ESR | Sprague Kemet |
| 34 | C9 | 0805YG474ZATMA | 0.47 μ , 16V, Y5V | AVX |
| 35 | C11-12 | 0805YG105ZATMA | 1 μ , 16V, Y5V | AVX |
| 36 | C13 | 08051A820KATMA | 82p, 100V, NPO | AVX |
| 37 | C17, 19 | 08055C103MATMA | 0.01 μ , 50V, X7R | AVX |
| 38 | C15-16, 20 | 08055C102MATMA | 1000p, 50V, X7R | AVX |
| 39 | | 216-40CT | Heatsink | Wakefield |

Term Definitions

| | |
|--------------|---|
| A_E | Magnetic Core Area |
| A_L | Core Inductance Rating |
| A_S | Core Surface Area |
| ΔB | Peak-to-Peak AC Flux Excursion |
| B_{PK} | Peak AC Flux Excursion ($\Delta B/2$) |
| C_{OSS} | MOSFET Output Capacitance |
| D | Duty-Cycle Factor |
| F_S | Switching Frequency |
| H | DC Magnetizing Force |
| ΔI | Output Inductor Ripple Current |
| I_{OUT} | Output Current |
| I_{PRI} | Primary Current |
| L_{MAG} | Transformer Magnetizing Inductance |
| L_{OUT} | Filter Inductance |
| l_{MP} | Core Magnetic Path Length |
| N | Inductor Turns |
| N_{AUX} | Transformer Auxiliary Turns |
| N_P | Transformer Primary Turns |
| N_S | Transformer Secondary Turns |
| P_C | Material Core Loss In mW/cm^3 |
| P_{COND} | MOSFET Conduction Power Loss |
| P_{COPPER} | Transformer/Inductor Copper Loss |
| P_{CORE} | Transformer/Inductor Core Loss |
| P_{GDR} | MOSFET Gate Drive Power Loss |
| P_{SW} | MOSFET Switching Power Loss |
| P_{TOTAL} | Transformer/Inductor Total Loss |
| Q_G | MOSFET Gate Charge |
| $r_{DS(ON)}$ | MOSFET On-resistance |
| R_{PRI} | Transformer Primary Resistance |
| R_{SEC} | Transformer Secondary Resistance |

Term Definitions (Continued)

| | |
|-----------|---------------------------------|
| T | Switching Period |
| t_{SW} | Switching Transition Time |
| V_{CC} | Bias Voltage |
| V_{DS} | MOSFET Drain-to-Source Voltage |
| V_E | Magnetic Core Volume |
| V_{FWD} | Schottky Rectifier Forward Drop |
| V_{IN} | Input Voltage |
| V_{OUT} | Output Voltage |
| V_{PRI} | Transformer Primary Voltage |
| V_{SEC} | Transformer Secondary Voltage |

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